Department of Electrical Engineering

Ph.D. Admissions 2026-27 (Spring Semester)

Abstracts of Projects
(only for TAP/RAP category)

Note:

1) These positions are other than TA positions.

2) Candidates admitted to TA category can choose any supervisor; however, candidates admitted under TAP/RAP category may have to work with the specific Project Investigators listed in this booklet.

List of TAP/RAP Topics (Project Positions)

Project Investigator: Prof. Shiladri Chakraborty

Title of the project: **Multi-functional wireless charger for LEVs with minimal on-board power electronics**

Desired specialization: EE 3 (Power Electronics and Power Systems)

Abstract of the project:

Wireless charging offers several advantages over conventional conductive charging, including enhanced user convenience, improved safety through the elimination of exposed electrical contacts, and reduced connector wear and maintenance. However, wireless charging for light electric vehicles (LEVs) presents unique design challenges due to their relatively low battery voltage, typically in the range of 48–96 V, compared with the approximately 400 V DC bus commonly used in front-end power factor correction (PFC) stages. This voltage mismatch often necessitates an additional buck converter, increasing the system's size, weight, cost, and complexity. This project aims to design and experimentally demonstrate a high-power inductive wireless charging system for 48 V electric vehicles, targeting a power transfer efficiency exceeding 90%. The proposed approach will focus on minimizing on-board power electronics to reduce vehicle weight and simplify the charging system. Furthermore, the potential integration of the wireless charger with the traction inverter will be investigated to enable multifunctional operation and eliminate redundant power conversion stages. The expected outcomes include reduced system-level size, weight, and cost, contributing to compact, efficient, and practical wireless charging solutions for next-generation light electric vehicles.

Project Investigator: Prof. Shiladri Chakraborty

Title of the project: **Unified power electronic interface (UPEI) for Electric Vehicles**

Desired specialization: EE 3 (Power Electronics and Power Systems)

Abstract of the project:

Conventional electric vehicles (EVs) employ separate power converters for the on-board battery charger, auxiliary power supply, and traction inverter, resulting in increased system size, weight, cost, and complexity. This research aims to design and demonstrate an integrated multi-port power electronic interface that combines these functionalities into a single compact system. The proposed architecture will incorporate high-frequency isolation between all ports to support electrical safety and compliance with relevant charging standards. The primary focus will be the integration of the on-board charger and traction inverter, with the potential inclusion of the auxiliary DC–DC converter to further enhance system integration. The proposed solution will be designed and experimentally validated to evaluate its performance, efficiency, power density, and suitability for EV applications. The expected outcomes include system-level reductions in size, weight, and cost, along with improved power conversion performance and enhanced customer convenience through on-board charging and the potential for faster charging.

Project Investigator: Prof. Shiladri Chakraborty

Title of the project: **Design and Development of 11kV Medium - Voltage SiC based DC Fast Charger**

Desired specialization: EE 3 (Power Electronics and Power Systems)

Abstract of the project:

Solid-State Transformers (SSTs) are emerging as a promising technology for next-generation power distribution systems, offering enhanced controllability, improved power quality, and integration with renewable energy sources and electric vehicle charging infrastructure. Medium-frequency transformers (MFTs) are key components of SSTs, enabling high power density and reduced size and weight compared with conventional line-frequency transformers. However, their design presents significant challenges in terms of high-frequency losses, thermal management, insulation coordination, parasitic effects, and overall efficiency. This project aims to investigate the design, modelling, and development of high-performance MFTs for SST applications. The study will focus on optimising transformer geometry, magnetic core materials, winding configurations, and insulation systems to achieve high efficiency, compactness, and reliable operation under medium-frequency, medium-voltage conditions. Analytical modelling, finite-element simulations, and experimental validation through prototype development will be employed to evaluate the proposed designs.

Project Investigator: Prof. Anil M. Kulkarni

Title of the project: **Stability analysis and Controller Design of IBRs using Frequency Scanning Techniques**

Desired specialization: EE 3 (Power Electronics and Power Systems)

Abstract of the project:

Stability of modern power systems is a major concern considering the proliferation of a large number of converter interfaced systems. The objectives of the research work include (but not limited to), stability analysis using numerical tools and techniques.

Skills sought: Power System Transient Simulation, Power System Dynamics and Control, Knowledge of power system simulation tools.

Project Investigator: Prof. Ashwin A. Seshia

Title of the project: **Reliability Physics of Vibrating and Impacting Nonlinear Microelectromechanical Devices**

Desired specialization: EE 5 (Electronic Systems), EE 7 (Solid State Devices)

Abstract of the project:

This project seeks to develop design-linked reliability models for MEMS devices such as resonators and switches operating under extreme nonlinear regimes and operational regimes resulting in continuous impact between surfaces.

The following objectives will be addressed:
• reliability models for vibrating and impacting nonlinear MEMS devices by a thorough consideration of all the applicable physical mechanisms;
• design approaches to circumvent limitations imposed including leveraging nonlinearities to address improved performance or new functionality;
• material/process enhancements to address reliability limitations towards the innovation of new classes of nonlinear MEMS that overcome current technological constraints;
• experimental validation of associated reliability models and distilling the generated insight towards optimization of MEMS design.

Skills sought: Academic background in Engineering or Physics discipline with a strong interest/knowledge in applied/engineering maths, scientific programming, and hands-on experimentation. Prior exposure to MEMS, micro/nanofabrication, sensors, and circuit design is a plus.

Project Investigator: Prof. Bhaskaran M.

Title of the project: **2D-Optoelectronic quantum technologies**

Desired specialization: EE 7 (Solid State Devices)

Abstract of the project:

This is a National Quantum Mission project aimed at developing device design modules for quantum optoelectronics based on 2D materials. We will further TCAD designs on 2D materials for single photon avalanche detection and also quantum transport modules for single photon emission.

Skills sought: Python, TCAD and device physics modeling

Project Investigator: Prof. Bhaskaran M.

Title of the project: **Photodetector device modelling for space applications**

Desired specialization: EE 7 (Solid State Devices)

Abstract of the project:

This is a DRDO project aimed at developing T2SL barrier photodetector design. The device modelling effort will be a full-stack modeling from materials to photodetector device structures involving band structure, mobility calculations and TCAD modeling. Successful device designs will be fabricated at DRDO.

Skills sought: Python, basic device physics and TCAD

Project Investigator: Prof. Chetupalli Srikanth Raj

Title of the project: **Robust Target Speaker Extraction for Speech Communication Applications**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:

Multi-speaker scenarios are common in speech applications, such as telephony, speech interfaces, and virtual meetings. In such scenarios, often there is only one speaker of interest and the other speakers are considered as interferers. Similar to background noise, interference from competing speakers affects speech intelligibility and adversely impacts digital speech interfaces. The problem is further compounded by room reverberation, which degrades the signal quality. Hence, extraction of a desired speaker's speech from a mixture recording containing multiple speakers and enhancing its quality, is of interest. In this project, the goal is to explore "Target Speaker Extraction" (TSE), which is the task of extracting a speaker of interest (desired / target) from a mixture speech recording containing multiple speakers, in a noisy, reverberant acoustic environment. Several variants of the problem are discussed in the literature, depending on the recording type (single microphone or microphone array), the auxiliary information used to specify the target speaker, the intended application (speech communication or for voice assistants), and the deployment platform (general purpose computers or embedded devices). The primary goal in this project is to study the different variants of TSE systems for real-time speech communication scenarios and to develop systems of varying computation complexities and memory footprints that can be deployed on general purpose computers and embedded hardware..

Skills sought: Signal processing, Machine learning, Programming

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Project Investigator: Prof. Debidas Kundu

Title of the project: **High-efficiency Power Amplifier Design**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:

This research work aims to identify and explore entirely new, overlooked impedance spaces in both the source and load matching networks to push the efficiency of Class F-1 and Class E power amplifiers to their absolute maximum limits. Standard design methodologies usually stick to conventional harmonic tuning, but this approach often fails to account for how complex transistor parasitics actually behave at high frequencies. By mapping out these non-traditional impedance regions, we can precisely shape the voltage and current waveforms to prevent them from overlapping. This technique will drastically cut down on power dissipation and switching losses, which are major bottlenecks in current high-speed systems. To pinpoint these optimal design nodes, we plan to utilize advanced multi-harmonic load-pull and source-pull simulations coupled with intelligent optimization algorithms. Ultimately, the objective is to fabricate and test physical hardware prototypes to validate that targeting these new impedance zones can deliver the ultra-high efficiency required for next-generation telecom infrastructure.

Skills sought: RF circuit design, EM theory, basic knowledge of microwave engineering and CMOS circuits, skills in embedded systems and PCB design, programming skills in MATLAB.

Project Investigator: Prof. Debidas Kundu

Title of the project: **Design and Development of Space-Time Coding Metasurface for Harmonic Beamforming Applications**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:
The project aims to develop space-time coded (STC) digital metasurface for harmonic beam steering with operating frequencies at C-band (4-8 GHz). In general, metasurfaces are inherently low-profile

and lightweight. Moreover, unlike a phased array which requires multiple RF chains, a digital coded metasurface requires only one RF chain. Therefore, they consume less power. The proposed metasurface will target to achieve high gain (>20 dB), low cross-pol level from the main lobe maximum (<15 dB), low scan loss (scan pattern ≈ cos θ), low beam squint error (<0.50), and scan range of ±400. Moreover, with the help of STC, a beam-steering up to harmonic order ±3 with a modulation frequency >12.5 MHz will be achieved.

Skills sought: EM theory, strong programming skills in MATLAB, basic knowledge of antenna theory, skills in embedded systems and PCB design.

Project Investigator: Prof. Dipankar Saha

Title of the project: **Single Photon Source and etector**

Desired specialization: EE 7 (Solid State Devices)

Abstract of the project:

Development of an on-demand single-photon source based on semiconductor quantum dots for quantum communication and photonic applications.
Design and integration of a superconducting nanowire single-photon detector (SNSPD) for high-efficiency, low-noise single-photon detection.
Investigate photon emission, collection, timing characteristics, and source–detector correlations at the single-photon level.
Develop an integrated experimental platform for quantum photonics, enabling studies of single-photon statistics, indistinguishability, and quantum communication..

Skills sought: Basics of semiconductors

Project Investigator: Prof. Gaurav Kasbekar

Title of the project: **Resource Optimization in Space-Air-Ground Integrated Networks**

Desired specialization: EE 1 (Communication & Signal Processing)

Abstract of the project:

Sixth-generation (6G) wireless cellular networks, which are a subject of extensive ongoing research in academia and industry, are expected to revolutionize wireless networks by significantly enhancing their performance and coverage relative to the current 5G standard, and supporting numerous novel applications. Space-air-ground integrated networks (SAGINs), which interconnect satellites, aerial platforms such as Unmanned Aerial Vehicles (UAVs) and high-altitude platforms (HAPs), and terrestrial nodes, have been widely acknowledged as a key component of future 6G networks, and offer a variety of use cases including connectivity in remote areas, disaster management, emergency response, intelligent transportation systems, environmental monitoring, military applications, etc.

A critical challenge in the design of SAGINs is resource optimization, as part of which several problems need to be solved, e.g.: (i) task/ computation offloading, (ii) spectrum sharing and interference management, (iii) user association and handover management, (iv) clustering of satellites and aerial platforms, etc. These problems need to be solved in order to achieve various goals, including throughput and capacity maximization, energy efficiency, delay minimization, increasing reliability, network deployment and operation cost minimization, etc. Moreover, the above problems need to be solved while addressing the unique challenges facing SAGINs, such as limited available resources (bandwidth, computing power, storage, energy, etc.) at satellites and aerial nodes,

interference among the transmissions of space, aerial, and terrestrial nodes, high mobility of satellites and aerial nodes, unbalanced traffic, long propagation delays, high path loss and vulnerability of wireless transmissions to atmospheric conditions, limited backhaul capacity, etc. Our objective in this project is to design efficient schemes for resource optimization in SAGINs and to evaluate their performance via mathematical analysis as well as simulations.

Our work on resource optimization in SAGINs in this project will be novel in several respects, including the following:

(i) the formulation of the task/ computation offloading and user association problems using classical multi-armed bandits (MAB) and restless multi-armed bandits (RMAB), and their solution using various indices such as upper confidence bound and the Whittle index,
(ii) solution of the task/computation offloading problem jointly with one or more of the following related problems in SAGINs: (1) Internet of Things (IoT) device-Space Aerial Platform (SAP) association, (2) power allocation, (3) precoding and beamforming, (4) task assignment, (5) trajectory planning, (6) task queue management, and (7) distributed inference,
(iii) design of a number of economic mechanisms such as auctions, markets, bargaining-based solutions, etc., to enable spectrum sharing,
(iv) design of algorithms for performing complex handovers,
(v) design of algorithms for dividing the set of all satellites or UAVs into clusters, which are optimal or have provable approximation ratios, etc.

The algorithms we develop in this project will significantly aid in enhancing the network performance of SAGINs, improving the user experience and Quality-of-Service (QoS) provided to the network users, effectively supporting various network applications, and addressing the unique challenges facing SAGINs. Since SAGINs will be a fundamental component of 6G networks, our work will have a high impact and significantly contribute towards their successful deployment and efficient operation..

Skills sought: The candidate is expected to be interested in solving engineering problems using a combination of analytical techniques and numerical experiments/ simulations.

Project Investigator: Prof. Kasturi Saha

Title of the project: **Design and development of quantum gyroscope**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

Join an exciting research programme to develop next-generation quantum gyroscopes using diamond-based quantum sensors and nitrogen-vacancy (NV) centres. The project aims to harness quantum sensing principles to achieve high-precision rotation measurement, with potential applications in GPS-denied navigation, aerospace, autonomous systems, and strategic technologies. Research will span quantum physics, spin dynamics, precision metrology, photonics, microwave engineering, and sensor integration. PhD scholars will contribute to developing and experimentally validating novel gyroscope architectures, integrating quantum sensors with conventional inertial systems - eg MEMS gyroscopes, and exploring pathways towards compact, robust, and field-deployable devices. Candidates passionate about experimental physics and interdisciplinary research are encouraged to apply.

Relevant paper: https://arxiv.org/html/1808.04494v2

Skills sought: Seeking PhD candidates with a background in electrical engineering, quantum physics, photonics, or instrumentation. Key skills include strong electrical engineering foundations, optics,

microwave engineering, precision measurements, and Python/MATLAB programming. Hands-on experimental experience, problem-solving abilities, and an interest in quantum sensing and inertial navigation are highly desirable.

Project Investigator: Prof. Parthib Khound

Title of the project: **Design and Development of Cooperative Adaptive Cruise Control under a Stochastic Framework**

Desired specialization: EE 2 (Control and Computing)

Abstract of the project:

A platooning control system is a collective system of intelligent vehicles following one another using automatic control technologies. Also known as automatic car-following systems, when optimally designed, these systems improve traffic flow, enhance safety, reduce fuel consumption, and lower pollutant emissions. Adaptive Cruise Control (ACC) and Cooperative Adaptive Cruise Control (CACC) are prominent automatic longitudinal control technologies used for platooning. ACC systems rely on onboard sensors for autonomous control. CACC systems enhance this functionality by integrating vehicle-to-vehicle (V2V) or vehicle-to-infrastructure (V2I) communication to exchange critical feedback and feed-forward information among vehicles. Both technologies can facilitate car-following maneuvers, with CACC being particularly more effective for addressing collective dynamic challenges in platooning. While considerable advancements have been made in this research area, many existing platooning control models remain deterministic and fail to account for stochastic factors such as model inaccuracies, sensor noise, cut-in/cut-out maneuvers, external disturbances, and other sources of uncertainty. As a result, this project aims to develop a robust control algorithm for CACC systems that preserves uncompromised collective dynamics amid stochastic uncertainties.

Skills sought: Linear Control Theory, Dynamic System Modelling, Decent Experience with Embedded Setup (Hardware and Software)

Project Investigator: Prof. Rahul Singh

Title of the project: **Analog/RF/Mixed-Signal IC Design for Readout Circuits Interfacing with Quantum Systems**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

Analog/RF/Mixed-Signal IC Design for Readout Circuits Interfacing with Quantum Systems

Skills sought: Strong Interest Analog/RF/Mixed-Signal IC Design. Background in Communication Theory, Circuit Theory, CMOS IC.

Project Investigator: Prof. Rohit Parasnis

Title of the project: **Incentives, Dynamic Networks, and AI for Real-World Systems**

Desired specialization: EE 1 (Communication & Signal Processing), EE 2 (Control and Computing)

Abstract of the project:

How can we design reward mechanisms for encouraging individuals to make decisions that benefit the larger social and engineered systems they belong to? This project aims to develop theoretical and computational methods (and test these models using multi-agent AI) for designing incentives in dynamic networks, with potential applications to energy systems, transportation, supply chains, and public health.

In these settings, decisions are interdependent: commuters affect one another's travel times, geographical regions share power resources, and people influence disease transmission. Crucially, interactions can change as people adapt or disruptions occur. Incentives designed for a static network may therefore become ineffective. The central challenge is to understand and shape collective behavior when both decisions and networks co-evolve.

We will model strategic decision-making using game theory and apply linear algebra and graph theory to understand how network structure shapes behavior and equilibrium. Mathematical optimization will help design effective incentive schemes, including how to allocate limited budgets across large networks. To complement the theory, we will analyze data on real networks from either electricity markets, interstate supply chains, or epidemic-related mobility. We will potentially explore multi-agent AI simulations in which LLM-based agents interact over networks, helping test the accuracy and limitations of theoretical models.

This project is ideal for students who want to go beyond applying existing tools by formulating models, testing assumptions, and developing solutions that are both technically sound and relevant to policy design for real-world systems. For more on what you can expect to gain from the project, see the PDF and the video.

Skills sought: Most important: Mathematical aptitude, an interest in mathematical reasoning, and a willingness to engage with real-world data analysis Expected preparation: Comfort with basic undergraduate mathematics, including calculus and linear programming Desirable but not required: Prior coursework or relevant experience in any of the following: control and dynamical systems, graph theory, convex analysis, optimization, linear algebra, game theory.

Project Investigator: Prof. S. Lodha

Title of the project: **Wafer-scale Emitter and Detector Arrays for Visible Wavelength Room Temperature Photonic Quantum Technologies**

Desired specialization: EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

The project is funded under the National Quantum Mission and is focused on developing 2D semiconductor-based single photon photodetector devices and arrays. There are 6 institutes involved and the project gives an excellent opportunity to work on quantum semiconductor devices all the way from materials growth, device fabrication/simulation/characterization to read-out circuit design. It will lead to high impact papers as well as job opportunities in the semiconductor and quantum startup ecosystem.

Skills sought: Basic understanding of semiconductor devices and circuits.

Project Investigator: Prof. S.P. Duttagupta

Title of the project: **Digital Twin Models and Implementation for Micro Modular Nuclear Reactor**

Desired specialization: EE 1 (Communication & Signal Processing), EE 2 (Control and Computing), EE 3 (Power Electronics and Power Systems), EE 5 (Electronic Systems), EE 7 (Solid State Devices)

Abstract of the project:

Design, fab, test, and reliability of multi-sensor data fusion applicable networks for Advanced Micro Modular Nuclear Reactors. Scope: photonics and electronics sensors, low noise amplifiers, remote and proximate sensing. Applications: Monitoring of temperature, pressure, vibration, strain, fluid flow and gamma radiation.

Collaborations: TIFR-Mumbai, IIT Madras, IISC Bangalore, CMET-Pune.

Skills sought: Multi-physics simulation and modeling, Mix signal circuit design, Power Electronics Device Simulation, AI/ML model.

Project Investigator: Prof. Sandip Mondal

Title of the project: **FPGA-Based Characterization of Oxide-Based RRAM for Neuromorphic Computing and AI Hardware**

Desired specialization: EE 1 (Communication & Signal Processing), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

Resistive Random Access Memory (RRAM) is a promising technology for energy-efficient artificial intelligence (AI) and neuromorphic computing. This research aims to fabricate oxide-based RRAM devices and develop an FPGA-controlled electrical characterization platform, with a major emphasis on the design and implementation of peripheral circuits for reliable device and crossbar-array operation. The PhD student will fabricate and optimize oxide-based RRAM devices and investigate their SET/RESET characteristics, resistance window, retention, endurance, and device variability.

A major component of the work will involve designing and integrating the read/write circuitry, including programmable voltage and pulse-generation circuits, row and column address decoders, analog multiplexers and switching networks, current-sensing circuits, transimpedance amplifiers, and analog-to-digital conversion interfaces. An FPGA will coordinate cell selection, write-pulse control, read-voltage application, measurement sequencing, and data acquisition. Circuit-level design will address voltage-level compatibility, current compliance during programming, sensing sensitivity, measurement accuracy, and isolation of unselected cells. Suitable biasing and sensing architectures will be investigated to reduce sneak-path currents and unintended switching in RRAM crossbar arrays. Finally, an optimized edge-compatible reconfigurable model will be implemented with the FPGA and partial RRAM-based memory.

The developed hardware platform will support automated characterization of individual devices and multi-cell arrays, enabling systematic evaluation of switching performance, circuit limitations, and array-level reliability. The ultimate goal is to establish an integrated RRAM device circuit FPGA characterization framework and assess its suitability for synaptic weight storage, neuromorphic computing, and energy-efficient AI hardware.

Skills sought: Skill Priority Analog electronics and circuit fundamentals Verilog/VHDL and digital design Circuit simulation and debugging Semiconductor devices and basic characterization PCB design and laboratory instrumentation-Strongly preferred.

Project Investigator: Prof. Sandip Mondal

Title of the project: **High Speed CV system for Semiconductor Memories for Next-Generation AI Hardware**

Desired specialization: EE 1 (Communication & Signal Processing), EE 2 (Control and Computing), EE 3 (Power Electronics and Power Systems), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

Semiconductor memories are critical components of modern computing systems, particularly artificial intelligence (AI), edge computing, and data-intensive applications. However, increasing memory density, complex device architectures, and demanding operating conditions create significant reliability challenges. Conventional characterization techniques often require numerous electrical measurements, extended testing durations, and direct access to device parameters that may not be readily available in commercial memory chips.

This research proposes the development of fast, automated, and minimally invasive techniques for evaluating the reliability of semiconductor memories, with particular emphasis on two-dimensional (2D) and three-dimensional (3D) flash memory. Building on previous research involving high-speed capacitance–voltage (C–V) measurements, fail-bit-count-based reliability analysis, and digital probing of activation energy, the proposed work will investigate the relationship between electrical degradation, charge-trapping mechanisms, temperature, magnetic fields, and memory architecture.

The research will combine custom-built instrumentation, automated flash emory characterization, statistical reliability modelling, and controller-based hardware platforms. The ultimate objective is to establish practical reliability assessment methodologies that minimize measurement overhead while enabling predictive evaluation of memory degradation in advanced computing systems.

Skills sought: A background in electrical engineering, electronics, materials science, or semiconductor physics. Understanding of semiconductor devices and dielectric materials. Experience with electrical characterization and experimental data analysis. Programming skills for scientific computing and model fitting. Interest in charge transport, dielectric physics, and non-volatile memory reliability.

Project Investigator: Prof. Sandip Mondal

Title of the project: **Flexible Non-Volatile Memory**

Desired specialization: EE 1 (Communication & Signal Processing), EE 2 (Control and Computing), EE 3 (Power Electronics and Power Systems), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

Flexible non-volatile memory is an emerging technology for wearable electronics, flexible sensors, electronic skins, and next-generation intelligent systems. Unlike conventional memory fabricated on rigid silicon substrates, flexible memory devices must maintain reliable data storage and electrical performance under bending, tensile strain, and repeated mechanical deformation.

This PhD project aims to develop solution-processed flexible charge-trapping memory devices using engineered dielectric materials and semiconductor nanostructures. Building on research in aluminium oxide phosphate (ALPO)-based charge-trapping dielectrics, quantum-dot memory structures, and

advanced electrical characterization, the project will investigate low-temperature fabrication processes, charge-storage mechanisms, multilevel memory operation, and mechanical reliability.

The research will focus on understanding how dielectric properties, charge-trapping sites, interfaces, and device architecture influence memory performance under electrical and mechanical stress. High-speed capacitance–voltage (C–V) measurements and pulse-based electrical characterization will be used to investigate charge-trapping and detrapping dynamics. Mechanical bending and tensile-strain experiments will establish the relationship between deformation, electrical characteristics, memory-window stability, retention, and endurance.

The ultimate goal is to develop reliable, low-temperature-processed flexible memory devices capable of multilevel data storage and stable operation under repeated mechanical deformation.

Skills sought: Fundamentals of semiconductor devices, electronic materials, and solid-state physics. Interest in experimental research, electrical characterization, and device fabrication. Basic data analysis and scientific programming using Python, MATLAB, or equivalent tools. Ability to interpret electrical measurements and investigate physical mechanisms.

Project Investigator: Prof. Sandip Mondal

Title of the project: **Digital Characterization and Reliability Analysis of Advanced NAND Flash Memory**

Desired specialization: EE 1 (Communication & Signal Processing), EE 2 (Control and Computing), EE 3 (Power Electronics and Power Systems), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

This PhD project aims to develop an automated hardware and software platform for the electrical characterization and reliability analysis of advanced 2D and 3D NAND flash memory. The research will build on existing work on digital probing, fail-bit-count statistics, activation-energy extraction, and memory degradation analysis.

The scholar will develop an FTDI-based controller interface to communicate with NAND flash memory devices, automate read operations, acquire memory data, and analyze fail-bit statistics. The platform will integrate hardware interfacing, firmware development, Python-based control software, and experimental reliability characterization.

The research will investigate the effects of temperature, data retention, program/erase cycling, and other stress conditions on NAND flash reliability. The acquired data will be used to develop digital characterization techniques and predictive models for identifying memory degradation. The scholar will also explore FPGA-based implementations and adaptive error-correction techniques for improving reliability in memory-intensive computing applications

Skills sought: Strong fundamentals in electronics, electrical engineering, or semiconductor devices; programming skills in Python; knowledge of digital electronics, communication interfaces, and embedded systems.

Project Investigator: Prof. Shalabh Gupta

Title of the project: **Optical Transceiver Chipset for High-Bandwidth 6G Wireless Links**

Desired specialization: EE 1 (Communication & Signal Processing), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

In this work, you would be designing and testing high-speed electronic or photonic integrated circuits for optical links & wireline interconnects. Circuits such as phase-locked loops, clock and data recovery circuits / SerDes, drivers, trans-impedance amplifiers etc. are being designed and integrated at a system level by team members. You will be working as part of the team. Good knowledge in the area of analog circuits, analog/digital communication systems, and interest in working with high-speed experimental setup will developed.

Sample publication: S. Chugh, R. Ashok, P. Jain, S. Naaz, A. Sidhique and S. Gupta, "An Analog EIC-PIC Receiver with Carrier Phase Recovery for Self-Homodyne Coherent DCIs," IEEE Transactions on Circuits and Systems II: Express Briefs (2022).

https://doi.org/10.1109/TCSII.2022.3167673

Skills sought: Strong fundamental knowledge of analog circuits, communications & signal processing (taught in undergraduate classes), along with good hardware skills, are needed. Other skills can be developed after joining the group.

Project Investigator: Prof. Siddharth Tallur

Title of the project: **Miniaturized quantum sensor systems**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

In this proposed PhD research, the student will join our team working on low-noise and high-stability electronic systems for quantum sensors. The research will involve investigation and implementation of suitable methods to miniaturize the sensor subsystem as well as the electronics modules to realize a truly compact quantum magnetometer suitable for handheld operation or for integration with a mobile platform such as a drone. Interested candidates may read our recent pre-print to get some idea of the system architecture that we are exploring in this research (note: our present work is not a miniature platform): https://arxiv.org/abs/2609.16901.

Other relevant reading:
https://quantumzeitgeist.com/portable-center-magnetometer-achieves-sqrt-sensitivity-enabling-robust/
https://www.sciencedirect.com/science/article/pii/S092596351830760X
https://advanced.onlinelibrary.wiley.com/doi/10.1002/qute.202000111

Skills sought: Interest in various aspects of microsystems: ASIC design (RF, mixed-signal), MEMS, hybrid packaging.

Project Investigator: Prof. Siddharth Tallur

Title of the project: **Low-noise and high-stability electronic systems for quantum sensors**

Desired specialization: EE 1 (Communication & Signal Processing), EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems)

Abstract of the project:

In this proposed PhD research, the student will join our team working on low-noise and high-stability electronic systems for quantum sensors. The research will involve investigation of error sources in field-deployed sensors (e.g. thermal drift, vibration, reliability and aging, in-field calibration drift etc.) and development of solutions with a goal of rugged implementations capable of robust performance in the field. Interested candidates may read our recent pre-print to get some idea of what will be involved in this research: https://arxiv.org/abs/2609.16901

Skills sought: Python, embedded C, RF circuit design, FPGA programming - HDL and HLS, PCB signal integrity and EMI design considerations, mechanical design and prototyping - some of these skills can also be picked up while pursuing PhD.

Project Investigator: Prof. Sudip Nag

Title of the project: **Bio-resorbable neural implants**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

Flexible, conformable, and bio-resorbable neural implants with AI integration.

Skills sought: Micro-fabrication (optional)

Project Investigator: Prof. Sudip Nag

Title of the project: **IoT systems for structural health monitoring of off-shore wind turbines**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

Industrial IoT system for harsh weather remote monitoring and reporting with AI+ML hardware.

Skills sought: PCB design

Project Investigator: Prof. Sudip Nag

Title of the project: **Engergy harvesting for neural implants**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:
Multi-domain and space constrained in-body harvesting systems for powering of edge-AI neural implants.

Skills sought: Optional: PCB or IC design.

Project Investigator: Prof. Sudip Nag

Title of the project: **Intelligent Neural Stimulator for Fully Implantable Prostheses**

Desired specialization: EE 5 (Electronic Systems), EE 6 (Integrated Circuit & Systems), EE 7 (Solid State Devices)

Abstract of the project:

AI, IC or PCB design for brain, nerve, and spinal cord. Animal studies.

Skills sought: Optional: PCB design, or IC design, AI/ML basics.

Project Investigator: Prof. V. Saravanan

Title of the project: **Design and Development of a Consent Management Platform for DPDP Act**

Desired specialization: EE 1 (Communication & Signal Processing, EE 5 (Electronic Systems)

Abstract of the project:

The Digital Personal Data Protection Act Rules 2025 place a significant burden on the data fiduciaries to implement and maintain a consent management platform. Small organizations may not have the resources to bear this burden. An open-source consent management platform will be an affordable solution for such organizations to comply with the DPDPA Rules 2025.

Skills sought: Cryptography, Java Programming, Web Development

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Project Investigator: Prof. Anshuman Shukla

Title of the project: **Development of Novel Energy Efficient, Compact, and Scalable Power Electronics Systems for Solar Power Plants**

Desired specialization: EE 3 (Power Electronics and Power Systems)

Abstract of the project:

The project aims to develop an efficient, scalable, and grid-supportive power conversion framework for solar PV systems using advanced modular and multilevel converter topologies, high-frequency conversion, and hybrid energy storage integration. The work will focus on improving energy extraction, power density, and conversion efficiency while enabling grid-connected, standalone, and grid-forming operation. Advanced control and energy management strategies will be developed for power smoothing, voltage and frequency regulation, and grid support. The proposed solutions will be investigated through modelling, simulation, hardware prototyping, and experimental validation, with emphasis on performance, reliability, scalability, and techno-economic viability.
