EE 735 Assignment 2

Simulating MOS Capacitors

Non Extendible Deadline: 4 Feb 2025 11:59 pm(100% Penalty for Late Submission)

Implement all codes using Python

Hints, assumptions, and instructions:

1. Please define all input variables at the beginning of your code and use proper comments while developing the code. Your code must work for other input values too.
2. Consider the body potential of the MOS Capacitor to be grounded.
3. Take the conduction band offset between Si and SiO_2 as 3.1eV.
4. It is mandatory to submit your code along with the report (in pdf) in a single zip file. Name the file `EE735_A2_RollNo_Name` for this assignment.
5. Reference for the assignment:
   - Taur, Y., & Ning, T. H. (2009). Fundamentals of modern VLSI Devices. Chapter 2, Sections 2.3.1 to 2.3.3
   - Vasileska, D., Goodnick, S. M., & Klimeck, G. (2017). Computational Electronics: Semiclassical and Quantum Device Modeling and Simulation. Chapter 4, Sections 4.1.1 to 4.1.7.
   - Solving a non-linear equation using Newton Rhapson Method: `https://www.youtube.com/watch?v=szQUIRPrAgQ`
   - Solving a system of non-linear equations: `https://www.youtube.com/watch?v=zPDp_ewoyhM`

Problems

Question1

Consider a NMOS Capacitor with a p doped Si substrate with doping $N_A = 1 \times 10^{17} cm^{-3}$ and thickness $t = 1\mu m$, SiO_2 as the dielectric material with oxide thickness $t_{ox} = 10nm$, and n+ doped poly-silicon gate (Consider the poly-silicon to be heavily doped such that $E_{f_m} = E_{c_m}$) and thickness $t_m = 10nm$.

A. Estimate the Flat Band Voltage and the Threshold Voltage for this MOSCap.

B. Plot the variation of the semiconductor surface potential (ψ_s) as a function of gate voltage.

C. Select 3 gate voltages such that the device will be in Accumulation, Depletion and Inversion respectively. Then for these three voltages carry out the following:

(i) Plot the potential versus distance in the substrate.

(ii) Plot the majority and minority carrier density versus distance in the substrate.

(iii) Plot the energy band diagram versus distance (gate, oxide, and substrate all included).

To get more accurate results use following equations for determining the semiconductor surface potential (ψ_s) and surface charge(Q_s).

$$V_{gs} = V_{FB} + \psi_s + \frac{Q_s}{C_{ox}}$$

$$Q_s = \pm\sqrt{2\epsilon_{Si}kTN_A}\left[\left(e^{-q\psi_s/KT} + \frac{q\psi_s}{kT} - 1\right) + \frac{n_i^2}{N_A^2}\left(e^{q\psi_s/KT} - \frac{q\psi_s}{kT} - 1\right)\right]^{0.5}$$

Question2

For the NMOS Capacitor defined in Question 1, generate High Frequency and Low Frequency C-V curves. Take the gate voltage range from -5V to +5V.

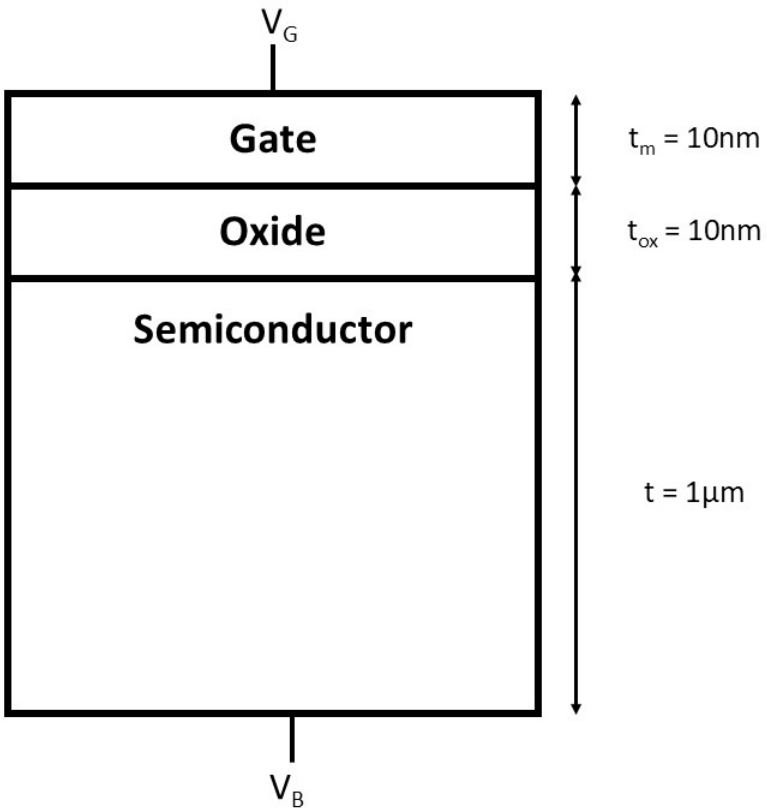

Figure 1: Structure for Q1 and Q2