Curriculum Vitae

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Dr. Hrishikesh Sharma

Objective

Carrying out both research as well as development of system designs, and design methods.

Areas of Interest

Algorithm-to-architecture mappings for various system specifications.
Design methodologies for platform-based system design.

Education

1994-1999 Indian Institute of Technology(IIT), Bombay

Integrated Master of Technology in Electrical Engineering
(Communications and Signal Processing as Specialization)

Thesis: Wavelet-based Approaches to Discrete Multitone Modulation, and its Implementation on DSP Processor

Advisor: Prof. V.M. Gadre

The aforesaid degree program is a time-shrinked B.Tech+M.Tech. equivalent program, with full courses and projects' load.

2008-2012 Indian Institute of Technology(IIT), Bombay

Doctor of Philosophy in Electrical Engineering
(High-level System Design, VLSI as specialization)

Thesis: Exploration of Projective Geometry-based New Communication Methods for Many-core VLSI Systems

Advisor: Prof. S. Patkar and Prof. S. Krishnan

Work Experience

A. TCS Innovation Labs, Tata Consultancy Services Ltd.

- 2004-2005 (Role: Researcher)

  Research on using scientific approach in system design methodologies. After detailed study, a taxonomic space representing the area system design was constructed, which was used to identify R&D opportunities for system-level design tools that are missing either production or in prevalence.

- 2005-2006 (Role: Lead Researcher)

  Tried to bridge algorithm-architecture gap for LDPC decoding using Karmarkar's architectural template, which uses finite projective geometry. Three individual patents were filed out of this project.

- 2006-2007(Role: Lead Researcher and Developer)

  European Union had sponsored a framework program to research about technologies for future wireless systems, similar to WIN effort by TIA. Such systems are envisaged to be runtime reconfigurable systems, and hence they need to make *intelligent* decisions. To design for this requirement, a core AI-based engine, using an extension to description logic was specified, designed and prototyped by me. More specifically, an ontology and a context interpretation framework, which is a logic-based reasoning engine, were developed by integrating various tools in Java language, to achieve a reasoning flow at runtime.

- Nov 2006- June 2007(Role: Participant and Reviewer in Supercomputer Design Discussions)

  A Tata group concern, CRL, was designing and developing the next generation supercomputer of India. The mathematics behind its envisaged structure was quite familiar to me. Hence I was invited for participation and reviewing in some of the design discussions by their core technical team.

- 2008-2011(Role: Sponsored Ph.D. Candidate)

  Have carried out full-time research work towards my doctoral thesis, while being on campus at IIT Bombay.

- 2012-till date(Role: Lead Researcher)

  Application of Forward Error Correction Techniques in Networks related to Ubiquitous computing.

B. Mobile Platforms Solution Division, Sasken Communication Technologies Ltd.

- 1999-2003(Role: Technical Leader as the major role)

  MobiTAAL® Middleware framework for GSM/GPRS/3G mobile phones. R&D work included futuristic conceptualization, detailed specification and development of middleware for mobile systems based on GSM Evolution Technologies. For details, please see attachment 1.

- May 2001-Oct 2001(Role: Project and Technical Leader)

  R&D work included defining, designing and complete implementation of a unified architecture for multi-configuration mobility management subsystem. For details, please see attachment 1.

Miscellaneous Projects

- Design of various GUIs, in VC++/Java, for testing/demonstrations.

- Design of a support tool for change management (cMoN) using bash scripting.
- Design of a tool to extract function call graph from any type of `C' software, using Lex/C.

Academic Advising

- Have guided 4 M.Tech. projects full-time, 3 M.Tech. projects part-time, and 2 B.Tech projects full-time between 2003-2012.

Patents Filed

1. An Efficient Decoder for Regular LDPC codes. 176/MUM/2007. January 2007.
2. A Decoder for Regular Split-Extended LDPC codes. 177/MUM/2007. January 2007.
3. A Decoder for regular LDPC codes with folded architecture. 205/MUM/2007. February 2007.
4. Method and System for Error Control Coding using Expander-like Codes. 2455/MUM/2010, September 2010.
5. Real-time, Reliable Transmission Scheme for Urgent/Critical Data in Internet of Things. In process of Patenting, September 2012 (expected).

Publications

1. *High Throughput Memory-efficient VLSI Designs for Structured LDPC Decoding.* Hrishikesh Sharma et al. 2011 International Conference on Pervasive and Embedded Computing and Communication Systems.
2. *A Folding Strategy for DFGs derived from Projective Geometry based graphs.* Swadesh Choudhary, Tejas Hiremani, Hrishikesh Sharma and Sachin Patkar. 2010 International Congress on Computer Applications and Computational Science.
3. *A Design Methodology for Folded, Pipelined Architectures in VLSI Applications using Projective Space Lattices.* Hrishikesh Sharma and Sachin Patkar. Submitted to Elsevier Journal of Microprocessors and Microsystems: Embedded Hardware Design.
4. *Finite Projective Geometry based Fast, Conflict-free Parallel Matrix Computations.* S.N. Sapre and Hrishikesh Sharma and Abhishek Patil and B.S. Adiga and Sachin Patkar. Submitted to International Journal of Parallel, Emergent and Distributed Systems.
5. *Optimal Folding of Data Flow Graphs based on Projective Geometry.* Swadesh Choudhary and Hrishikesh Sharma and Sachin Patkar. Submitted to World Scientific Journal of Discrete Mathematics, Algorithms and Applications.

6. *Expander-like Codes based on Finite Projective Geometry.* B.S. Adiga and Swadesh Choudhary and Hrishikesh Sharma and Sachin Patkar. Submitted to IEEE Transactions on Information Theory.
7. *A Context Interpretation Framework for Cognitive Network Devices.* Hrishikesh Sharma and Balamurali P. International Conference on Software-defined Radio, 2007.
8. *A Service-oriented Architecture Approach to Multimedia Applications.* Hrishikesh Sharma and Subramanian P.S. National TACTICS Conference, 2006.

I have also formally refereed 3 articles for IEEE International Global Communications Conference, 2012 (and few more informally, for another conference).

Thesis

A. Doctoral Thesis (Exploration of Projective Geometry-based New Communication Methods for Many-core VLSI Systems)

Used the geometric structure of finite projective geometry to evolve a family of interesting bipartite graphs. Such graphs were then further used to design many communication subsystems for various VLSI systems.

B. Master's Thesis (Wavelet-based Approaches to Discrete Multitone Modulation, and its Implementation on DSP Processor)

Involved study and usage of wavelet transforms in the modulation scheme, to boost the signal recovery performance. Studied various wavelet transforms, and chose one to be used. Implemented, tested and noted performance results for the modulator and demodulator on digital signal processor, TMS320C50.

Awards and Honors

- Performer of the Quarter, April-June 2000, Silicon Automation Systems.
- Was awarded the National Talent Search Examination Scholarship in 1992.
- 14th in overall merit list in UP Board Secondary Education Exams, 1992.

References

1. Ramprasad Moudgalya. Email id: ramp.ramp@gmail.com
2. Dr. Sunil Sherlekar. Email id: sunil.d.sherlekar@gmail.com
3. Prof. Sachin Patkar. Email id: patkar@ee.iitb.ac.in

Annexure 1(Work Details at Sasken Communication Technologies Ltd.)

A. MobiTAAL Middleware Framework for GSM/GPRS/3G Mobile Phones

Contribution

The ETSI/3GPP standardization for GSM/GPRS/3G protocol stacks define upto layer 3, or networking aspects. Much more components go into making of an entire mobile system that can be used by various mobile applications. In general, technical knowledge of such components is proprietary technologies of various companies, which design such systems.

I was entrusted with futuristic conceptualization, detailed research and development of the middleware part for the mobile systems. My role in program was the following.

- Complete technical responsibilities for the program
- Technical interfacing with various customers for the project
- Creating and mentoring the tem into proprietary technology handling
- Individual contributions as the technical leader for this program

I have given following contributions to this program.

- Formal Problem Specification. I was able to provide theoretical framework for the entire work, based on notions of service and service capabilities.
- Creating a holistic requirement specification for the product. This was verified and approved by various customers.
- Creating a scalable architecture of the middleware platform. The overall platform design was approved by National Semiconductor Corporation, and the same customer immediately launched a demo phone using the first-cut platform we provided. The overall architecture was developed jointly.
- R&D of the separate but co-existing SIM application toolkit. The salient feature of this toolkit was a real-time event scheduler having a novel priority-based, non-preemptive scheduling algorithm, and a complex interpreter for context-dependent grammar of SIM command suites.
- Designing an entire API specification, first time, for the mobile platform.

B. Multi-configuration Mobility Management Entity Design and Development

Contribution

Mobility Management Entity is one of the most complex entities of any mobile system. For the GSM/GPRS/3G product line, multiple protocol stack specifications required multiple configurations of mobility management as well. It was felt that single unified software architecture should be possible for all six required configurations. Based on my research, I came up with the unified architecture. Subsequently, I also got the entity developed under my leadership.