Device Design & Optimization of Nanoscale FinFETs using 3D TCAD simulations

Presentation

by

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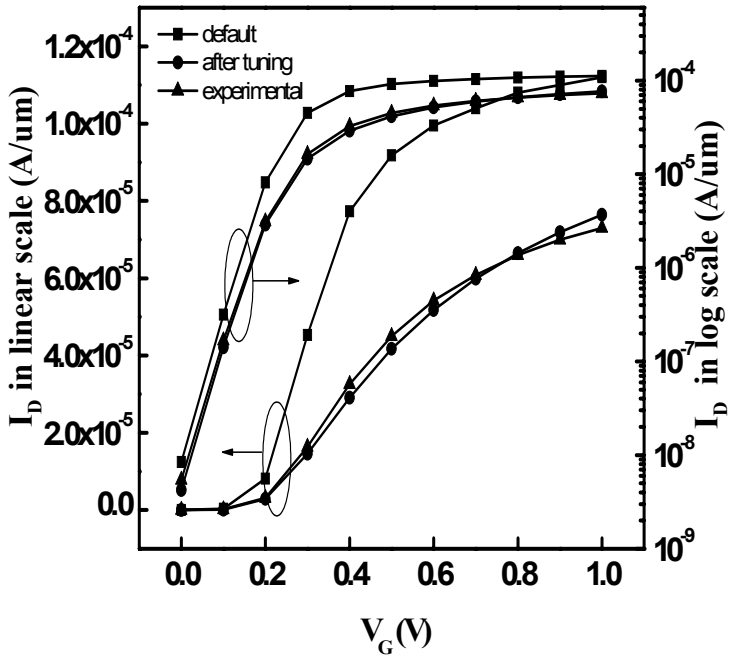
Outline

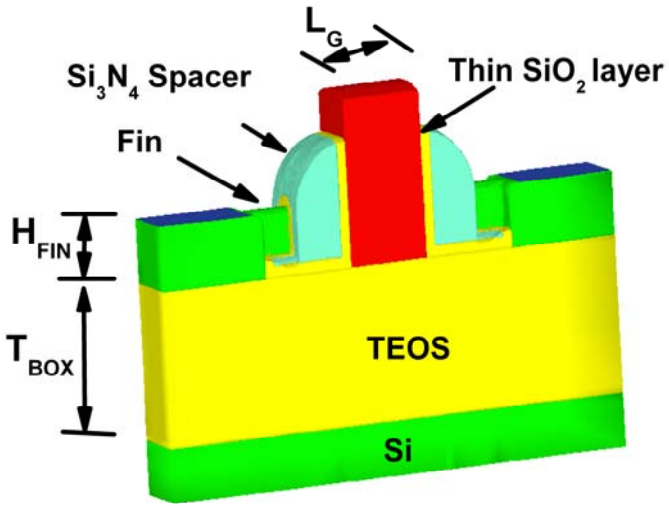
- TCAD Tuning for FinFETs
- High-K FinFETs Simulations
- Bulk FinFETs Optimisation study
- Fin pitch and Parasitcs
- FinFET vs Planar parasitics
- Conclusions

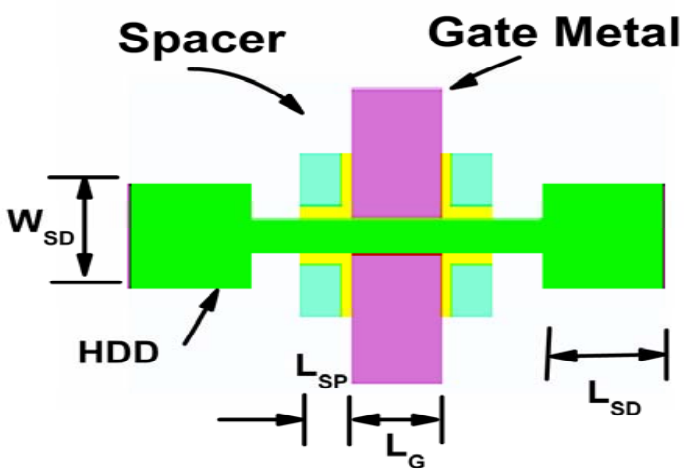
TCAD Tuning for FinFETs



- FinFETs current flow plane different from conventional planar MOSFETs
- TCAD tool use default 100 plane mobility
- So tuning the mobilty to account for plane of conduction is essential for FinFETs.
- μ & ρ are tuned mainly to achieve matching

3D process structure & 2D cut plane

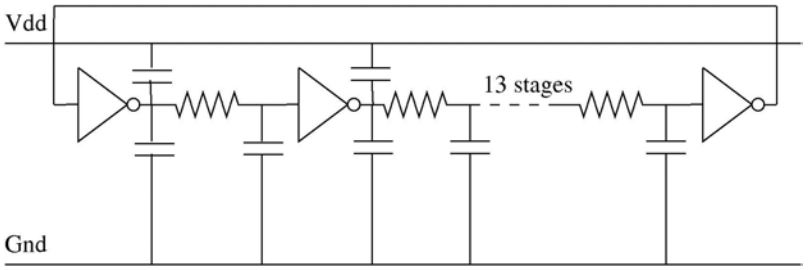


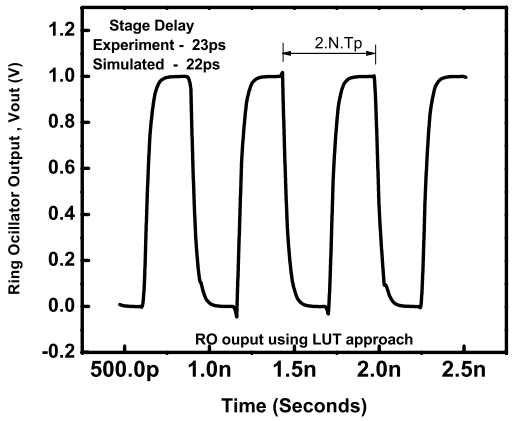


3D and 2D view of the process simulated FinFET structure

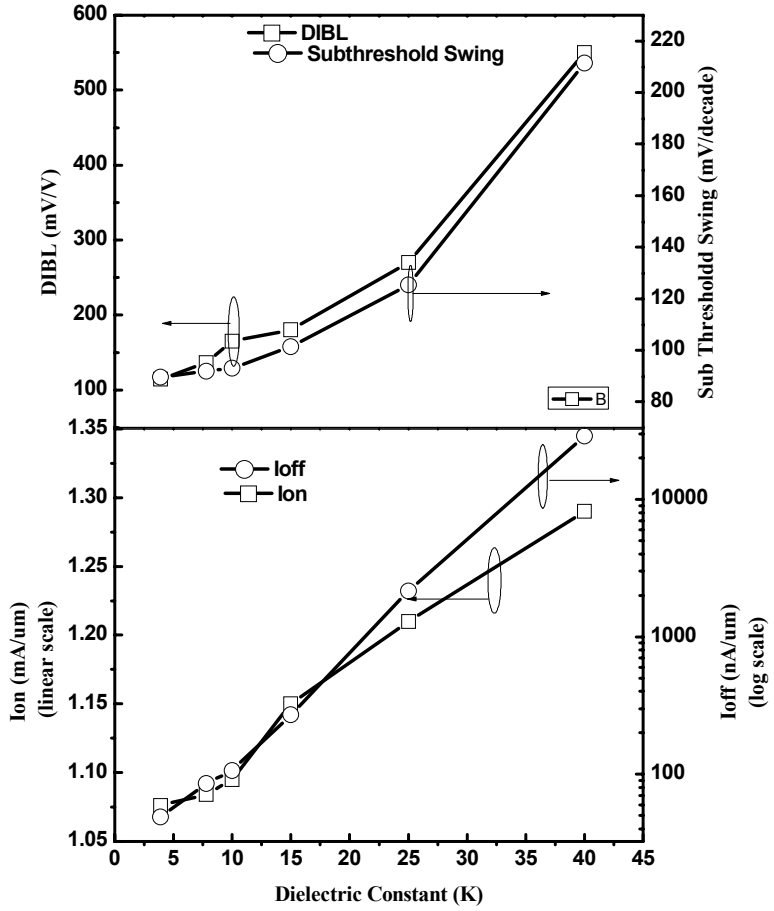
Circuit Simulations

- LUT was generated for the matched devices.
- Sequel simulations done for RO
- Parasitic capacitance was extracted from the layout, ploy resistance was estimated from the length of the poly and its doping level.
- Simulations matched close to expt result



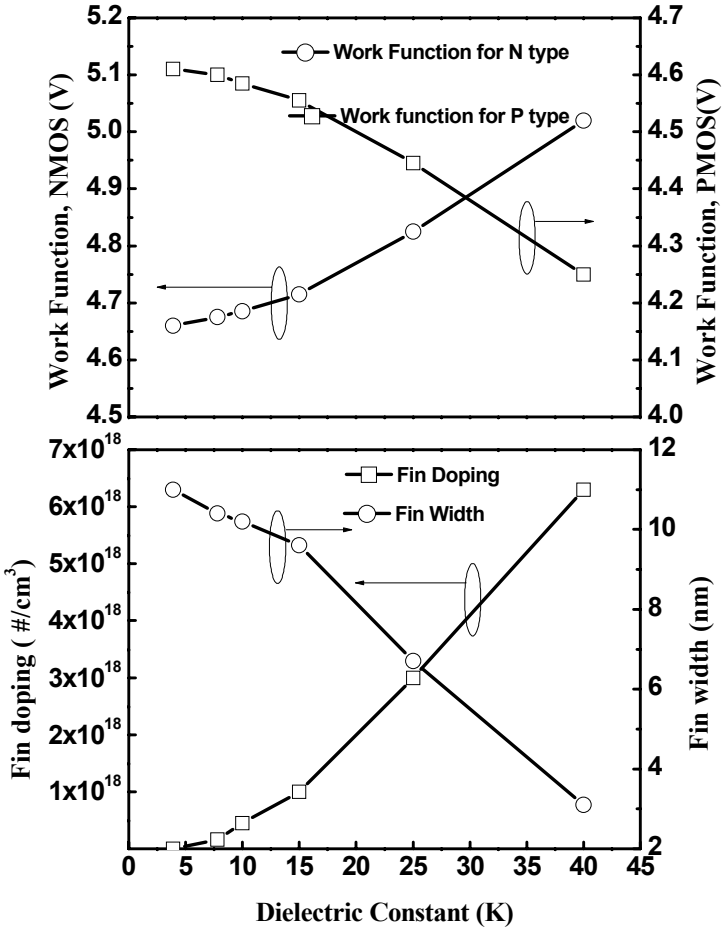


High-K FinFET simulation Results



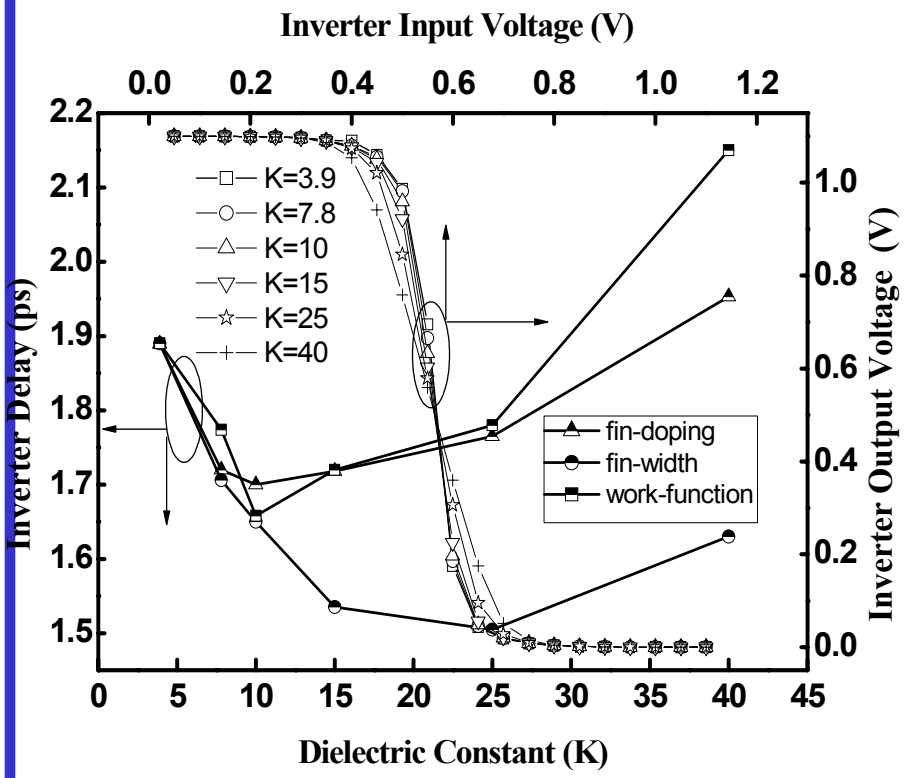
- K=3.9 (SiO2), 7.8 (Si3N4), 11.7 (Al2O3), 15 (LaAlO3), 25 (HfO2) and 40 (TiO2) with EOT being 1.1 nm simulated
- SCE effects worsen due to Fringing Fields, (more noticeable for higher- K values)
- Needs Vt adjustment to make iso-I_{off} comparison

High-K FinFET simulation Results



- Fin doping, Fin width & work function adjusted to keep iso-I_{off}
- Fin width scaling gives the optimum K for high –K circuit applications
- Work function range required may be large.

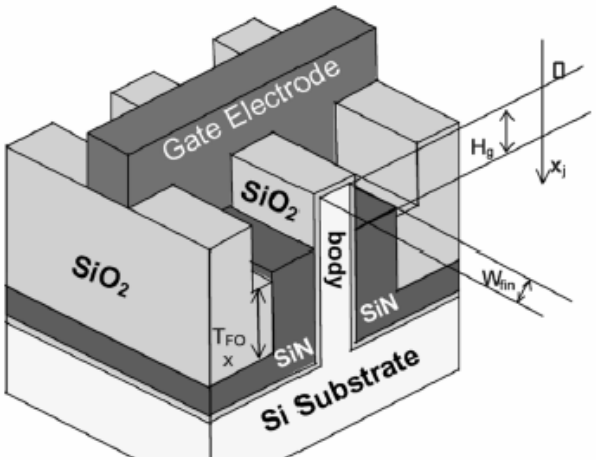
Impact of High- K on FinFET Circuit Performance

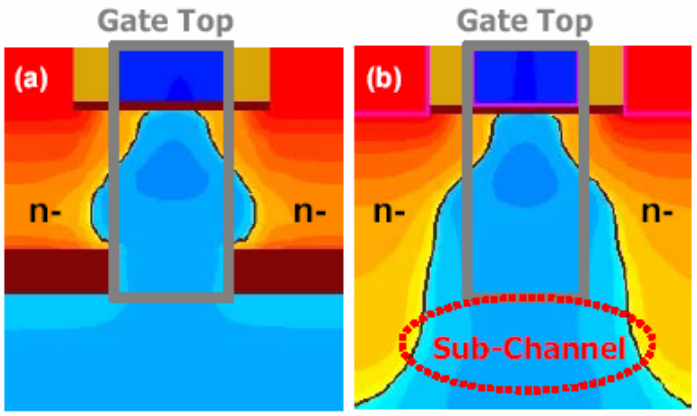


IEEE Electron Device Letters, April 2007

- Degradation in Noise Margins for Digital Applications
- Improved Speed compared to SiO2
- Optimum K is around 20-25, (Hafnium)

Bulk FinFETs

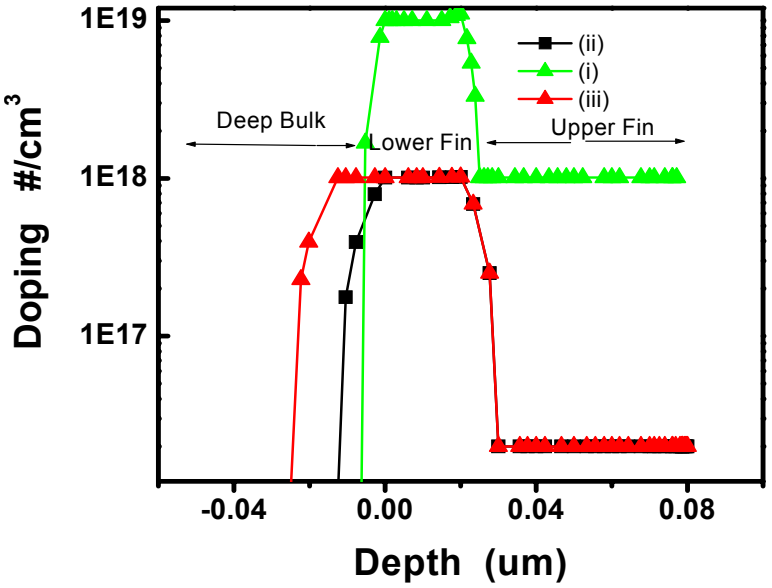


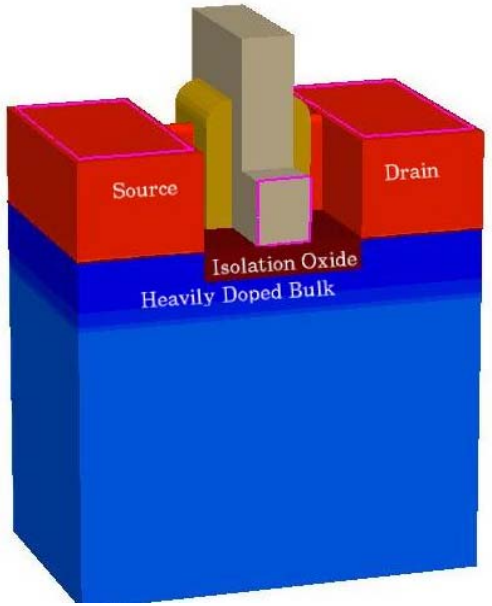


IEDM 2006

- They are very leaky without anti punch through (body doping)
- So body doping has been proposed as make it viable from leakage perspective

Body doping profiles

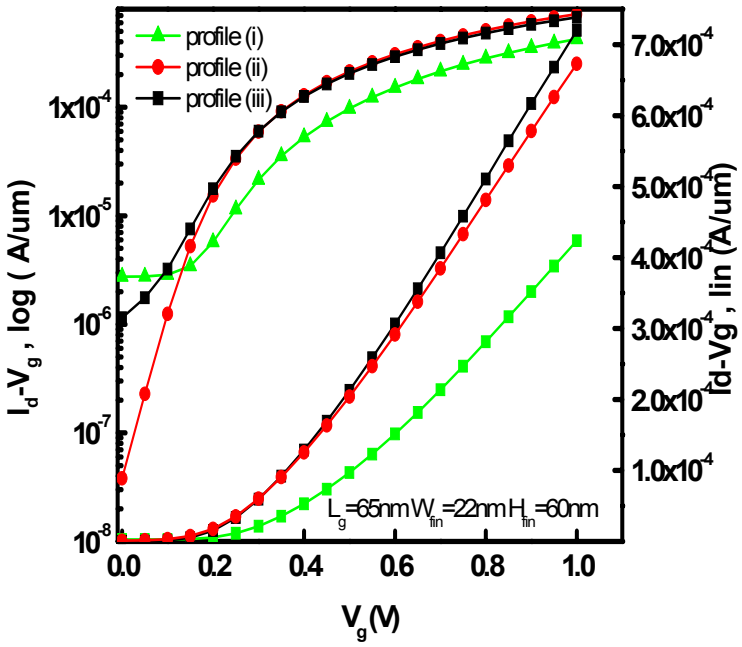




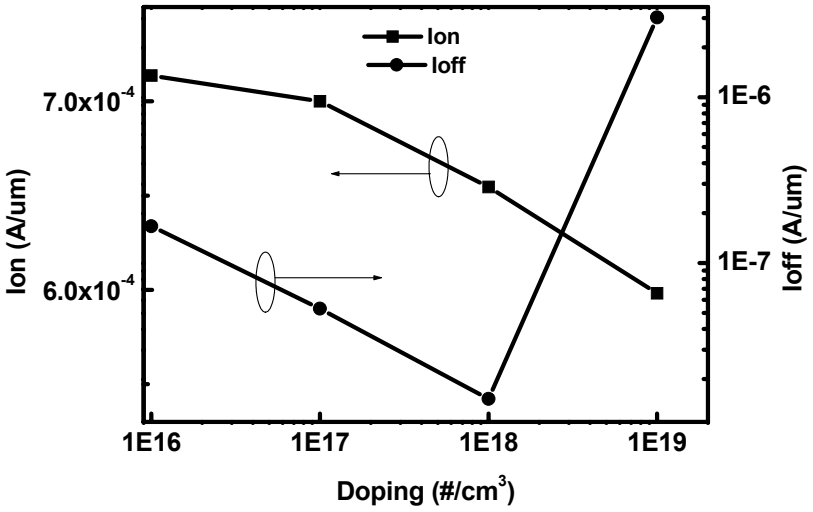
Optimized doping profile can give better Ioff in Bulk FinFETs

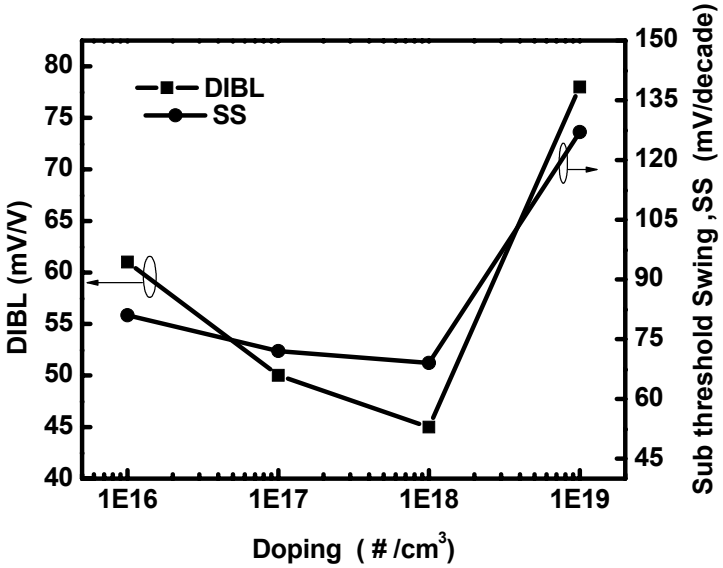
Body doping profiles

- Reported profiles show heavy leakage current due to BTBT
- Profile (ii) and (iii) gives much better DC performance



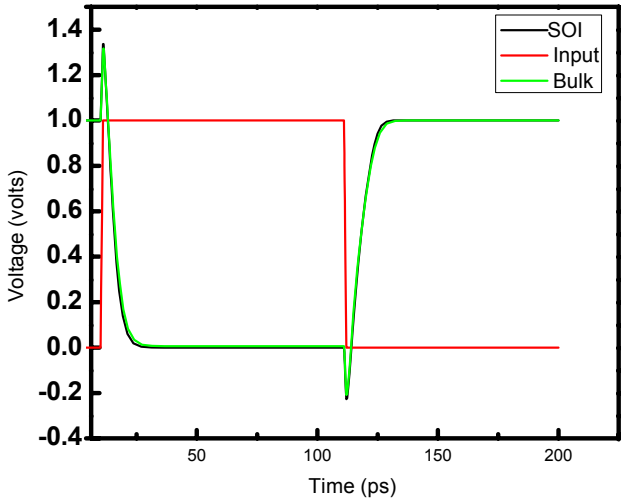
Optimum body doping

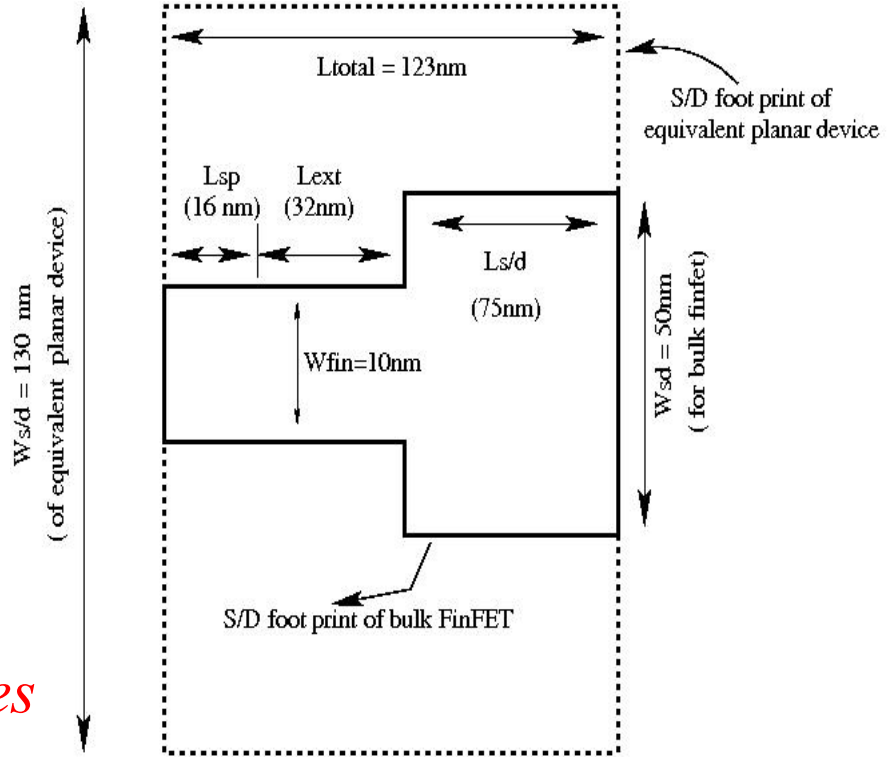




Higher anti punch through (APT) doping always not beneficial.
There exists an optimum APT doping owing to BTBT

FinFET's Transient Performance

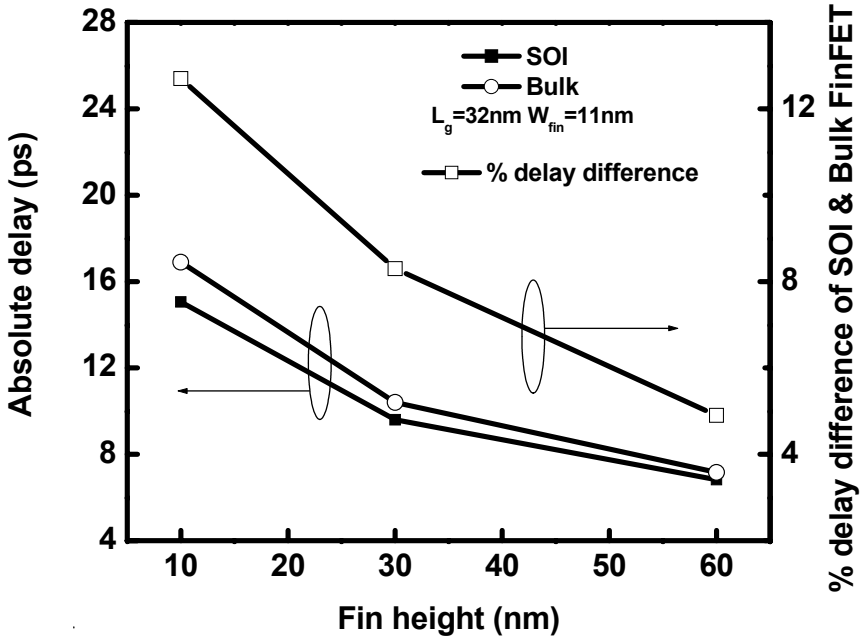




IEEE Trans. on Electron Devices 2008 FEB

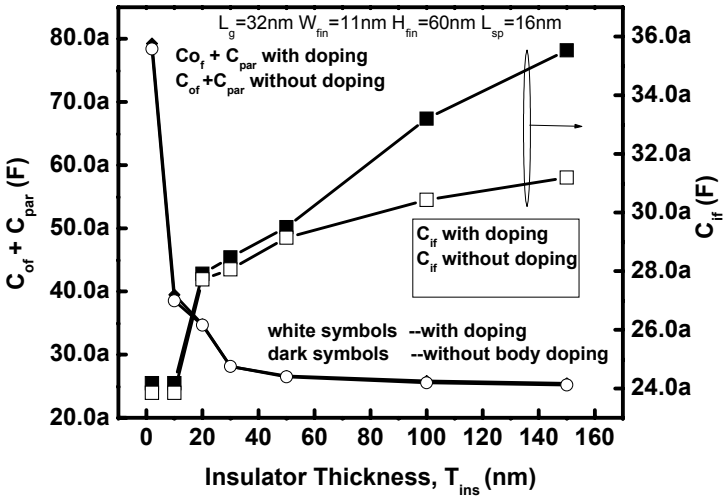
Bulk FinFETs have same performance as SOI FinFET unlike planar counter parts. Verified by layout rule based calculations.

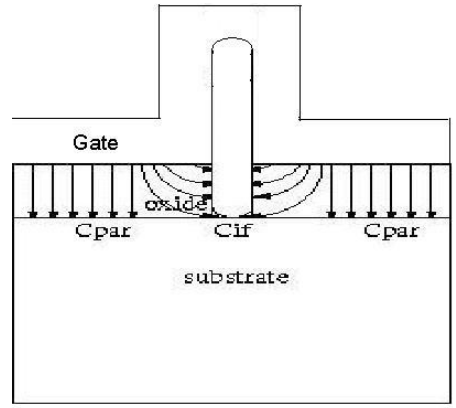
FinFET's Transeint Performance

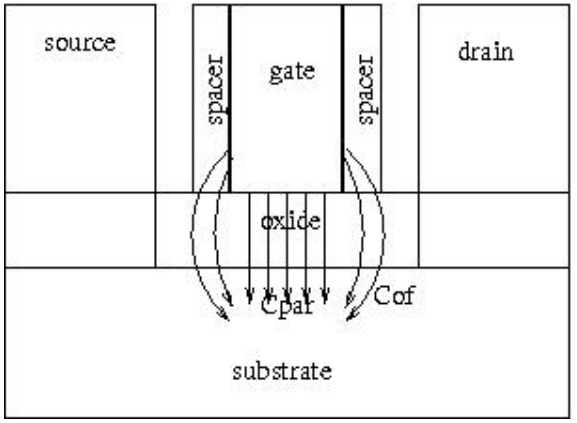


Performance advantage significant for taller fins, owing to lesser junction capacitance.

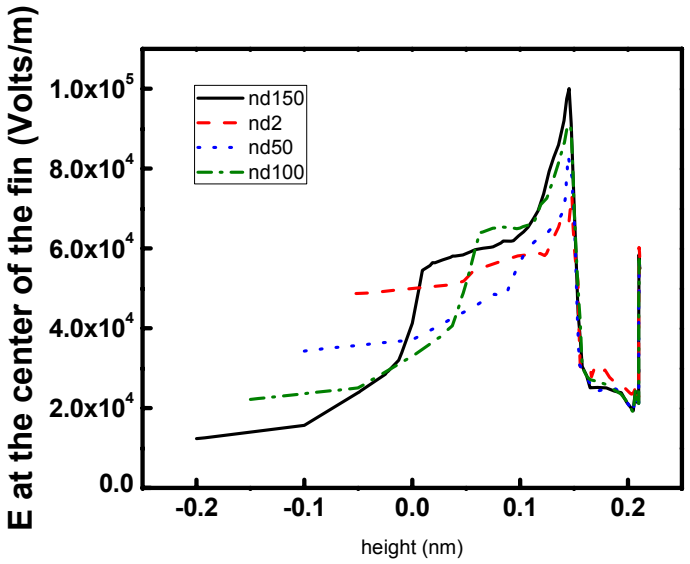
Impact of STI height

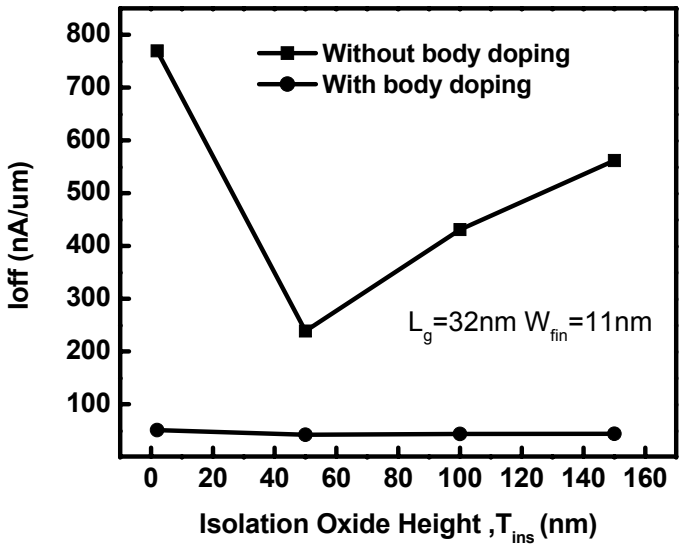






Impact of STI height





Parasitics Modeling

$$C_{pp} = \frac{2\varepsilon_{ox} H_{sd}}{L_{ext}}[P - W_f - 2T_{ox}]; T_g > H_{sd}$$

$$C_{ff} = \frac{2\varepsilon_{sp}}{\pi}\ln(1 + \frac{T_g}{T_{ox}})[2H_f + W_f]$$

$$C_{if} = \frac{2\varepsilon_{ox}}{\beta}\ln(1 + \frac{T_{f\sin\beta}}{2T_{ox}})[2H_f + W_f]$$

$$C_{pf} = \frac{4\varepsilon_{sp}}{\pi}\ln(1 + \frac{L_g}{L_{ext}})[P - W_f - 2T_{ox} - 2T_g]$$

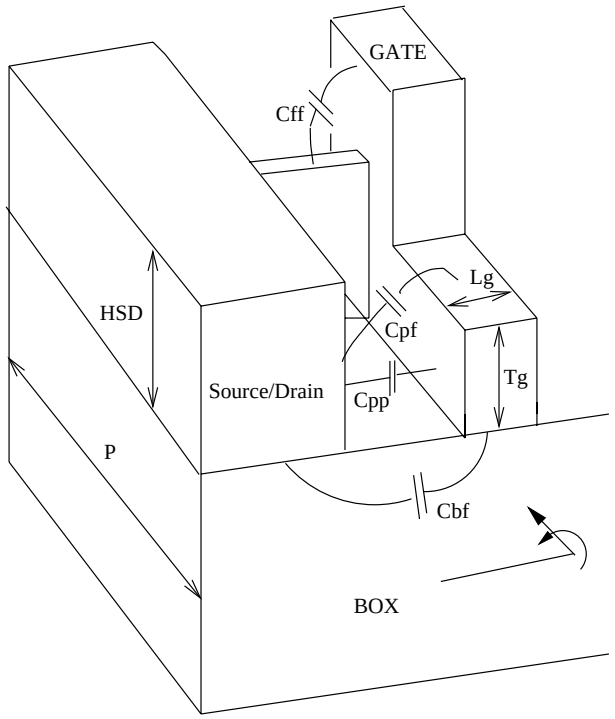
$$C_{bf} = \frac{\varepsilon}{\theta}\ln(\frac{d_2}{d_1})[P - 2T_{ox} - W_f]; d_1 = \frac{L_{ext}}{2}, d_2 = \frac{L_g + L_{ext}}{2}$$

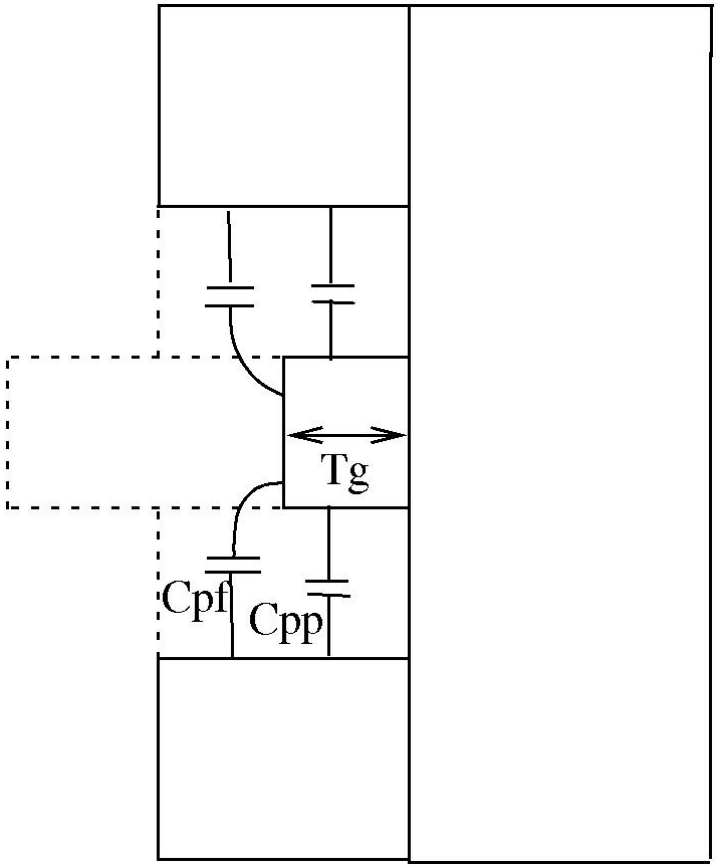
Simulation =8.151e-17

Modeling=8.8e-17

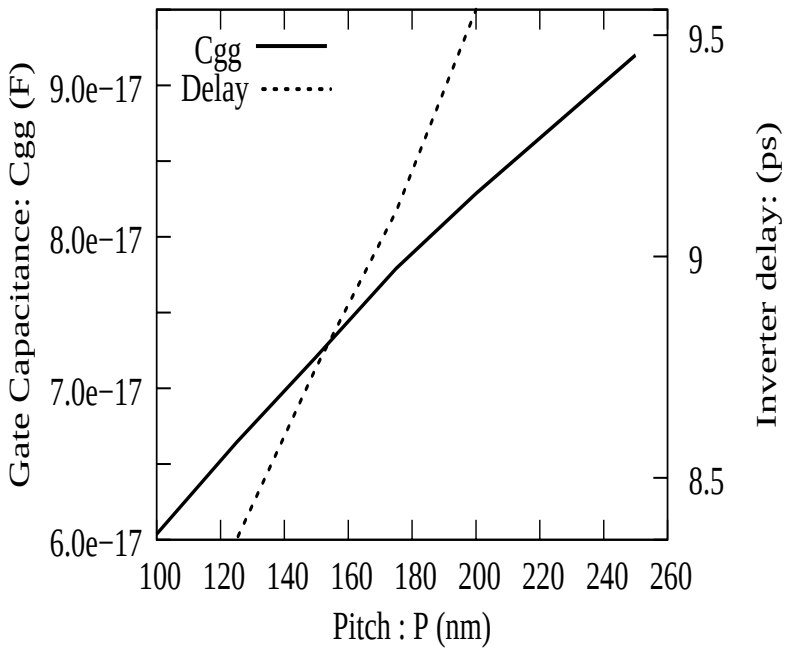
For P=200nm

Fin Pitch Parasitics





Impact of Pitch



Slope =0.2124fF/um

Model=0.275 fF/um

$$\frac{\delta C_{para}}{\delta P} = \frac{\delta C_{fringe}}{\delta P} + \frac{\delta C_{pp}}{\delta P}$$

$$= \frac{2\varepsilon_{ox}[T_g + \frac{L_g}{2}]}{Lext}$$

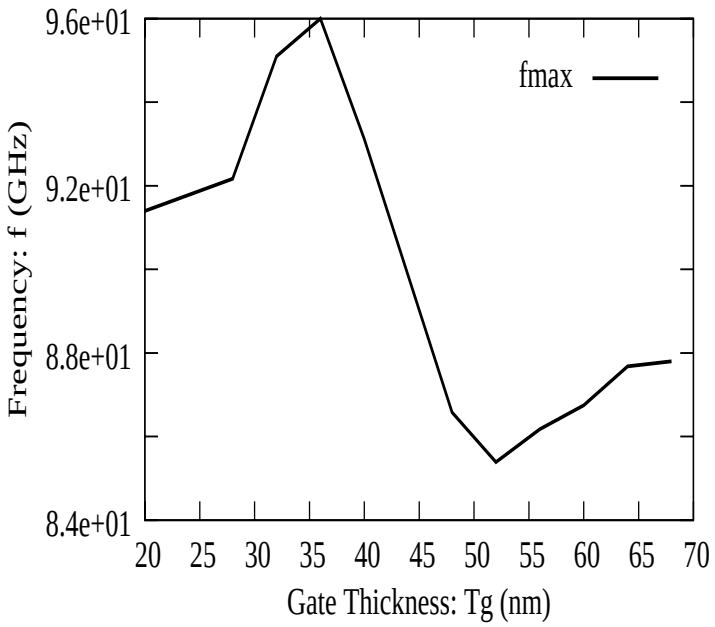
$$+$$

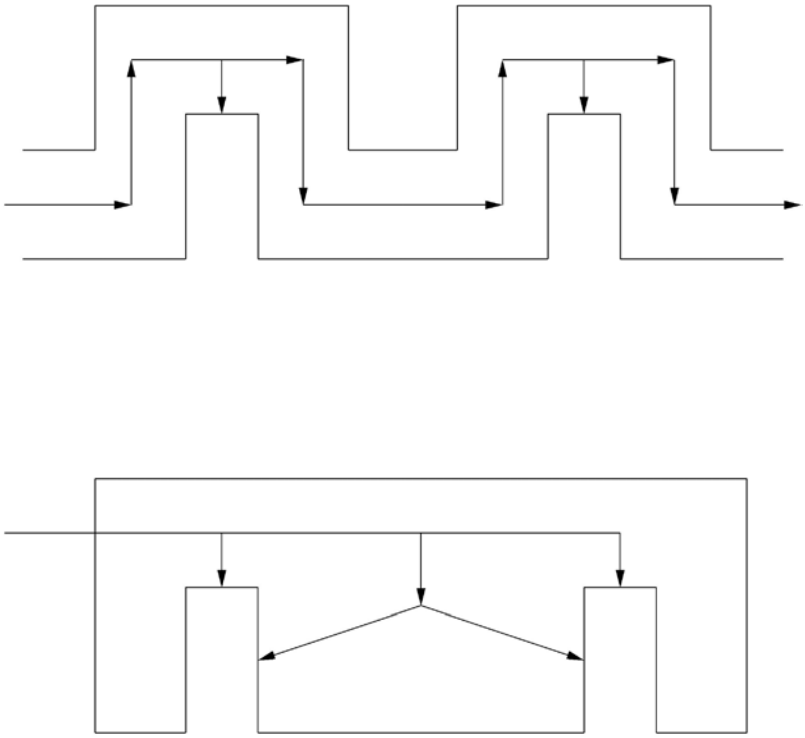
$$\frac{4\varepsilon_{ox}}{\pi}[\ln(1 + \frac{L_g}{2L_{extn}})]$$

$$+$$

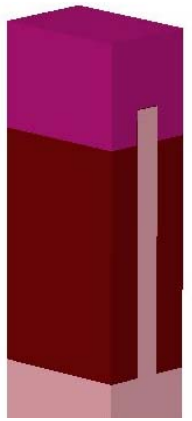
$$\frac{2\varepsilon_{ox}}{\pi}[\ln(1 + \frac{T_g}{2L_{extn}})]$$

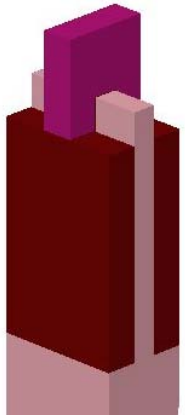
Patterned gate

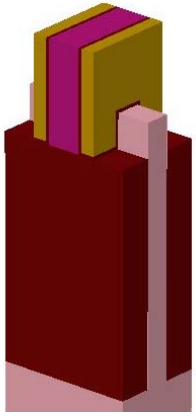


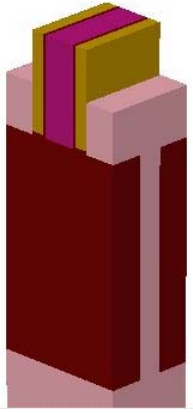


Bulk FinFET Process Flow ..

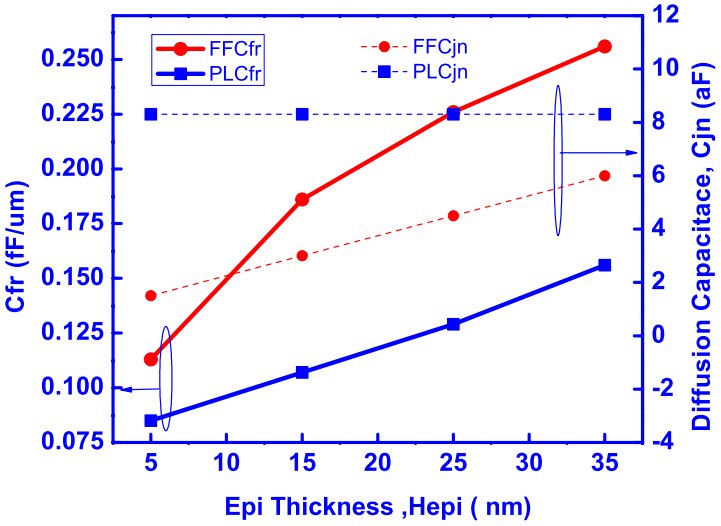


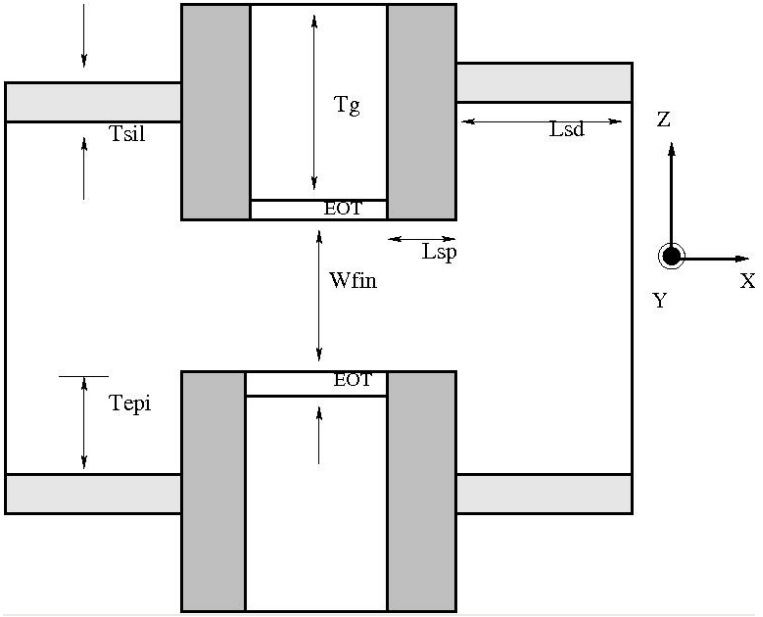






Epi thickness vs Delay

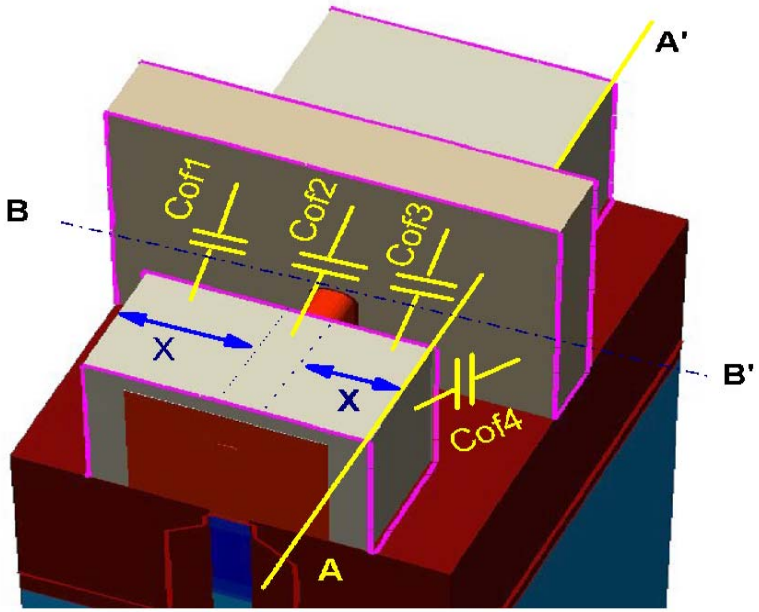




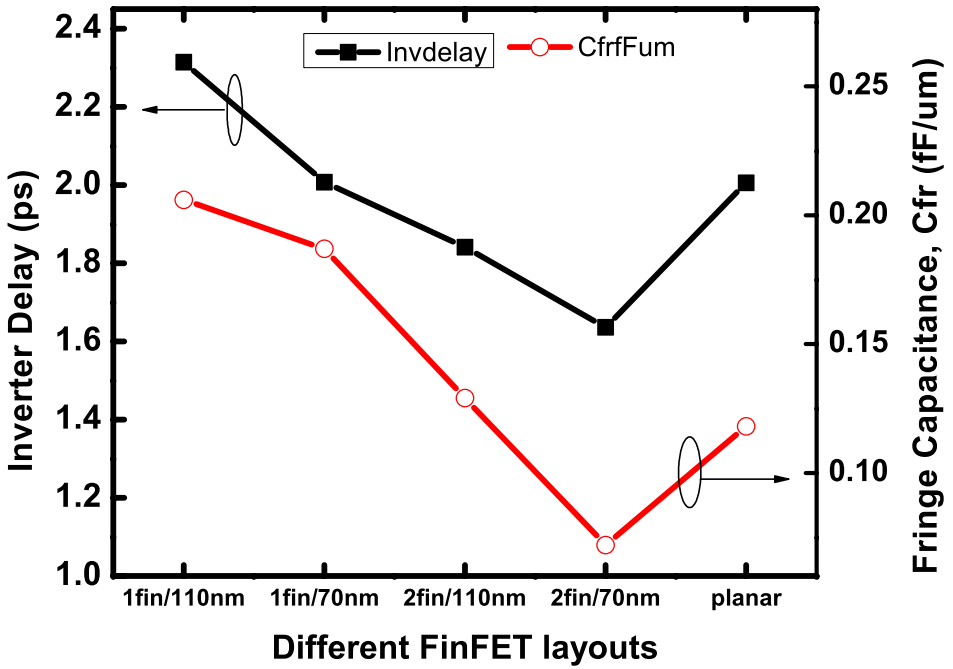
FinFETs fringe parasitics (Cfr) almost 100% more than equivalent planar devices!. But junction capacitance is lesser than planar device.

Additional Parasitics in 3D

- Extra increase in Cfr is clear from the 3D picture.
- Cof1 & Cof3 are extra in FinFETs.
- In planar these additional components will get normalized by Weff. (effective width). But in FinFET they simply gets added to the total Cfr.



Delay/ Fringe Comparison

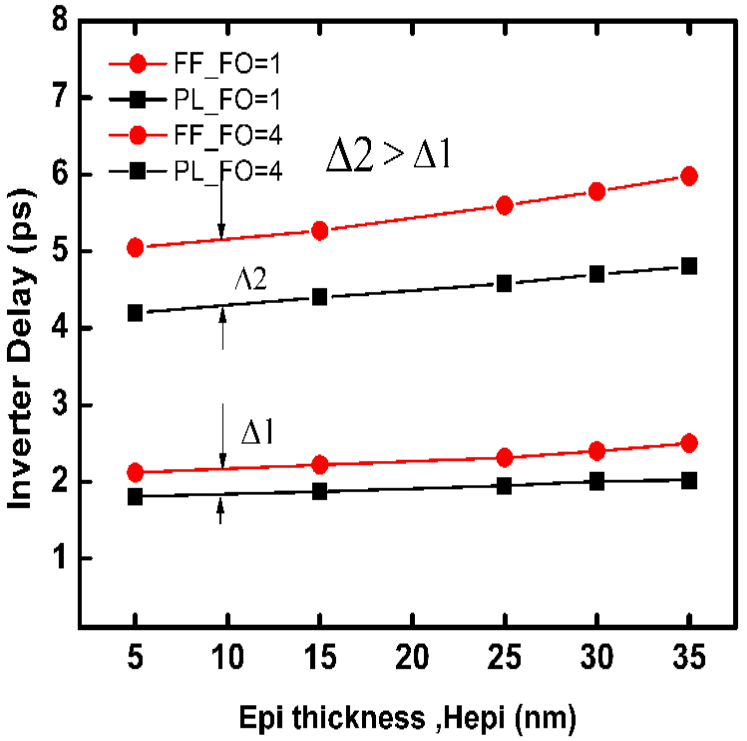


- Current ITRS picth (110nm) over estimates the dealy.
- Aggressive fin pitch reduction essential for making FinFETs performance competent.

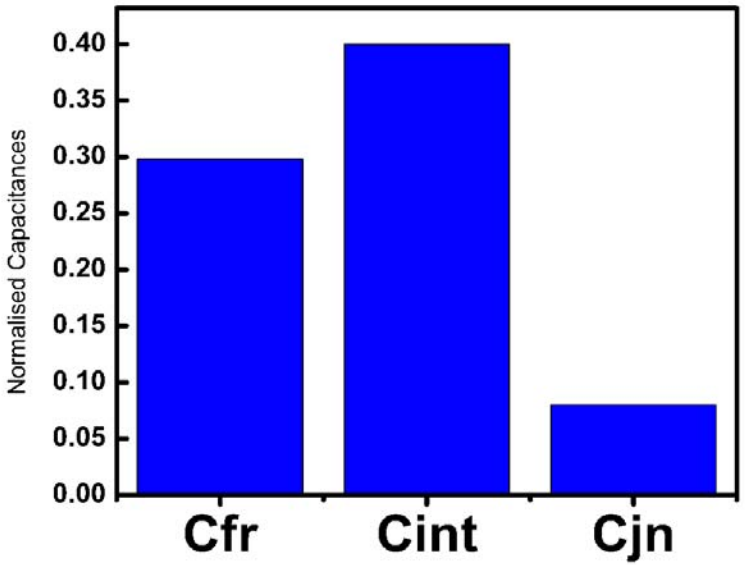
1fin with 110nm pitch gives poor performance than planar. 2fin with 70 nm pitch makes it superior.

Impact of Cfr- Comparison FinFET/Planar (22nm node)

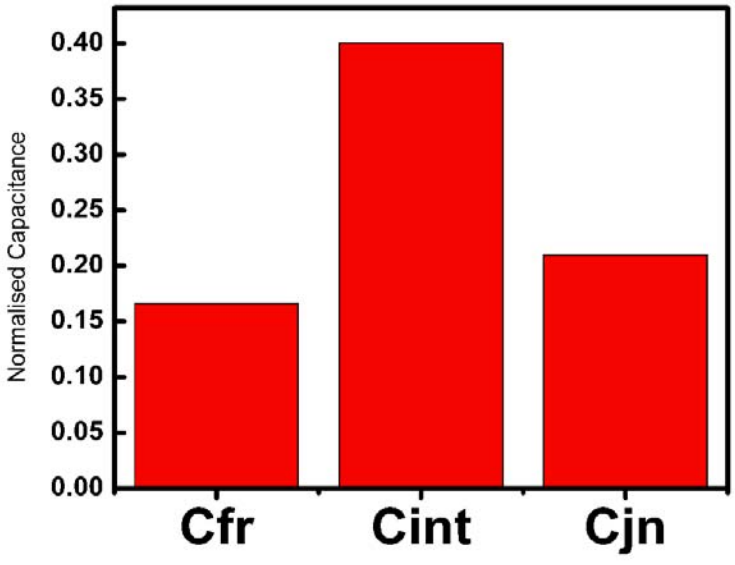
- Enhanced Cfr will cause the performance of FinFETs to be inferior to eqvt planar device (22nm node).
- More serious issue for large fanout circuits



Comparison with planar

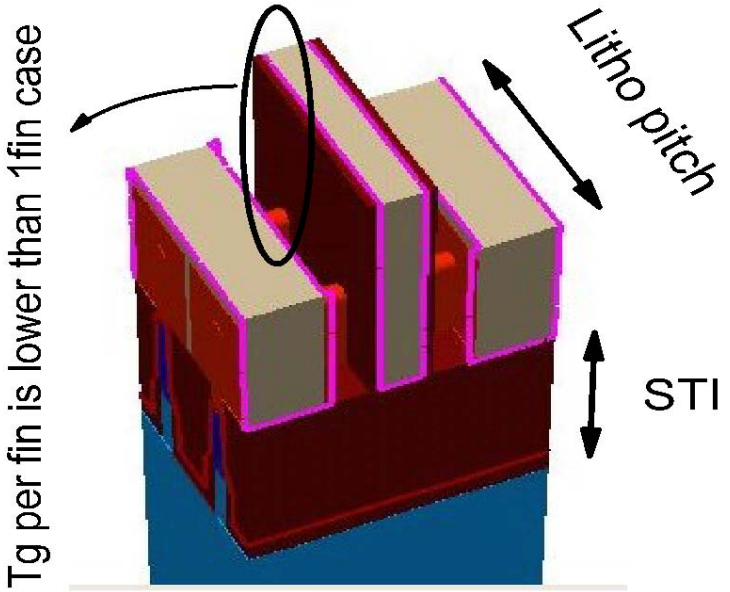


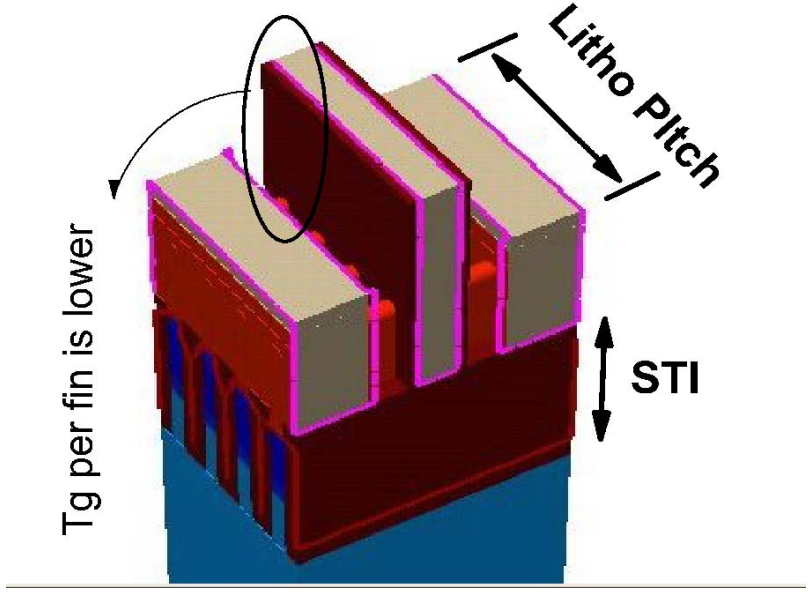
FinFET



Planar

Solutions -Spacer Fins





Packing two or more fins in a single pitch will reduce the total parasitics

Electrical Method for Bottom Fin Doping Extraction

- Bottom fins are difficult to be doped as uniform as the top fin.
- Insufficient doping increases ON resistance
- SIMS may fail in thin fins
- We need a easier method to profile the doping value at the fin bottom

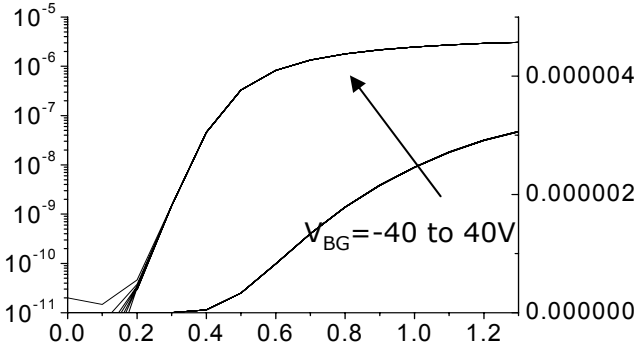
Electrical Method for Bottom Fin Doping Extraction

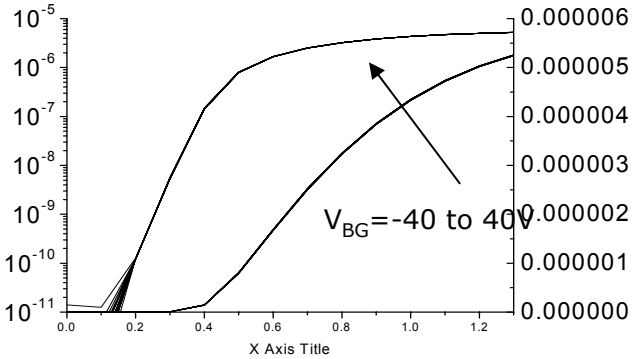
Vd = 50mV

Tilt 10

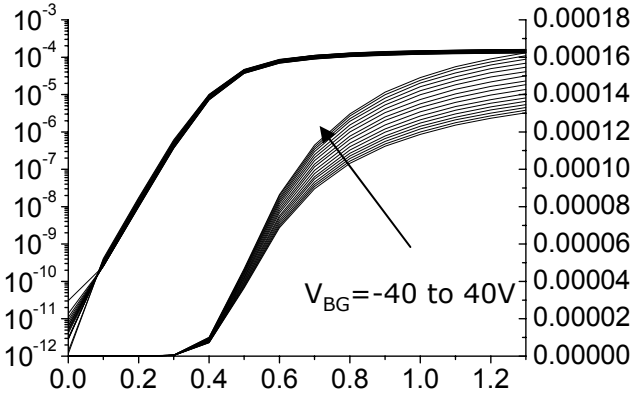
Tilt 45

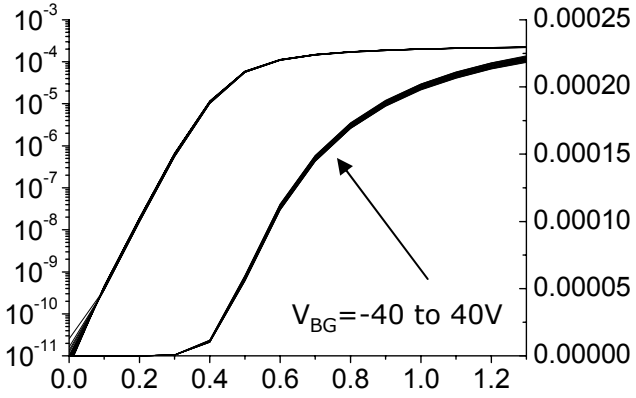
L_G = 10um





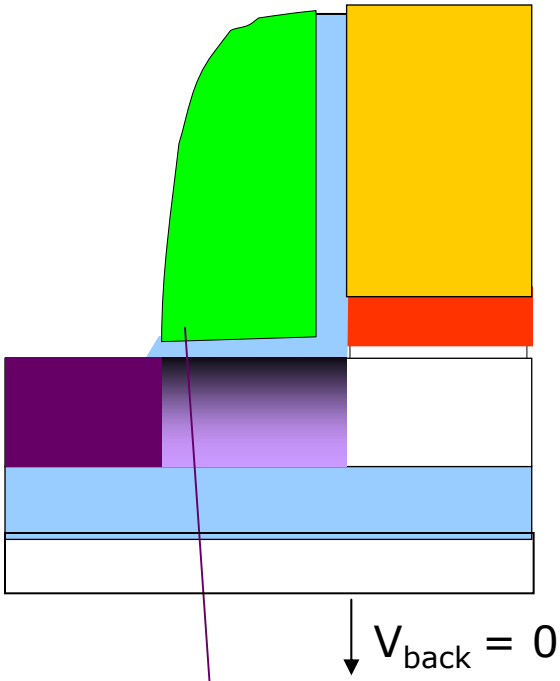
L_G = 110nm



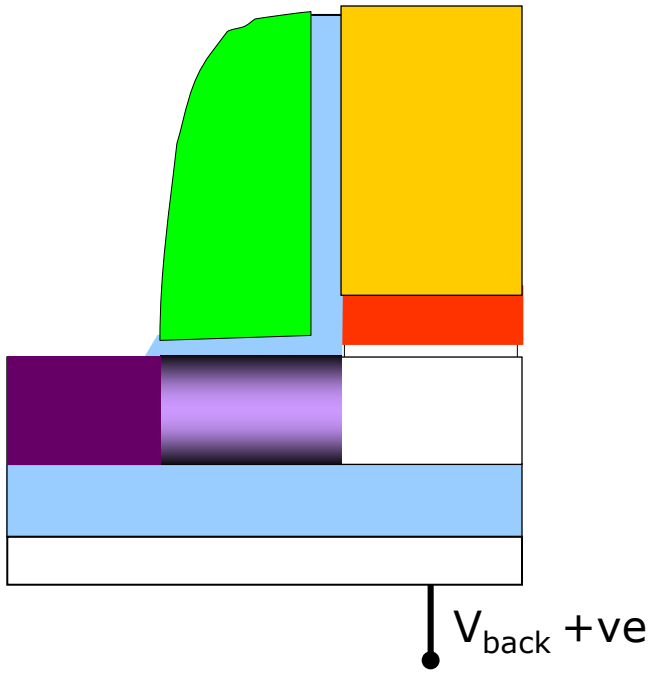


FinFETs Id-Vg with substrate voltage varied from -40 to +40V

Conceptual Model: NMOS

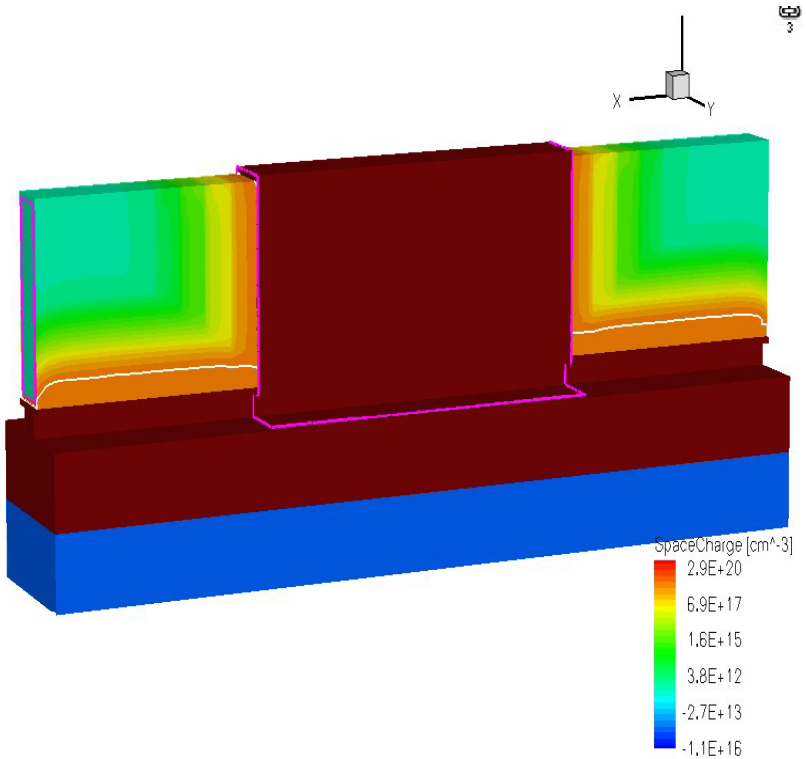


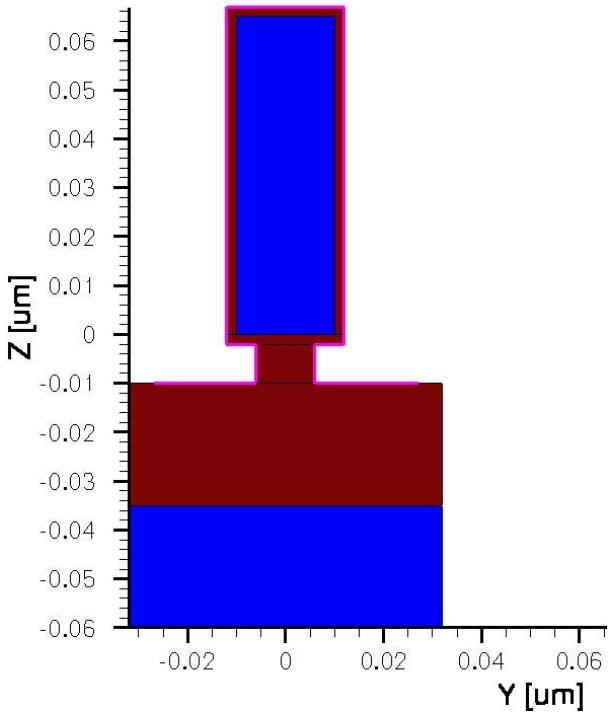
N+ extension high dose at the top



- A positive (negative) bias on the back gate causes accumulation (depletion) of electrons at the extension – BOX interface
- The channel is fully under gate control when the fins are narrow enough

Verification by 3D simulations





Depletion in bottom fin changes resistance and thus Ion (but not Ioff as channel not affected).

Extension Doping Implants

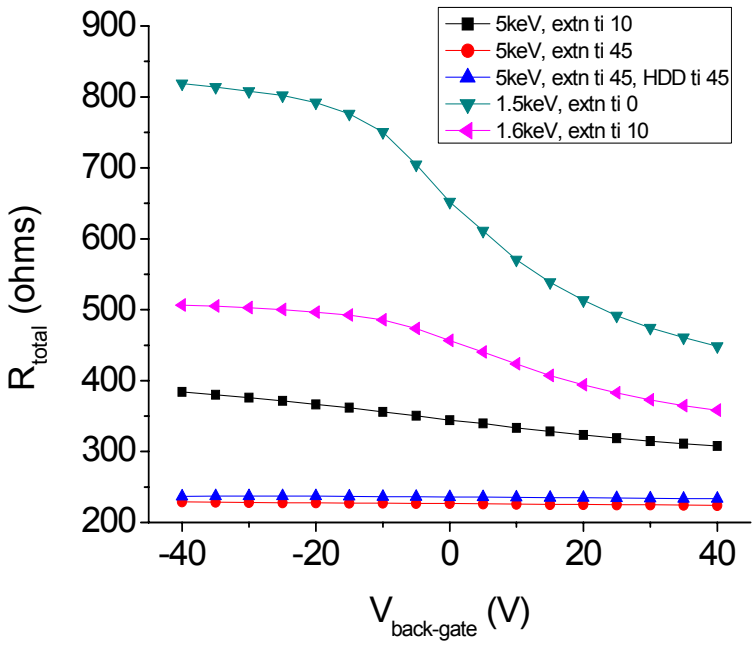
D03 5keV , 10°

D05 5keV , 45°

D08 5keV , 45°, , HDD ti

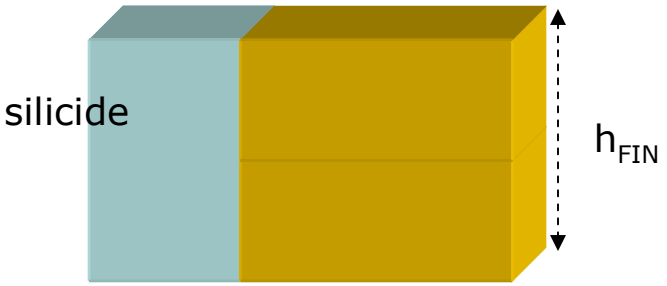
D09 1.5keV , 0°

D03 1.6keV , 10°



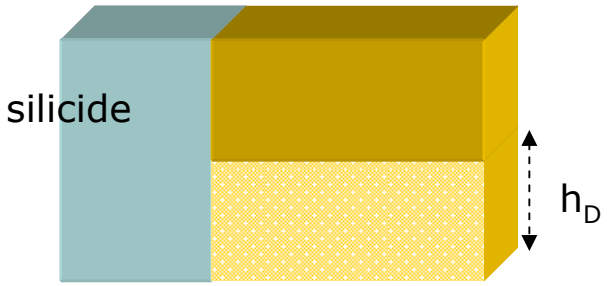
Rsd sensitivity for different wafer lots with different energy and tilt

First Order Model



Extension with a positive bias on the back gate

$$R_{ext} = \frac{\rho_{ext} L_{sp}}{h_{fin} W_{fin}}$$



Extension with a negative bias on the back gate

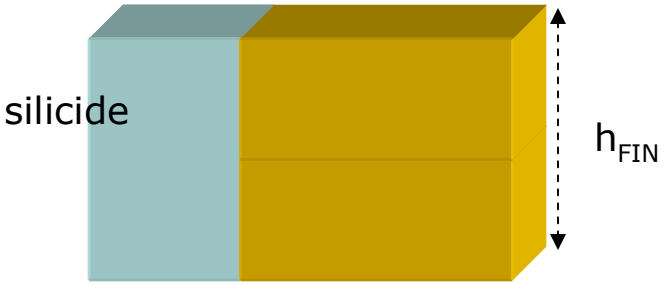
$$R_{ext} = \frac{\rho_{ext} L_{sp}}{(h_{fin} - h_D) W_{fin}}$$

R_{ext} - Extension resistance

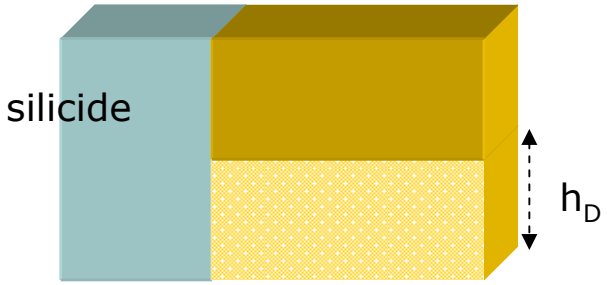
L_{sp} - Spacer length

ρ_{ext} - Average resistivity of the extension.
- It is assumed that the current flows through the entire extension in the absence of depletion
- Also that the average resistivity does not change with h_D

First Order Model



Extension with a positive bias on the back gate



Extension with a negative bias on the back gate

$$R_{cont} = \frac{\rho_c}{h_{fin} W_{fin}}$$

R_{cont} - contact resistance

$$R_{cont} = \frac{\rho_c}{(h_{fin} - h_D) W_{fin}}$$

ρ_c - Average resistivity of the contacts.
- It is assumed that the fin is fully silicided (for simplicity)
- Also that the contact resistivity does not change along the fin height

First Order Model

$$R_{tot} = 2(R_{ext} + R_{cont})$$

$$R_{tot-\min} = \frac{2(\rho_{ext} L_{sp} + \rho_c)}{h_{fin} W_{fin}}$$

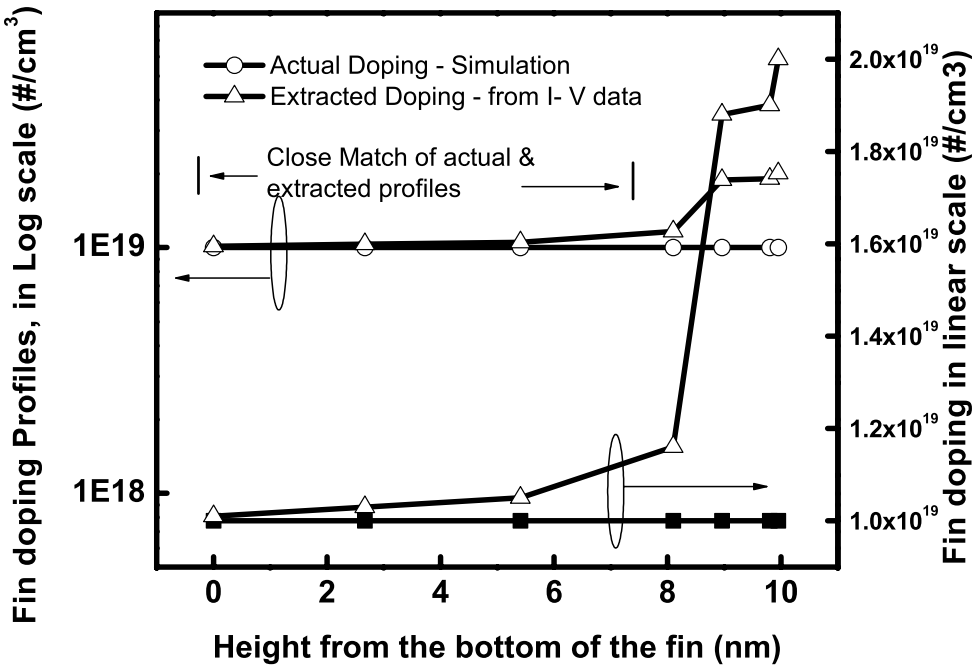
$$R_{tot}(V_{sub}) = \frac{2(\rho_{ext} L_{sp} + \rho_c)}{(h_{fin} - h_D(V_{sub}))W_{fin}}$$

$$\frac{R_{tot-\min}}{R_{tot}(V_{sub})} = 1 - \frac{h_D(V_{sub})}{h_{fin}}$$

The highest value of resistance is reached when h_D is the maximum => maximum "equivalent" depletion width at the bottom interface

$h_{D\text{-max}}$ can then be used to calculate an "equivalent average" doping at the bottom part of the fin

Doping extraction



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Extracted doping exactly matched with the actual profiles in the fin bottom.

Conclusions

- Proper TCAD tuning essential for meaningful FinFET simulations
- Optimum High-K dielctric for FinFETs propsed, from the performance perspective.
- Bulk FinFETs are optimized for better DC performance.
- Reported that Bulk FinFETs are equally attractive from the performance perspective unlike the conventional perception..
- Compared the FinFET fringe parasitics with equivalent planar and propose solutions to optimise the enhanced FinFET fringe parasitics.
- Proposed a novel approach for extracting the bottom fin doping in ultra thin fins.

Publications

- C.R.Manoj, V. Ramgopal Rao, "Impact of High K Gate Dielectrics on the Device and Circuit Performance of Nanoscale FinFETs", IEEE Electron Device Letters, Vol. 28, Issue: 4, p.295, April 2007.
- C.R.Manoj, et al, "Device Design & Optimization Considerations for Bulk FinFETs", IEEE Transactions on Electron Devices, Vol. 55, No.2, p. 609-615, February 2008
- A. B. Sachid, C.R. Manoj., Dinesh K. Sharma, V. Ramgopal Rao, "Gate Fringe Induced Barrier Lowering in Underlap FinFET Structures and its Optimization", IEEE Electron Device Letters, Vol. 29, Issue 1, pp.128-130, January 2008.
- Yusuke K., C. R. Manoj, Kazuo Tsutsui, Venkanarayan Hariharan, Kuniyuki Kakushima, V. Ramgopal Rao, Parhat Ahmet, and Hiroshi Iwai, "Parasitic effects in multi-gate MOSFETs", IEICE Transactions on Electronics (Japan), Vol. E90-C, No.10, October 2007.
- C.R. Manoj, V.Ramgopal Rao, Chang Yun Chang and Clement-Wann, "Enahnced Fringe Capacitance Parasitcs in 22nm Bulk FinFETs and its Optimisation", To be submitted to IEEE TED 2008.
- C.R. Manoj, Meenakshi. N, Dhanya V. and V.Ramgopal Rao, "Optimization of Nano-scale Bulk FinFETs", Proceedings of the 14 th International Workshop on the Physics of Semiconductor Devices, Mumbai, December 16-20, 2007
- C.R Manoj, N. Meenekshi, V.Ramgopal Rao, "Optimum Body Doping for Improving the Bulk FinFETs Performance", Proceedings of the 14th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), 11-13 July 2007, Bangalore, India
- Manoj C.R, Abhinav Mangal, V.Ramgopal Rao, Hiroshi Iwai,"Parasitic Effects in Multi-gate MOSFETs", International Workshop on Nano CMOS, Jan 30- Feb 1, 2006, Mishima, Shizuoka prefecture, Japan (Invited)
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