Rohit Modak

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Second year MTech student
Dept. of Electrical Engg.
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Education

Indian Institute of Technology Bombay *July '06 - Present*
- Second Year Mtech student, Dept. of Electrical Engineering
- Advisor : Prof. Maryam Shojaei Baghini
- Current CPI - 9.44/10.0

S.G.S.I.T.S, Indore *July '02 - June '06*
- Bachelor of Engineering, Electronics and Instrumentation Engineering
- Percentage :78.4

Research Interests

- Power Management, CMOS Analog Design, VLSI digital design.

Research Projects

- **Single input Dual output Buck converter**
  - **Advisor** - Prof. Maryam Shojaei Baghini
  - The M. Tech project aims at designing a dual output buck converter with high efficiency. The input voltage (battery) can vary from 2.8V to 5.5V with maximum load current of 200mA. CADENCE custom IC design tool set is used and the technology is standard 0.35um MM CMOS process for which I/O devices with higher breakdown voltage than those of core devices are available. First stage of the project involves a versatile modeling of various losses using MATLAB under different values of input voltage and the load. This modeling is used for optimum sizing of the transistor switches. At the second stage of the project, driver and controller for high efficiency will be designed.
- **Automatic Number Plate Identification System**
  - **Advisor** - Prof. V. M. Gadre
  - Implemented the system to automate the identification of the vehicle number. Firstly, the number plate is located and extracted from the acquired image of the vehicle using the MATLAB image processing toolbox. Next, the digits are cropped from the extracted number plate. Passing those images through a neural network then identifies the number of vehicle.

Other Academic Projects

- **CMOS Analog Design : LDO**
  - **Advisor** - Prof. A.N. Chandorkar
  - Designed and simulated Low drop out voltage regulator using Eldo, with output voltage of 1.8 V and dropout of 0.3V and maximum load current of 150 mA.

- **Hardware Description Language : 4 by 4 Data Switch**
  - **Advisor** - Prof. M.P. Desai
  - 32-bit data from each of the input port is routed to the output port indicated by the first 2 bits of the data. Designed and synthesized in VHDL using Xilinx synthesis tools.
- **System Design: 32-bit multiplier**
  - **Advisor** - Prof. M.P. Desai
  - Designed and implemented using control and data path decomposition technique in VHDL.
- **DSP and its Applications: Band pass filter**
  - **Advisor** - Prof. V.M. Gadre
  - Designed IIR band pass filter and simulated using MATLAB.
- **Microelectronics Lab: MOS capacitor fabrication**
  - **Advisor** - Prof. Souvik Mahapatra
  - Fabricated a MOS capacitor with oxide thickness of 10nm and extracted its parameters using C-V plots.
- **VLSI Design Lab: Single bit SRAM cell**
  - **Advisor** - Prof. V.M. Gadre
  - Laid out in MAGIC and simulated in spice.

Courses Taken

- Physical Electronics, Physics of Transistors, VLSI technology, VLSI design.
- System Design, CMOS Analog Design, Hardware Description Languages, DSP and its applications.

Software Proficiency

- Design tools: Cadence, Eldo and NGSpice
- Devices tools: dios, desSis and ISEextract
- Digital design tools: ModelSim, Xilinx synthesis tools and IRSim
- Layout tools: Virtuoso from Cadence, magic
- Computation tools: Matlab, Origin

Other Interests

Singing, listening music and playing cricket.