

STATISTIC METHOD BASED DEVICE MODELING WITH PROCESS VARIATION

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Abstract

Due to the diminishing device sizes and the large die sizes, the impact of process variations on device modeling plays a major role in design for manufacturability. In our work, we attempt to statistically model the device parameters taking process variations into account. The statistical tool that is used to develop the models is based on the acclaimed Monte-Carlo method of simulations for varying the process parameters on a known probability density function and the Response Surface Method (RSM) to fit the device response based on the statistic variation.

Introduction

Random statistical variations are inevitable during the IC fabrication process. This is an important aspect that cannot be overlooked in today's CMOS technologies. The manufacturing

variations impacts IC performance and yield. Hence, a high level of process control and sophisticated metrology is required. Traditionally, the effect of device variations on circuit timing is captured by the worst/best case corner point methods. In our work, we obtain a quantitative understanding of the impact of statistical process variations on electrical performance of the device. Our simulations are based on 0.25 μ m NMOS device.

Monte Carlo simulation methods typically use sequence of correlated vectors of pseudo random numbers generated for the process parameters and subsequent evaluation of the circuit performance corresponding to each random vector instance, either by directly using SPICE, or via RSM modeling.

Response Surface Methodology is the procedure of fitting a series of regression models to the responses of the

simulation model evaluated at several points and trying to optimize the resulting regression function. RSM is a relatively efficient method of simulation optimization in terms of the number of simulation experiments needed. It can be decomposed into

- Design of Experiments (DOE)
- Determining the best fit mathematical model
- Determining the optimal settings of the experimental factors

A Word on Process Variations

The parameters of a transistor vary from wafer to wafer, or even between transistors on the same die, depending upon the position. This observed random distribution between supposedly identical devices is primarily the result of the variations in the process parameters such as impurity concentration densities, oxide thicknesses, and diffusion depths, caused by non-uniform conditions during the deposition and/or the diffusion of the impurities. The result in diverging values for sheet resistances and transistor parameters such as the threshold voltage.

The other factor is the variations in the dimensions of the devices, mainly resulting from the limited resolution of the photolithographic process. This causes deviations in the W/L ratios of MOS transistors and the widths of the interconnect wires. It is observed that quite a number of these deviations are totally uncorrelated. For instance, the variations in the length of an MOS transistor are unrelated to variations in the threshold voltage because both are set by different process steps.

The threshold voltage V_{T0} can vary for numerous reasons such as changes in oxide thickness, substrate, polysilicon and implant impurity levels, and the surface charge. Accurate control of the threshold voltage is an important goal for many reasons. The main cause for variations in the process transconductance K_n' , is changes in the oxide thickness. Variations can also occur in the mobility, but to a lesser degree. Variations in W and L are mainly caused by the lithographic process. These variations are totally uncorrelated because, the first is determined in the field oxide step, while the second is defined by the polysilicon

definition and the source and drain diffusion processes.

The measurable effect of the process variations may be a substantial deviation of the circuit behavior from the nominal or expected response, and this could be in either positive or negative directions.

Modeling the Parameters

In this work, we simulate the variations in V_{T0} , K_n' , W and L and fit a response model for the device using RSM. The PSPICE 9.1 tool allows the Monte Carlo simulation of the parameters V_{T0} , K_n' . The Monte Carlo simulation can be done for a Uniform or Gaussian probability distribution. The Monte Carlo analysis varies the lot or device tolerances of devices between multiple runs of an analysis. Before running the analysis, the model and/or lot tolerances of the model parameter must be set up. Multiple runs of the selected analysis are done while parameters are varied. The selected analysis is repeated in subsequent passes of the analysis. W and L cannot be varied statistically in conjunction with the Monte Carlo analysis in PSPICE 9.1 [8]. We have accomplished the same

task by manually varying these parameters by using a random number generator in C++. We have assumed a uniform distribution of the parameters in PSPICE simulations as well as in C++. The results are based on optimizing the fall-time (high-to-low transition) for a CMOS 2-input NAND in 0.25 μ m technology and sized accordingly for equal rise and fall times.

Monte Carlo Simulations

The NAND gate was designed using PSPICE MBreakN3 and MBreakP3 models, which allow customized parameters for the MOSFETS. V_{T0} and K_n' were allowed to follow a uniform distribution with a worst-case lot and device tolerance of 15%, independently. Transient time analyses were performed for a pulse input with 5ns rise and fall time to observe the output. A nominal 75 runs was performed on the uniformly distributed V_{T0} and K_n' , each varying independently. Fall time was considered as the goal function and calculated for the dataset simulated by PSPICE. The consolidated plot for 75 runs with the performance analysis using histogram is shown below:

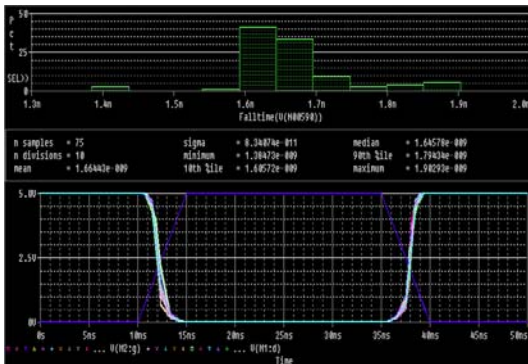


Fig 1. V_{T0} and Kn' , Monte Carlo Simulation.

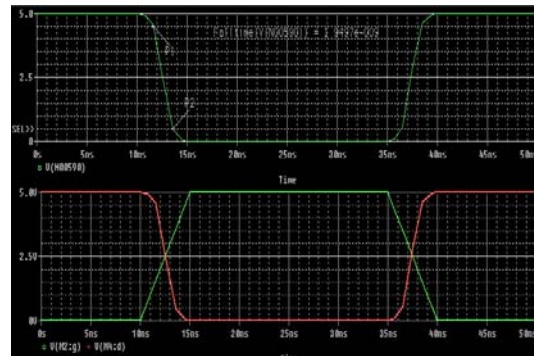


Fig 4. W and L Monte Carlo Simulation.

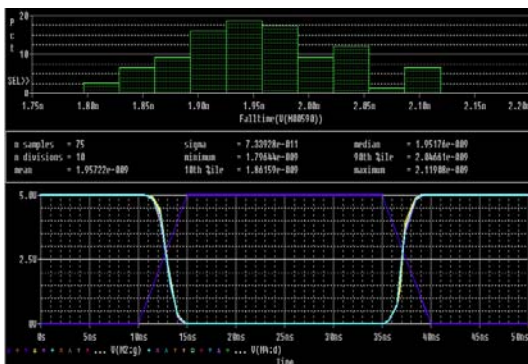


Fig 2. V_{T0} Monte Carlo Simulation.

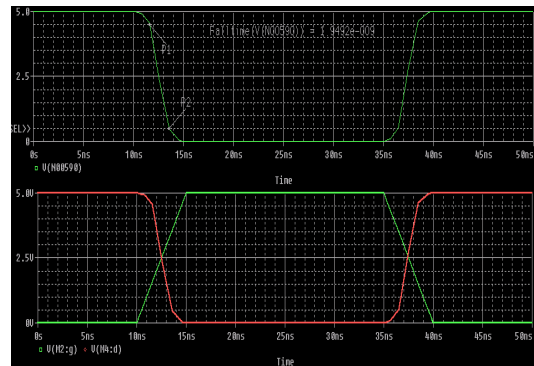


Fig 5. W and L Monte Carlo Simulation.

The first figure shows the consolidated plot of the V_{T0} and Kn' statistical variation affecting the rise and fall times of the circuit. The histogram plot is a performance analysis plot with time in nanoseconds on the x-axis with the number of corresponding outputs for the particular output on the y-axis. The second and the third plots show the variation of rise and fall times with a singular variation of V_{T0} and Kn'

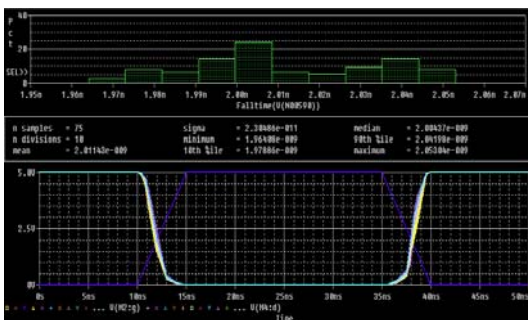


Fig 3. Kn' Monte Carlo Simulation.

respectively. The increase in the number of runs would be a convergence towards the response model to be fitted. But, the number of runs was limited due to the overhead the PSPICE can handle. The first three plots also provide information on the performance statistical parameters such as sigma, mean and median.

Since the values for W and L cannot be used in conjunction with Monte Carlo in PSPICE, uniform random values with 15% device tolerance were generated using C++ and fed manually to PSPICE breakout models for subsequent analysis. The number of runs was limited to 10 since the process involved is cumbersome and requires a manual intervention for goal function calculation.

The simulation plots for W and L variation shown above depict a random scenario and their respective fall time analysis. The fall times were recorded for every value of the independently and uniformly varied W and L values. This hence provides input to the RSM for the fitting of a response model for the W and L process variation.

Response Surface Method

With the values obtained from the simulation models, the response variable (fall time) was tabulated with corresponding statistical parameters.

The proposed model form relating V_{T0} (X_1) and Kn' (X_2) (also a separate model for W and L) is

$$Y_u = \beta_0 + \beta_1 X_{u1} + \beta_2 X_{u2} + \beta_{12} X_{u1} X_{u2} + \beta_{22} X_{u2}^2 + \epsilon_u \quad u=1,2,\dots,N$$

In matrix notation, the model can be expressed as

$$Y = X\beta + \epsilon$$

The normal equations are

$$X'Xb = X'Y$$

and the solutions to the normal equations are

$$b = (X'X)^{-1}(X'Y)$$

The fitted second order model then becomes

$$\hat{Y}(x) = b_0 + b_1 x_1 + b_2 x_2 + b_{12} x_1 x_2 + b_{22} x_2^2$$

The Total Sum of Squares

$$SST = \sum (Y_u - \tilde{Y})^2$$

(where \tilde{Y} is the mean of Y)

The SST can be partitioned into two parts, the Sum of Squares due to Regression (SSR or sum of squares explained by the fitted model) and the Sum of Squares unaccounted for by the fitted model.

$$SSR = \sum (\hat{Y}(x_u) - \tilde{Y})^2$$

The quantity SSE called the Sum of Squares of the Residuals is given by

$$SSE = \sum (Y_u - \hat{Y}(x_u))^2$$

These values are calculated and Analysis Of Variance (ANOVA) is tabulated. In the ANOVA table, the source of variation other than regression and total has also been labeled residual.

The F-ratio for testing the hypothesis

$$H_0 : \beta_1 = \beta_2 = \beta_{12} = \beta_{22} = 0$$

against the alternatives H_a : at least one of the parameters of β in H_0 is not 0 is

$$F = \frac{\text{Mean Square Regression}}{\text{Mean Square Residual}} \\ = \frac{SSR/(p-1)}{SSE/(N-p)}$$

Where N and p are number of observations and number of parameters the fitted model contains, respectively ($N > p$).

If the computed F exceeds the table value for F the hypothesis at H_0 is rejected at the 0.01 level of significance. Having rejected H_0 it can be inferred that at least one of the parameters other than β_0 in the model equation, based on the co-efficient estimates in the fitted model, is not 0. The value of R^2 for the fitted model can be calculated using

$$R^2_A = \frac{SST/(N-1) - SSE/(N-p)}{SST/(N-1)}$$

This value of R^2 is converted to a percentile to verify for the optimality of the fitted model.

Results

The above procedure for RSM was implemented using MATLAB and the results are attached as auxiliary files to the report (also PSPICE Monte Carlo simulation results and graphs).

Fitted equation for W and L process variation:

$$\hat{Y}(x) = -8.5227 - 16.0759x_1 - 61.9915x_2 - 69.9897x_1x_2 - 71.3979x_2^2$$

SST	=	0.0234
DOF	=	9
SSR	=	0.0230
DOF	=	4
SSE	=	3.2675e-004
DOF	=	5
F	=	70.5107

which is greater than the table value

$F_{0.01, 4, 70} = 11.39$, the hypothesis H_0 is rejected. The value of R^2 for the fitted model is 0.9748, which means that approximately **97.48%** of the total variation is explained by the fitted model.

Fitted equation for W and L process variation:

$$\hat{Y}(x) = 2.6487 - 0.1164x_1 - 1.8735x_2 + 0.1022x_1x_2 + 0.8671x_2^2$$

SST	=	0.4033
DOF	=	74
SSR	=	0.1845
DOF	=	4
SSE	=	0.2188
DOF	=	70
F	=	11.8073

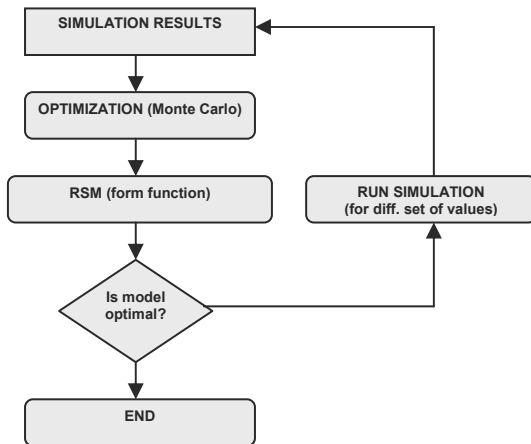
which is greater than the table value

$F_{0.01, 4, 70} = 3.60$, the hypothesis H_0 is rejected. The value of R^2 for the fitted model is 0.4264, which means that approximately **42.64%** of the total variation is explained by the fitted model.

Conclusion

It is inferred that the parameters W & L are easier to model with the incumbent process variations, giving an almost optimal design. The other two parameters give a suboptimal design due to the exaggerated 15% device as well as lot tolerances. So, the model could be fit again by optimizing the LOT parameters

and reiterating with a different set of simulation criteria and parameters as shown in the flow diagram.



References

[1] Gattiker, A., Sani Nassif, Rashmi Dinakar and Chris Long, “Static Timing Analysis Based Circuit-Limited-Yield Estimation”, *Proc. 2002 IEEE International Symposium on Circuits and Systems*.

[2] Okada, K. and Hidetoshi Onodera, “Statistical Modeling of Device Characteristics with Systematic Variability”, *IEICE TRANS Fundamentals, VOLE84-A, NO2 Feb 2001*

[3] Azadivar, F., “A tutorial on simulation Optimization”, *Proceedings of 1992 winter simulation conference*.

[4].Rabaey, Jan.M, Anantha Chandrakasan, Borivoje Nikolic, *Digital Integrated Circuits – A Design Perspective*, NJ:Prentice Hall 2003.

[5] Zeitzoff Peter M., “Modeling the Statistical Variability and Optimal Process Control Requirements for a 0.18mm NMOS Transistor”, *International SEMATECH Inc, May 25, 200*.

[6] Liu Y., Sani R. Nassif, Lawrence T. Pileggi and Andrzej J. Strojwas, “Impact of Interconnect Variations on the Clock Skew of a Gigahertz Microprocessor”, *Proc. 2000. 37th IEEE Design Automation conference*.

[7] Khuri, A.I., John A. Cornell, *Response Surfaces – Designs and Analyses*, NY: Marcel Dekker Inc. 1996.

[8] Orcad Inc., *Orcad PSPICE A/D Reference guide*, November 1999.