A
SEMINAR REPORT ON
USE OF DSP FOR WIRELESS AND MOBILE COMMUNICATION
Submitted in partial fulfillment of the requirements for the Degree of Doctor of Philosophy in Electrical Engineering
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ABSTRACT

In the transition from 1G to 2G in mobile communications, new standards are deployed which are digital in nature. So, due to the need to operate on larger data streams, more MAC (complex multiply and accumulate) and ACS (Accumulate compare and select) operations are required. It is here that DSP plays a role in wireless communication. Signal processing has always played a critical role in the research and development of wireless communication systems. In the course of the wireless revolution, as the demand for high capacity and high reliability systems increases, signal processing has an even more important role to play. It has brought unprecedented excitement in it.

Today’s programmable DSPs are pervasive in the wireless handset market for digital cellular telephony. This seminar presents the argument that DSPs will continue to play a dominant, and in fact increasing, role in wireless communications devices by looking at the history of DSP use in digital telephony, examining DSP-based solution options for today’s standards, and looking at the trends in low power and application specific DSPs.
1. Introduction:

The wireless revolution has brought unprecedented excitement into the field of signal processing. On the other hand, communicating over wireless channels presents formidable challenges to signal processing; the wireless channels introduce time-varying interference of various types: interference from multipath propagation, interference from other users and interference from other services. In order to provide reliable communication over a spectrum of limited bandwidth and under strict power constraints, sophisticated signal processing techniques are necessary to cope up with various issues ranging from efficient source, and channel coding to modulation and receiver designs. On the other hand, communication signals and systems are man-made and there are ample structures that can be exploited for high performance algorithms. Due to advent in Digital Signal Processors technology side, low cost and low-power DSP makes implementation of highly advanced signal processing algorithms a reality.

There have historically been two distinct approaches to the implementation of cellular handsets and infrastructure equipment [1]. One approach emphasizes programmable DSPs for flexibility in the face of changing standards, while the other approach focuses on hard-wired application-specific integrated circuit (ASIC) techniques to improve implementation efficiency. The right answer has been and will likely continue to be some combination of both approaches. If anything flexibility is becoming more of an issue, and therefore the programmability offered by DSP is even more desirable. Since power is the greatest potential roadblock to increased DSP use, we summarize trends in power consumption and millions of instructions per second (MIPS).

2. A Historical Perspective on Wireless architecture and use of DSP:

The first-generation (1G) cellular wireless mobile system were analog and were based on frequency-division-multiple access (FDMA) technology. The second boost for the cellular industry came from the introduction of the second-generation (2G) digital technology standards, including Global System for Mobile (GSM), IS-136 (Time Division Multiple Access, TDMA), and Personal Digital Cellular (PDC) [2].
This boom in the digital technology in second generation required operation on data streams, more MAC (complex multiply accumulate), ACS (accumulate compare select), and some other operations. Hence, gives rise to the idea of DSP in wireless and mobile. Where DSP is a specialized microprocessor that performs mathematical operations on a data stream in real time to produce a second (modified) data stream.

There is a continuing debate over the role of DSPs in wireless communications. To provide a historical basis for our arguments, we examine the case of Global System for Mobile (GSM) evolution. The assumption is, of course, that third-generation cellular (3G) products will evolve in a similar manner to GSM.

3. DSP in GSM:

Figure-1 shows the block diagram of mobile communication systems such as GSM and IS-136. GSM is the European standard for digital cellular systems. We selected GSM as a major application for analysis and benchmarking because it is one of the popular mobile communication standards in the world, and many of its algorithms are similar to those of other standards.

![Figure-1: A functional block diagram of GSM phone](image-url)
3.1 From ASIC to DSP in GSM:

We recognize a classical digital communication model with signal compression, error correction, encryption, modulation and equalization. In the early days of GSM it was assumed that the low power requirement would mean that most of the phones would be implemented in ASIC. In what follows, it proved that the power difference between DSP and ASIC was not significant enough compared to other factors that drove GSM phone evolution.

The coder used in GSM phase-1 compressed the speech signal at 13 kb/s using the rectangular pulse excited linear predictive coding with long term prediction (RPE-LTP). The voice coder is the part of the architecture that most engineers agree should be done on a DSP, and in early designs the DSP was included mainly to do the vocoding. However once the DSP was included, a certain amount of “mission creep” started to occur. As DSPs became more powerful, they started to take on other physical layer-1 tasks until all the functions in the “DSP functions” box in figure-1 were included.

Flexibility was also important in the evolving standard. GSM phase-2 saw the introduction of half-rate (HR) and enhanced full rate (EFR). HR was suppose to achieve further compression at a rate of 5.6 kb/s for the same subjective quality, but at the expense of an increased complexity, and EFR had to provide better audio qualities and better tandeming performance, also at the expense of higher complexity, using an enhanced Vector-Sum Excited Linear Prediction (VSELP) algorithm. Along with these changes, came changes in the implementation of the physical layer as better performance, cost and power saving combinations were found. As a result, each generation of phone had a slightly different physical layer from the previous one, and upgrades to ASIC based solutions became costly and difficult. Because DSPs were now being designed with low-power wireless applications in mind, the power savings to be had from ASIC implementation of DSP functions was not significant enough that system designers were willing to live with the lack of flexibility. After 1994, a single DSP was powerful enough to do all the DSP functions, making the argument for a DSP-only solution for the baseband even more compelling. To improve system power consumption and board space, several DSPs
such as Motorola 56652 [3] and TI's Digital Baseband Platform [4] integrate a RISC microcontroller to handle the protocol and man-machine interface tasks to free the DSP for communication algorithm tasks. Presently most popular partitioning of GSM is as shown in figure-2.

Figure-2 : GSM function partitioning

It is also true that as GSM phones have evolved, they have gradually moved
beyond the simple phone function and this has led to an increase in the fraction of the DSP MIPS used by something other than physical layer-1. This evolution is shown in figure-3.

With the advent of wireless data applications and increased bandwidth of 3G, we expect this trend to accelerate.

3.2 MIPS requirement for signal processing in GSM:

Figure-4 shows the simplified block diagram of GSM mobile communication system.

![Figure-4: Simplified block Diagram of GSM](image)

The baseband processing blocks of GSM are shown as shaded in figure, where the functional blocks with relatively less significant complexities such as interleaving/de-interleaving and enciphering/deciphering are not included. The received signals are sampled at the baud (symbol) or higher (fractional) rate before processing them for any of the purpose. Depending upon the sampling rate, one has either a single input/single output (SISO) (baud rate sampling) or a single input/multiple output (SIMO) (fractional sampling), complex discrete-time equivalent baseband channel in the single user case, and the multiple input/multiple output (MIMO) complex discrete time equivalent baseband channel in the multiuser case.

Figure-5 shows the required processing power of each component of the GSM baseband functions [5].

Most general-purpose DSPs cannot support all the baseband functions, as the total required processing power for GSM itself is 53 million instructions per second.
(MIPS). Furthermore, future systems will have a bigger demand on the power requirement, aggravating the already tight power budget. Figure-5 shows that nearly 80% of the total processing power (42 out of the total 53 MIPS) is consumed just for equalization. Therefore it is important to accelerate the execution of equalization for performance improvement.

Figure 5: Required processing power, in MIPS, of each of GSM's baseband functions

4. Signal Processing in improved baseband functionalities:

As the research on equalization methods accelerating for performance improvement and it needs maximum MIPS requirement, the signal processing in it is explained here. Also the most important, space time signal processing in presence of fading channels is also explained.
4.1 Blind equalization:

The traditional techniques for channel estimation and equalization use training data, which not only consumes a significant portion of available bandwidth but also requires a perfect co-operation between the transmitter and receiver. In recent years, the so-called blind techniques have been explored intensively in the literature. The blind techniques do not use any training data except for certain prior information inherent in the original strings of symbols, which hence saves the bandwidth and relaxes the relationship between the transmitter and receiver. Consequently, the blind techniques have a clear potential to increase the capacity and reliability of wireless systems. As a subject area, the blind techniques have had in recent years a very fast growing rate in the general field of signal processing for communications [6]. Its problem statement is given below –

The following baseband equivalent discrete time white noise filter model is assumed for a typical digital communication systems:

\[ y_k = \sum_{n=0}^{L} f_n I_{k-n} + \eta_k \]

where \( \{\eta_k\} \) is a white Gaussian noise sequence, \( \{I_k\} \) is the zero-mean, i.i.d., information sequence, possibly complex, taking values from a finite set; \( \{f_k\} \) is a finite impulse response (FIR) linear filter (with possibly complex coefficients) that represents the equivalent channel; and \( \{y_k\} \) is the (possibly complex) baseband equivalent received signal.

Given the data \( \{y_k, 1 \leq k \leq N\} \) and having no access to the information sequence (no training sequence), the objective is to estimate the (equivalent) channel impulse response \( \{f_n\} \) and/or to estimate the information sequence \( \{I_k\} \) (up to a delay and a scale factor). The length of the channel is not necessarily known.

The problem of blind system/channel identification has attracted significant interest recently due to its potential applications in wireless communications. As a result, many blind channel estimation algorithms have been developed.
4.2 Space time signal processing for wireless:

In addition to additive noise, another problem, which has plagued communication channel, is fading. Communication in the presence of channel fading has been one of the most challenging issues in recent times [7]. In a fading channel severe attenuation makes it impossible for the receiver to determine the transmitted signal. One way to overcome this is to make several replicas of the signal available to the receiver with the hope that at least some of them are not severely attenuated. This technique is called diversity. It is perhaps the most important contributor to reliable wireless communication. Examples of diversity techniques are (but not restricted to) –

- Time diversity
- Frequency diversity
- Antenna diversity or space diversity

A simple space diversity scheme, which does not involve any loss of bandwidth, is to use multiple antennas at the receiver. The optimal way (in terms of Signal-to-Noise-Ratio [SNR]) to combine the outputs of different antennas is the maximal ratio combining.

In space-time, modems operate simultaneously on all the antennas [8]. The key leverage that we get from this scheme is that the co-channel interference can be significantly reduced in a way, which is not possible with single antenna modems. The reason why this is possible is that the co-channel interference and the desired signal almost always arrive at the antenna array (even in complex multipath situation) with distinct and well separated spatial signatures, thus allowing the modem to exploit this difference to reduce the co-channel interference. Likewise, the space-time transmit modems can use spatial selectivity to deliver signals to the desired mobile while minimizing the interference for other mobiles.

4.2.1 The set up and signal processing:
Consider a transmitter with \( m \) antennas and a receiver with \( n \) antennas [7] as shown in figure-6.

Figure-6 : Transmitter-receiver set-up for space-time diversity

Let \( A \) be the \( n \times m \) channel gain matrix. Thus the \( ij\)-th element of \( A \) is the (complex) gain factor for the path from the \( j\)-th transmit antenna to the \( i\)-th receive antenna. Let \( S \) denote the transmitted symbol. In order to achieve time diversity the transmission is repeated \( N \)-times. Thus the transmission of \( S \) lasts over \( N \) symbol periods. During each symbol period the transmitter transmits a scaled version of \( S \) through each antenna. Let \( X_k \) be the \( m \times 1 \) vector whose \( i\)-th element denotes the scaling factor used by the \( i\)-th transmitter antenna during the \( k\)-th symbol period. \( X_k \) is called the transmit weight vector which may change from one symbol period to another but remains constant over a symbol period.

We assume that the receivers use a matched filter and the channel is corrupted by Additive White Gaussian Noise (AWGN). The output of the matched filter, after sampling at the \( k\)-th symbol period is the \( n \times 1 \) vector.

\[
r_k = AX_kS + n_k \quad k = 1,2,\ldots,N
\]

where \( n_k \) is the noise vector. The noise vector is complex Gaussian distributed and both temporally and spatially white.
4.2.2 General framework for detection:

At the receiver linear processing is done. This keeps the computational complexity down and also simplifies the analysis. Thus the receiver takes a weighted sum of the outputs of the different antennas and averages them over $N$ symbol periods. At a given instant $k$, $1 \leq k \leq N$, the linear combiner used at the receiver is an $n \times 1$ vector such that the complex conjugate of its $i$-th element is used to weight the output of the $i$-th antenna. We denote it by $Z_k$. Thus $Z_k$ is the receiver linear-combiner vector. The symbol detection is done based on the observation:

$$D = \frac{1}{N} \sum_{k=0}^{N} Z_k^* [AX_k S + n_k]$$

In the case of a BPSK scheme ($S = \pm 1$) the decision of the transmitted symbol is based on whether $D$ is positive or negative. An error occurs when $S = +1$ and $D$ is negative, or vice versa. The probability of error decreases as the SNR increases.

4.3 Signal Processing advances in CDMA systems:

In CDMA multi-access systems, each user utilizes a different signature waveform to enable the receiver to separate different transmissions [7]. In this the received signal consists of a superposition of all signals from all transmitters. In particular, if $J$ users are transmitting and linear modulation is used, the received continuous time signal is:

$$y_c(t) = \sum_{j=0}^{J} y_{c,j}(t) + v(t)$$

$$y_{c,j}(t) = \sum_{k=-\infty}^{\infty} b_j(k) h_{c,j}(t - \tau_j - kT_s)$$

where $h_{c,j}(t)$ denotes the signature of user $j$ while $b_j(k)$ and $\tau_j$ denote its transmitted symbol sequence and delay respectively; $T_s$ is the symbol period, $v(t)$ is additive Gaussian noise. If no multipath presents, $h_{c,j}(t)$ coincides with the transmitter user waveform (or “code waveform”)

With the increased interest in CDMA solutions for wireless voice and data services in the last decade, there has been equally increased interest in appropriate receiver structures and detection techniques for improved performance. Relatively simple matched
filter-based, single-user receivers were originally envisioned for spread spectrum systems [9]. The works till mid 80s demonstrated that substantial performance gains can be achieved if the structure of the multi-user interference (MUI) is taken into account and all received signals are jointly demodulated [10]. The promise of dramatic performance gains of optimal multi-user detection spurred a host of activity in the area which continues unabated till today. In order to address the exponential complexity of optimal solutions, suboptimal linear receivers have received attention. One design methodology aims at completely suppressing MUI resulting in what is termed zero forcing or decorrelating receivers [11], [12], [13]. In order to avoid noise amplification problems associated with decorrelating receivers, linear MMSE receivers may be developed in batch and adaptive forms [14], provided that training data are available. MMSE receivers do not suffer from the noise amplification problems but require training data. However blind, adaptive linear receivers with MMSE performance are possible by minimizing the received output energy [15].

Between the two extremes of optimal CDMA receivers, and suboptimal linear ones [11], [12], [14], [15], there exists a number of other methods based on iterative schemes. They typically employ successive (or parallel) interference cancellation using decoded soft (or hard) user information from the previous iteration [16], [17], [18], [19], [20], [21]. Those solutions improve the performance of linear receivers without the complexity penalty of optimal ones. In the case of single-user receivers, one needs only to worry about the multipath distortion of the waveform of the user of interest. In fact, the large bandwidth of spread-spectrum signals somewhat facilitates the situation by rendering in many cases the multipath copies resolvable. Under there conditions, the RAKE receiver has been popular, which combines the contributions of a number of matched filters, each one synchronized with a different multipath copy of the transmitted signal, [22], [23]. Extension of the RAKE concept to combine signals from multiple antennas has also been studied [24].
5. DSP Technology trends in wireless:

5.1 Low power DSP trends:

The digital baseband section is critical to the success of wireless handsets and, as mentioned previously, programmable DSPs are essential to provide a cost-effective flexible upgrade path for the variety of evolving standards. Architecture, design and process enhancements are producing new generations of processors that provide high performance while maintaining the low power dissipation necessary for battery-powered applications. Many communications algorithms are multiply-accumulate (MuAcc) intensive. Therefore, we evaluate DSP power dissipation using milliwatts per million MuAcc (MMuAcc), where MuAcc consists of fetching two operands from memory, performing a multiply accumulate and storing the result back in memory. As shown in figure-7, DSP power dissipation is following a trend of halving the power every 18 months [25].

As the industry shifts from 2G to 3G wireless, we see the percentage of the physical layer MIPS that reside in the DSP going from essentially 100% in today’s technology for
GSM to about 10% for wide-band code-division multiple access (WCDMA). However, the trend shown in figure-7 along with more efficient architectures and enhanced instruction sets, implies that the DSP of couple of years from now will be able to implement a full WCDMA physical layer with about the same power consumption as today’s GSM phones.

5.2 Wireless application specific DSPs:

Because of the growing importance of the wireless market there are now several DSPs on the market that have been designed with wireless applications in mind. Initially in the case of GSM and IS-136 DSPs have only been applied to specific areas such as speech codec because of their limited performance. To overcome these limitations, a number of application specific DSPs have been developed. For example, Lucent’s DSP 1618 performs the Viterbi decoding using a coprocessor [26], which supports various decoding modes with control registers at the cost of chip area. On the other hand, TMS 320C54X supports specific instructions for the Viterbi decoding [27], which makes it very popular for mobile communication. However, since it has only one multiplier, it is difficult to handle the multiplication and accumulation (MAC) of complex numbers, which is quite often used in such applications as channel equalization. Recently, several DSPs that can support two MAC operations per cycles were developed. For example, very-long-instruction-word based TMS320C6X which lacks a dedicated MAC unit but has two multipliers and six arithmetic units, performs MAC operations by using separate multiply and add instructions [28]. Also, the dual MAC unit in Lucent’s DSP 1600 performs two multiplications and two accumulations in one cycle and support instructions for the Viterbi decoding [29].

Another example of application specific DSP is the DSP with a special functional block called the Mobile Communication Accelerator (MCA) developed using the MetaCore framework, which is a design framework for generating application-specific instruction set processor for DSP applications, along with the generator set for software tools such as compiler, assembler and instruction-set simulator. Its example is MDSP-II, a 16-bit DSP [5]. The special functional block as well as an instruction
set optimized toward the mobile communication applications. Therefore, the remaining processing power can be used for other features such as echo cancellation and speech recognition for voice dialing. At least, the remaining processing power always helps to reduce, the power consumption to make such DSPs more competitive for portable applications, simply by performing the same functionality at the reduced clock rate with the assistance of MCA, the GSM base-band functions, which need 53 million instructions per second (MIPS) on the general-purpose Digital Signal Processors, can be performed only with 19 MIPS.

Another trend in DSP evolution is toward VLIW processors to support a compiler-based programmer-friendly environment [1]. Examples of this include TIs TMS320C6X [30], ADIs Tiger-SHARC [31], and Lucent and Motorola’s Star*Core [32]. These VLIW processors use explicitly parallel instruction computing (EPIC) with prediction and speculation to aid the compilers. The processors are also statistically scheduled, multiple issue implementations to exploit the instruction-level parallelism inherent in many DSP applications. Although the application of this to physical layer processing in the handset is not apparent so far, these devices allow very efficient compilation of higher-level code, thus reducing the need for DSP-specific assembly level coding of algorithms. As a result, the trend of wireless toward an open application-driven system will make this kind of DSP much more compelling as a multimedia processor in the handset.

6. DSP in mobile: where are we going?:

Digital signal processors (DSPs) have become a key component for the design of communications ICs. Application customization leads to key market advantages but also to enormous problems of having too many different DSPs and their software development tools.
6.1 Technology Side:

The communications market is very dynamic and has a high growth rate. Hence DSPs for communications must evolve to continue being a platform for achieving and sustaining a competitive standing. How can this be achieved?

The performance of DSPs is evolving further by advances in semiconductor technology. This leads e.g. to higher clock frequencies as well as reduced power consumption per MIPS. Additional performance improvements can be gained by the development of new DSP architectures, where performance is measured by a reduced MIPS requirement per algorithm (improved efficiency), reduced power consumption, or allowable higher clock frequency.

6.1.1 What is driving DSP Technology?

For any application to become a technology driver:

- It needs to have a high growth market,
- it needs to have a substantial market volume today,
- it requires to push technology limits (clock, die size, power consumption, packaging)

Clearly, communications is the DSP technology driver today. Mobile communications DSPs in particular are becoming a semiconductor technology driver due to high performance as well as stringent power consumption and packaging constraints.

6.1.2 What kind of DSPs are needed?

DSPs cover a very wide range of architectural customizing for applications. We can divide DSPs into three general classes, i.e.

- application specific DSP (AS-DSP)
- domain specific DSP (DS-DSP)
- general purpose DSP (GP-DSP)

AS-DSPs are typically customized to an application to serve high-end application performance requirements, or to minimize die size/cost. Generally the market volume must allow for a custom solution to be developed, and customizing is carried out to gain market advantages. However, time-to-market constraints must allow for a long design cycle. Examples of AS-DSP can be found e.g. for speech coding.
Application customizing can be found in the datapath, address generation, bus architecture, memory, and I/o.

DS-DSPs are targeted to a wider application domains, as cellular modems (TI C540, TCSI Lode). They can be applied to a variety of applications, however they were designed “with a target application in mind”. Due to special instructions and additional hardware they can run domain specific algorithms efficiently (e.g. Viterbi algorithm and equalizers). A DS-DSP is designed for a market with a volume high enough to allow specialized solutions. Its main advantage over an AS-DSP is its fast availability, and access to a small software library base.

GP-DSPs have evolved from the classic FFT/filtering multiply-accumulate design paradigm. Examples are TIC50, Lucent 16xx, Motorola 563xx, ADI 21xxx and DSP-Semi’s Oak/Pine. GP-DSPs are readily available, are widely applicable, and have a large software base. However, they lack in performance when compared to more customized solutions for specific applications.

### 6.1.3 Architecture Development Technology Flow:

High-end applications require innovation and application specific customizing to enable the design of solutions. As semiconductor technology evolves, these architecture ideas can be applied to DS-DSPs, and then to GP-DSP architectures, as shown in figure-8.

![Figure-8: Architecture technology flow](image)

This case study clearly allows drawing two conclusions:

- tailorization of DSPs enables key market advantages
- DSP technology is not one core only
6.1.4 The software-hardware nightmare:

As discussed before, today’s mobile communications equipment, as cellular phones, comprise several functional units, which require signal-processing tasks

- baseband modem (a typical DSP task)
- speech codec (atypical DSP task)
- protocol and control unit (on a microcontroller)

In previous section we have seen that tailorization leads to key advantages. This however leads to a heterogeneous design with 3 different processor platforms, one for each area of customizing. The resulting problem for the communications equipment designer is to maintain and develop software on 3 different incompatible platforms. Adding future functional units can worsen this problem, see figure-9. Semiconductor manufacturers on their side need to maintain and update multiple processor platforms.

Figure-9: Software-hardware nightmare

This problem we call the software-hardware nightmare. Semiconductor as well as equipment manufacturers need one integrated library based DSP family design approach, as sketched out in figure-. Using the same software design tools as well as library based reuse of hardware units in an integrated DSP design system is key to solving the heterogeneous software-hardware nightmare. Lucent addresses this problem by allowing customized acceleration units to be added to the DSP 16xx core.
The baseline of the software-hardware nightmare is:

We need a solution as sketched in figure-10: the tailorization of DSPs within an integrated DSP architecture family, programmable with one set of software design tools.

![Integrated System Diagram](image)

**Figure-10 : Integrated hardware/software DSP design**

### 6.2 Signal processing algorithm side:

In recent years a lot of work has been done to develop newer algorithms for various base-band functionalities like equalization, diversity etc. The goals [33] of the algorithm writers are –

i) Bandwidth saving: Efforts to develop new ideas to reduce the constraints of bandwidth requirement. For example blind equalization, spatial diversity etc.

ii) MIPS requirement by DSP: This is the effort to develop the algorithm of interest with minimum MIPS requirement from processor.

iii) Rate of convergence: This is defined as the number of iterations required for the algorithm, in response to stationary inputs, to converge close enough to the optimum solution. A fast rate of convergence allows the algorithm to adapt rapidly to a stationary environment of unknown statistics. Furthermore, it enables the algorithm to track statistical variations when operating in a non-stationary environment.
iv) Misadjustment: For an algorithm of interest, this parameter provides a quantitative measure of the amount by which the final value of the mean square error, averaged over an ensemble of adaptive filters, deviates from the optimal minimum mean square error.

v) Computational complexity: This is the number of operations required to make one complete iteration of the algorithm.

vi) Numerical properties: When an algorithm is implemented numerically, inaccuracies are produced due to round-off noise and representation errors in the computer. These kinds of errors influence the stability of the algorithm.

6.3 Requirement on DSP for future wireless devices:

The transition to digital technology driving a transition from voice-only cell phones to an environment, which can deliver a variety of data services to a broad range of mobile devices. Bits, after all, are just bits, and they can be used to transmit data as well as voice. So, although voice communication will probably always be the dominant mobile service, this century will see a proliferation of targeted data services for mobile subscribers [1].

Examples of such services could include:

- Imaging Service
- Location based services
- Audio and visual entertainment

A common theme in all of these services will be an insatiable thirst for signal

![Graph showing communication and applications DSP MIPS](image)

*Figure-11: Applications drive DSP MIPS*
processing power. Figure-11 illustrates that even as communication processing needs become more demanding, applications requirements will also drive a need for more powerful DSPs, i.e. with more MIPS capability, video codec capability, and high performance-processing unit for algorithm of interest.

Future wireless devices may be based on software radio concept. Software radio is an emerging technology, thought to build flexible radio system, multiservice, multistandard, multiband, reconfigurable and reprogrammable by software [34]. As most of the radio functionalities defined by software, DSP and its software will be an integral part of it, in order to define, as many radio functionalities as possible in software. So, demand for more fast and advanced DSP will go on increasing in future.

7. Discussion and conclusions:

In this seminar we discussed how the efforts are going on to define as many radio functionalities as possible by DSP and associated software. Mostly algorithm guys are concentrating on more and more efficient algorithms ignoring Digital Signal Processor architecture implementation issues and its developments. In fact the processor design companies are the people who seems to be running behind the algorithm guys and are trying to make the hardware more and more like the way the algorithms are written. It means that the processor designers are compensating the unwillingness on the part of algorithm writers to concentrate on implementation issues by changing their design paradigms. Mostly algorithm guys’ problem solved is the hardware designer’s problem created!

So far as research area goes, one can choose the following – Forget implementation; look at some Digital Signal Processing techniques, its applications. May be one can look at new techniques and solve wireless communication problems. Also one can look at generic design methodologies, suggest what is the best by looking at ASIC implementations, FPGA implementation, DSP based implementation or combination of either of those. One can concern about real time issues that arise, may be software issues. Things like what goes better with different hardware: Object Oriented Programming (OOP) or other kind of technologies as people are thinking about configurable computing architecture.
Anyway, the explosion of wireless communication clearly has extended worldwide, with the extremely high growth rate. This has greatly improved the communication model that we used to have, and it offers opportunity to enhance the quality of life.
REFERENCES


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