AN ULTRA LOW-POWER CMOS INSTRUMENTATION AMPLIFIER FOR BIOMEDICAL APPLICATIONS

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ABSTRACT

An ultra low-power biopotential instrumentation amplifier, based on the current balancing technique is presented. An internal programmable high-pass filter has been included in the instrumentation amplifier to filter out low-frequency artifacts if necessary. The instrumentation amplifier was fabricated in a multi-project test chip in 0.35 $\mu$m mixed mode CMOS process through MOSIS. Measurement results show that the instrumentation amplifier draws a current of 9 $\mu$A from a 3.3V lithium-ion battery and it has CMRR of 100dB and input voltage dynamic range of $\pm 6$mV. The input referred noise voltage is 0.3 $\mu$V/$\sqrt{Hz}$ with a flicker noise corner frequency of 15Hz. Design methodology and experimental results along with measurement issues are given in this paper.

1. INTRODUCTION

Instrumentation amplifiers are important signal conditioning blocks in many instrumentation systems for biomedical applications. Biopotential signals range from tens of $\mu$V for Electroencephalograms (EEG) to a few mV for Electromyograms (EMG) [1]. In low power applications like low power personal monitoring, biopotential instrumentation amplifiers with high common mode rejection ratio (CMRR), low input referred noise voltage and low offset as well as very low power consumption are required. In this paper an ultra low power biopotential instrumentation amplifier based on the current balancing technique, which has been designed and fabricated using a 0.35$\mu$m CMOS process, is presented. The current balancing technique is a low-cost approach for designing instrumentation amplifiers [2,3]. This useful technique has been used previously for design of instrumentation amplifiers for special applications [2,3]. The distinguishing features of the presented design as compared to earlier work is its very low power consumption and a programmable high-pass filter, which can be used for base line drift compensation. Circuit description and design implementation issues of the instrumentation amplifier along with measurement and experimental results are given in this paper.

2. CIRCUIT DESCRIPTION

Monolithic implementation of instrumentation amplifier by using traditional three operational amplifiers configuration needs accurate matching of the resistors used in its feedback network to achieve high CMRR. Also this structure is not a proper solution for very low power design.

Another approach for design of instrumentation amplifiers is to use current-balancing technique shown in Fig. 1[2]. At the transconductance stage, the input difference voltage is converted into a differential current $i_g$, flowing across resistor $R_g$. The input referred noise voltage is $0.3\mu V/\sqrt{Hz}$ with a flicker noise corner frequency of 15Hz. Design methodology and experimental results along with measurement issues are given in this paper.

$$i_g = \frac{v_{out} - v_{ref}}{v_{in} - v_{in-}} = \frac{R_s}{R_g}$$ (1)

The approach illustrated in Fig. 1 was used as the core of herein focused instrumentation amplifier. The goal was to have a low-power general-purpose biopotential amplifier. This goal led to some considerations at both circuit structure and sizing. We made the high-pass filter action to be programmable by using two external control bit lines and if necessary bypass it as shown in Fig. 1. Sizing issues will be explained in section 3 of this paper.

The circuit schematic of the fabricated instrumentation amplifier is shown in Fig. 2. Transistors ML1 and ML2 act as active load for input transistors M1 and M2. Transistors MGm1 and MGm2 make an internal transconductance amplifier with feedback path to the input stage through the cascode current mirrors. This feedback path makes drain currents of M1 and M2 remain constant. When a differential voltage is applied, the output currents of the transconductance amplifier become unbalanced in order to maintain the drain currents of M1 and M2 equal. Therefore input voltage will drop across $R_g$. At the transimpedance stage transistors M7 and M8, linearized by the internal op-amp, convert an input current into a voltage across resistor $R_c$. Thus input voltage is amplified at the output node by a value of
**R*/Rg.** The advantage is that the CMRR does not depend on any matching of resistor values [2].

We used the cascode current mirror to obtain high CMRR [3]. To avoid any extra current dissipation the cascode current mirror was sized such that its bias voltage can be taken from available voltages from cascode beta multiplier used for bias generation.

The main concern in the design was to fabricate a very low-power instrumentation amplifier while its main specifications satisfy requirements of analog front-end modules for portable biomedical instruments. To do this, the target CMRR was taken to be at least 90dB, maximum input referred noise voltage to be less than 10µV RMS in 200Hz BW and minimum input voltage dynamic range to be ±5mV. We decided to use on-chip resistors Rg and Rs to have less external components. Two external capacitors CHPF and CLP determine the lower and higher cutoff frequency of the amplifier, respectively. Frequency response of HPF is programmed by using two control bits. Also HPF can be disabled by setting both control bits at zero.

### 3. DESIGN AND IMPLEMENTATION ISSUES

Design of an ultra low-power instrumentation amplifier was our main concern while satisfying our target specifications. For a proper sizing procedure of low-power design, a sizing flow starting from an initial very low bias current guess was followed. This power-oriented design procedure for the transconductance stage is shown in Fig. 3. Setting very low bias current for input transistors M1 and M2, cascode current mirror transistors and active load transistors of the transconductance stage may provide very high CMRR. However, in the ultra low current...
region transistors are more sensitive to process parameter variations, which may increase the transistor mismatches. This effect increases the common-mode to differential-mode voltage conversion ratio. To reduce sensitivity of input offset voltage to the variation of the process parameters input transistors were kept in moderate inversion with absolute value of gate source overdrive voltage not less than 0.1V below the absolute value of threshold voltage. The corresponding constraint has been specified as $V_{GST_{\text{min}}}$ in Fig. 3. This consideration along with very low value of bias current at the input stage as well as area considerations leads to a maximum value for aspect ratio of transistors M1 and M2.

Value of $R_g$ and bias current of cascode current mirror stage determine input voltage dynamic range. For low power design we need to compromise between value of $R_g$ and power. However increasing $R_g$ increases contribution of current mirror transistor mismatches as well as $MGm1$ and $MGm2$ mismatches, in the offset voltage. This is because mismatch between these transistor pairs translates to a differential current flowing through resistor $R_g$. Hence all transistors of the transconductance stage sized by using high value of transistor length and also laid out in common-centroid fashion.

Design for low-noise performance needs to size active load transistors ML1 and ML2 to have enough lower transconductance than that of M1 and M2 [2]. This also helps to reduce threshold voltage mismatch between ML1 and ML2 on offset performance. The fabrication process limited the maximum transistor length to 20µm because of the lack of model parameters.

Our target was to use on-chip resistors to reduce number of external components. Poly resistors of high sheet resistance were not available in the fabrication process. Hence the $P^+$ implant layer with sheet resistance of 158.3 $\Omega/\square$ was used to implement $R_g$ and $R_s$. To reduce the area of the resistors we chose gain value of $R_s/R_g=6$. To have less sensitivity of $R_s/R_g$ ratio to temperature and process variations, these resistors were laid out in a common centroid inter-digit structure. If on-chip resistors of high sheet resistance are available, this structure can be used in a configurable manner to have programmable gain for instrumentation amplifier as per the target biopotential voltage. Values of $R_g$ and $R_s$ in the implemented instrumentation amplifier are 8k$\Omega$ and 48k$\Omega$, respectively.

After several iterations of the procedure shown in Fig. 3 the bias current of each one of the transconductance stage transistors was set to 0.65µA and the aspect ratio of input transistors M1 and M2 was set to 15.

### 4. MEASUREMENT AND EXPERIMENTAL RESULTS

The instrumentation amplifier was fabricated in a multi project chip through MOSIS. Fig. 4 is a

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**Figure 3. Power-oriented sizing procedure of the transconductance stage of instrumentation amplifier**

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise,CMRR,Offset,Area,$V_{GST_{\text{min}}}$</td>
<td>Size M1 &amp; M2</td>
</tr>
<tr>
<td>Dynamic range, Area</td>
<td>Size $R_g$</td>
</tr>
<tr>
<td>Noise,Offset,$V_{CM_{\text{min}}}$</td>
<td>Size ML1 &amp; ML2</td>
</tr>
<tr>
<td>Loop gain</td>
<td>Size $MGm1$ &amp; $MGm2$</td>
</tr>
<tr>
<td>Internal bias voltage, $V_{CM_{\text{min}}}$</td>
<td>Size cascode current mirror transistors</td>
</tr>
</tbody>
</table>
photograph of a part of the chip, in which the instrumentation amplifier is highlighted in a black rectangle. The area of the instrumentation amplifier is 0.2 mm$^2$.

Measured parameters of the fabricated instrumentation amplifier are given in Table 1. To accurately measure the CMRR we used a DSP lock-in amplifier [4]. Fig. 5 shows the measurement setup for measuring common mode gain, from which CMRR was calculated. Lock-in amplifier was used in differential-mode input to avoid errors due to external noise sources like ground loop and analog ground noises [4]. Noise performance of the amplifier, while disabling HPF and removing external CLPF, is shown in Fig. 6. Noise spectrum of the instrumentation amplifier was measured by using FFT spectrum analyzer. To obtain a smooth power spectral density of the noise we used linear averaging with uniform windowing with zero overlap and average number set to 800.

5. CONCLUSIONS

A single supply battery-operated ultra low power high CMRR instrumentation amplifier fabricated in 0.35 µm CMOS technology is presented in this paper. This instrumentation amplifier draws 9µA from a 3.3V lithium-ion battery and has a programmable high pass filter response. Design issues for ultra low-power design along with the sizing procedure are also explained.

6. ACKNOWLEDGMENT

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7. REFERENCES


