

# Call for participation: validation and deployment of IRNSS/GPS receiver SOC developed by IIT-Bombay

Department of Electrical Engineering  
IIT Bombay, Mumbai

October 16, 2020

## 1 Background

IITB is building an IRNSS+GPS receiver system-on-chip (SOC) for GNSS applications. The project is funded by MeITY. Some of the unique features of this receiver SOC are as follows:

- Three independent radio frequency front-end (RF-ADC) interfaces: can simultaneously work with three RF channels (L1 for GPS, L5 and S for IRNSS).
- Up to 64 satellites can be acquired and 36 can be tracked simultaneously.
- Fully programmable co-processor based architecture offers flexibility to application developers.

This SOC is a fully indigenous implementation, which uses the AJIT processor developed at IIT Bombay, together with novel co-processor and RF signal processor.

A complete FPGA prototype of the system has been completed and is being validated. A 65nm test chip implementation of the SOC will be ready by March 2021.

## 2 Call for participation

We invite interested parties to collaborate with IIT-Bombay in the following phases

- Validation phase: work with IIT-Bombay to validate the receiver functionality using the FPGA prototype of the system. IIT-Bombay will make the FPGA prototype available to interested parties for the duration of the validation phase, and will also provide a training program on the use and programming of the prototype.
- Test product development phase: Based on the 65nm ASIC samples, we propose to work with interested parties to design and develop proof of concept products. The 65nm ASIC provides two mechanisms (UART/SPI) using the NMEA 0183 standard protocol to connect user hardware to the receiver SOC.
- Mass production and deployment plan: IITB proposes to implement the validated receiver SOC in a lower power 28nm ASIC technology and provide these chips to device manufacturers on a large scale for mass deployment. Interested parties are welcome to collaborate with IITB in the development and deployment of the ASIC.

## 3 Contact information

Interested parties can contact us at the following address:

Department of Electrical Engineering  
Indian Institute of Technology, Bombay  
Powai, Mumbai 400076  
Attention: Head, Department of Electrical Engg.  
email: [head@ee.iitb.ac.in](mailto:head@ee.iitb.ac.in), [eeoffice@ee.iitb.ac.in](mailto:eeoffice@ee.iitb.ac.in)