Study of flicker noise and RTN for characterization of gate dielectrics in MOS systems

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By

Bijesh R

Roll No – 08307015

(bijeshr@ee.iitb.ac.in)

Under the guidance of

Prof. Anil Kottantharayil

Department Of Electrical Engineering

Indian Institute Of Technology, Bombay

Thesis Approval

The thesis entitled

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Abstract

Low frequency noise is getting increasing attention as dimensions scale down. Ths study of LFN is important because of its appearance as a fundamental limit for scaling, its impact on RF and analog applications but most importantly it can serve as a diagnostic tool for quality and reliability of MOSFETs. The interface between the dielectric and channel is not ideal. Further as newer materials are introduced to propel scaling further, the interface goes far from ideal and it become necessary to characterize them. LFN comprises of 1/f noise and RTN. RTN is seen in devices with low dimensions where the probability of having a single dominant trap is high and is characterized by Lorentzian spectrum in the frequency domain and two level current fluctuations. 1/f is seen in devices when the trap density is high and is understood as the summed up response of several traps. This report deals with exploring LFN as a diagnostic tool for characterizing MOSFETs and tries to explain the theory behind them as well as the experimental results obtained.

Measuring RTN is challenging because of line frequency interface (50 Hz and its harmonics). Details of the troubleshooting done and how the setup was fixed are explained. Using the modified setup, RTN measurements were done on RENESAS wafers and analysis was done to correlate it with frequency domain spectrum. A comparison of noise between capped and non-capped wafers were also done.

Study of flicker noise in SiGe pMOSFETS are also included in this report which includes flicker comparison between control, Si capped SiGe pMOSFET and non-capped SiGe pMOSFET. Also NBTI correlation of flicker degradation for non-capped SiGe pMOSFET is done.

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Chapter 1
Introduction

Dimensional scaling continues to drive the developments in CMOS. Shrinking the active area of the transistors has tremendous impact on its low frequency noise which increases with reduction in active area as well as oxide thickness [1]. For transistors with lower dimensions, the total number of active noise centres becomes small, so that local process variations can lead to large device to device variations in the noise [2]. Also in these devices random telegraph signals are observed, giving rise to a Lorentzian type of spectrum whereas in larger devices LFN takes the form of 1/f noise (actually $1/f^{\gamma}$ where γ varies from 0.6 to 1.3) [3].

The growing dominance of low frequency noise (LFN) with scaling has triggered strong interest in its study as it may form a fundamental limit for scaled devices [4, 5]. LFN is also of interest due to its impact on radio frequency and analog applications [6]. For example, the phase noise of voltage controlled oscillators can be dominated by LFN. Similar is the case with analog circuits like amplifiers, CMOS cameras where LFN is crucial for proper device operation. Besides all these, LFN can also serve as a good reliability and quality monitor and is very sensitive to technological factors [7].

This report is organized into six chapters. Chapter 2 covers the theory of LFN (both flicker and RTN) and also explains how flicker and RTN are related to each other. Chapter 3 deals with the debug activities done to remove the line frequency interference and make the system ready for RTS measurements. In Chapter 4, measurements done on RENESAS pMOSFETs are explained. RTS measurement was taken and analyzed. Flicker noise data was also taken and correlated to RTS. The study on SiGe devices are explained in Chapter 5. Comparison of flicker noise between control, SiGe pMOSFET with Si capping and SiGe pMOSFET without cap was done. Also, correlation between NBTI and flicker degradation was done. Finally in Chapter 6 summary of the work done as part of this thesis have been presented and future work also suggested.

Chapter 2
Literature Review

2.1 Random Telegraph Noise

RTS measured in the drain current of a MOSFET as a function of time shows itself in the form of switching events between two or more states. It is attributed to the trapping-detrapping events caused by an individual defect near the channel-dielectric interface. The times in the high- and low-current states correspond to carrier capture and emission times. The bias voltage dependence of the capture and emission times allows one to determine the type and location of the defects. This chapter explains how to extract trap parameters from RTN, the flicker noise theory and different noise models.

2.1.1 Capture and Emission Times

Carrier transitions between the oxide traps and the channel are governed by Shockley-Read-Hall (SRH) statistics [8], where capture and emission times are expressed as[8]

$$\tau_c = \frac{1}{\overline{c_n}.n} = \frac{1}{\sigma.V_{th}.n} \tag{2.1}$$

$$\tau_e = \frac{1}{\overline{e_n}} = \frac{\tau_c}{g}\exp\left[-\frac{E_T - E_F}{k_B T}\right] \tag{2.2}$$

where g is the degeneracy factor, k_B is the Boltzmann constant, T is the temperature, σ is the capture cross section, V_{th} is the thermal velocity , and n is carrier concentration. E_F and E_T are Fermi and trap energy levels, respectively. σ is the capture cross section, $\overline{e_n}$ is the emission probability defined as the inverse of the emission time.

The gate voltage dependence of the RTS up and down times can be used to identify the polarity of the trap i.e. whether acceptor or donor type [9]. From Eq. (2.2) the change of ratio of τ_c / τ_e with respect to the position of Fermi level can be used to identify the type of the trap. For an nMOSFET, as the gate voltage is increased $E_T - E_F$ decreases and hence the ratio τ_c / τ_e decreases which mean the trap is more likely to be full. If the trap is acceptor type, then with increased gate bias, increase in $\bar{\tau}_0$ will be observed. For donor type trap, the opposite behaviour would be seen.

2.1.2 Extracting the position and energy of the trap

If the trap is locate at x_T in the oxide and y_T along the channel measured from the source then Eq. (2.2) can be rewritten as [9],

$$\ln\frac{\tau c}{\tau e} = -\frac{1}{k_B T}\left[(E_{cox} - E_T) - (E_C - E_{Fp} + qV_c) - \phi_0 + q\varphi_s + q\frac{x_T}{T_{ox}}(V_{gs} - V_{FB} - \varphi_s) \right] \qquad (2.3)$$

E_{cox} is the conduction band edge of the oxide, E_C is the conduction band edge of the silicon, ϕ_0 is the difference between the electron affinities of Si and SiO2, φ_s is the amount of band bending, V_{FB} is the flat-band voltage, T_{ox} is the oxide thickness.

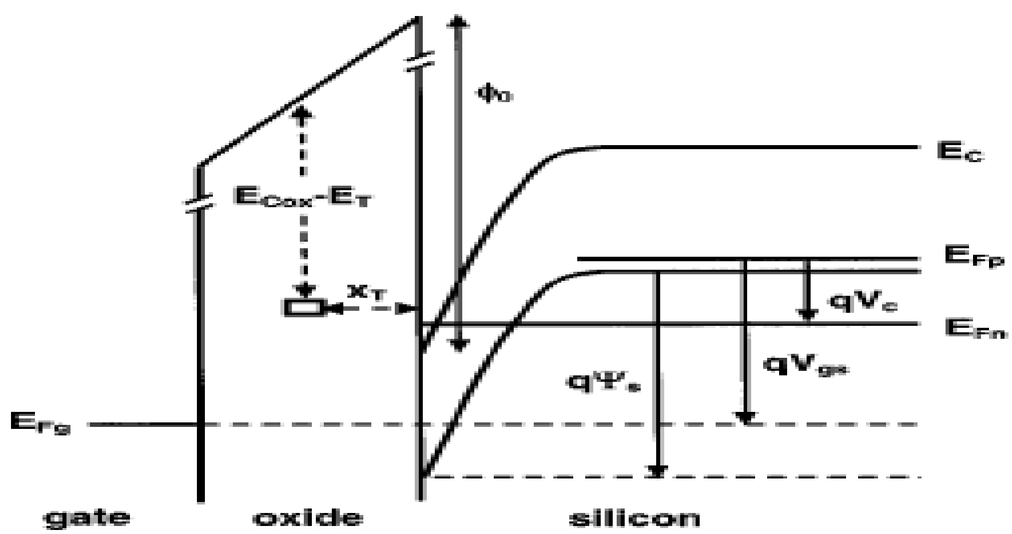

Fig. 2.1 The energy band diagram of the oxide-channel interface

Position of the trap can be extracted by the V_{gs} dependence of $\ln\frac{\tau c}{\tau e}$ which is [9],

$$\frac{d(\ln \frac{\overline{\tau c}}{\overline{\tau e}})}{dV_{gs}} = -\frac{q}{k_B T}\frac{x_T}{T_{ox}} \tag{2.4}$$

To locate y_T, drain voltage dependence of $\overline{\tau_c}$ and $\overline{\tau_e}$ in forward and reverse modes of operation would be required (reverse in the sense when the role of source and drain are exchanged). Hence [9],

$$\ln\left[\frac{(\bar{\tau}_c/\bar{\tau}_e)_{f_{\max}}}{(\bar{\tau}_c/\bar{\tau}_e)_{r_{\max}}}\right] = \frac{q}{kT_B}\frac{x_T}{T_{ox}}\left[\frac{y_T}{L}V_{ds\,f_{\max}} - \left(1-\frac{y_T}{L}\right)V_{ds\,f_{\max}}\right] \tag{2.5}$$

The energy level of the trap can be found using Eq. (2.3) once x_T and y_T are known.

2.1.3 Complex RTS

Complex RTS showing three or more levels have been reported [10], but a complete physical explanation hasn't been offered yet. Complex RTS can be attributed to many scenarios. A single trap might exist in more than one metastable state causing multiple levels. There could also be multiple independent traps. It might also be possible that multiple traps exist whose occupancies are affected by each other

2.2 Flicker (1/f) Noise

There are three major theories to explain the physical origin of flicker noise in MOSFETs: the number fluctuation theory based on the McWhorter's charge trapping model, the bulk mobility fluctuation theory based on Hooge's hypothesis and the unified flicker noise model. The unified flicker noise model came into existence because reconciliation hasn't been reached between the first two models.

2.2.1 Number Fluctuation Theory

As per this theory [11], the gate referred noise is given as,

$$S_{vg} = \frac{kTq^2}{8WLC_{ox}{}^2\alpha}\frac{N_t(E_{fn})}{f} \tag{2.6}$$

where k is the Boltzmann constant, T is the temperature in Kelvin, I_d is the drain current, L is the length of the channel, f is the frequency, V_d is the drain voltage, $N_t(E_{fn})$ is the apparent oxide trap density at energy level corresponding to quasi Fermi level.

Assumptions taken in formulating the above equation are:

a) The trapping of an inversion layer carrier by an oxide trap is assumed to induce only a carrier density fluctuation and mobility fluctuation due to scattering of the trapped charge is negligible.
b) Inelastic tunneling is regarded as unlikely.
c) The device is biased in the linear region.
d) The oxide tunneling barrier seen by an inversion layer carrier is a rectangular barrier of height ϕ_B where ϕ_B is the height of the oxide conduction band edge from the silicon conduction band edge .
e) When one unit of charge is trapped at a distance within oxide , it produces a charge fluctuation in the channel that is less than one unit of charge, but can be treated as same if the trap distance is very small compared to the oxide thickness.

In case of non-uniform trap distribution, the spectrum changes from pure $1/f$ to $1/f^{\gamma}$ where $\gamma \neq 1$.For a trap distribution that is skewed toward the interface, there are a greater number of high-frequency traps leading to $\gamma < 1$. Similarly for a trap distribution that is skewed away from the interface, there are a greater number of low-frequency traps leading to $\gamma > 1$.

2.2.2 Mobility Fluctuation Theory

This theory considers the flicker noise as a result in the fluctuation of bulk mobility based on Hooge's empirical relation [11],

$$\frac{S_{Id}}{I_d^2} = \frac{\alpha_H}{fN_{total}} \tag{2.7}$$

where S_{Id} is the spectra of the drain current, Id is the drain current, α_H is Hooge's parameter which is an empirical parameter, N_{total} is the total number of free carriers in the channel, f is the frequency. This theory predicts an input referred noise power which is proportional to $(Vg - Vth)C_{ox}^{-1}$.

2.2.3 Unified Theory

This theory incorporates both the number fluctuation and surface mobility fluctuation mechanisms. The latter is attributed to the scattering effect of the fluctuating oxide charge. As these fluctuations have the same cause, they are correlated with each other. Using the correlation theory of 1/f theory, the fluctuation in the drain current due to a single electron capture and emission by a defect can be expressed as [12],

$$\frac{\delta Id}{Id} = \frac{1}{\Delta N}\left[\frac{\delta \Delta N}{\delta \Delta N_t} \pm \frac{1}{\mu_{eff}}\frac{\delta \mu_{eff}}{\delta \Delta N_t}\right]\delta \Delta N_t \tag{2.8}$$

where ΔN_t is the number of occupied traps per unit area, ΔN is the change in channel carrier density. Using the Mathiessen's rule [12],

$$\frac{1}{\mu} = \frac{1}{\mu_n} + \frac{1}{\mu_{ox}} = \frac{1}{\mu_n} + \alpha N_t \tag{2.9}$$

(2.7) where μ_{ox} is the mobility limited by oxide charge scattering, and μ_n is the mobility limited by other scattering mechanisms

The total drain current noise power spectrum is given by [12],

$$S_{Id}(f) = \frac{kTI^2{}_d}{\gamma f W L^2}\int_0^L N_t(E_{fn})\left[\frac{1}{N(x)} \pm \alpha\mu\right]^2 dx \tag{2.10}$$

At low drain voltages, the carrier density is uniform along the channel and hence the above expression can be rewritten as [12],

$$S_{Id}(f) = \frac{kTI^2{}_d}{\gamma f W L}\left(\frac{1}{2} + \alpha\mu\right)^2 N_t(E_{fn}) \tag{2.11}$$

and $Svg(f)$ becomes [12],

$$Svg(f) = \frac{kTq^2}{\gamma f W L C^2{}_{ox}}\left(1 + \alpha\mu N\right)^2 N_t(E_{fn}) \tag{2.12}$$

Chapter 3

Improving 1/f noise measurement setup for RTN measurements

3.1 Introduction

This chapter explains the problems associated with the existing experimental setup for measuring flicker noise and why the same setup can't be used for measuring RTN. The details of the troubleshooting done are explained and solutions proposed.

3.2 Problems with the existing measurement set-up

The current setup comprises of the Low Noise Amplifier (Manufactured by Stanford Research, model number SR570) which forces the drain bias and senses the drain current, Spectrum Analyzer (Manufactured by Stanford research, model number SR760) which generates the spectrum of the drain current, Source Measure Unit (Manufactured by Keithley, model number K237) which provides the gate bias, Digital Storage Oscilloscope (Manufactured by Tektronix, model number TDS210). The setup has been facing line frequency interference (50 Hz and its harmonics) which interferes with the drain current noise of MOSFET. This is not a serious issue when we measure 1/f noise since the data can be manually edited post measurement. In case of RTN, the noise is to be studied in time domain and hence we would be observing either sine waves (if 50 hertz is dominant one) or a complex periodic signal (if other harmonics are also dominant).

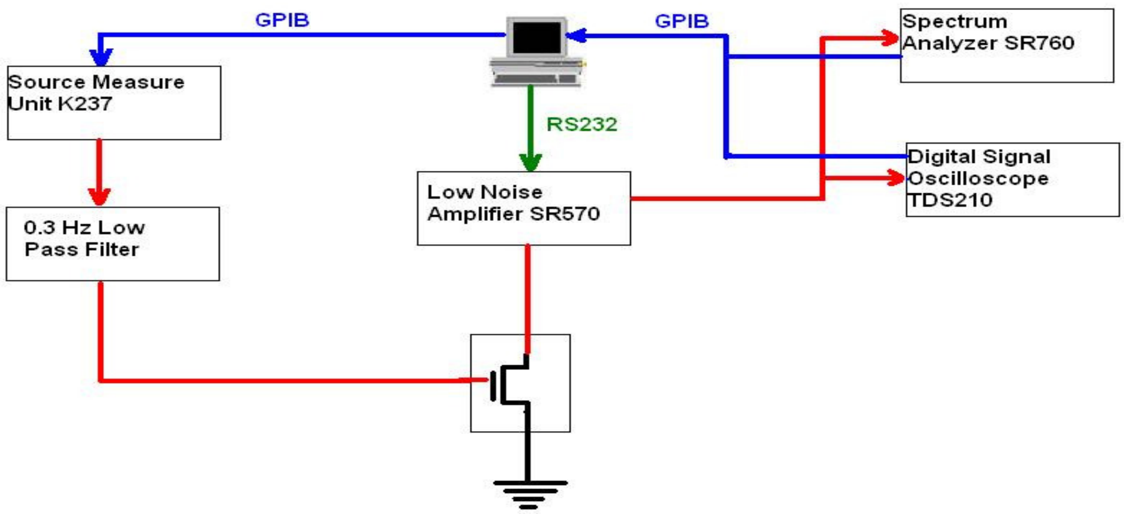

Fig. 3.1 Block diagram of the current experimental setup for measuring noise

To better understand the problems associated with the current setup and find solutions a set of experiments were done which are discussed in section 3.2

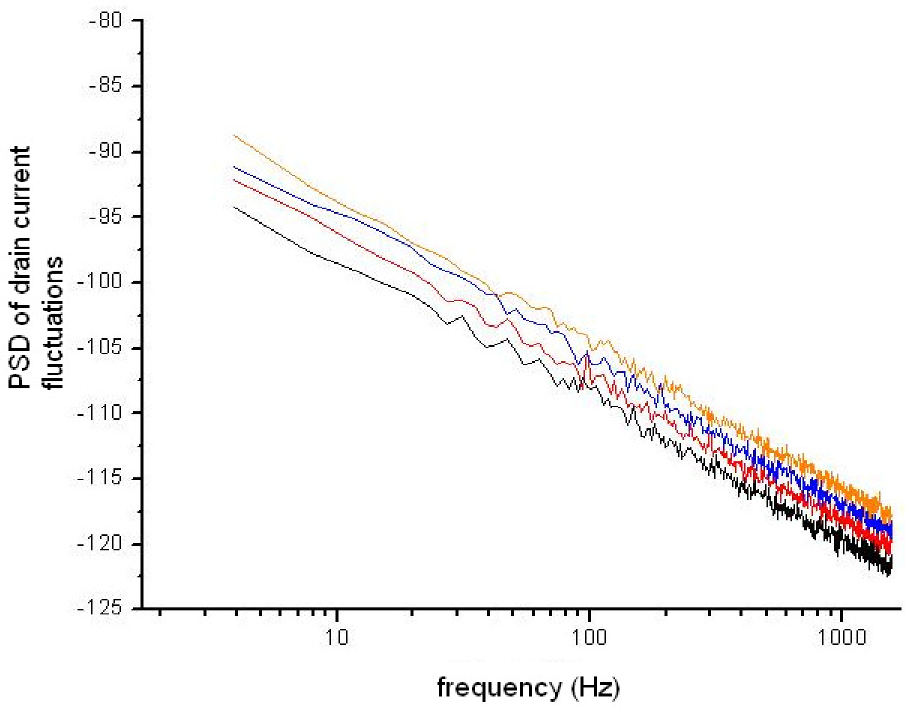

Fig. 3.2 Interference free flicker noise spectrum

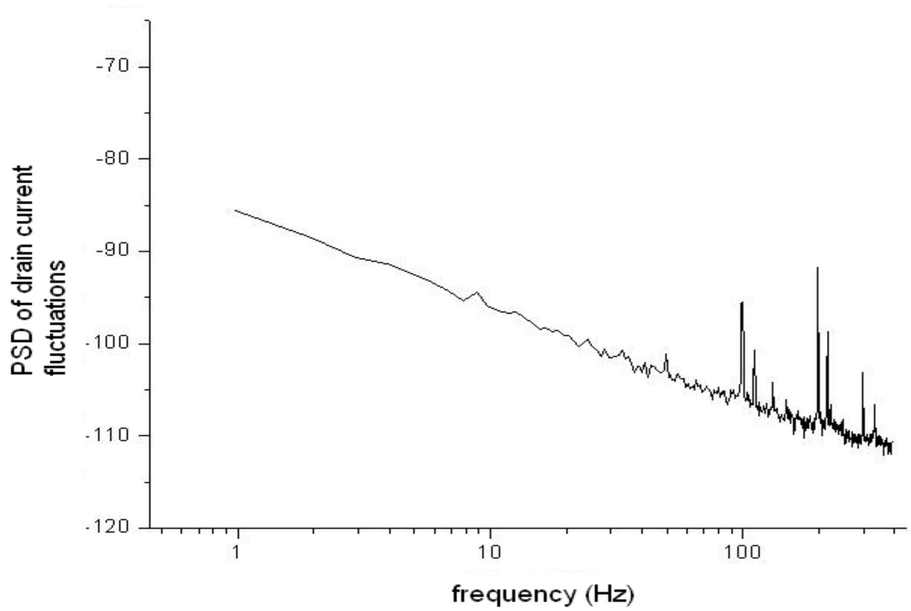

Fig. 3.3 Flicker noise spectrum corrupted by line frequency interference

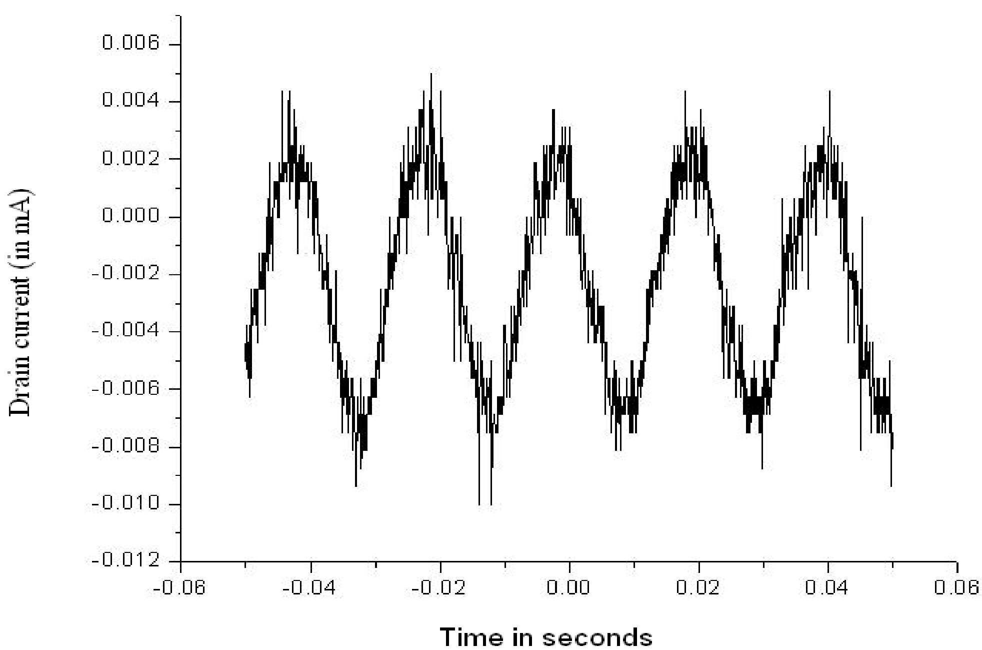

Fig. 3.4 Corrupted noise when seen in the time domain (50Hz is clearly visible)

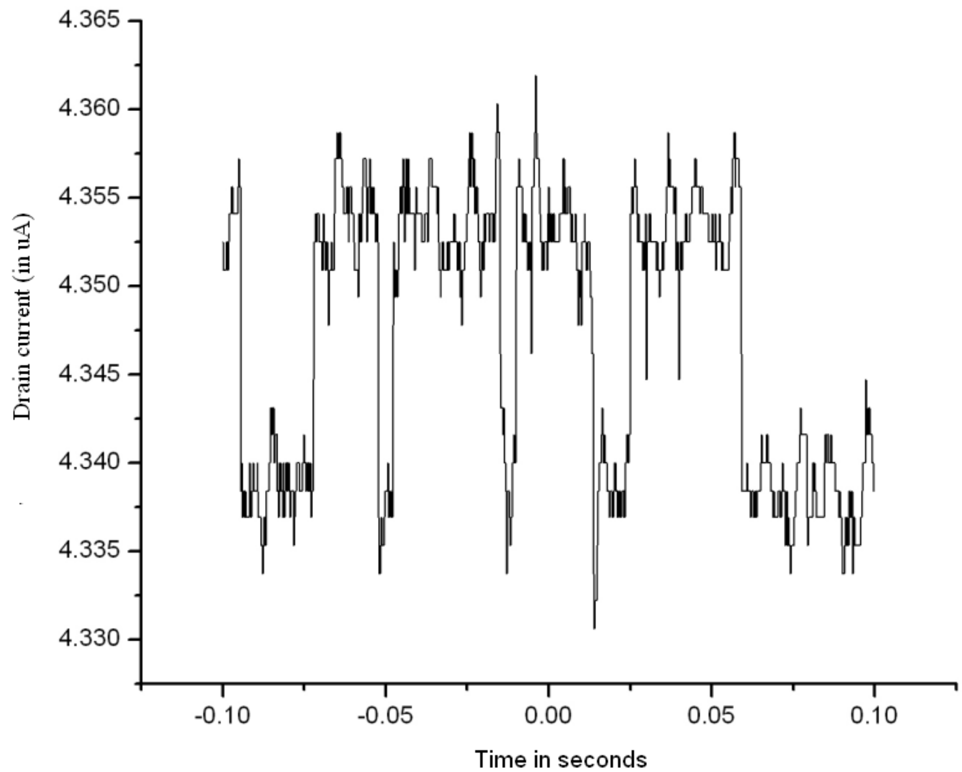

Fig. 3.5 RTN seen in time domain (two level fluctuation is seen)

3.3 Troubleshooting the setup

A. Incorporating isolated voltage supply (SIM 928):

The idea was to make the complete biasing circuitry isolated from the mains. SIM 928 has two batteries internal to it. One battery can provide dc supply while the other needs to be charged using external dc supplies. The code was developed to generate Id-Vg characteristics using SIM 928 as the gate bias. But when noise measurement was made using SIM 928 as the gate bias, no appreciable improvement was seen in the noise spectra. The reasoning for this unexpected observation follows from the explanations given in the section **3.3B**. It turned out that SIM 928 is no better than the normal SMU with a low pass filter connected to it

B. Using differential mode of the spectrum analyzer (SR 760)

SR 760 can operate in differential mode in which it will first take the difference between signals in its two input ports A and B before proceeding with generating spectrum. Assuming that the noise generated is due to pick up through ambient, then it is fair to say that two identical cables kept side by side would have the same noise pick up. Hence an identical cable was connected to port B and noise spectrum taken. No difference was observed in terms of the interference seen. This proves that the noise was not picked up by the cable that connects SR760 to the LNA.

C. Testing different cables for noise pick up

Motivated from the observations seen in the above experiment, different cables in the setup were tested individually. For this, cables were connected to Digital Storage Oscilloscope (DSO) and the other end was kept floating. It was seen that most of the BNC cables (which have a ground shielding surrounding the signal line) with BNC (Bayonet Neill-Concelman) connectors at either ends, picked up 50Hz noise.

D. Checking for ground loops

Ground loops have been cause of worry in audio systems because they can pick up 50 Hz noise. The connections were analyzed in detail for the presence of ground loop. One ground loop was identified in the setup and was removed, but no improvement was seen from interference point of view. This means that noise pick up due to ground loops is not a major factor or rather, there is another source of noise which introduces so much interference that the role of ground loops can be neglected.

E. Testing the spectrum analyzer

It was proposed that the interferences could be generated from the spectrum analyzer (SR760), and the input port of SR760 was connected to DSO. A periodic waveform of period 50 Hz was seen in the DSO which shows that SR760 itself generates noise. As a result, SR760 was removed from the setup and drain current of MOSFET was observed directly on the DSO where 50 Hz signal was seen. This showed that though SR760 is noisy, that is not the main reason for the interference seen. Further, from flicker noise point of view, this is not a problem since the interference can be removed manually, but for RTN this could be a problem but can be solved by removing SR760 from the setup during RTN measurements.

F. Working on UPS

It was thought was that working on UPS might isolate the circuit from external interferences, but no appreciable improvement was seen.

G. Testing the LNA

It was seen that if the gate SMU is removed from the setup and the LNA is used to bias and measure the noise in a resistor, noise free spectrum was seen. Hence, it can be said that when LNA is acting alone, the interferences disappear and that the gate SMU is noisy.

Based on the observations from the above set of experiments, it has been found that there are two ways in which noise gets injected to the circuit: 1) Noise pick up from ambient.2) Noise generated within the setup.

3.4 Major sources causing interference

A. Noise pick up from ambient

The source of this radiation could be anything. Some of them are extension cords, faulty plugs, air conditioners, machines that consume high current. It has also been seen that there is a basic problem involving the wiring in the characterization lab (and also in most other areas of IIT Bombay). A hanging wire connected to a DSO is able to pick up sine waves of 50 hz. This is due to improper wiring, wherein the forward and return current paths are not identical thus generating a net magnetic field. The problem with noise coming from radiation pick up is that they ride on top of a signal, independent of how strong the signal is driven. Hence, if this pick up cannot be controlled, then it is impossible to get noise free environment for RTN measurements.

B. Noise generated within the setup

The motivation for this line of thought is as follows. It has been observed that whenever the gate of the MOSFET loses control and the MOSFET behaves as a resistor, the noise spectrum is seen to be nearly free from any interference. This shows that there is a problem associated with the SMU that bias the gate. This SMU works on supply, hence its expected that its output is noisy. As a result a low pass filter of 0.13 hz has been inserted between this SMU output and the gate terminal of the MOSFET. This will of course ensure that the gate bias is silent (DC), but with respect to its own ground. It was observed that the ground point of the SMU is very noisy (with respect to earth) and sine wave of magnitude as high as 4v p-p has been observed. The drain bias is through a low noise amplifier (LNA) which works on battery. Hence the drain bias is silent with respect to its ground. But the problem arises when we try to connect the SMU and LNA together because the two grounds are of different phase. As a result, noise is generated in the drain current from within the circuit which later gets amplified by the LNA (which is actually meant to amplify flicker/RTS noise).

3.5 Proposed Solutions

A. To control noise pick up through ambient

Proper shielding is the only way to prevent noise pick up from the ambient. Hence, if possible, shielded BNC cables have to be used everywhere in the setup. To connect to ports which are not BNC type, proper adapters have to be used. Once this is done, the next step is to check the four probes (drain, source, gate and substrate) for noise pickup. The probes are connected to BNC cables. It is a good practise to connect the probes to DSO before starting the experiment for verifying possible noise pickup. If there is noise pickup, then the user has to try turning off electric switches which are closer to these probes and make sure there is no noise pick up through the probes. Once these steps are done, then we can be sure that there is no noise pick up through ambient.

B. To control noise generated within the circuit

Ideally an SMU which operates on battery with single ground point and two source/measure points is needed, but such kind of an instrument is currently not available in the market. Hence the next best alternative is to replace the current gate SMU which works on supply by identical LNA that is used for drain bias.

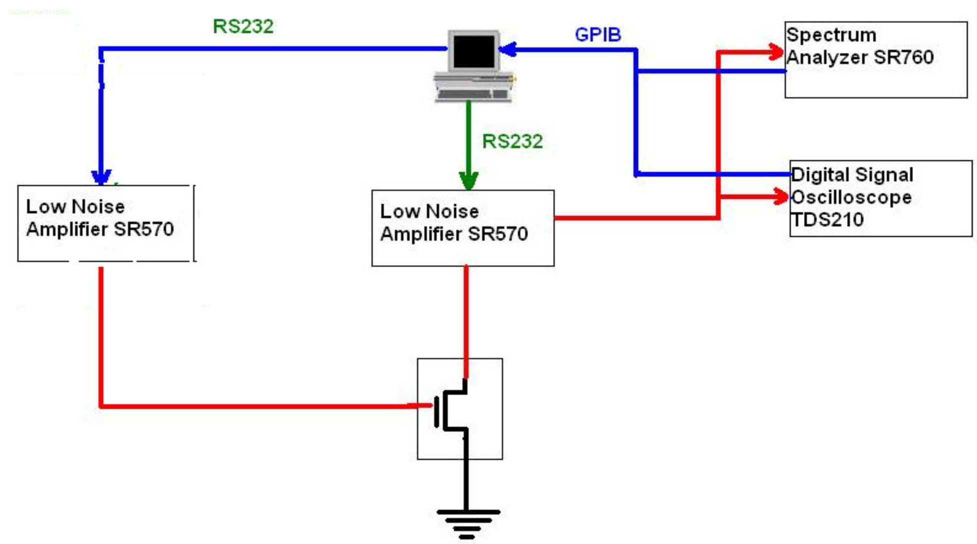

Fig. 3.6 Block diagram of the new experimental set-up for measuring RTS noise

3.6 Results

Interference issue was solved successfully following the solutions proposed in section 3.4. The interference free plots generated from the new set-up are shown in chapter 4.

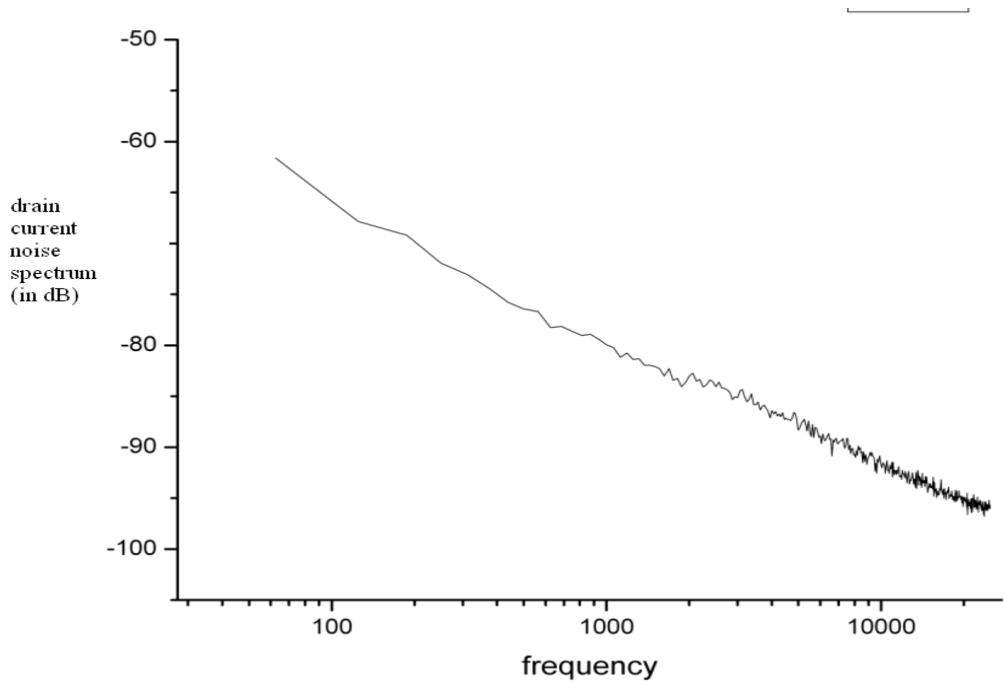

Fig. 3.7 Drain current spectrum free of interference measured with the new setup

Chapter 4

Time domain and frequency domain correlation of Random Telegraph Noise

4.1 Introduction

Following the solutions suggested in Chapter 3, considerable reduction in the line frequency interference was observed. As a result, discrete fluctuations in the drain current could be observed in the time domain data (captured by DSO). An attempt was done to correlate the frequency domain spectrum to the discrete fluctuations in the time domain the details of which are explained in this chapter. Flicker noise comparison between AlO capped and non-capped pMOSFETS are given.

4.2 Theory of RTN

RTS are two level switching events between state 0 (low level) and state 1 (high level). The three parameters that define the RTS are its amplitude *ΔI*; the average time for state 0, $\bar{\tau}_0$; and the average time for state 1, $\bar{\tau}_1$. Assuming that the probability of transition from state 1 to state 0 is given by $1/\bar{\tau}_1$ and the probability of transition from state 0 to state 1 can be given by $1/\bar{\tau}_0$. This means the probability that the RTS is in state 1 can be given as $\bar{\tau}_1/(\bar{\tau}_0+\bar{\tau}_1)$, and the probability that RTS is in state 0 is $\bar{\tau}_0/(\bar{\tau}_0+\bar{\tau}_1)$. Further, it can be assumed that state 0 has amplitude x_0 and state 1 has amplitude $x_1 = \Delta I$. Defining $P_{10}(t)$ and $P_{11}(t)$ as the probability of an odd and even number of transitions from state 1 at time t, respectively, then [3, 13]

$$P_{10}(t) + P_{11}(t) = 1 \tag{4.1}$$

The probability of an even number of transitions in time *t+dt* is given by the probability of an odd number of transitions in the time t and one transition in time *dt*, and the probability of an even number of transitions in the time t and no transition in time *dt*; the two being mutually exclusive events.

$$P_{11}(t+dt) = P_{10}(t)\frac{dt}{\tau_0} + P_{11}(t)(1-\frac{dt}{\tau_1}) \qquad (4.2)$$

Substituting Eq. (4.1) into Eq. (4.2),

$$P_{11}(t+dt) - P_{11}(t) = \frac{dt}{\tau_0} - P_{11}(t)\left(\frac{dt}{\tau_0}+\frac{dt}{\tau_1}\right) \qquad (4.3)$$

If the time dt is small enough that the probability of having a second transition during the time dt is negligibly small, Eq. (4.3) can be written as

$$\lim_{dt\to 0}\frac{P_{11}(t+dt)-P_{11}(t)}{dt} = \frac{1}{\tau_0} - P_{11}(t)\left(\frac{1}{\tau_0}+\frac{1}{\tau_1}\right) \qquad (4.4)$$

which gives rise to the differential equation

$$\frac{dP_{11}(t)}{dt} + P_{11}(t)\left(\frac{1}{\tau_0}+\frac{1}{\tau_1}\right) = \frac{1}{\tau_0} \qquad (4.5)$$

Solving this equation and making use of the autocorrelation function, the power spectral density of the fluctuations as

$$S_{\mathrm{I}}(f) = \frac{4(\Delta I)^2}{(\tau_0+\tau_1)[(1/\tau_0+1/\tau_1)^2+(2\pi f)^2]} \qquad (4.6)$$

This equation can be expressed of the form

$$S_{\mathrm{I}}(f) = \frac{k}{1+(f/f_0)^2} \qquad (4.7)$$

where

$$f_0 = \frac{1}{2\pi\tau} \qquad (4.8)$$

with τ defined as

$$\frac{1}{\tau} = \frac{1}{\tau_0}+\frac{1}{\tau_1} \qquad (4.9)$$

4.3 Experimental

The devices were supplied by Renesas and two wafers were available- one with AlO cap and one without AlO cap (figure 4.1).

Wafer	channel F dose	IL	N% in IL	HfSiON	AlO cap	Gate electrode
23	none	1nm	-	~1.5nm	0.4nm	polySi/TiN
24					none	

Fig. 4.1 Renesas wafer details

In order to study RTN, the smallest possible device was chosen from the wafer(as the possibility of a single dominant trap would be high in that case). The smallest dimension available was W/L of 0.5um/0.04um. Further, RTN could only be observed in the devices with AlO cap.

Comparisons of flicker noise between the two wafers were also done. Device dimensions chosen for this purpose were W/L of 0.5um/0.16um, 0.5um/0.24um and 0.5um/0.30um.

4.4 Results

4.4.1 RTN

Fig. 4.2 and Fig 4.3 show the time domain and frequency domain representation of RTN. The time domain is characterized by discrete two level fluctuations (not exactly two level fluctuation because of background noise). The drain bias was set -0.1V and the gate bias was -0.7V (the threshold voltage of the MOSFET being -0.6V). The frequency domain shows a distinct corner frequency (as expected from the derivation in section 4.2). The corner frequency as seen from the frequency domain is around 14 Hz whereas the calculations from the time domain (from equation 4.8 and 4.9) give this to be around 2 Hz (the MATLAB codes used for this calculation is given in Appendix A). Also the slope of the spectrum after the corner frequency is seen to be around 15dB instead of the expected 20db (from equation 4.7).

At higher gate bias(-1.0V), it was seen that the fluctuations in time domain involved multiple levels (fig 4.4). In the frequency domain, it was seen that the distinct corner frequency is no longer visible, rather the spectrum looked like flicker noise spectrum. The reason for this could be that higher number of traps were present near the valence band energy level and due to high gate bias and the resulting band bending, the quasi Fermi level came closer to the valence band and hence higher number of active traps were present , and the resulting spectrum came out to be combined trapping/de-trapping events of all these traps.

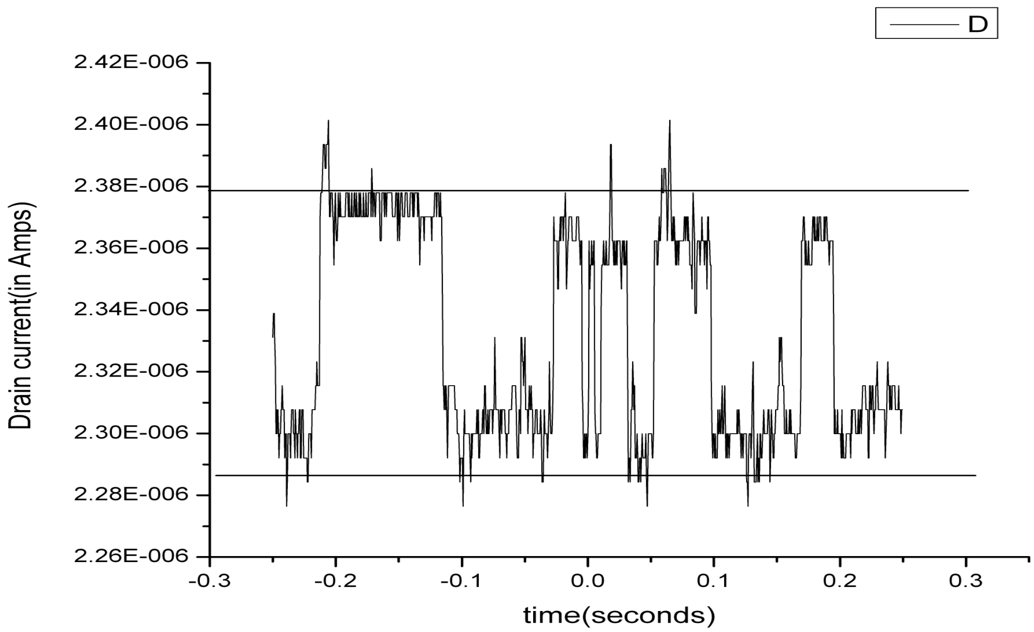

Fig. 4.2 RTN captured in DSO at gate bias of -0.7V

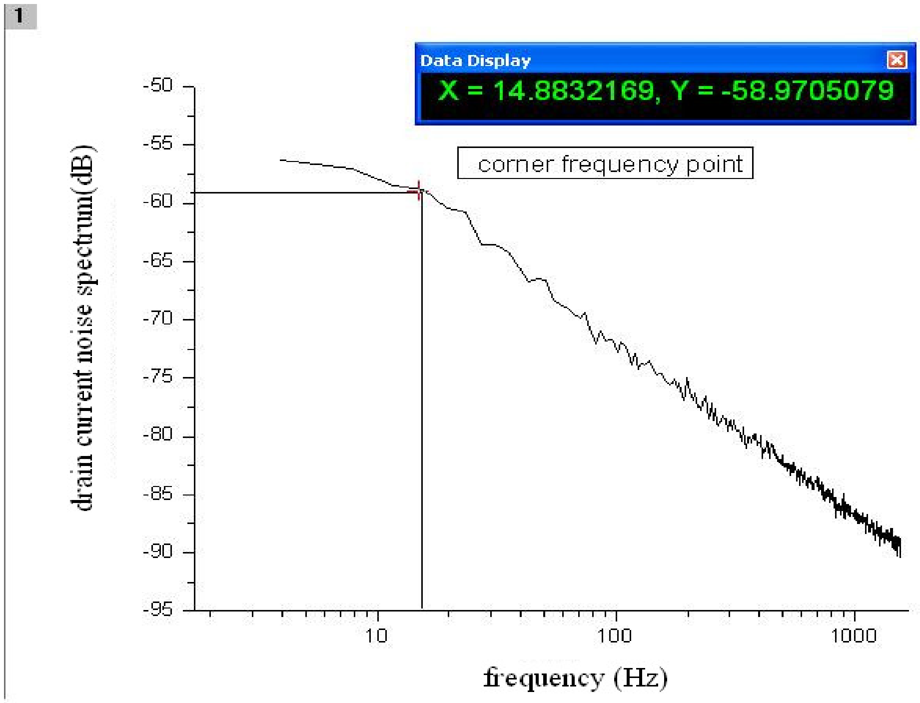

Fig. 4.3 Frequency spectrum of the time domain signal of Fig. 4.2

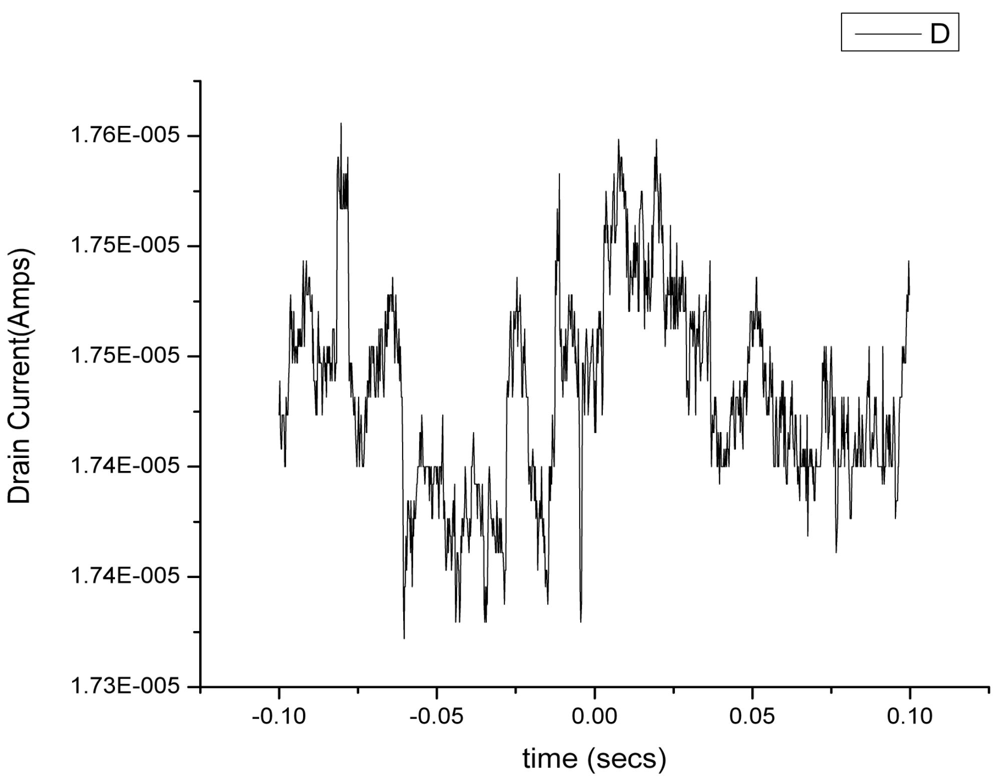

Fig. 4.4 Time domain version of drain current fluctuation at higher gate bias (-1.0V)

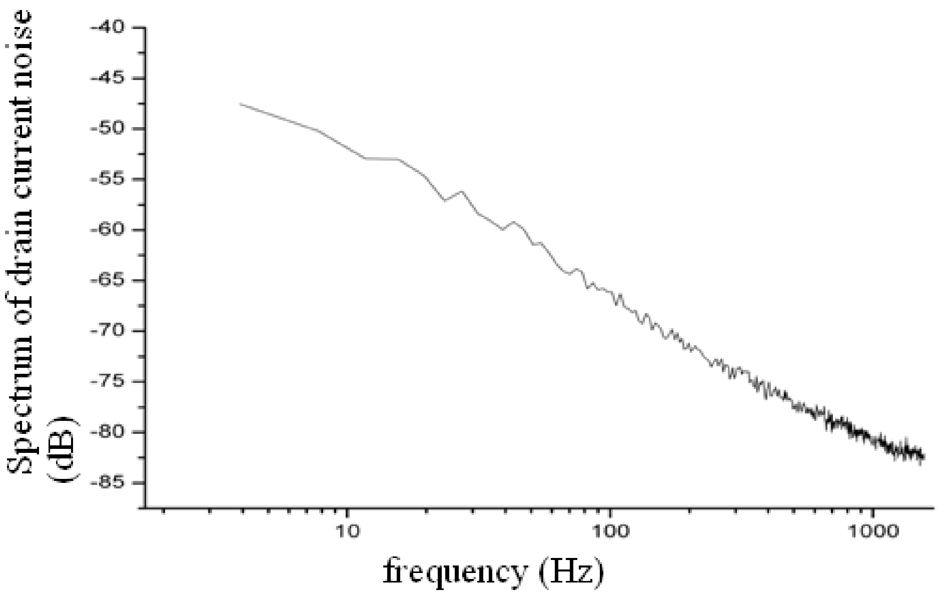

Fig. 4.5 Drain current spectrum at higher gate bias(-1.0V)

4.4.2 Flicker noise comparison between capped and non-capped devices

Flicker noise measurements were done at room temperature and at low drain bias of -0.1v. Comparison of flicker noise between the two devices showed that capping lead to higher flicker noise strength (Fig 4.6, Fig 4.7). This might be expected as the introduction of a different material on top of hi-k dielectric can lead to additional defects being generated in the hi-k layer, which means higher trap density and hence higher flicker noise content.

It was also seen that the capped devices were showing Lorentzian spectrum whereas non-capped devices didn't show. This could be because the introduction of capping layer introduced a single dominant active trap.

To understand the noise generation mechanism, S_{vg} was plotted with respect to the gate overdrive (Fig 4.8, Fig 4.9). For both the wafers, increasing S_{vg} with respect to the gate overdrive points towards mobility fluctuation as the dominant mechanism.

4.5 Conclusion

RTN and flicker noise measurements were done for Renesas pMOSFETs. RTN measurements had some inconsistencies and further detailed study couldn't be done as the results couldn't be replicated (most of the pMOSFETs had failed to work). Gate current RTN measurements were tried, but the system noise floor is above the gate current noise level and hence couldn't be taken. Conclusive remarks cannot be made based on flicker noise comparisons (possibly because of moisture seeping in as the wafer shipment came during monsoon). NBTI measurements to correlate with flicker noise couldn't be done as the devices were breaking down at higher temperatures even with zero gate bias. Detailed study of RTN and its correlation with flicker can be done if working devices are available.

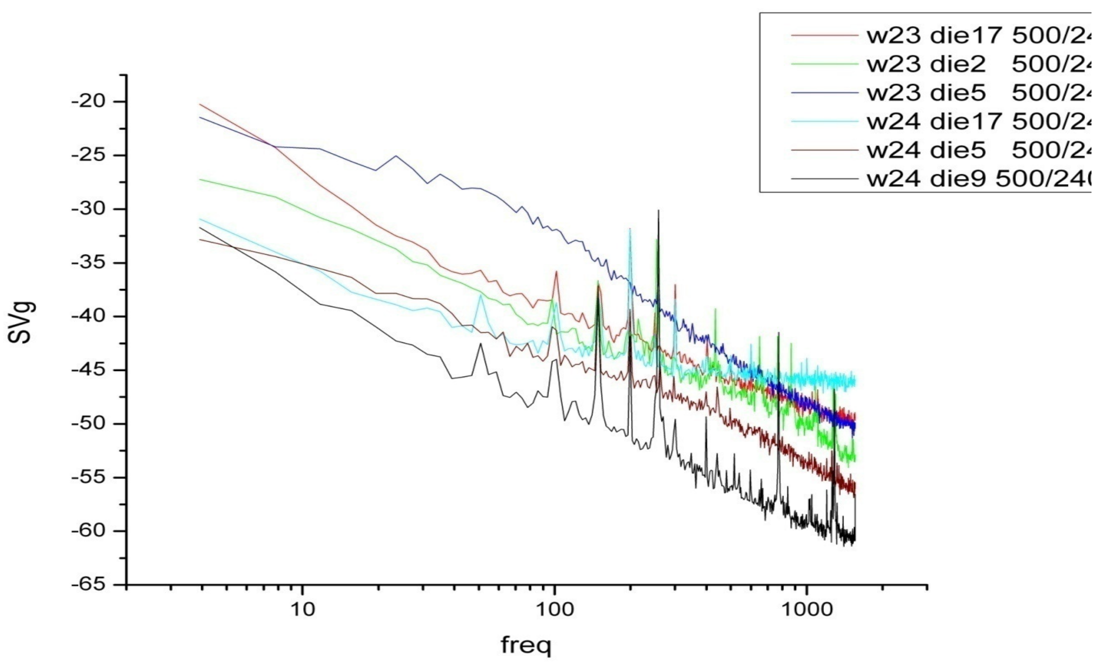

Fig. 4.6 Drain current spectrum comparison of capped and non-capped wafers at low gate bias (100mv above threshold)

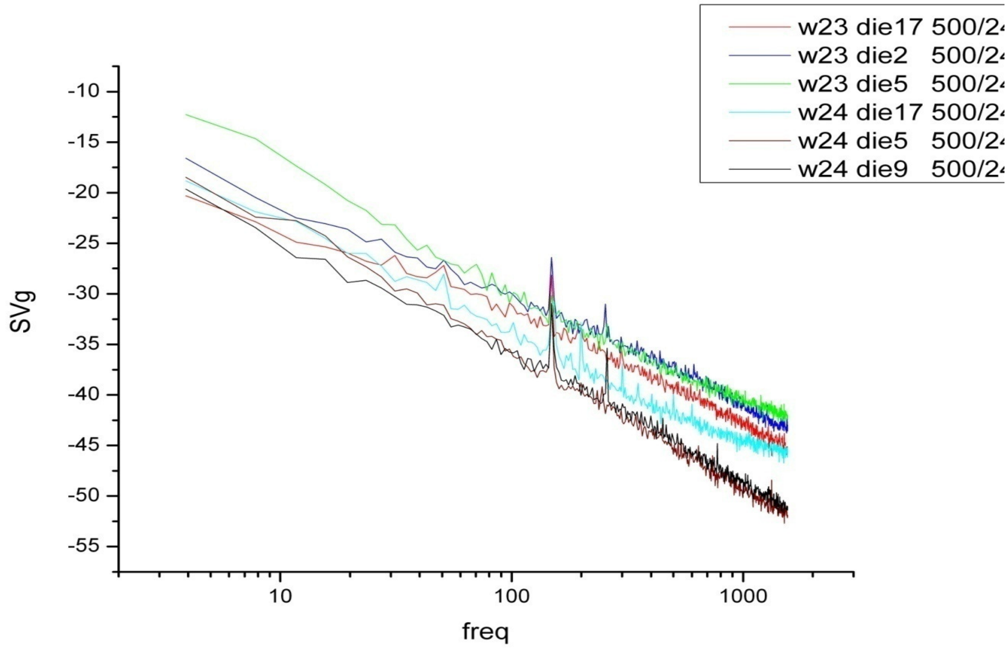

Fig. 4.7 Gate referred noise spectrum comparison of capped and non-capped wafers at high gate bias (-1.0V)

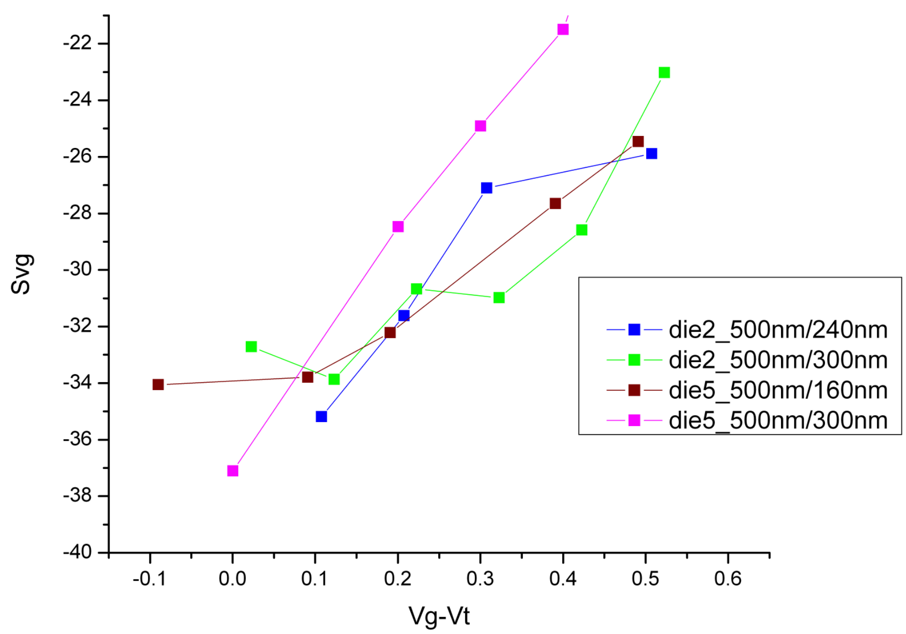

Fig. 4.8 Gate referred noise vs gate overdrive for capped pMOSFETs (Wafer 23)

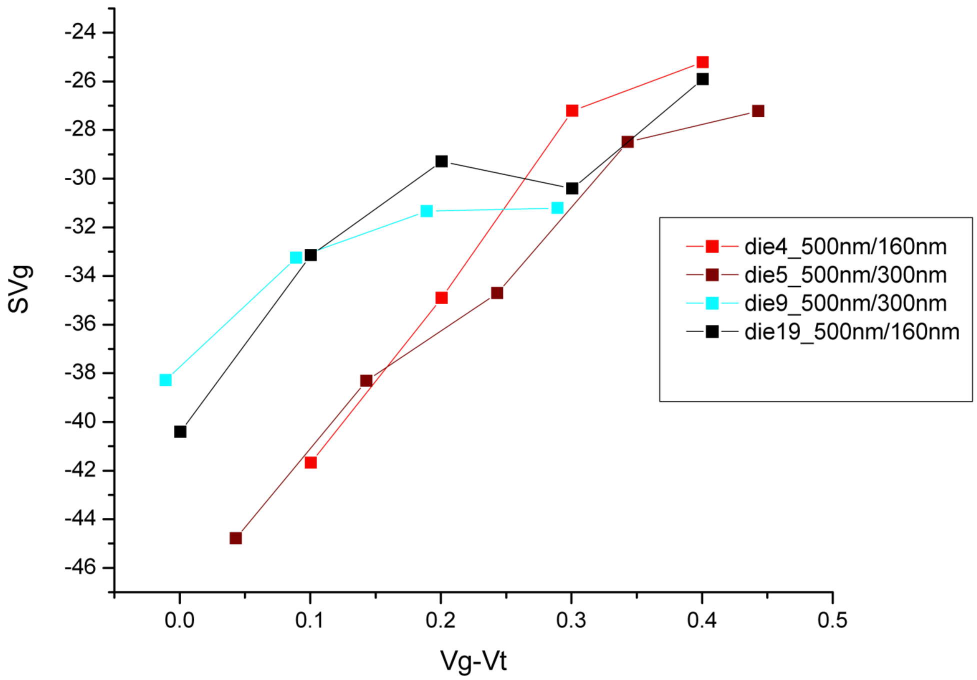

Fig. 4.9 Gate referred noise vs gate overdrive for non-capped pMOSFETs (Wafer 24)

Chapter 5

Study of flicker noise in SiGe pMOSFETs

5.1 Introduction

Incorporation of high-k dielectric to facilitate downscaling of CMOS devices has lead to the problem of mobility degradation and threshold voltage degradation. A promising candidate to address this problem is introduction of compressively strained SiGe into Si-based MOSFETs. Buried channel SiGe pMOSFETs have higher current drive capability, transconductance and mobility because of two reasons [14] : 1) Effective mass of holes is reduced to strain induced band bending 2) The confinement of carriers in buried SiGe quantum wells reduced carrier scattering at the Si/SiO2 interface. In this chapter, details of flicker noise studied in Si pMOSFETs, SiGe pMOSFETs and Si/SiGe pMOSFETs are given. Also correlation of flicker noise degradation and threshold voltage degradation following NBT stress is explained.

5.2 Experimental

Two kinds of SiGe devices were subjected to study: a) with Si capping layer (3nm/30nm, 20% Ge) b) without Si capping layer(30nm, 20% Ge). For Si-cap/SiGe devices flicker noise measurements were done on virgin devices and compared with the control wafer. For non-capped devices, impact of nbti stress on flicker noise was also studied.

The devices were biased with a drain voltage of -1.0v during flicker noise measurements. High drain bias was chosen because the devices didn’t have dedicated substrate pads (the chuck had hence to be grounded to make the circuit complete) and hence interference noise levels were high. In all the cases the device dimensions were chosen to be 3um(W)/2um(L)

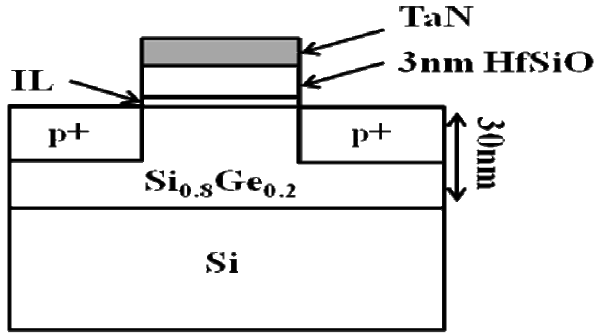

Fig. 5.1 Schematic of the strained SiGe channel p-MOSFET

5.3 Results

5.3.1 Flicker study in virgin SiGe pMOSFETs

To understand which model need to be adopted to study the 1/f characteristics, the gate referred flicker noise S_{VG} is plotted against the gate overdrive V_G-V_T. Since S_{VG} is increasing with V_G-V_T, the model to be used is the unified model has to be used for analysis purpose.

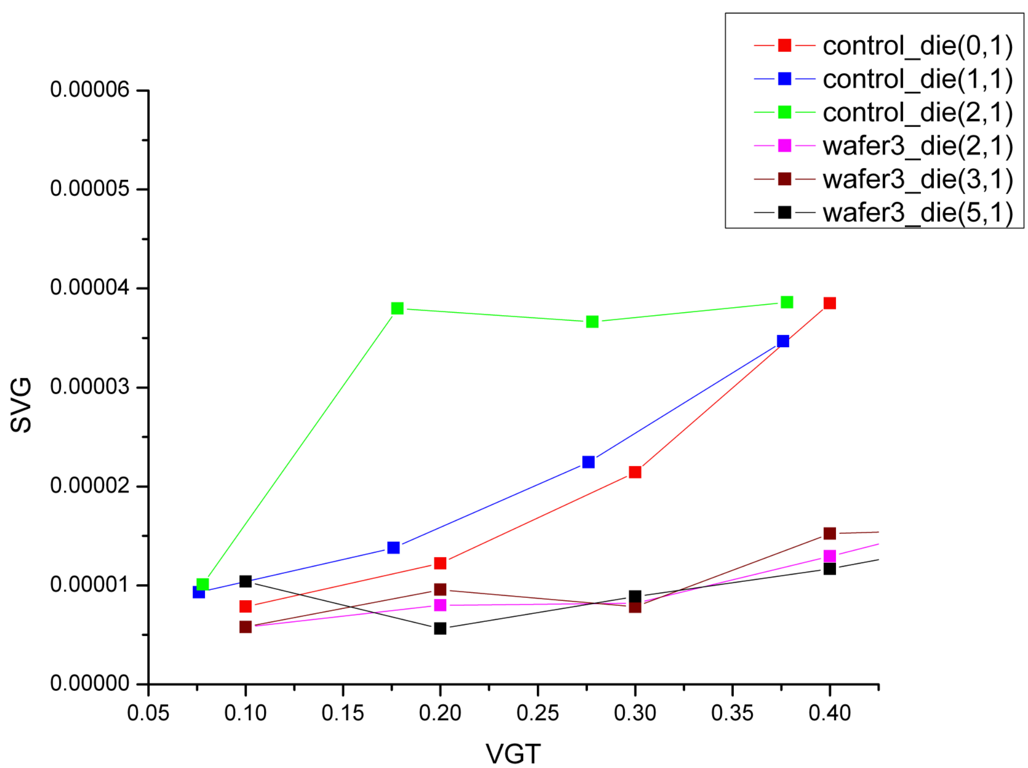

Fig. 5.2 Gate referred noise vs gate overdrive voltage for non-capped devices

From the unified model [12], the drain current noise power spectral density $S_{Id}(f)$ is given as

$$S_{Id}(f) = \frac{kTqI_d\mu_{eff}}{\gamma f L^2}\int_0^{V_d} N_t^*(E_{fn})\frac{1}{N}dV \tag{5.1}$$

where k is the Boltzmann constant, T is the temperature in Kelvin, I_d is the drain current, μ_{eff} is the effective mobility (not including the horizontal field), γ is the attenuation constant of the wave function of carrier in the oxide, L is the length of the channel, N is the inversion carrier density, f is the frequency, V_d is the drain voltage, $N_t^*(E_{fn})$ is the apparent oxide trap density that produces the same noise power if there were no contribution from the mobility fluctuation and is given by,

$$N_t^*(E_{fn}) = Nt(E_{fn})(1+\alpha\mu_{eff}N)^2 \tag{5.2}$$

In equation 5.2, the integration term appears because under saturation the inversion carrier density varies with position in the channel. The gate referred noise S_{vg} *(f)* is given by $S_{Id}(f)/gm^2$

From equation 5.1, hence it can be seen that S_{vg} *(f)* depends upon the term $\frac{1}{\gamma}\int_0^{V_d} N_t^*(E_{fn})\frac{1}{N}dV$, as μ_{eff} gets cancelled out, and if we make sure other terms remain the same when we are comparing control and SiGe devices. γ is given by,

$$\gamma = \frac{4\pi}{h}\sqrt{2m^*\phi_B}$$

where m^* is the effective mass of the carrier in the oxide, h is the Planck's constant and ϕ_B is the tunnelling barrier height seen by the carriers at the interface. For SiGe devices, ϕ_B is about 0.35ev higher than for control wafer. The ratio of γ for the SiGe device and control is around 1.03 which can be approximated to 1. Hence it can be said that the difference seen in Svg is due to the term inside the integral which is the contribution of traps which are located at same energy level as the quasi- Fermi level. Hence higher trap density will have to be assumed in the control wafer compared to the SiGe pMOSFETs .

5.3.2 Flicker study in virgin Si-cap/SiGe pMOSFETs

The capped devices have a 3nm Si cap between the dielectric and SiGe. This kind of structure makes sure the carriers are confined in the buried SiGe channel and hence will have higher mobility compared to the non-capped devices because of reduced surface roughness scattering. This is clearly seen in fig. 5.4 where even though the threshold voltage is nearly same, the current levels are different because of the difference in the mobility values.

As shown in fig. 5.5, the gate referred noise Svg has been found to be lower than that of the non-capped devices. This is expected as the carriers are away from the dielectric interface.

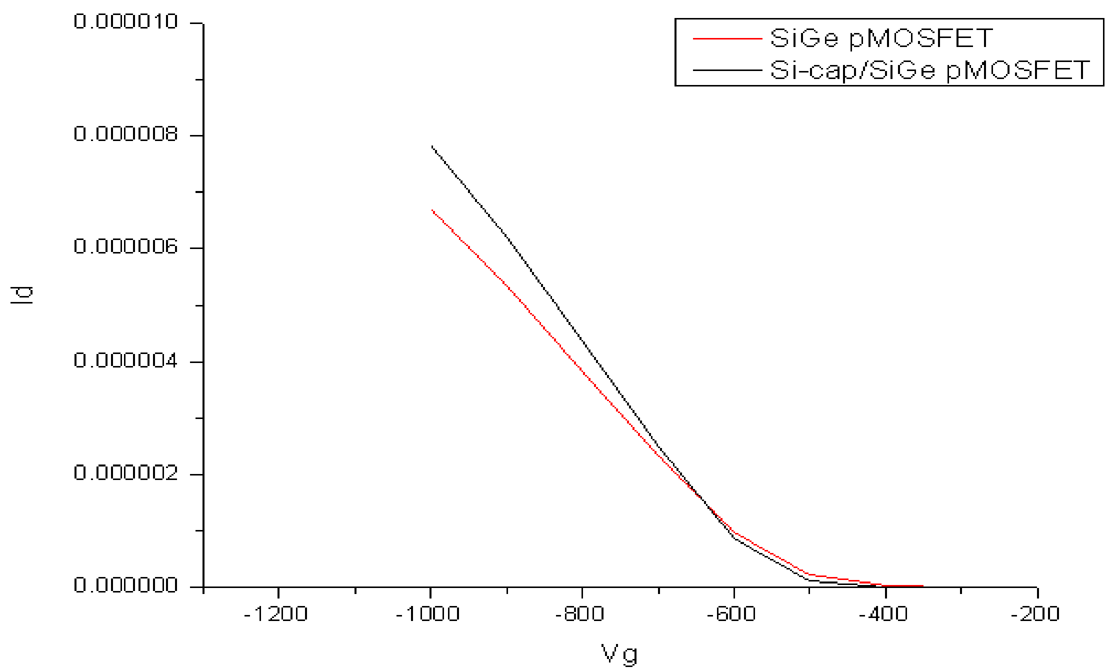

Fig. 5.3 Id-Vg plots for capped and non-capped SiGe devices

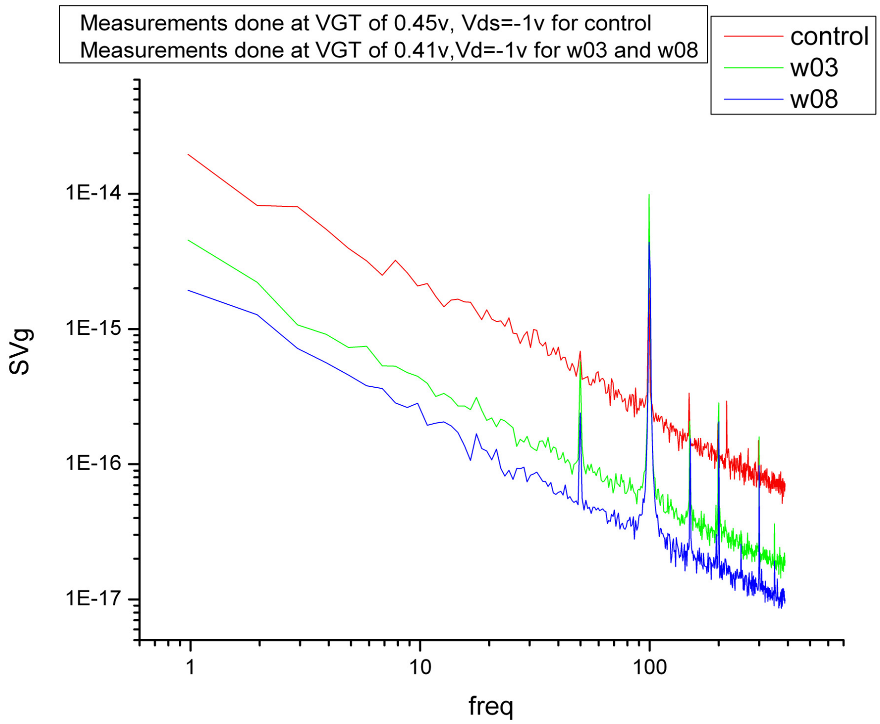

Fig. 5.4 Gate referred noise comparison between the control device, non-capped (w03) and capped device (w08)

5.3.3 Study of flicker noise degradation with NBTI stress in SiGe pMOSFETs

NBTI stress experiments were performed on devices from wafers 1,2 and 3 (details are given in table 5.1). The idea was to try to correlate the observed NBTI degradation with the degradation observed in flicker noise characteristics. The devices were subjected to NBTI stress at various gate bias voltages (drain bias was set to zero during stress measurements). The stress temperature was 125c and was done for 1000s followed by 500s relax period in which the gate bias was set to zero.

Flicker noise measurements were done before and after NBTI stress and the increment in the gate referred noise was measured with respect to the stress voltage. The results are plotted in fig. 5.6.

It is seen that the control wafer is showing higher degradation both in terms of threshold voltage degradation as well as flicker noise degradation. As discussed in section 5.3.1, $S_{vg}(f)$

depends on the term $\frac{1}{\gamma}\int_0^{V_d} N_t^*(E_{fn})\frac{1}{N}dV$. The increment in S_{vg} *(f)* however doesn't depend on γ which doesn't change after stress. Hence the factor $\int_0^{V_d} N_t^*(E_{fn})\frac{1}{N}dV$ changes due to stress and is reflected in the increment in S_{vg} *(f)*.

Hence Δ S_{vg} *(f)* = $\int_0^{V_d} \Delta N_t^*(E_{fn})\frac{1}{N}dV$, where $\Delta N_t^*(E_{fn})$ is the increment in the trap density. This is analogous to the ΔV_T expression of NBTI measurements which is proportional to ΔN_{it} which has exponential dependence on the electric field. Hence it can be said that $\Delta N_t^*(E_{fn})$ could also have exponential dependence on the stress field which gave rise to the plot shown in fig. 5.6

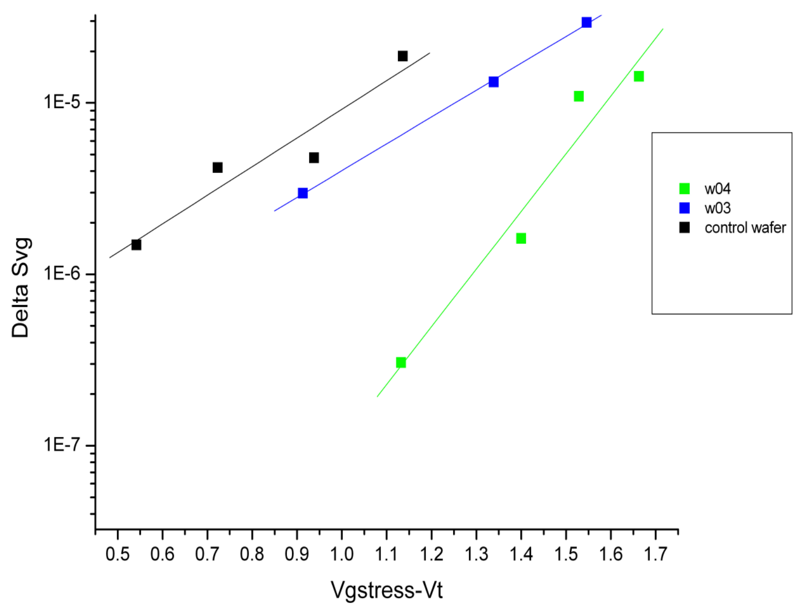

Fig. 5.5 Increment in gate referred noise after stress plotted against the stress bias

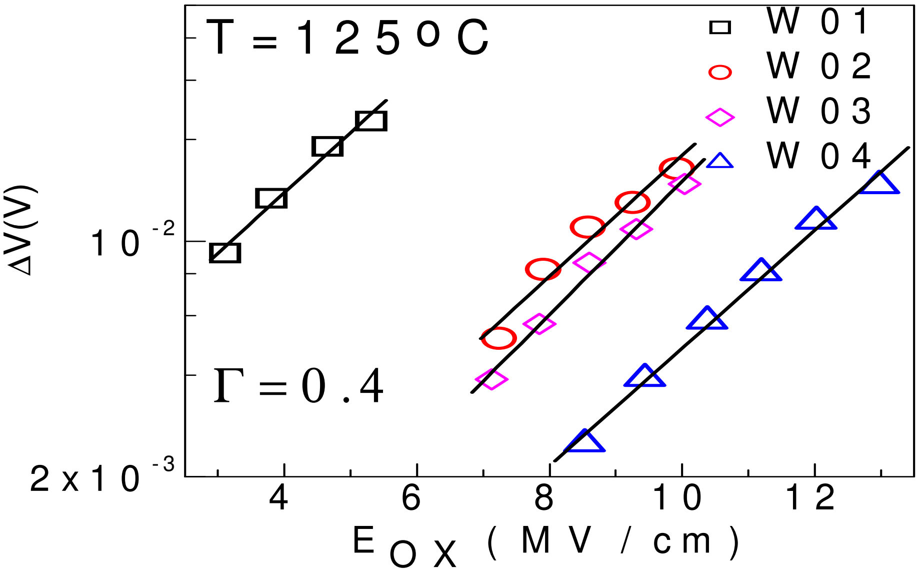

Fig. 5.6 Threshold voltage degradation vs the stress electric field taken using on the fly (OTF) technique

Chapter 6
Conclusions and Future Work

The main aim of this work was to solve the problems that existed in the current setup to measure flicker noise due to which RTS couldn't be measured. Through lots of troubleshooting the problems with the setup were identified and solved, thus making the system capable of RTS measurements.

RTS measurements were done on RENESAS wafers in which low dimension MOSFETs where available (the lowest dimension being W/L of 0.5um/0.4um). Two types of wafers were available-one with AlO capping and the other without AlO capping. RTS could be observed in pMOSFET with AlO capping. Attempt was made to correlate the RTS in time domain and its frequency spectrum. The corner frequency seen in the spectrum didn't match with the calculated frequency from RTS in time domain. Further measurements couldn't be done either because they didn't give reproducible results or they didn't work at all. Flicker noise measurements were also done on larger area MOSFETs and comparison was done between the two wafers. Capped devices showed higher flicker noise content, but this can't be concluded with full confidence owing to reasons described before. NBTI measurements couldn't also be done because the devices were breaking down at high temperature even with zero gate bias.

Study of flicker noise in SiGe pMOSFETs was also done and the results were correlated with NBTI results. Flicker comparison of SiGe devices with and without Si cap layer was done with reference to control wafer.

The setup has the capability to measure RTN in time domain as well as frequency domain provided the devices have dedicated substrate pad. Measuring gate current RTN is still a challenge due to high noise floor in the lab. RTN along with flicker is a powerful combination in decoding trap dynamics and estimating device reliability. RTN measurements can also help in developing models that could be used in analog circuit simulations.

Appendix – A
Program Codes

A.1 MATLAB Code for determining threshold level of RTN fluctuation

```
clear;
[index,current] =        textread('dsodata.txt','%f %f','headerlines',1);
threshold=0;

maximum=current(1);
minimum=current(1);


for n = 2:(length(index))

    if (current(n)>maximum)
        maximum=current(n);
    end

    if (current(n)<minimum)
        minimum=current(n);
    end


end

threshold=(minimum+maximum)/2;
```

A.2 MATLAB Code for smoothening RTN

```
[index,current] =        textread('dsodata.txt','%f %f','headerlines',1);
threshold=4.0891;
for n = 1:(length(index))

    if (current(n)>threshold)
```

```
        modified(n)=1;
    else
        modified(n)=0;
    end
end
```

A.3 MATLAB Code for extracting average high time and low time of RTN

```
[index,current] =        textread('Data3.txt','%d %d','headerlines',1);

     x=1;y=1;
     high(1:3)=0;
     low(1:3)=0;
 for n = 1:(length(index))



            if (current(n)==5)
              a=1;


           if n~=(length(index))
             if (current(n+1)==0)


                high(x)=high(x)+1;

                x=1;
             else
                 x=x+1;

             end

           else
               high(x)=high(x)+1;
           end
```

```
   elseif (current(n)==0)

      if n~=(length(index))
       if (current(n+1)==5)


          low(y)=low(y)+1;


          y=1;
       else
           y=y+1;

       end


      else
          low(y)=low(y)+1;
      end
   end
end
```

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