Fabrication and Characterization of Graphene Field Effect Transistors

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by

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June, 2016

To my parent

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I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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Abstract

The aim is to establish an optimized fabrication process flow for graphene field effect transistors. The optimization includes, evaluating compatible resists, resist removers and contact metals by means of electrical and material characterization of graphene FETs. It is found that, ambipolar nature and high mobility of graphene are preserved when devices are processed using AZ5214E resist and AZ 100 remover. In addition to this, graphene transfer using PMMA is observed to show better mobilities compared to EL9 copolymer. Ni/Au contact metal is observed to have low contact resistance to graphene. The performance of graphene FETs is perceived to be influenced by issues like unintentional doping of graphene, hysteresis in transfer characteristics, asymmetry in transfer characteristics and stability of devices during measurement. Forming gas annealing is discovered to show stable electrical characteristics. Established fabrication process flow could be used to explore different applications and devices structure.

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Chapter 1

Introduction

1.1 Motivation

Graphene is a one atom thick two dimensional (2D) allotrope of carbon. Graphene excellent material properties like light and strong, good conductor of heat and electricity and 98% optical transparency. In addition to this, ambipolar field effect has been experimentally observed in graphene [1]. Furthermore, amazing electronic properties like low temperature mobilities upto 2,00,000 [2], saturation velocities upto $4X10^7$ cm/s [3] and high thermal conductivity(upto 4000 W/mK) [4] appeal its use in high speed analog applications [5].

The aim is to use graphene as a channel material in FETs and establish an optimized fabrication process flow using e-beam and optical lithography. Optimization work involves, investigating compatible resists, solvents and contact metals for graphene FET fabrication through electrical and material characterization techniques.

1.2 Thesis Outline

In chapter 2, chemical properties like bonding and electrical properties like crystal structure, energy band structure and mobility are discussed.

Different methods for synthesis of graphene like mechanical exfoliation, Chemical Vapor Deposition (CVD) and epitaxial growth on silicon carbide are discussed. Finally, applications of graphene are listed.

In chapter 3, structure of graphene FET, energy-band diagram and current-voltage characteristics of GFET are discussed.

Chapter 4, mobility is a important performance parameter that is used to assess compatibility of resist and solvents with graphene. Mobility can be extracted using field effect measurements. Comparative and detailed study of mobility extraction methods based on field effect measurement is provided. Methods include Transfer Length Method (TLM), Direct Transconductance Method (DTM) and Fitting Method (FTM).

In chapter 5, fabrication and characterization of exfoliated graphene FET is discussed. Exfoliated graphene FET is fabricated using e-beam lithography. Graphene identification using Optical imaging and Ramam measurement are also discussed. Finally, transfer and resistance vs gate voltage characteristics of exfoliated graphene FET is discussed.

In chapter 6, fabrication and characterization of CVD graphene FET using optical lithography is discussed. Optimization of fabrication process flow involved investigation of suitable resist for graphene transfer and device fabrication. transfer and resistance vs gate voltage characteristics are also discussed. Mobility variation with channel dimensions are analyzed.

In chapter 7, different performance degrading issues like unintentional doping, hysteresis in transfer characteristics, asymmetry in transfer characteristics and stability of devices during measurement.

In chapter 8, different methods to improve performance of graphene FET are discussed.

chapter 9, summaries the thesis with future direction.

Chapter 2

Graphene

2.1 Properties of graphene

Graphene is one atom thick 2D allotrope of carbon. it is a basic building block for many graphitic allotropes (e.g., Carbon nanotube, Fullerenes, Bucky balls etc.) of a carbon. It was believed that 2D, materials do not exist because of their thermal instability. This was disproved, and it is demonstrated that not only 2D materials exist but also they are thermally stable under ambient conditions [6]. In 2004 A.K. Geim and K.S. Novoselov isolated single layer of graphene from graphite using mechanical exfoliation method [6]. Different chemical and electrical properties of graphene are discussed in this chapter. Finally, different applications of graphene are listed.

2.1.1 Chemical properties

(a) σ bonding (b) π bonding

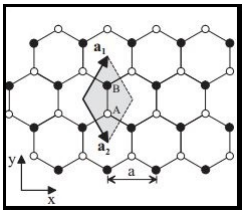
Figure 2.1.1: Chemical bonding in graphene.

Unit cell graphene consist of carbon atoms arranged in hexagonal

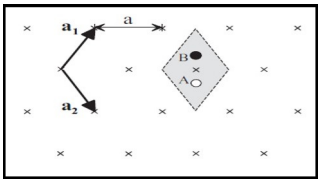
structure. Each carbon atoms has three sp^2 hybridized orbitals and a left over P_z orbital. The sp^2 hybridized carbon atoms get bonded with neighboring carbon atoms by sigma (σ) bond (fig. 2.1.1a) [7]. σ bonding provides mechanical strength to graphene. This type of bonding between carbon atoms form a σ bands in graphene. The electrons in the σ bands are tightly bound to nuclei, hence they do not participate in conduction process. The P_z orbitals of carbon atom which are perpendicular to plane, get bonded with each other by π bond (fig. 2.1.1b). Due to of weak nature of this bond, electrons in these orbitals are not localized to any particular atom but they are free to move. These P_z electrons form π bands, which are responsible for conduction in graphene.

2.1.2 Electronic properties

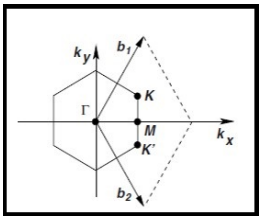
Crystal structure



(a) Honeycomb lattice structure



(b) Premitive unit cell



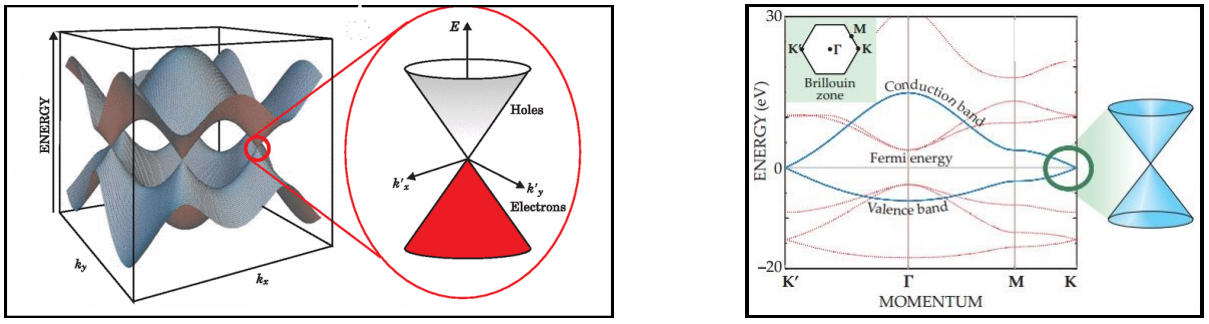
(c) Brillouine zone

Figure 2.1.2: Crystal structure of graphene.

Crystal structure of graphene in real space is shown in fig. 2.1.2a [8]. Hexagonal arrangement of carbon atoms forms an honeycomb like crystal structure. There are two types of atoms in an unit cell i.e., A and B. If we carefully observe fig. 2.1.2a, we find that with basis of one atom, the crystal structure is not a one of the $2D$ bravais lattices. Because of this reason,

we can not convert this honeycomb real space crystal structure directly into reciprocal space. Instead of taking basis of one atom, take basis of two atoms per unit cell (fig. 2.1.2b). The primitive vectors a1 and a2 represent crystal in real space. Crystal structure of graphene in reciprocal space has brillouin zone which is hexagonal in shape. The primitive vectors b1 and b2 represent honeycomb structure in reciprocal space. There are six wavevector (k) points at which E−K diagram touches first brillouin zone boundary, out of which only three are inequivalent. This is because of symmetry. Gamma (Γ) point represents the centre of brillouin zone.

Electronic band structure



(a) Dispersion relation (b) Energy band diagram

Figure 2.1.3: Electronic band structure of single layer graphene.

Dispersion relation of graphene is as shown in fig. 2.1.3a [9]. There are six k points where energy-momentum (E−K) diagram touches brillouin zone boundary. The point at which two inverted cones touch each other is called Dirac point. dispersion relation is linear at low energies near Dirac point. Dirac fermions (electrons and holes) in graphene act as relativistic particles (e.g., neutrino, photons etc.) with zero mass. For relativistic particles, energy dispersion relation is given by,

$$E = \sqrt{m^2c^4 + p^2c^2} \tag{2.1}$$

E is energy of a particle, m is mass of a particle, c is velocity of light,

and p is momentum of a particle. Near Dirac point, dispersion relation for graphene can be written as,

$$E = \hbar v_f |k| \tag{2.2}$$

Where, vf is fermi velocity $\simeq c/300$, $\hbar$ is modified planks constant, $|k|$ is magnitude of wave vector. If m is set to zero in Eq. 2.1 then,

$$E = pc \tag{2.3}$$

Now, if we compare Eq. 2.2 and Eq. 2.3, we find that dispersion relation of Dirac fermions in graphene has same form except the difference in velocity (which is $\sim 10^6$ m/s). Hence, Dirac fermions act like mass-less relativistic particle.

Figure 2.1.3b shows the conduction band, valence band, and fermi energy in band structure of graphene [6]. There here are deep valence and conduction bands (Red colored lines). These bands are formed due to interaction of tightly bound σ electrons, so they do not take part in conduction process. The blue color bands shows the conduction and valence bands formed due to interaction of P_z electrons. These electrons participate in conduction process. Energy bands are touching each other at Dirac points, showing zero energy band gap of graphene.

Mobility

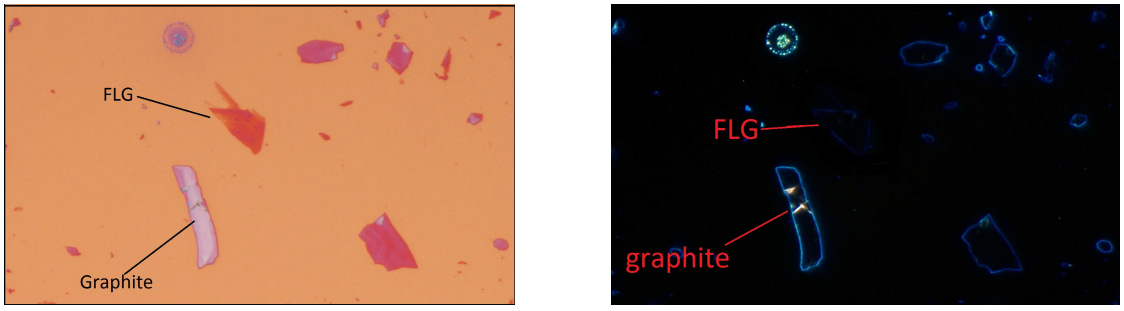
Linear and symmetric dispersion relation of graphene near Dirac point results in very high and equal mobilities for electrons and holes. Mobilities upto 15,000 cm^2/V-s on SiO_2 [10], upto 27000 for epitaxial graphene [11], and upto 2,00,000 for suspended graphene [12] have been reported. However, different processes like charged impurity scattering, defects and ripples limit the excellent charge carrier mobility of graphene. Mobility

degradation because of charged impurity scattering will be discussed in chapter chapter 7.

2.2 Graphene synthesis methods

In 2004 Novoselov et al. [1], produced graphene from mechanical exfoliation of graphite using scotch tape. Mechanical exfoliation is simple method but it's not suitable for preparation of large area graphene. There are other methods developed for preparing large scale graphene like, epitaxial growth from silicon carbide, Chemical Vapor Deposition and self-assembly of soluble graphene.

2.2.1 Mechanical exfoliation



(a) Bright field image (b) Dark field image

Figure 2.2.1: Optical images of mechanically exfoliated graphene.

In this method, naturally available graphite is used for preparing micron sized graphene flakes. Graphite consist of different graphene layers stacked and held together by van der Waals force. Peeling off these layers from graphite using scotch tape and repeated peeling on fresh part of tape can give us multilayer, few layer and single layer graphene. These flakes are then transferred onto suitable substrate like 300 nm SiO_2. Optical microscope is used to identify graphene flakes. Graphitic flakes appear bluish in color while graphene flakes appear purple in color. Dark field mode in optical microscope can also be used to identify graphene flakes.

Graphite flakes glow more as compared to few layer graphene flakes. Figure 2.2.1 show bright field(fig. 2.2.1a) and dark field (fig. 2.2.1b) optical images of mechanically exfoliated graphene. Raman measurement is also used to characterize graphene, which will be discussed in chapterchapter 5.

2.2.2 Chemical Vapor Depostion

This method is used to prepare large area graphene. Metals like Ni, Cu, Pt, Ir are used as substrate for growing graphene. In chemical vapor deposition (CVD) process, precursors react at high temperature in presence of metal substrate catalyst. Metal substrates also act as nucleation site in formation of graphene lattice [13]. Metal acts as catalyst to lower reaction temperature, which eventually affects quality of graphene. Growth of graphene on metal substrate is advantageous from transfer process point of view, since some metals can be etched using acids [14]. Produced graphene can be transferred onto suitable substrate using PMMA or PDMS films [15].

2.2.3 Epitaxial graphene from Silicon Carbide (SiC)

Thermal desorption of silicon at temperatures between 1250^o C to 1450^o C from silicon carbide (0001) substrate in vaccum forms graphene [15]. Using Raman characterization, it is found that the epitaxial graphene layers are compressively strained [16, 17]. This method produces graphene flakes larger than mechanical exfoliation method but high thermal budget limits its electronic application.

2.3 Applications

Graphene is thinnest, strongest and transparent material ever found. excellent electronic properties of graphene make it potential candidate for high speed analog application. Graphene nanoribbons have bandgap so

they can be used for switching applications. Graphene is transparent material, it absorbs only 2.3% of the light [1]. Because of very high electrical conductivity it can be used as electrode. Few applications [18] of graphene are listed below,

- Electronic devices
  - Field-effect transistors
  - Memory devices
  - Molecular electronic devices
- Optical devices
  - Touch screens
  - Liquid crystal displays
  - Light emitting diodes
  - Solar cells
- Transparent and flexible electronics
  - Transparent displays
  - Transparent smart cards
  - Invisible security circuits

Chapter 3

Graphene Field Effect Transistors

3.1 Structure of GFETs

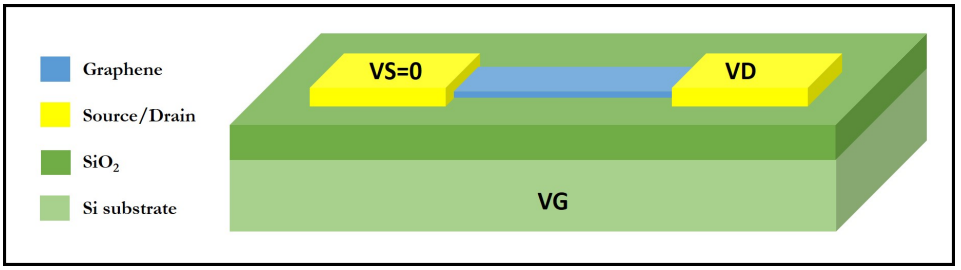


Figure 3.1.1: Structure of back-gated GFET.

Figure 3.1.1 shows structure of back-gated graphene FET(GFET). Heavily doped p-type silicon acts as back-gate contact. Thermally grown 300nm SiO_2 acts as back-gate dielectric and graphene lying on SiO_2 acts as channel material. Graphene is contacted using metals which act as source and drain regions.

3.2 Energy band diagram

Figure 3.2.1 [19] shows energy band diagram of GFETs when constant V_{DS} is applied and V_{GS} is varied. When no gate voltage is applied, Fermi energy will be at zero potential and no current will flow (ideally). When gate voltage greater than Dirac point voltage is applied, fermi level moves in conduction band and electrons carry current. When gate voltage less

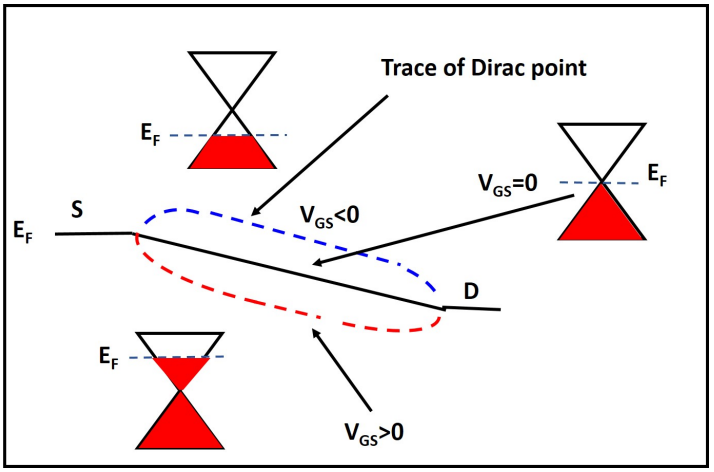


Figure 3.2.1: Energy band diagram of GFET.

than Dirac point voltage is applied, fermi level moves in in valence band and hole current flows.

3.3 Current-Voltage characteristics of GFETs

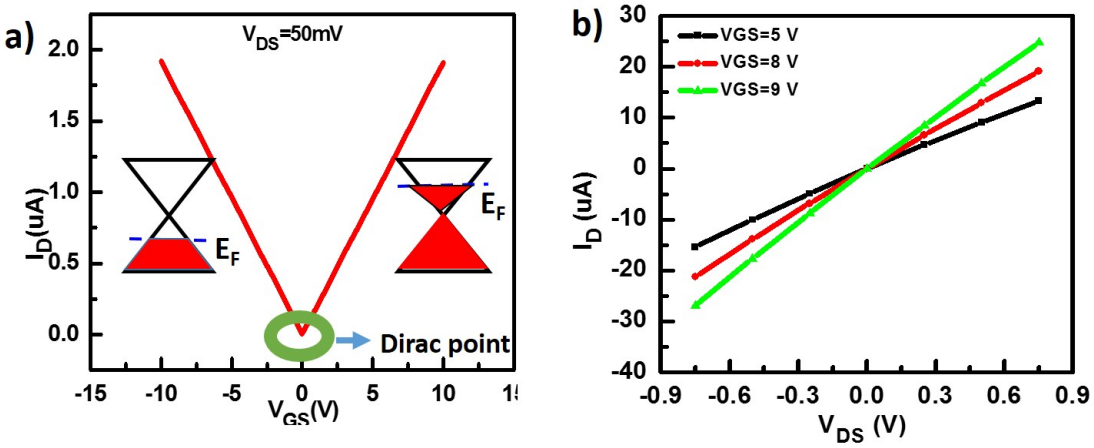


Figure 3.3.1: Simulated current-voltage char. of GFETs; a) Transfer, b) Output.

Graphene exhibits ambipolar behavior. Ambipolar nature of graphene can be understood with a model of 2D metal with small overlap between conduction band and valence band [1]. Gate voltage induces charge density $n_s = C_{OX}/e * (V_{GS} - V_0)$ in the channel and accordingly shifts fermi level away from Dirac point. The electric field doping in graphene con-

verts shallow overlap semi-metal into completely either hole or electron conductor.

Theoretically, transport in graphene is ballistic or quasi-ballistic. Different factors like substrate interaction, fabrication processes and structure of device force us to use well developed conventional drift-diffusion model to describe transport in GFETs [20]. Drift-diffusion current equation developed for MOSFETs operating in linear region can be used for GFETs. Threshold voltage (V_T) term in drain current equation of MOSFETs is replaced by Dirac point voltage. Drift-diffusion drain current for GFETs is given by,

$$I_d = \mu C_{OX} \frac{W}{L}[(V_{GS} - V_0)V_{DS} - \frac{V_{DS}^2}{2}] \tag{3.1}$$

where I_D is drain current, μ is charge carrier mobility, W is width of channel, L is length of channel, V_{GS} is gate−source voltage, V_{DS} is drain-source voltage and V_0 is Dirac point voltage. Equation 4.8 is applicable for $V_{DS} < V_{GS}$-V_0. Minimum conductivity point is always larger than universal minimum conductivity($4e^2/h$) due to thermal excitation and inhomogeneity [10].

Figure 3.3.1 shows simulated transfer characteristics of of model described by eq. 4.8. "V" shaped transfer characteristics of fig. 3.3.1a clearly shows ambipolar behavior GFETs. Figure 3.3.1b shows simulated output characteristics for GFETs. Output characteristics show linear behavior For $V_{DS} << V_{GS} - V_0$.

Chapter 4

Mobility Extraction Methods for GFETs

Mobility is important figure of merit that can be used to assess quality of graphene. Carrier mobilities can be extracted from two kinds of measurements, i.e., Hall measurement [21] and field effect measurement. Accurate measurement of mobility can be done using hall measurement, however it requires complex device fabrication and measurement setup. Field effect method involves fabrication of two terminal devices. Simplicity of fabrication process makes field effect based method more popular. In this chapter field effect measurement methods like transfer length, direct transconductance and fitting method are discussed.

4.1 Transfer Length Method (TLM)

Two probe total resistance (R_T) of a semiconductor device is given by

$$R_T = 2R_c + R_{semi} \tag{4.1}$$

R_c is contact resistance associated with metal/semiconductor interface, R_{semi} is resistance of semiconductor, which is given by,

$$R_{semi} = R_{sheet}\frac{L}{W} \tag{4.2}$$

R_{sheet} is sheet resistance of semiconductor, L is length of semiconductor and W is width of semiconductor. Total resistance is is then given by,

$$R_T = 2R_c + R_{sheet}\frac{L}{W} \tag{4.3}$$

Total resistance of devices with different lengths and similar widths has to measured and fitted to eq. 4.3. Illustrative example is is shown in fig. 4.1.1.

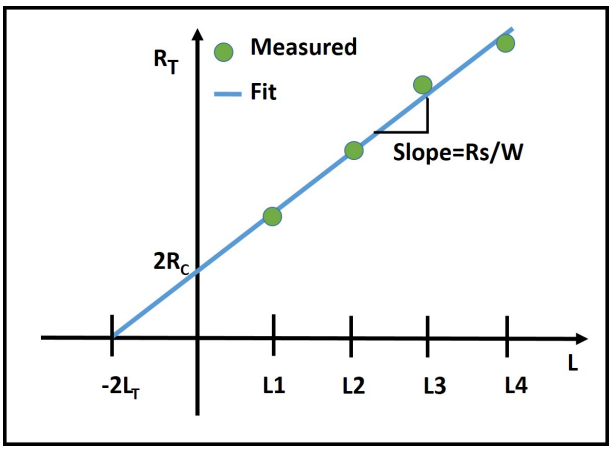


Figure 4.1.1: Fitting of total resistance equation to measured data.

Y-intercept gives contact resistance R_c and slope gives sheet resistance R_{sheet} of semiconductor material. Transfer length (L_T) which is average distance an electron travels before it flows up into contact, can also be found from x-intercept of fitted data.

TLM method requires fabrication of devices with similar width and different lengths. Typical structure is shown in figure 4.1.2.
For graphene, total resistance is given by,

$$R_T = 2R_c/W + R_{sheet} * L/W \tag{4.4}$$

R_c is width (channel width) normalized contact resistance, and R_{sheet} is sheet resistance of graphene.

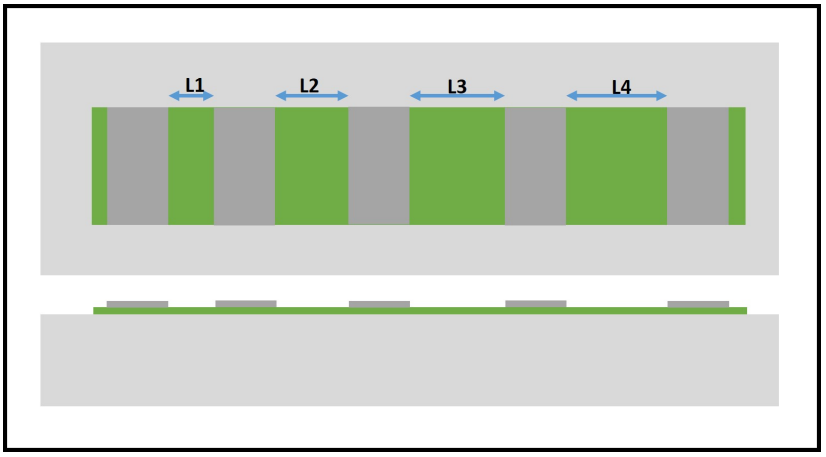


Figure 4.1.2: Typical TLM measurement structure

By linear fitting R_T of GFETs with different lengths under fixed $V_{GS} - V_0$, R_c and R_{sheet} at this gate voltage can be extracted from intercept and slope [22]. Gate voltage dependent R_{sheet} and R_c can be calculated using method described above. Gate voltage dependent mobility extracted with TLM method (μ_{TLM}) using $R_{sheet} - (V_{GS} - V_0)$ relation is given by,

$$\mu_{TLM}(V_{GS} - V_0) = \frac{1}{qn(V_{GS} - V_0)} R_{sheet}(V_{GS} - V_0) \tag{4.5}$$

$n(V_{GS} - V_0)$ is gate voltage dependent carrier concentration in graphene. $n(V_{GS} - V_0)$ includes residual carrier density n_0 (Carrier concentration when no gate voltage is applied). Hence total charge induced by gate voltage is given by,

$$n(V_{GS} - V_0) = \sqrt{n_o^2 + (C_g(V_{GS} - V_0))^2} \tag{4.6}$$

In back-gated GFTEs, graphene lays on dielectric like SiO_2. C_{ox} is dielectric capacitance which is given by,

$$C_{ox} = \epsilon_0 \epsilon_r / t_{ox} \tag{4.7}$$

ϵ_0 is dielectric constant of air, ϵ_r is dielectric constant and t_{ox} is thickness of dielectric used in GFETs. if quantum capacitance is neglected [22] then

C_g will be C_{ox}.

In summary TLM method uses sheet resistance to calculate mobility, hence theoretically eliminates effect of contact resistance and presents accurate gate voltage dependent mobility and contact resistance.

4.2 Direct Transconductance Method (DTM)

This method is also based on two probe measurement similar to TLM method. Drift-diffusion equation described in chapter 3 for GFETs is given by,

$$I_D = \mu C_{ox} \frac{W}{L}[(V_{GS} - V_0)V_{DS} - \frac{V_{DS}^2}{2}] \tag{4.8}$$

if $V_{DS} << V_{DS} - V_0$ then equation 4.8 becomes,

$$I_D = \mu C_{ox} \frac{W}{L}[(V_{GS} - V_0)V_{DS}] \tag{4.9}$$

In equation 4.10 I_D has linear relation with V_{DS} and $V_{GS} - V_0$. DTM involves finding slope of transfer characteristics in linear region which is given by,

$$g_m = \frac{\partial I_d}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} V_{DS} \tag{4.10}$$

$$\mu_{DTM} = \frac{g_m}{C_{ox} V_{DS}} \frac{L}{W} \tag{4.11}$$

Where, g_m is slope of transfer characteristics. Gate voltage dependent g_m can be found from transfer characteristics and hence gate voltage dependent mobility.

Figure 4.2.1 is an illustrative example showing extraction of transconductance from transfer characteristics. Hole mobility μ_h of 93.04 $cm^2/V-s$ and electron mobility μ_e of 86.05 $cm^2/V-s$ is obtained using DTM.

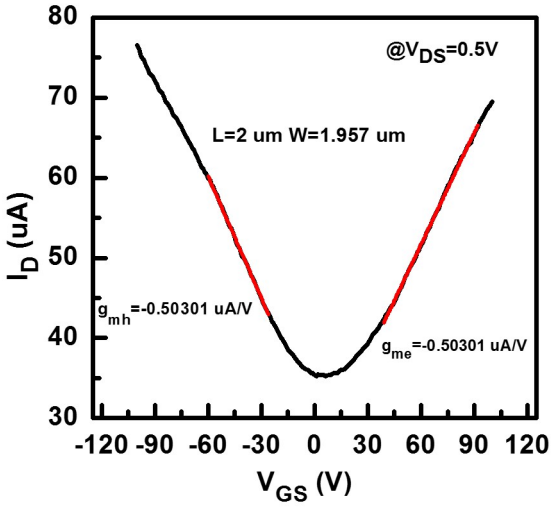


Figure 4.2.1: Illustrative example to find transconductance from transfer characteristics.

DTM neglects effect of contact resistance i.e., it assumes that applied V_{DS} appears across channel. In reality, finite contact resistance causes voltage drop across it, hence effective V_{DS} appearing across channel is V_{DS}-$I_d R_c$, which is less than V_{DS} being used in calculation of mobility. This is why DTM underestimates charge carrier mobilities. Accurate measurement of mobilities using DTM requires low contact resistance and higher channel lengths (i.e., higher channel resistance as compared to contact resistance) [22].

4.3 Fitting Method (FTM)

Fitting method is another popular method for mobility extraction based on transfer characteristics of GFETs. This method is developed by Kim et al. in 2009 [23]. This method extracts carrier mobilities, residual charge carrier density and contact resistance simultaneously by fitting a model to a measured total resistance versus gate voltage characteristics. FTM involves fitting of following model equations,

$$R_T = R_{contact} + R_{channel} \tag{4.12}$$

$$R_T = R_{contact} + \frac{N_{sq}}{n_{tot} e \mu_{FTM}} \tag{4.13}$$

R_T is total contact resistance, $R_{contact}$ is contact resistance of metal/graphene interface, $R_{channel}$ is channel resistance, N_{sq} = L/W is number of squares, n_{tot} is total charge induced by gate voltage, e is electronic charge and μ is gate voltage independent carrier mobility. n_{tot} is given by,

$$n_{tot} = \sqrt{n_0^2 + n(V'_{GS})^2} \tag{4.14}$$

n_o is residual carrier density, which is carrier density when no gate voltage is applied. Residual carrier density is ideally zero for disorder free graphene. However, it is induced by impurities present in dielectric or graphene/dielectric interface [23]. $n(V'_{GS})$ is gate voltage dependent part of n_{tot} and is related to v'_{GS} as,

$$V_{GS} - V_0 = \frac{e}{C_{ox}} n + \frac{\hbar v_f \sqrt{\pi n}}{e} \tag{4.15}$$

$\hbar$ is reduced planks constant, v_f is Fermi velocity of carriers $\sim 10^6$ m/s. Equation 4.15 can be solved to find explicit relation between n and V_{GS} as follows, let a=$\hbar$ v_f $\sqrt{\pi}$/e, b=e/C_{ox} and $V'_{GS} = V_{GS} - V0$, then eq. 4.15 becomes

$$V'_{GS} = bn + a\sqrt{n} \tag{4.16}$$

$$V'_{GS} - bn = a\sqrt{n} \tag{4.17}$$

Squaring both sides of eq. 4.17 and solving quadratic equation for n gives us following relation

$$n = \frac{2bV'_{GS} + a^2 \pm a\sqrt{4V'_{GS} + a^2}}{2b^2} \tag{4.18}$$

Using eq. 4.13, 4.14 and 4.18 model can be fitted to measured data. Separate fitting for $V_{GS} \leq V0$ by taking e=-1.6$X10^{-19}$ C and for $V_{GS} \geq V_0$ with e=1.6$X10^{-19}$ C has to be done to find out parameters for holes and

electrons respectively.

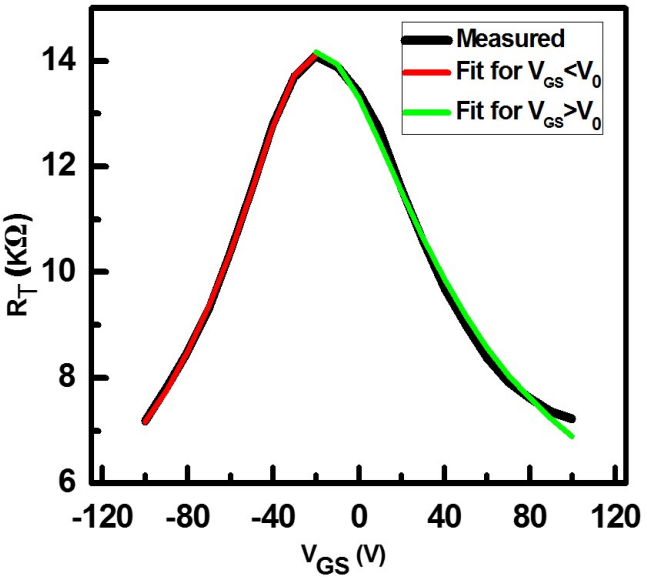


Figure 4.3.1: Illustration of FTM for extraction of different parameters.

Extracted parameters using data of fig. 4.3.1 and FTM are listed in table 4.3.1

Table 4.3.1: Extracted parameter using FTM.

Extracted parameter	μ_h $(cm^2/V-s)$	μ_e $(cm^2/V-s)$	R_{ch} $K\Omega\ \mu m$	R_{ce} $K\Omega\ \mu m$	n_{0h} cm^{-2}	n_{0e} cm^{-2}
Value	180.4	150	3.413	4.749	$2.8*10^{12}$	$3.55*10^{12}$

Fitting method is quite popular because it provides mobility, contact resistance and residual charge density simultaneously. However, FTM treats contact resistance and mobility as constant, although they depend on gate voltage [22]. Mobility of carriers near Dirac point is very high. FTM method focuses on data points near Dirac point, hence always overestimates mobility and contact resistance. Mobility extracted using FTM is independent of channel length where as contact resistance depends on channel length [22]. Contact resistance increases with channel length, hence

for higher lengths error in contact resistance increases. In order to increase accuracy of FTM, devices with short channel length should be fabricated.

4.4 Comparison of mobility extraction methods

TLM gives most accurate measurement of carrier mobility as it eliminates effect of contact resistance. It also provide charge dependent mobility and contact resistance. disadvantage of TLM method is the fabrication of devices with different channel lengths and similar widths [22]. DTM is easiest method and provides carrier density dependent mobility. Disadvantage of DTM is that it doesn't consider effect of contact resistance, hence underestimates mobility. FTM provide more information than that of DTM and TLM. Disadvantage of FTM is that it assumes charge carrier density independent mobility and contact resistance. Comparison of three methods is shown in table 4.4.1.

Table 4.4.1: Comparison of mobility extraction methods.

Method	**TLM**	**DTM**	**FTM**
Device fabrication complexity	High	Low	Low
Mobility Accuracy	High	Underestimates	Overestimates
Contact Resistance Accuracy	High	Unable	Overestimate

Chapter 5

Exfoliated Graphene Field Effect Transistors

In chapter 2, different methods of graphene synthesis were discussed, which included mechanical exfoliation, chemical vapor deposition and epitaxial graphene on SiC. Mechanically exfoliated graphene is fabricated from naturally available graphite crystal and it of highest quality. In this chapter, fabrication and electrical characterization of back-gated exfoliated graphene field effect transistor using e-beam lithography is discussed.

As discussed in chapter 3, GFET consist of heavily doped Si acting as back-gate contact, thermally grown SiO_2 acting as dielectric, graphene laying on SiO_2 acts as channel and metal contacts acting source and drain regions. Optical imaging and Raman measurements are used to identify graphene flakes. Electrical measurements are done to extract different parameters like mobility, residual charge density and contact resistance.

5.1 Fabrication

GFET has heavily p$-$doped Si wafer with resistivity of $<0.005\ \Omega$ cm. First step in fabrication of GFETs is to do RCA cleaning of wafers to remove any organic and ionic contaminant from wafer surface followed by growth

of 300 nm SiO_2 thermal oxide. Fabrication steps are shown in fig. 5.1.1, which are discussed in brief.

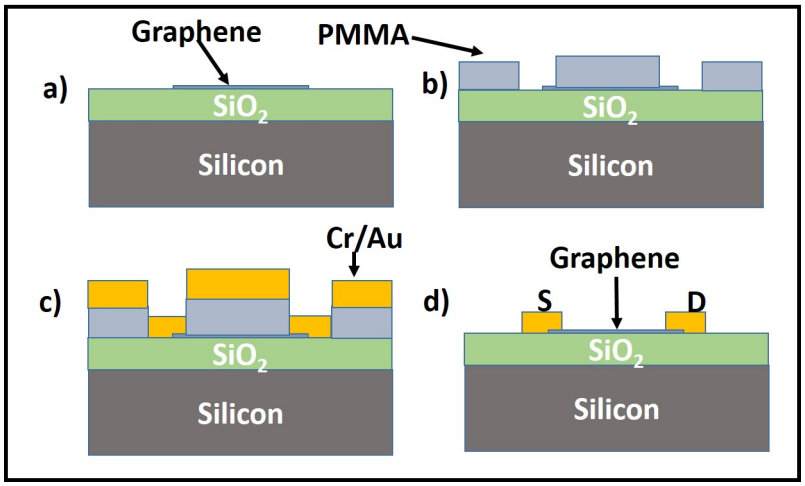


Figure 5.1.1: GFET fabrication steps; a) graphene transfer, b) resist patterning, c) metal deposition, d) Fabricated device after lift-off.

5.1.1 Graphene transfer on Silicon dioxide

following steps are involved in transfer of graphene on SiO_2 substrate:

- Adhesive scotch tape is placed on block of HOPG (Highly oriented pyrolytic graphite) and gently pressure is applied with plastic twiser.
- This process will peel top layers of HOPG crystal on scotch tape. Repeated peeling on fresh part of the tape will create few layer and single layer graphene flakes on tape.
- Immediately tape is pressed on to sample, and pressure is applied gently with plastic twiser.
- After some time, scotch tape is pulled off the sample slowly, this leaves behind multilayer, few layer and single layer graphene flakes on sample.

Next step is identify graphene and few layer graphene flakes.

5.1.2 Marker lithography

Identifying location of graphene flakes is important for further processing. Markers are formed on SiO_2 using e-beam lithography and Cr/Au (10 nm/60 nm) metal depositions. Graphene flakes can be precisely located using these markers. Figure 5.1.2 shows optical image of markers.

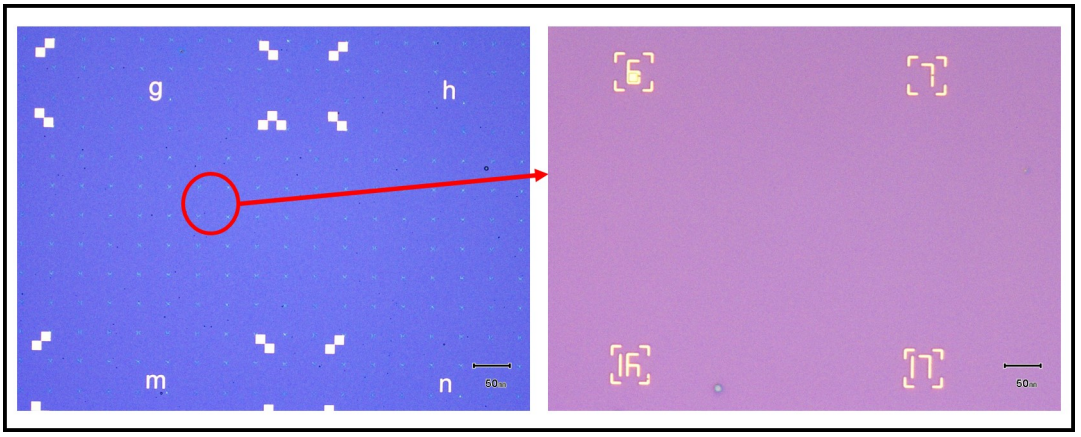


Figure 5.1.2: Optical image of marker used to identify graphene flakes for electrode design.

5.1.3 Identification of graphene flakes using optical microscope

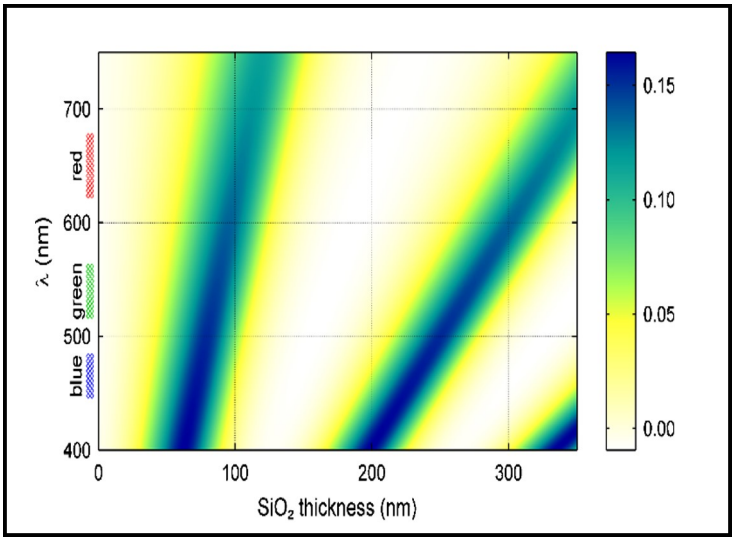


Figure 5.1.3: Contrast of graphene as function of SiO_2 thickness and wavelength of light.

Graphene can be seen on top of proper thickness of SiO_2. Graphene is 97.5% transparent [1], but can add to optical path with proper thickness

of SiO_2 [24]. Figure 5.1.3 shows that the graphene can be viewed on any thickness of SiO_2 using proper light filters, except for $\approx$ 150 nm and below 30 nm oxide thickness. Green light is most comfortable to human eyes, hence oxide thicknesses 90 nm and 280 nm can be used with or without green light filters.

On 300 nm thickness of SiO_2, graphene appears purple while graphite appears bluish in color. As discussed in chapter 2, dark field mode in optical microscope can also be used to distinguish few layer graphene flakes from graphite flakes. Using optical microscope, few layer graphene flakes are identified and can be further verified using Raman measurement.

5.1.4 Source/Drain contact formation

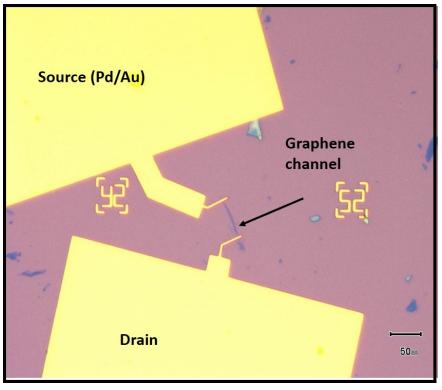


Figure 5.1.4: Optical image of fabricated device showing source, drain and graphene channel.

After identification of graphene flakes next step is to create metal contact to these flakes to enable electrical measurements. Contacts are designed using optical images and Clewin software. E-beam lithography is used to pattern contact areas. Metal deposition is done using Cr/Au (10 nm/70 nm) thermal evaporator and Lift-off is carried out in acetone. Figure 5.1.4 shows optical image of fabricated device.

5.2 Characterization

5.2.1 Raman characterization

Raman measurement is extremely versatile tool for characterization of graphene. Raman measurement is used to identify number of layers, quality and type of edges, strain, perturbation like electric and magnetic field, doping and functional groups [25]. In this section identification of graphene using Raman measurement is discussed. Figure 5.2.1 shows Raman spec-

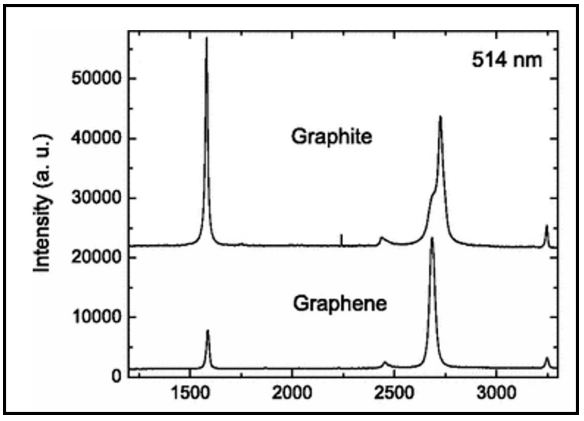


Figure 5.2.1: Raman spectrum of graphite and single layer graphene.

trum of graphite and single layer graphene at 514 nm laser wavelength. It consist of G peak at 1580 cm^{-1}, 2D peak at 2700 cm^{-1}, D (defect) peak at $\sim$ 1350 cm^{-1}. D peak appears when there are defects in graphene i.e., edges. Raman spectrum of graphite has very intense G peak as compared to graphene. 2D peak of graphene can be fit with single Lorentzian peak.

Identification of number of layers can be done by finding FWHM (Full width half maximum) of G and 2D peaks using single Lorentz peak fit. 13.5 cm^{-1} and 18.2 cm^{-1} are FWHM values for G peak of single and bilayer graphene. 26.3 cm^{-1}, 52.1 cm^{-1}, 56.1 cm^{-1} and 62.4 cm^{-1} are FWHM values for 2D peak of single layer, bilayer, trilayer and four layers of graphene. Deconvolution of 2D peak can also be used to identify number of graphene layers [26]. Figure 5.2.2 shows deconvolution of 2D peak to identify number

of layer. Raman spectrum of bilayer graphene and devconvolution of 2D is shown in figure 5.2.3

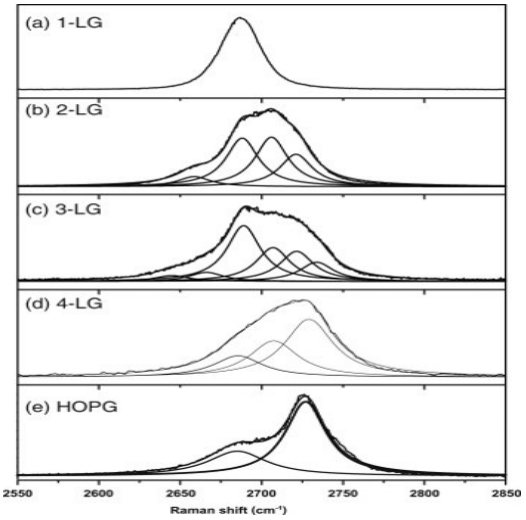
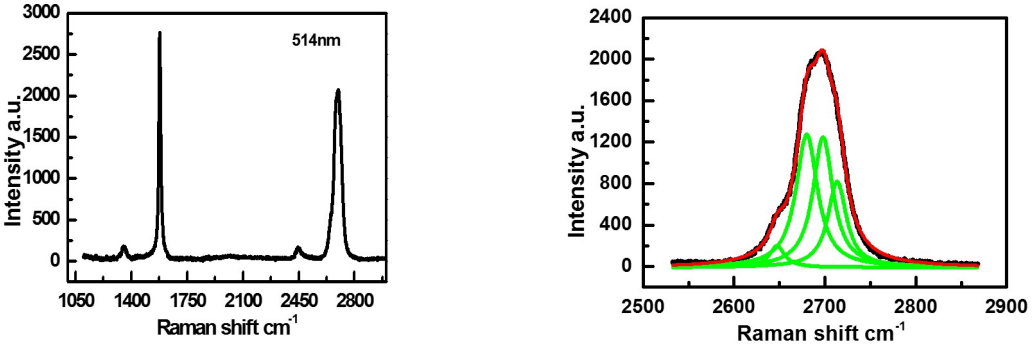


Figure 5.2.2: Number of layer identification using deconvolution of 2D peak



(a) Raman spectrum

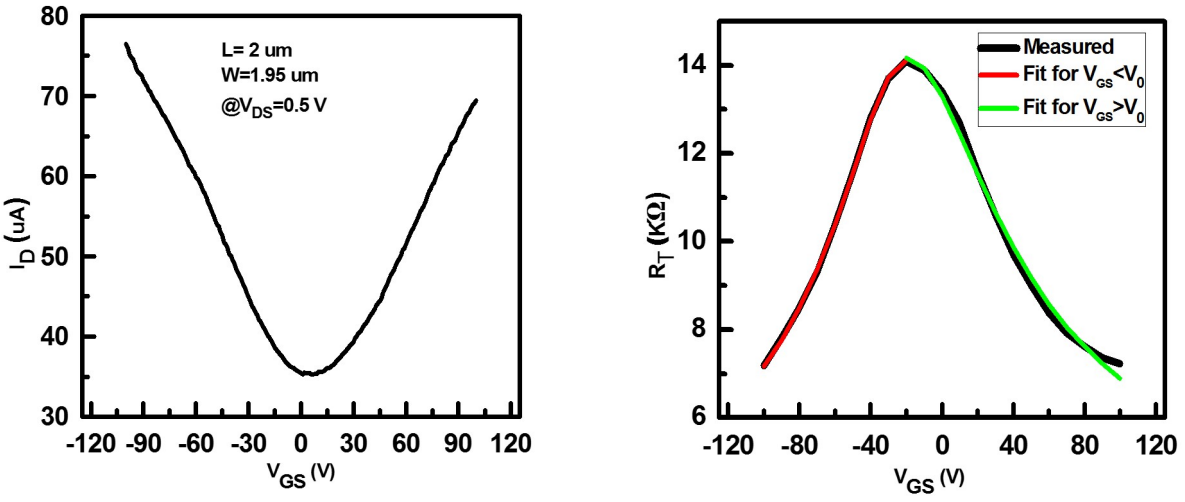
(b) Deconvolution of $2D$ peak

Figure 5.2.3: Raman spectrum of bilayer graphene and deconvolution of 2D peak.

5.2.2 Electrical characterization

After device fabrication, electrical measurement are performed. GFET consist of back-gate Si, SiO_2 dielectric and graphene channel. Si rests on chuck of Proxima B1500 system. Back-gate voltage is swept at fixed V_DS to measure transfer characteristics.

Figure 6.3.4a shows transfer characteristics of GFETs with channel length of 2 um and width of 1.95 um. Back-gate voltage is swept from -100



(a) Transfer characteristics

(b) Resistance vs gate voltage

Figure 5.2.4: Electrical characteristics of GFET.

V to +100 V and drain current is measured. Transfer characteristics show modulation of drain current in response to gate voltage. Minimum conductivity point (Dirac point) is at +7 V. Ideally, Dirac point should be at zero gate voltage, however it shifts because of different parameters like unintentional doping from atmospheric gases, resist residues and organic solvents. Doping mechanisms and sources of unintentional doping will be discussed in chapter 7 and some of the methods to restore Dirac point voltage close to zero volt will be discussed in chapter 8. Peak transconductance for $V_{GS} < V_0$ is found to be -0.50 μS and for $V_{GS} > V_0$ it is 0.47 μS. Mobilities extracted using DTM for holes and electrons are 93.04 $cm^2/V-s$ and 86.05 $cm^2/V-s$ respectively.

Figure 6.3.4b is plot of total resistance vs gate voltage. Total resistance includes contact resistance from graphene/metal interface and resistance of graphene channel. This plot can be generated by sweeping V_{DS} for given value of V_{GS} and extracting slope of $I_D - V_{DS}$ curve. Above procedure is followed for gate voltage from -100 V to +100 V with step of 5 V to get plot of fig. 6.3.4b. $R_T - V_{GS}$ can be used to extract important parameters

like mobility, residual carrier density and contact resistance using FTM. Extracted parameters using FTM are listed in Table 4.3.1.

Chapter 6

CVD Graphene Field Effect Transistors

Although exfoliation method produces high quality graphene and has low production cost, it's crude, produces irregularly shaped graphene flakes and has limited commercial and electronic application [27]. On the other hand, CVD method can grow very thin layers and produce large are high quality graphene. CVD graphene can be patterned into desired shapes and sizes. Large area and continuous sheet of CVD graphene can be used in photovoltaic, transparent conductive coating, Transmission Electron Microscopy and integrated circuits [28].

In this chapter, optimization of fabrication process flow for for CVD GFETs using photolithography is discussed. Mobility is used for assessing compatibility of resists and solvents with graphene. Electrical characterization of CVD GFET is also discussed. Finally, dependence of mobility on length and width of graphene channel is studied.

6.1 Fabrication of back-gated devices

Fabrication process of CVD GFETs using photolithograpy is shown in fig. 6.1.1 and will be discussed in brief in subsequent sections.

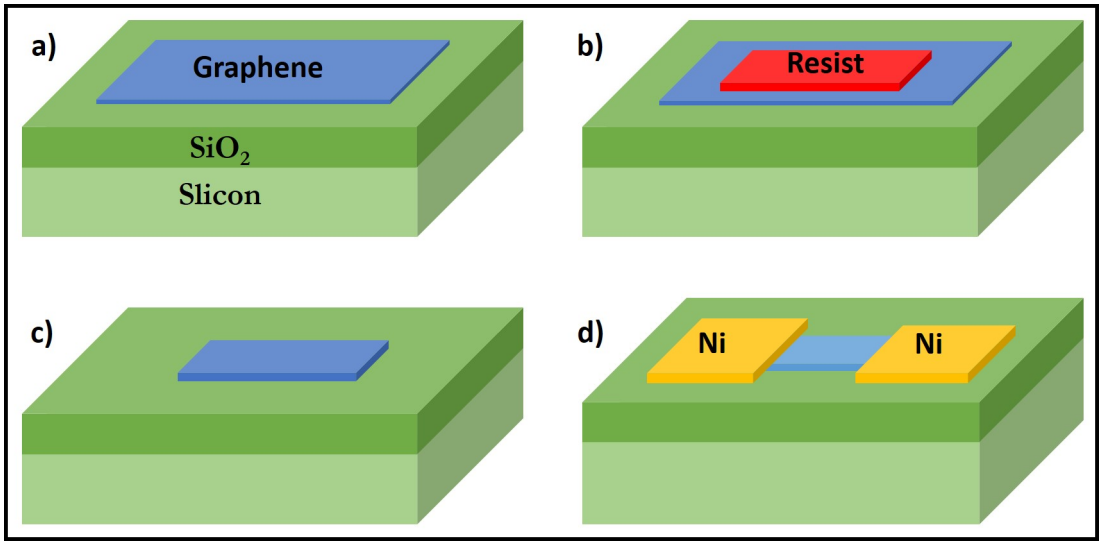


Figure 6.1.1: CVD GFET fabrication process; a) Graphene transfer on SiO_2, b) Grapahene patterning lithography, c) Patterned graphene, d) device structure after metal deposition and lift-off.

6.1.1 Alignment marks formation in SiO_2

First step in fabrication of CVD GFETs is to create alignments to facilitate subsequent lithography steps. Alignment marks can be created using photolithography (S1813 photoresist) and metal deposition or etching patterned SiO_2 using 5:1 buffered hydrofluoric acid (BHF). Metal deposition increases device fabrication time, hence etching of patterned SiO_2 was used. Etching is done by keeping sample in horizontal and vertical position in petridish. Etch rate for horizontal position decreases after some time, whereas it is constant in vertical position. In vertical position, byproducts of etching reaction are carried away easily from etching site because of gravity. Etch rate obtained for vertical position is $\sim$ 173 nm/min at room temperature. Comparison of two cases is shown in fig. 6.1.2.

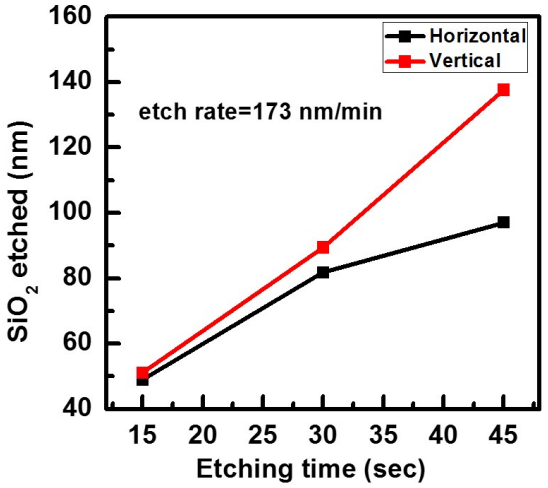


Figure 6.1.2: Comparison of SiO_2 etching in horizontal and vertical position using 5:1 BHF

6.1.2 Graphene patterning

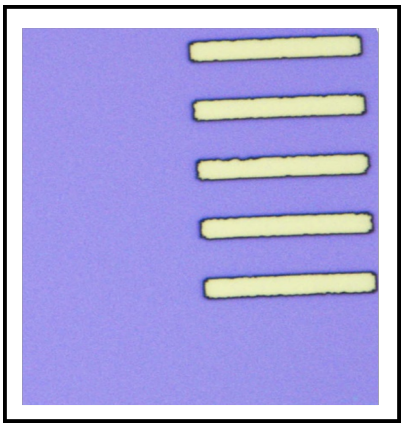


Figure 6.1.3: Optical image of patterned resist on top of graphene.

After alignments are created, next step is to transfer graphene on SiO_2 substrate and pattern it. Graphene transfer is carried out using standard PMMA transfer method. After natural drying and resist removal, patterning lithography is performed using AZ5214E. Patterning lithography creates strips of photoresist (Fig. 6.1.3). Sample is then exposed to O_2 plasma at 50 W, 50 sccm O_2 for 5 min to etch graphene from unwanted exposed regions. After exposure to O_2 plasma, resist is stripped using AZ 100 remover.

6.1.3 S/D contact formation

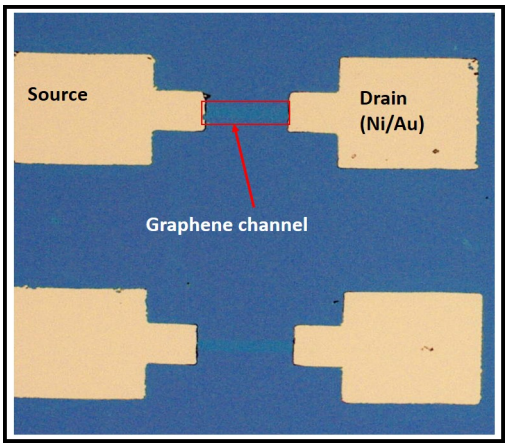


Figure 6.1.4: Optical image of fabricated CVD GFETs showing source, drain and patterned graphene channel.

Source/drain regions are patterned using AZ5214E photoresist. Ni (80 nm) is deposited using 4TEBE (4-target e-beam evaporator). Lift-off is carried out in AZ 100 remover. Optical image of device after lift-off is shown in fig.

6.2 Fabrication of top-gated devices

Back-gated devices are fabricated with Ni/Au (Nickel/Gold) contact using previously described fabrication procedure. Gold (Au) is used as capping layer to protect Ni (Nickel) from 2% HF (hydrofluoric acid) solution used during dielectric patterning step. Figure 6.2.1 shows fabrication steps which are described in consecutive sections in brief.

6.2.1 Top-gate dielectric Deposition

Top gate dielectric (Al_2O_3) is deposited using sol−gel technique. In this technique, 2−Methoxyethanol ($C_3H_8O_2$) is mixed with Aluminum nitrate nanohydrate ($Al(NO_3)_3 9H_2O$) to form 0.6 M (Molar) solution. The solution is sonicated for 2 hours and spin coated on top of sample. Solution is spin

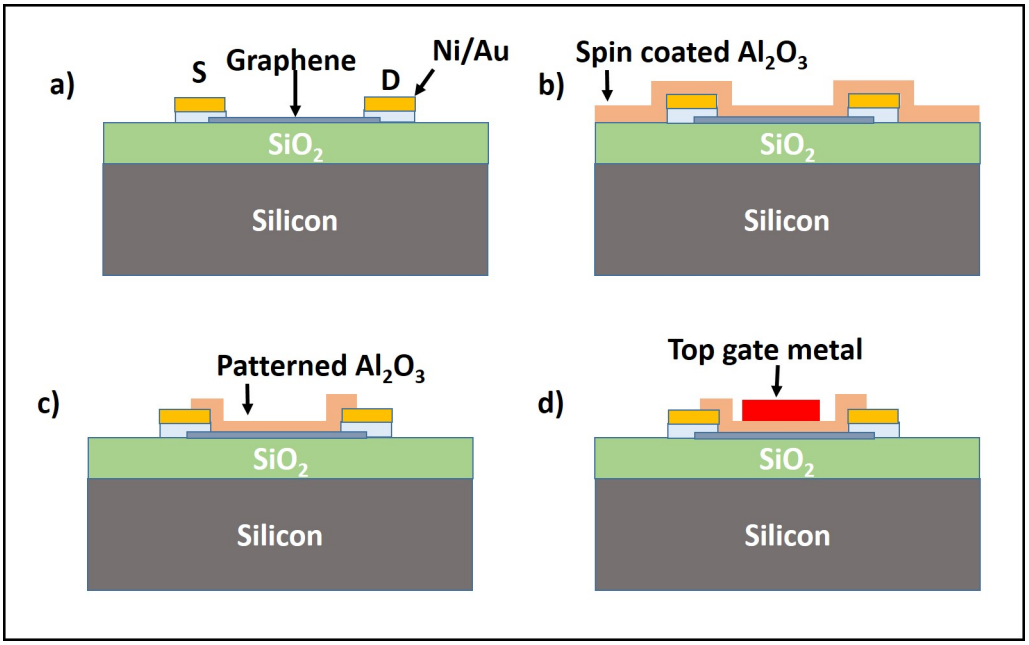


Figure 6.2.1: Fabrication steps for top-gated GFETs; a) Back-gated device, b) Conformal dielctric deposition using spin coating technique, c) Dielectric patterning, d) Top gate metal deposition.

coated at 5000 RPM and then baked at 250 ^{o}C for 10 min, twice. To make spin coated Al_2O_3 robust, forming gas annealing is done at 560 ^{o}C for 8 min. Next step is to pattern spin coated dielectric in the form of top gate dielectric strips.

6.2.2 Dielectric patterning

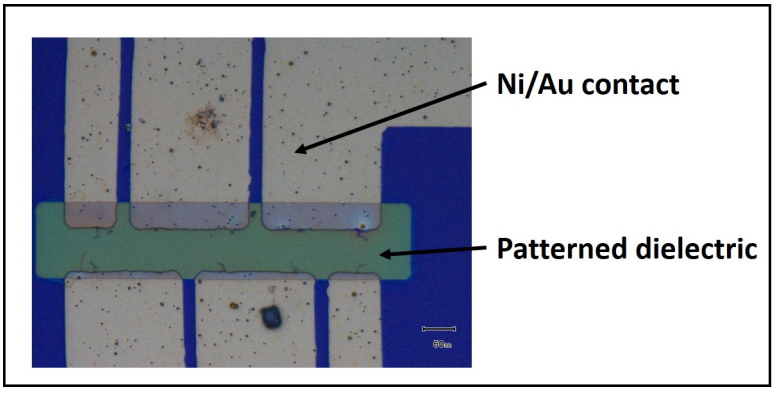


Figure 6.2.2: Optical image of patterned top gate dielectric.

Spin coated Al_2O_3 is patterned in the form of top gate dielectric.

Dielectric patterning lithography is carried out using S1813 positive photoresist followed by wet chemical etching using 2% HF solution. Figure 6.2.2 shows optical image of patterned Al_2O_3.

6.2.3 Top-gate metallization

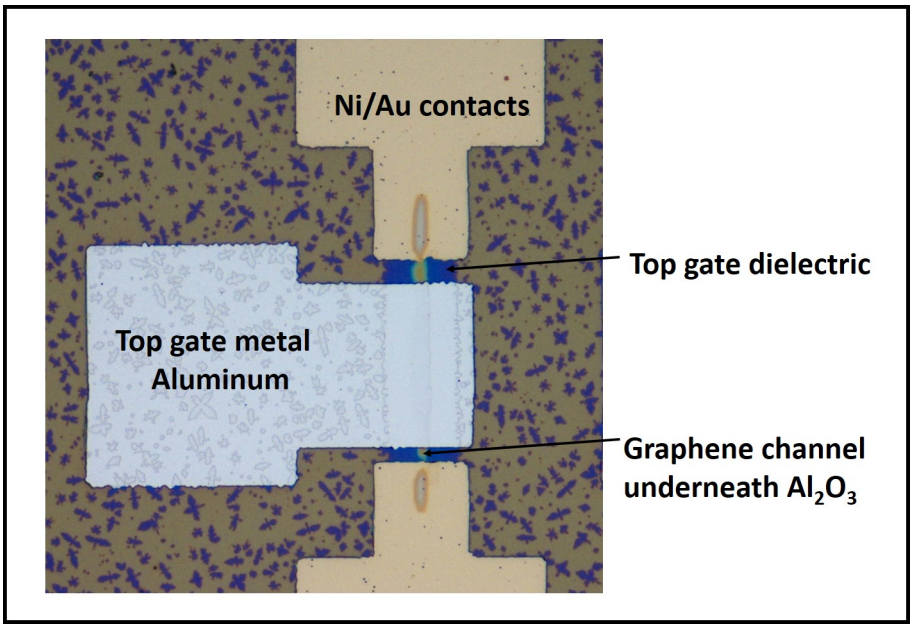


Figure 6.2.3: Optical image of top-gate GFET after metal deposition.

Final step in fabrication of top-gated GFETs is to deposit top-gate metal. Top gate metallization lithography is done using S1813 PPR. Aluminum is deposited using 4TEBE and lift-off is carried out in PG remover. Figure 6.2.3 shows optical image of fabricated top-gate device after metallization.

6.3 Electrical characterization

6.3.1 Suitable resist for fabrication of GFETs

Graphene transfer was done using EL9 copolymer for devices fabricated using AZ5214E and S1813 resist. Figure 6.3.1 shows comparison of transfer

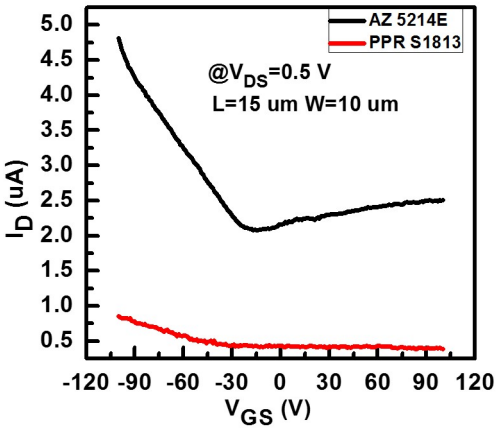


Figure 6.3.1: Comparison of CVD GFETs fabricated using S1813 and AZ5214E photoresist and graphene transfer using EL9 copolymer.

characteristics of devices fabricated using AZ5214E and S1813 resist. electron current is suppressed for devices fabricated using S1813 resist. This could be because of heavy p−doping of graphene during device processing using S1813 [29].

Devices fabricated using AZ5214E resist showed better performance as compared to S1813. Dirac point is at -15 V. Small electron current modulation with gate voltage could be because of doping from charged impurities present in Cu etchant or defects in transferred graphene [30] or charge trasfer from contacts [19].

6.3.2 Suitable resist for graphene transfer

Figure 6.3.2 shows comparison of graphene transfer carried out using EL9 copolymer and PMMA resist. Both the samples were processed using AZ5214E photoresist. Channel was 15 μm in long and 10 μm wide. Table 6.3.1 shows comparison of different electrical parameters from EL9 and PMMA transfer process. There is large improvement in carrier mobility for graphene transfer done using PMMA, indicating good quality (less breakages and defects) of transferred graphene.

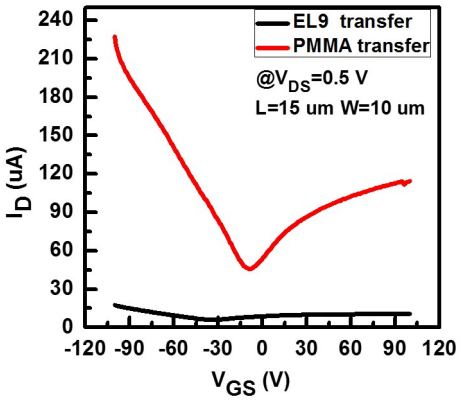


Figure 6.3.2: Comparison of graphene transfer using PMMA and EL9. Devices are fabricated using AZ5214E resist and optical lithography.

Table 6.3.1: Comparison of different electrical parameters for EL9 and PMMA transfer

	μ_h $(cm^2/V-s)$	μ_e $(cm^2/V-s)$	$V_0(V)$
PMMA	489.04	354.47	-8
EL9	8.41	1.97	-15

6.3.3 Suitable resist remover for AZ5214E

Figure 6.3.3 shows comparison of transfer characteristics of devices fabricated using AZ5214E and resist removal using acetone and AZ 100 remover. In case of acetone, resist might not have been completely removed during lift-off or any other resist removal step. It is well known that the AZ5214E resist dopes graphene p-type [31]. This can be the reason for current saturation for devices in which acetone is used for resist removal. Samples for which AZ 100 remover is used for removing resist, improved transfer characteristics and Dirac point is also obtained.

In summary AZ5214E resist, graphene transfer using PMMA, resist removal and lift-off using AZ 100 remover are suited for graphene field effect devices fabricated using photolithography.

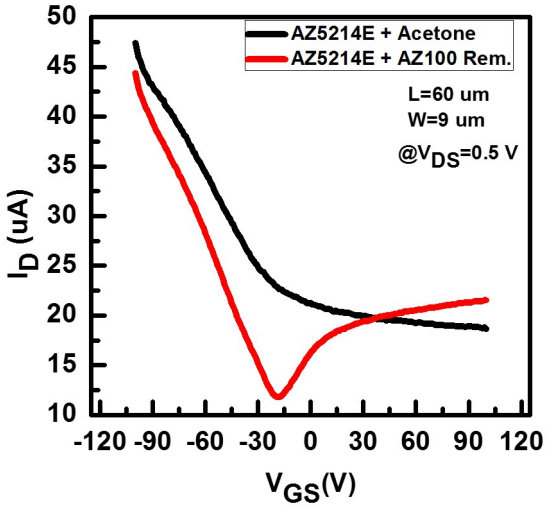
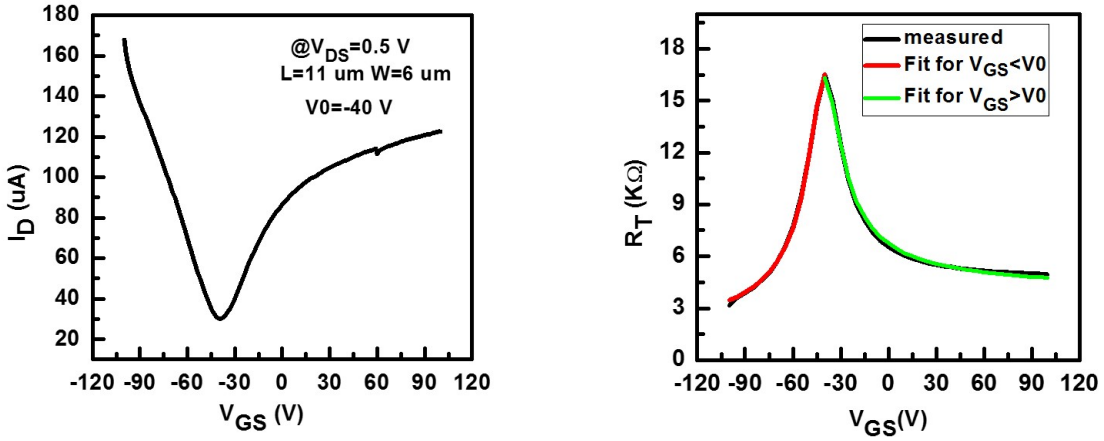


Figure 6.3.3: Comparison of AZ5214E resit removal using Acetone and AZ 100 remover.

6.3.4 Transfer and resistance vs gate voltage char.



(a) Transfer characteristics

(b) Total resistance vs gate voltage

Figure 6.3.4: Current-voltage and resistance-voltage char. of CVD GFET fabricated using optical lithography.

Transfer (I_D-V_{GS}) and resistance vs gate voltage (R_T-V_{GS}) characteristics of device fabricated using AZ5214E phtotresist and graphene transfer using PMMA is shown in Fig. 7.1.3. Device is 11 μm long and 6 μm wide. Dirac point is at -40V. Different electrical parameters extracted using FTM and DTM are listed in table 6.3.2.

Table 6.3.2: Extracted parameters using DTM and FTM.

	μ_h (cm^2/V−s)	μ_e (cm^2/V−s)	R_{ch} KΩ μm	R_{ce} KΩ μm	n_0 /cm^2
DTM	775.135	531.83	–	–	–
FTM	1046	1413	0.8538	3.986	$6.75*10^{11}$

Table 6.3.2 shows unequal electron and hole mobility, unequal contact resistance for holes and electrons and electron current saturation after certain gate voltage. All these issues will be discussed in chapter 7

6.3.5 Highest mobility device

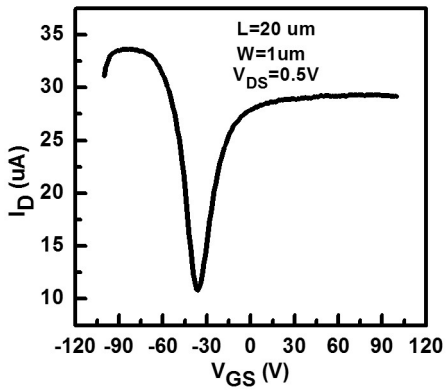
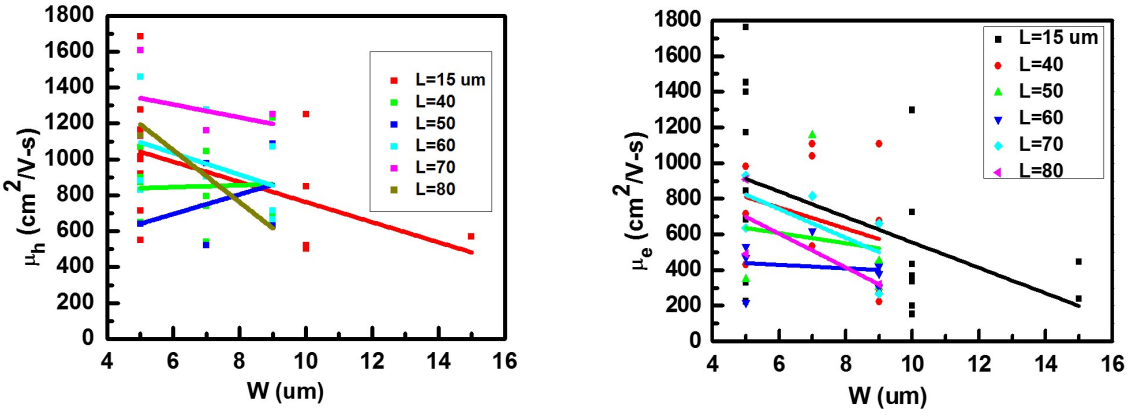


Figure 6.3.5: Transfer characteristics of highest mobility device fabricated using CVD graphene and e-beam lithography. Treated with AZ 100 remover for 12 hours.

Figure 6.3.5 shows transfer characteristics of the device for which highest mobility obtained. This device was fabricated using CVD graphene and e-beam lithography. After fabrication, devices were treated with AZ 100 remover for 10 min. Hole and electron mobilities are 4,622 cm^2/V−s and 3,197 cm^2/V−s respectively. Graphene channel was 20 um long and 1um. Reason behind such a high mobility for these devices is explained in next section.

6.4 Mobility dependence on dimensions of graphene

Mobility is a property of a materiel and is independent its dimensions. In case of graphene, mobility variation with its dimensions is observed. This section discusses mobility dependence of carriers on width and length of graphene channel.



(a) hole mobility

(b) electron mobility

Figure 6.4.1: Dependence of carrier mobility on dimensions of graphene.

Mobility values are calculated using transconductance method. From fig. 6.4.1, it is clear that mobility values decrease with increasing width (for a fixed length) of graphene channel. Inverse dependence of mobility on width can be explained by considering strip capacitor model. In case of GFETs, graphene (W_{ch} is width of graphene) acts as one of the plates of the capacitor and back-gate silicon acts as other plate with SiO2 (t_{ox}) as a dielectric. When t_{ox}/W_{ch} >0.01, fringing electric field lines cause enhanced conductivity at the edges [32]. This causes enhancement of overall conductivity and hence mobility at low channel widths. As width of channel increases, charge distribution becomes more uniform and hence mobility start to decrease and saturates after certain value.

Length dependence doesn't show any trend as such in our devices. From literature, it has been observed that mobility first increases with length

and then saturates at channel length of several micrometers. This trend is observed in the devices because graphene devices operate in both quasi-ballistic and diffusive regime depending on length.

Chapter 7

Issues with characterization GFETs

Graphene being 2D material, it's very sensitive to environment humidity, adsorbates, and charge traps at graphene/dielectric interface. atmospheric gases dope graphene, and interface traps lead to hysteresis in current-voltage characteristics. In this chapter, different issues with electrical characterization of graphene devices like shift in Dirac point due to unintentional doping, mobility degradation because of graphene/dielectric interface traps, Hysteresis behavior of devices and asymmetry in current-voltage characteristics are discussed.

7.1 Unintentional doping

Doping in graphene is induction of charge carriers, either holes or electrons, because of electric field or by chemical means. Electrical doping happens in GFETs when type and concentration of carrier is tuned by applying gate voltage. When gate voltage is greater than Dirac point voltage, electrons will carry the current ans graphene is said to be n−doped. Holes carry current when gate voltage is less than Dirac point voltage and graphene is p-doped.

Chemical doping happens when graphene interacts with other chemical species. There are two types of chemical doping, surface charge transfer and

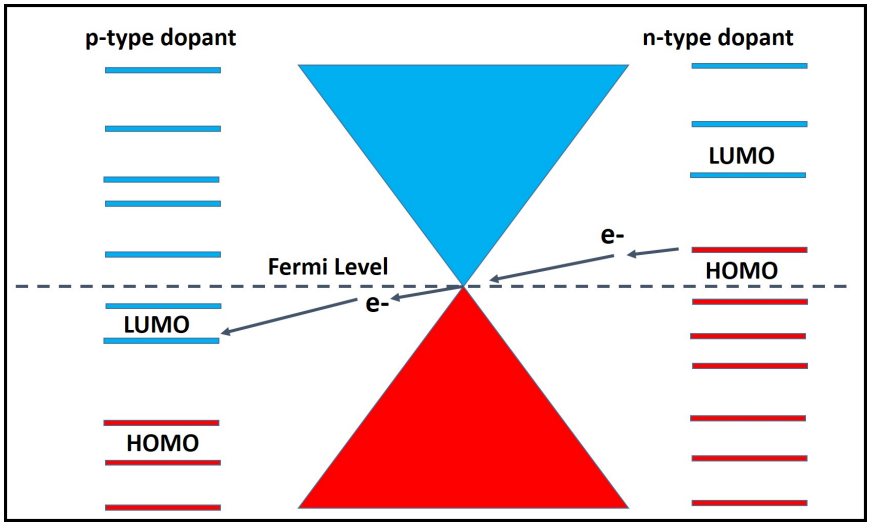


Figure 7.1.1: Mechanism of chemical doping by charge transfer due to surface adsorbates.

substitutional doping. In surface charge transfer, charge transfer happens between surface adsorbates and graphene because of difference in electronic chemical potential at the interface [33]. Figure 7.1.1 shows mechanism of chemical doping by charge transfer from/to surface dopants. When fermi energy of graphene is above LUMO (Lowest Unoccupied Molecular Orbital) levels or adsorbates, graphene gets p-doped. Fermi energy below HOMO (Highest Occupied Molecular Orbital) levels of adsorbate dope graphene n-type.

7.1.1 P-type doping of fabricated devices

P-doping of graphene mainly happens from adsorbed water and oxygen molecules [34], resist contamination introduced during device processing and adsorbates attached to silanol (SiOH) groups [35]. Shift of Dirac point is observed due to doping from adsorbates or adsrobates attached to SiOH group at graphene/ SiO_2 interface. Figure shows p-doped fabricated GFET. Dirac point of device has shifted to +41 V. Methods to restore Dirac point near 0 volt are discussed in chapter chapter 8

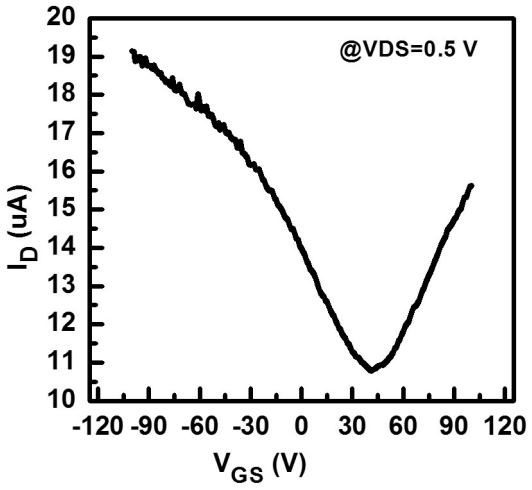
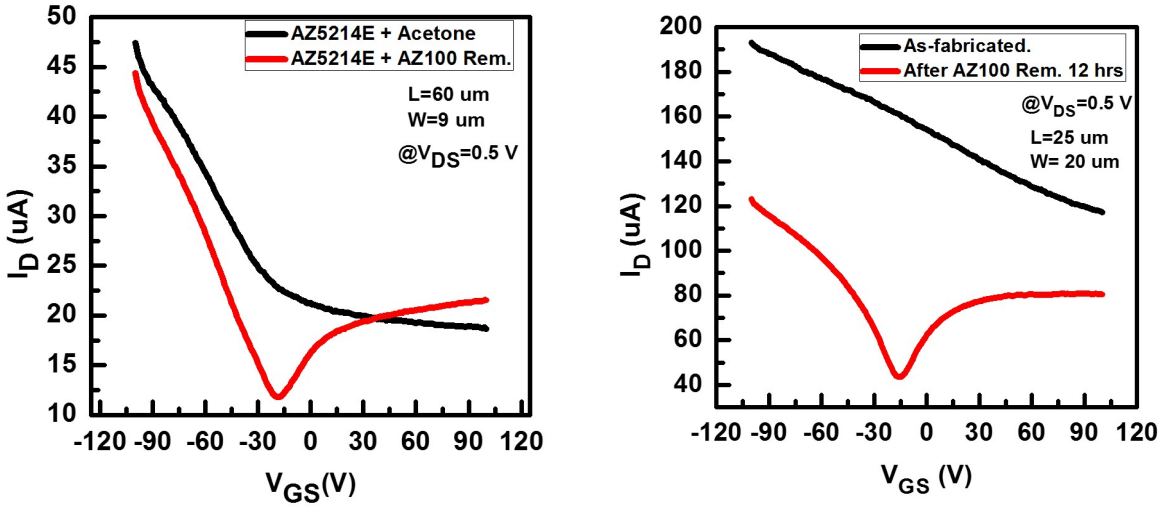


Figure 7.1.2: Shift in Dirac point of p-doped as-fabricated device due to unintentional doping. Devices were fabricated using exfoliated graphene and e-beam lithography.

7.1.2 N-type doping of fabricated devices



(a) (b)

Figure 7.1.3: Effect of treating CVD graphene with AZ 100 remover; (a) devices fabricated using AZ5214E resist, acetone and AZ 100 remover used for stripping resist, (b) Devices fabricated using PMMA resist and treated with AZ 100 remover for 12 hours.

Graphene devices fabricated using photolithography and AZ5214E resist showed negative Dirac point voltage, showing n−type doping. We are using AZ 100 remover for stripping AZ5214E resist lift-off. Negative shift of Dirac point could be coming from AZ 100 remover or AZ5214E re-

sist. AZ5214E resist dopes graphene p−type [31]. To verify this, we used acetone and AZ5214E photoresist for resist removal and lift-off process. Comparison of transfer characteristics of the devices are shown in figure 7.1.3a. Devices fabricated using AZ5214E and acetone showed no Dirac point and electron current saturation, where as devices fabricated using AZ5214E resist and AZ 100 remover showed negative Dirac point voltage. From transfer characteristics of the figure 7.1.3a, devices fabricated using AZ 100 remover are n-doped in contrast to acetone, which are p-doped.

We also fabricated devices using e-beam lithography and PMMA resist. PMMA resist is known to dope graphene p-type which is evident in figure 7.1.3b. Devices were kept in AZ 100 remover for 12 hours. Figure 7.1.3b shows that the graphene was n-doped with Dirac point shifted to negative gate voltage.

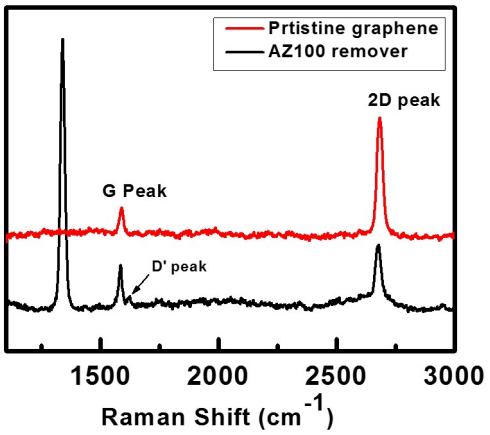
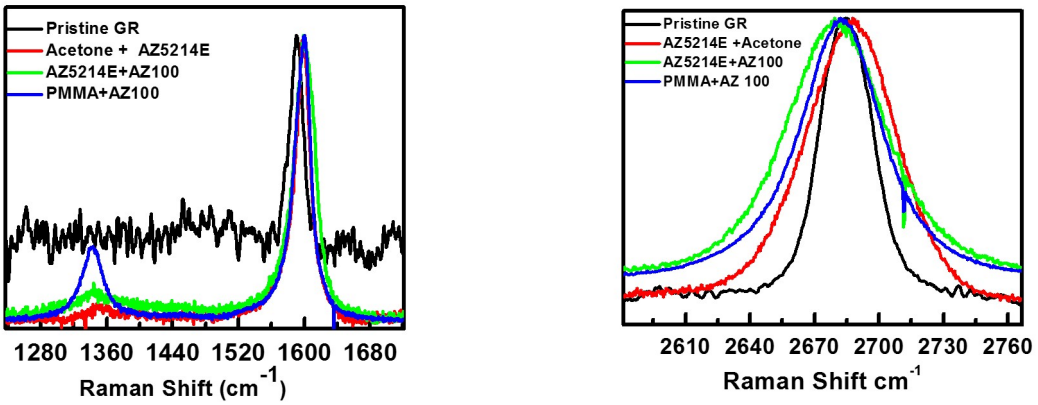


Figure 7.1.4: Raman spectrum of pristine CVD graphene, AZ5214E spin coated and removed using AZ 100 remover and graphene treated with AZ 100 remover.

Doping due to AZ 100 remover can also be seen from Raman spectrum. Figure 7.1.4 shows comparison of Raman spectrum of pristine graphene, graphene spin coated with AZ5214E and stripped using AZ 100 remover and graphene dipped in AZ 100 remover only. From figure 7.1.4, Large

D peak is observed in sample treated with AZ 100 remover, which shows structural defect induced due to nitrogen doping in graphene. PG (Pristine graphene) has G peak at 1590 cm^1 and 2D peak at 2685 cm^1. Graphene treated with AZ 100 remover has G peak at 1586 cm^1, 2D peak at 2676 cm^1, D′ peak at 1625 cm^1 and very high D peak at 1341 cm^1. In comparison with PG, there is blueshift of 4 cm^1 and 9 cm^1 in both G and 2D peak, respectively. This happens because of electron doping from nitrogen and compressive strain induced by substituted nitrogen [36]. D′ peak appearing at shoulder of G peak is also prominent and is a evidence of defects introduced in graphene [37].



(a) G and D peaks

(b) 2D peaks

Figure 7.1.5: Comparison of shift in G and 2D peaks of Raman spectrum of fabricated devices. Devices fabricated using CVD graphene, AZ5214E and PMMA resists, resist removal using acetone and AZ 100 remover.

Figure 7.1.5 raman measurement on fabricated devices. G peaks and 2D peaks have been normalized to compare Raman shift due to doping. In figure 7.1.5a, pristine graphene has G peak position at 1590 cm^{-1}. There is blueshift of 8 cm^{-1}, 10 cm^{-1}, 8 cm^{-1} for resist removal using acetone and AZ 100 remover respectively. Blueshift in G peak is signature of electron doping in graphene [36]. We also fabricated devices using PMMA resist and e-beam lithography. After fabrication devices were kept in AZ 100 remover for 12 hours. Figure 7.1.5a also shows Raman spectrum for these devices.

In case of devices fabricated using e-beam lithography, very prominent D peak at 1342 cm^{-1} is observed. which is signature structural defect introduced due to nitrogen from AZ 100 remover.

Figure 7.1.5b shows comparison of 2D peak for different devices. Pristine graphene has 2D peak at 2684 cm^{-1}. Redshift of 7 cm^{-1} is observed in case of devices fabricated using AZ5214E and AZ 100 remover. This shows electron doping of graphene [36]. Blueshift of 2 cm^{-1} is observed in case of devices fabricated using AZ5214E resist and acetone, which shows hole doping in graphene [36]. Devices fabricated using e-beam lithography also show redshift of 4 cm^{-1} in 2D peak.

In summary, n-type doping observed in our devices is introduced due to substitutional doping from nitrogen present in AZ 100 remover.

7.2 Hysteresis and performance degradation

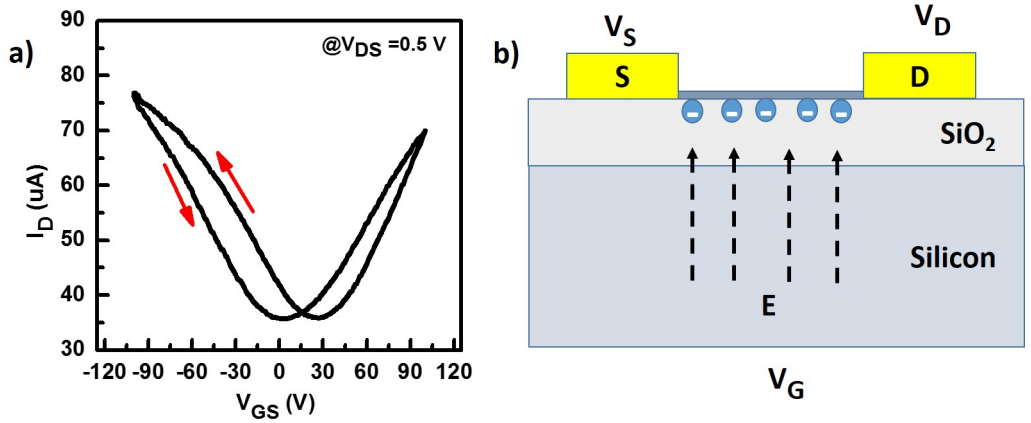


Figure 7.2.1: Hysteresis behavior of exfoliated GFET fabricated using e-beam lithography; (a)Hysteresis in transfer curve, (b)charge screening mechanism in GFETs.

Figure ??a shows typical hysteresis curve obtained from measured device. Forward sweep has Dirac point at +7 V, while it shifted to +29 V during back-sweeping. This can be explained using schematic diagram

shown in figure **??**b. When gate is swept in negative region, holes are trapped into interface traps and electric field from gate is screened by these trapped charges, in effect graphene sees less negative potential as compared to what is applied at gate, hence Dirac point shifts to left side of expected value. When gate voltage is swept in positive voltage region, electrons are accumulated in graphene/SiO_2 interface and graphene sees less positive potential as compared to what is applied at gate, hence Dirac point shifts to right side of expected value [38]. Hysteresis voltage also

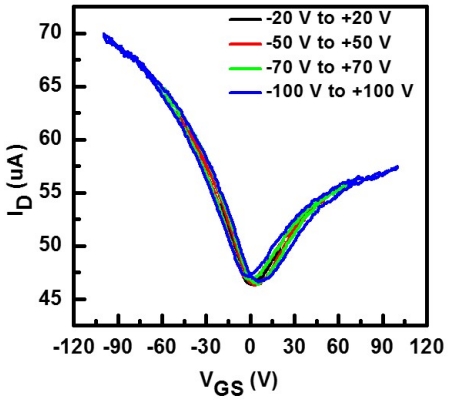


Figure 7.2.2: Shift in Dirac point of voltage of exfoliated GFET with gate voltage sweep range.

depends on gate voltage sweep range. Figure 7.2.2 shows shift of Dirac point for different gate voltage sweep ranges. Amount of shift increases as gate voltage sweep range increases, because number of trapped charges increase with increase in applied gate voltage. For sweep range from -20 V to +20 V, -50 V to +50 V, -70 V to +70 V and -100 V to +100 V have Dirac point shift of 1.5 V, 3.5 V, 4.5 V and 7 V respectively. This analysis shows that electrical measurement itself has significant impact on test device.

Trapped charge density can be calculates using amount of shift in Dirac point (ΔV_0). Number of trapped charges is given by,

$$N = \frac{1}{2e} C_{ox} \Delta V_0 \tag{7.1}$$

C_{ox} is the gate capacitance, ΔV_0 is amount of shift in Dirac point, e is electronic charge and N is trapped charge density. Hysteresis curve of fig. 7.2.1a has +22 V of Dirac point shift, this results in $7.19X10^11/cm^2$ trapped charge density. Number of trapped charges at graphene/SiO_2 interface are in the same range as that of Si/SiO_2 interface ($N_{it} \approx 5X10^{10}$ /cm^2, $N_{ot} \approx 5X10^11$ /cm^2) [38]. Movement of Dirac point can be effectively explained using trapped charge density.

Interface trap charges act as scattering centers for carrier in graphene. Trap states at graphene/SiO_2 interface can be charged or discharged via graphene channel depending on position of fermi energy of graphene relative to trap states and degrade mobility of charge carriers by scattering process. Reducing graphene/SiO_2 interface trap charge density would improve performance of GFETs [39]. Different methods to reduce hysteresis will be discussed in chapter chapter 8

7.3 Asymmetry

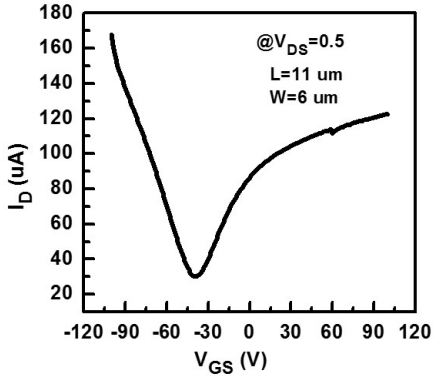


Figure 7.3.1: Asymmetry observed in transfer characteristics of CVD GFETs because of p-doping from Nickel contacts. Devices are fabricated using CVD graphene and optical lithography.

Figure 7.3.1 shows transfer characteristics of GFET with channel length of 11 μ m and with of 6 μm, hole mobility of 775.135 cm^2/V-s,

electron mobility of 531.81 cm^2/V-s, Ni source/drain contacts deposited using e-beam evaporation and Dirac point at -39 V. It is Evident from transfer characteristics of the fig. 7.3.1 that there is asymmetry and in hole and electron current branch. This happens because of charge transfer at metal/graphene interface [19]. Charge transfer happens between graphene and metal depending on work function difference between them.

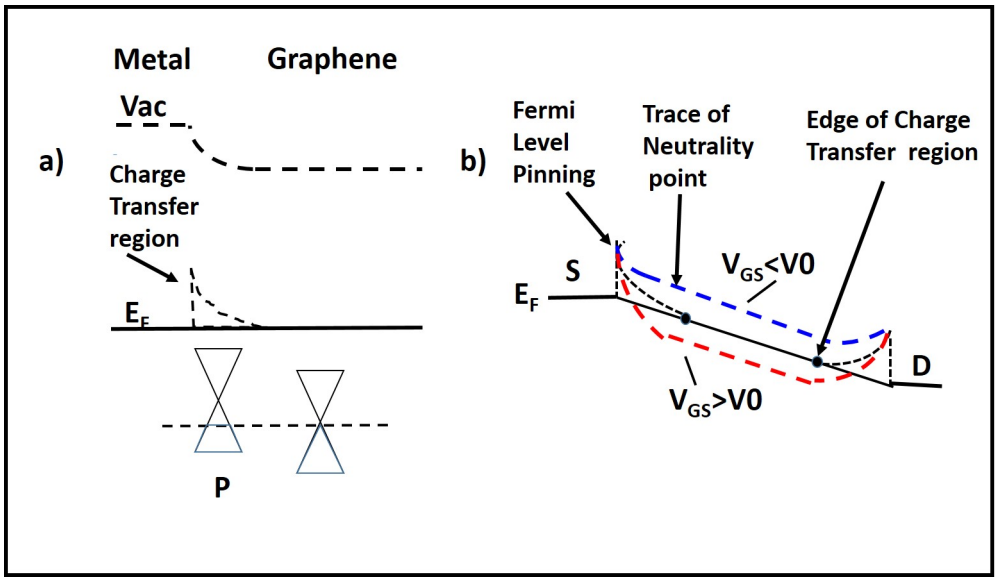


Figure 7.3.2: Charge transfer in graphene/metal interface, a) Hole doping of graphene near metal/graphene interface, b) $p-n-p$ region formation for $V_{GS} > V_0$

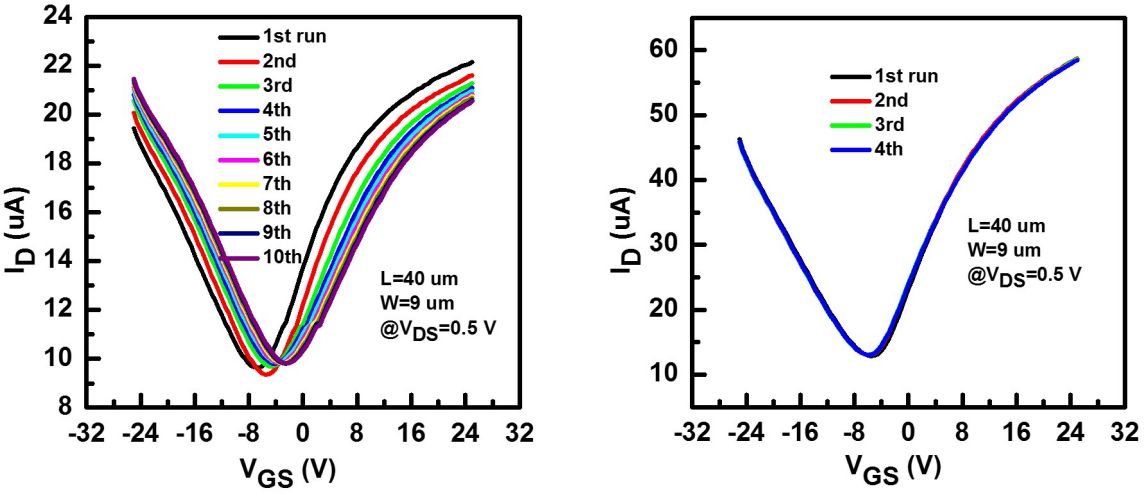
Figure 7.3.2a shows that charge transfer happens not only underneath metal but also extends away from metallurgical junction into graphene because of low density of states in graphene near Dirac point [19]. Figure 7.3.2b shows band diagram of GFETs when V_{DS} and V_{GS} are applied. When $V_{GS} > V_0$, there is formation of p−n−p junction near contact, creating additional barrier for electrons. When $V_{GS} > V_0$, there is p−p−p region formed hence no additional resistance for hole conduction.

Figure 7.3.1 shows asymmetry of current in electron branch, this is because Ni ($\phi_m = 5.2eV$) dopes graphene ($\phi_{Graphene} = 4.5eV$) p-type near contact regions. This condition is similar to one shown in 7.3.2. The fermi

level at metal and graphene interface doesn't move with gate voltage because of fermi level pinning at interface. when positive gate voltage is applied, ferm level moves below Dirac point in bulk graphene region but is pinned at interface. Hence this creates crossover between trace of neutrality point and fermi level as shown in figure 7.3.2. because of low density of states around Dirac point in graphene, additional resistance is introduced at crossover point forming p-n-p region. Carriers have to travel from p to n to p region incurring extra resistance at crossover points. This extra resistance is because of density of states limitation around Dirac point in graphene [40].

Asymmetry is also observed for metals like Ti/Au [19]. Cr has work function of 4.6 eV, hence it doesn't show any doping effects and hence no asymmetry [19].

7.4 Stability



(a) Without FGA (b) FGA

Figure 7.4.1: Stability of devices during measurement. Devices fabricated using 90 nm thermal oxide, CVD graphene and optical lithography.

In this experiment, 100 nm dry oxide is thermally grown on p-type

silicon. Forming gas annealing is performed at 430 ^{o}C for 30 min for sample (S1) and other sample (S2) was not annealed. following analysis is for sample S2.

Repeated measurements were performed one after another. It is observed that, Dirac point shift to less negative voltages with each run. In addition to this, electron current branch is showing slope degradation. Dirac point shift can be explained with the help of fig. **??**b. When gate voltage is positive for the previous measurement, electrons are trapped in interface trap states and screen the gate electric field during next measurement [41] (because of finite recovery time). This causes graphene to see more negative voltage than what is applied at gate. In simple terms, trapping of electrons cause graphene to be p-doped and shift Dirac point to the right of expected value.

Slope (transconductance) degradation is observed due to presence of interface traps [42]. The slope degradation could happen because of coulombic scattering mechanism. Interface traps present at SiO_2/graphene interface capture carriers from channel and act as scattering centers. slope degradation can be explained using figure 7.4.2.

Figure 7.4.2 shows the mechanism of charge trapping and de$-$trapping [42]. ϵ_t is trap state and E_F is the fermi energy. There are two types of interface traps, acceptor like and donor like. acceptor like traps are negatively charged when they are filled and neutral when empty. Donor like traps are neutral when filled and positive when empty. Mobility degradation for electrons can be explained using assumption that, the interface traps are acceptor like. When positive gate voltage is applied, fermi enery moves into conduction band, negatively charging acceptor like state. These charged states now act as scattering centers for electrons in graphene chan-

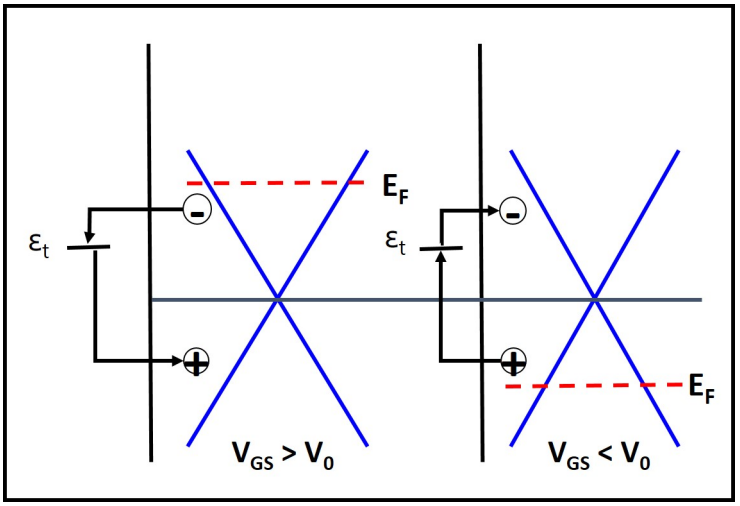


Figure 7.4.2: Mechanism of charge trapping and de-trapping depending on position of fermi level with respect to interface trap state.

nel, hence reducing their mobility. When negative voltage is applied these states are neutral, hence do not degrade hole mobility.

Table 7.4.1: Effect of repeated measurement on mobillity and Dirac point

Test run	μ_h ($cm^2/V-s$)	μ_e ($cm^2/V-s$)	V_{Dirac} (V)
1^{st}	156	207	-7
2^{nd}	161	203	-5.5
3^{rd}	162	170	-5
4^{th}	154	160	-4
5^{th}	159	154	-3.75
6^{th}	161	155	-3.5
7^{th}	161	152	-3
8^{th}	162	152	-2.5
9^{th}	159	150	-2.5
10^{th}	160	150	-2.5

Table 7.4.1 shows mobility and Dirac point values for repeated test runs. Mobility values for electrons are degrading with each run whereas hole mobilities are almost constant. Dirac point also shift to less negative voltage. Both electron mobility and Dirac point voltage start to saturate after some time. This could be happening because with time, the acceptor states get filled completely and stay charged, hence no further mobility

degradation and Dirac point shift.

Sample S1 was annealed in forming gas. Transfer characteristics for this sample under repeated measurement is shown in fig. 7.4.1b. They are stable with repeated test runs. The stability could be because of reduced interface trap density due to forming gas annealing.

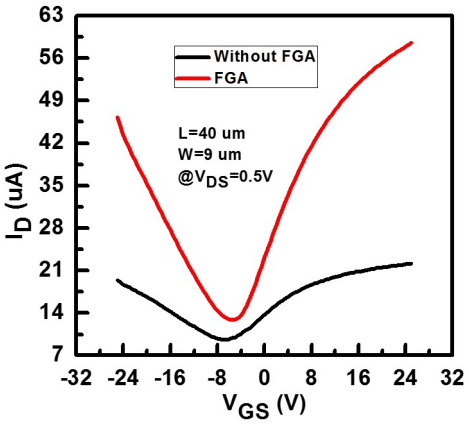


Figure 7.4.3: Comparison of transfer char. of devices fabricated using SiO_2 with and without FGA

Figure 7.4.3 shows comparison of transfer characteristics of sample with and without forming gas annealing. Because of reduction in interface trap density, slope of both current branches have significantly improved for annealed sample. Forming gas annealed sample shows higher mobility. Table 7.4.2 shows comparison of mobility values for two samples.

Table 7.4.2: Effect of forming gas annealing on mobility

Sample	μ_h (cm^2/V−s)	μ_e (cm^2/V−s)
FGA	472	639
W/O FGA	156	207

In summary, unintentional doping, asymmetry in I_D-V_{GS} and effect of interface traps on hysteresis are discussed. Forming gas annealing of Si/SiO_2

samples help in reducing interface trap state density, hence improve the mobility of graphene.

Chapter 8

Methods to improve performance of GFETs

In chapter 7, different issues like shift of neutrality point due to unintentional doping, hysteresis because of interface traps, mobility degradation because of charged impurity scattering and finally asymmetry arising in electron and hole current branches were discussed. In this chapter, different methods to reduce some of those issues will be discussed in brief.

8.1 Removal of resist residues

Resist residues are inevitable during fabrication of GFETs. Resist residues are introduced during transfer of CVD graphene using PMMA and lithography steps. Resist residues can degrade device performance by acting as scattering centers for charge carriers. PMMA also dopes graphene p-type [43]. CVD graphene device fabrication using photolithography and S1813 photoresist also dopes graphene p-type [29]. AZ5214E resist also leaves resist residues on graphene [44]. Some of the methods to remove resist residues will be discussed here.

Annealing devices in Ar [45, 46], H_2 [47], Ar/H_2 [48] or vaccum [49, 50, 51] can remove resist residues. Current annealing or joule heating, passing high

current trough graphene, induces local heating and helps in removing resist [38, 51, 52].

Different solvents like chloroform cleaning [51], formamide [53] can also be used to remove resist contaminant from graphene surface. When using photolithography for graphene device fabrication, use of NEP (N-ethyl-2-pyrrolidone) based removers can help in removing resist residues [29]. In photolithography, TMAH based developers are used. Thin aluminum capping layer can also be used between graphene and photoresist to reduce resist contamination [44].

8.2 Alternate substrate

Hysteresis is introduced because of charge trapping in SiO_2/graphene interface. Performance of graphene devices is also affected by impurity charged scattering. Reducing substrate interaction can help in reducing hysteresis and improve performance.

SiO_2 is hydrophilic in nature, water can get trapped in between graphene and SiO_2 and act as charge trapping center. Use of hydrophobic substrates like parylene [54], HMDS (hexamethyldisilazane) [55], PMMA, and Mica [56].

8.3 Passivation

Methods like annealing, cleaning using solvents and use of alternate substrate do not provide long term stability of graphene devices [57]. One of the methods to improve stability and robustness of graphene devices is to protect encapsulate devices using some protective layer. Passivation layer act as barrier for any atmospheric gases.

Passivation layers like pentacene [58], amine based SAM [59], PECVD grown Si_3N_4 [60], Boron nitride [61] and ALD Al_2O_3 [57]. Direct growth of ALD Al_2O_3 is non−uniform because of lack of nucleation sites on graphene. Deposition of 2 nm aluminum using e-beam evaporation acts as seed layer for further uniform growth of ALD AL_2O_3.

8.4 Forming Gas Annealing

Forming gas annealing helps in reduction of interface trap density at SiO_2/graphene interface, which in turn help in improving mobility of graphene. Effect of forming gas annealing is discussed in detail in section 7.4.

Chapter 9

Conclusion and Future work

9.1 Conclusions

1. Established fabrication process flow for exfoliated graphene FETs using PMMA resist. Achieved mobilities upto 3287 $cm^2/V-s$.

2. CVD graphene transfer using PMMA results in higher mobilities for carrier i.e., less breakages and defects are observed in transferred graphene

3. Established fabrication process flow for back-gated CVD graphene GFETs. Use of AZ5214E resist for device fabrication resulted in better mobilities for carriers than S1813 PPR. Although AZ 100 remover dopes graphene n-type, it preserves ambilpolar nature of graphene. Whereas, use of acetone results in heavy p-doping from AZ5214E, hence elctron current saturation. Achieved mobilities upto 1762 $cm^2/V-s$ using photolithography.

4. Negative dirac point observed in the devices is because of n-type doping from Nitrogen present in AZ 100 remover. This is confirmed with Raman measurement. In addition to raman measurement, it is also confirmed by fabricating devices using ebeam lithography and treating them with AZ 100 remover, which resulted in n-type doping of devices.

5. CVD graphene devices are fabricated using ebeam lithography and PMMA resist. Current saturation is observed in as-fabricated devices. To get ambipolar current-voltage characteristics, devices were treated with AZ 100 remover. Achieved mobilities upto 4622 $cm^2/V-s$.

6. Ni as contact metal offers a low resistance for graphene FETs. Contact resistance upto 850 Ω μm are obtained in our devices.

7. Issue of unintentional doping is solved by thermal or current annealing of devices. Asymmetry issues is solved using alternate contact metals like, Cr/Au.

8. Interface traps at Si/SiO_2 have effect on hysteresis behavior, stability during measurement and mobility of graphene. Forming gas annealing is observed to reduce these effects and improve mobility significantly.

9. Established fabrication process flow for top-gated CVD graphene GFETs using spin coated Al_2O_3 as a dielectric.

9.2 Future work

- Passivation of CVD graphene devices using spin coated Al_2O_3
- Resist left from lithography steps, can affect metal/graphene contact. Before going for metal deposition, graphene/metal junstion region needs to be cleaned using low power RF plasma.
- Graphene devices can be fabricated using alternate substrate like HMDS, PDMS and Mica to reduce effect of substrate.
- Fabrication and characterization of buried-gate graphene devices.
- Transfer of graphene after Source/Drain contact formation to reduce number of lithography steps that graphene goes through.

- Fabrication and characterization of CVD graphene and exfoliated top-gated graphene devices.

Appendix A

Process recipes for fabrication of exfoliated GFETs using e-beam lithography

Wafer specifications

- Substrate : Silicon
- Substrate size: 2”
- Doping type : P
- resistivity : < 0.005 Ωcm
- Orientation : 100
- Surface : Single sided polished (SSP)

RCA Cleaning

Tool: Wet process bench.

- 2% HF dip: 1152 ml DI water + 48 ml(49% HF) for 30 sec;
- RCA1: NH_4OH:H_2O_2:DI water in the ratio 125ml:250ml:875ml 75^oC, duration: 1200 sec;
- 2% HF dip: 1152 ml DI water + 48 ml(49% HF) for 30 sec;
- RCA2: HCl:H_2O_2:DI water in the ratio 125ml:250ml:875ml 75^oC, duration: 1200 sec.;
- 2% HF dip: 1152 ml DI water + 48 ml(49% HF) for 30 sec;

300 nm Pyrogenic oxide growth

Tool: 2" Pyrogenic oxidation furnace

- H_2 gas flow: 70 sccm
- O_2 gas flow: 100 sccm
- Temperature : 1050 ^oC
- Time : 1140 sec

Forming Gas Annealing

Tool: 2" General purpose annealing furnace

- Forming gas : $H_2(5\%)$ + $N_2(95$
- Temperature : 420 ^oC
- Time : 1800 sec

Substrate cleaning before graphene transfer

Tool: Wet process bench and Sonicator Sonicate sample in acetone for 5 min before graphene transfer.

Exfoliated graphene transfer on SiO_2

following steps are involved in transfer of graphene on SiO_2 substrate:

- Adhesive scotch tape is placed on block of HOPG (Highly oriented pyrolytic graphite) and gently pressure is applied with plastic twiser.
- This process will peel top layers of HOPG crystal on scotch tape. Repeated peeling on fresh part of the tape will create few layer and single layer graphene flakes on tape.
- Immediately tape is pressed on to sample, and pressure is applied gently with plastic twiser.

- After some time, scotch tape is pulled off the sample slowly, this leaves behind multilayer, few layer and single layer graphene flakes on sample.

Marker lithography

Tool: RAITH150 Two

- Resist: 950K PMMA A4-(+ve) e−beam resist
- Dehydration bake: 1 min at 170 ^{o}C
- PMMA spin coat:

Table A.0.1: PMMA spin coating recipe

Step	RPM	Time(s)	Acceleration
Step1	300	10	> 150
Step2	3000	45	> 1500
Step3	0	10	112

- Prebake: at 180 ^{o}C for 90 sec
- Exposure parameters:
  - Acceleration: 10 KV
  - Aperture : 30 μ m
  - Dose: 80 uC/cm^2
  - Developer: MIBK:IPA:: 3:1
  - Development time: 30 sec
  - Stopper: 2-propanol (IPA) pure
  - Stopping time: 15 sec

Metallization

Tool: Cr/Au thermal evaporator

- Metal : Cr/Au
- Thickness: 10nm/70nm

Lift-off

Tool: Wet process bench

- Lift-off solvent: acetone
- Duration: 24 hrs.

Identification of flakes

Tools: Optical microscope, Raman spectroscopy

- Identify few layer flakes using optical microscope and capture images at 100X magnification.
- Perform Raman measurement to investigate number of layers of graphene.

Electrode design

Tools: Clewin 4 layout editor
Using optical images of flakes, design electrodes with the help of optical images and Clewin 4 layout editor.

Contact lithography

Tool: RAITH150 TWO
Use recipe similar to one used for marker lithography.

Metallization

Tool: Cr/Au thermal evaporator, 4TEBE

- Metals: Cr/Au, Pd/Au, Ni/Au etc.
- Thickness: 10 nm/60 nm

Lift-off

Tool: Wet process bench

- Lift-off solvent: acetone
- Duration: 24 hrs.

Appendix B

Process recipes for fabrication of CVD GFETs using optical lithography

Alignment marks lithography

Tool: Double sided aligner

- Resist : Shipley microposit S1813 phtotoresist
- Step 1 − dehydration bake : 5 min at 120 C
- Step 2 − spin coat :

Table B.0.1: S1813 PPR spin coating recipe

Step	RPM	Time(s)	Acceleration
Step1	500	10	336
Step2	6000	45	3136
Step3	0	5	112

- Step 3 − pre-exposure Bake : 3 min at 90 C
- Step 4 − exposure Dose : 60 mJ/cm^2
- Step 5 − development :
  - Developer− MF 319 (use beaker for development)
  - Development time− 8 sec

Alignment marks etching using 5:1 BHF

Tool: Wet process bench

- 5:1 BHF
- etch rate: 2.88 nm/sec
- etch time: 50 sec

Resist stripping

- PG Remover : 300 sec
- IPA : 180 sec
- DI water : 180 sec

Substrate cleaning before graphene transfer

Tool: Wet process bench and Sonicator Sonicate sample in acetone for 5 min before graphene transfer.

Graphene transfer

- PMMA spin coat:

Table B.0.2: PMMA spin coating recipe

Step	RPM	Time(s)	Acceleration
Step1	300	10	> 150
Step2	3200	60	> 1500
Step3	0	5	112

- Cut the edges using scissor and keep in copper etchant for $3-4$ hours. make sure that there is no copper left on graphene/PMMA stack.
- Treat Si/SiO_2 sample with Argon plasma (Tool Orion sputter) or O_2 plasma (Tool: Plasma Asher) to improve adhesion of transferred graphene to SiO_2.
- Immediately transfer graphene on SiO_2 using standard transfer method.
- Keep sample for natural drying in desiccator filled with silica gel for about $10-12$ hours.

- Heat sample in acetone at 70 ^{o}C for 30−40 min.
- Clean in IPA and DI water.

Developer for AZ5214E resist

- 5% TMAH solution as a developer
- 5% TMAH solution preparation: 10 ml of 25% TMAH + 40 ml DI water.

Graphene patterning lithography

Tool: Double Sided Aligner (DSA)

- Resist: AZ5214E
- Step 1 − Dehydration bake : 5 min at 120 C
- Step 2 − Spin coat :

Table B.0.3: AZ5214E resist spin coating recipe

Step	RPM	Time(s)	Acceleration
Step1	500	10	336
Step2	5000	40	> 2500
Step3	0	5	112

- Step 3 − pre-exposure bake : 50 sec at 110 C
- Step 4 − exposure dose : 65 mJ/cm^2
- Step 5 − development :
  - Developer− 5% TMAH (use beaker for development)
  - Development time− 9 sec

Graphene Patterning recipe

Tool: Plasma Asher

- O_2 gas flow: 45 sccm

- RF Power : 50 Watt
- Time : 180 sec

Resist stripping

Tool: Wet process bench

- AZ100 remover: 240-300 sec
- IPA : 180 sec
- DI water : 180 sec

Contact lithography

Tool: Double Sided Aligner

Use recipe similar to graphene patterning lithography.

Metallization

Tool:4 Target e-beam evaporator (4TEBE)

- Metal: Ni/Au
- Thickness: 30nm/50nm

Lift-off

Tool: Wet process bench

- Chemical : AZ 100 remover
- Time : 24 hrs
- IPA : 180 sec
- DI water : 180 sec

Appendix C

Process recipes for fabrication of CVD GFETs using e-beam lithography

Alignment marks lithography

Tool: RAITH150 Two

- Dehydration bake: 1 min at 170 ^{o}C
- First layer:
- Resist:495K PMMA A4

Table C.0.1: PMMA spin coating recipe

Step	RPM	Time(s)	Acceleration
Step1	300	10	150
Step2	1500	45	1000
Step3	0	10	112

- Prebake: at 180 ^{o}C for 300 sec
- Cooling: 5 min
- Second layer:
- Resist:950K PMMA A4

Table C.0.2: PMMA spin coating recipe

Step	RPM	Time(s)	Acceleration
Step1	300	10	150
Step2	4000	45	1000
Step3	0	10	112

- Prebake: at 180 ^{o}C for 300 sec
- Cooling: 300 sec
- Exposure parameters:
  - Acceleration: 20 KV
  - Aperture : 30 μ m
  - Dose: 150 uC/cm^2
  - Developer: MIBK:IPA:: 3:1
  - Development time: 30 sec
  - Stopper: 2-propanol (IPA) pure
  - Stopping time: 15 sec

Metallization

Tool: Cr/Au Thermal evaporator

- Metal: Cr/Au
- Thickness: 10 nm/100 nm

Lift-off

Tool: Wet process bench

- Lift-off solvent: Acetone
- Duration: 24 hrs.

Graphene transfer

Refer substrate cleaning and graphene transfer process mentioned appendix B

Graphene patterning lithography

Refer recipe used for marker lithography in appendix A for exfoliated graphene device fabrication

Etch mask metal deposition

Tool:TEBE

- Metal: Copper (Cu)
- Thickness: 40 nm
- Vaccum: 5x10^{-2} mbar

Lift-off

Tool: Wet process bench

- Lift-off solvent: acetone
- Duration: 24 hrs.

Graphene Patterning recipe

Tool: Plasma Asher

- O_2 gas flow: 45 sccm
- RF Power : 50 Watt
- Time : 110 sec

Copper etching

Tool: Wet process bench

- Chemical : Copper etchant
- time: 300 sec

Contact lithography

Tool: RAITH150 TWO

Spin coating recipe is same as one used for alignment marks lithography. During exposure, use 60 um aperture.

Metallization

Tool: Cr/Au Thermal evaporator
Deposit Cr/Au (10 nm/70 nm).

Lift-off

Tool: Wet process bench

- Lift-off solvent: Acetone
- Duration: 24 hrs.

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