Design and Optimization of Tunneling Field Effect Transistors for Low Power Applications

A thesis submitted in partial fulfillment of
the requirements for the degree of

Doctor of Philosophy

by

Hasanali G. Virani

Roll No: 07407303

Supervisor

Prof. Anil Kottantharayil

Department of Electrical Engineering
Indian Institute of Technology, Bombay
2011

To

My Wife and Children,

without whose unflinching support and many sacrifices I would not have been able to undertake this effort,

My Parents,

for supporting my pursuit of knowledge at all times since my childhood,

and

Other Family Members.

Abstract

The tunnel FET device is emerging as a promising candidate for the future device technology due to the low subthreshold slope and absence of short channel effects. However the poor ON currents acts as a serious deterrent to its practical use. We show that by using high-k spacer engineering, the ON current of sub 22 nm channel length tunnel FET is improved due to enhanced fringe field coupling through the thin high k spacer. We further extend this concept to dual-k spacer i.e. a spacer made up of low k and high k material, which represent a more realistic scenario.

The n-channel TFET is optimized using single high-k spacers. Using underlap structure and dual-k spacers, further optimization of n-channel TFET is done for different gate dielectric made of SiO_2, Al_2O_3 and HfO_2 with same EOT of 1.1 nm. A more realistic gate dielectric case of HfO_2 layer on SiO_2 layer is also studied. Similar improvement in ON current of p-channel TFET using high k spacer engineering and an underlap structure is also demonstrated for the above mentioned gate dielectrics.

The impact of increased device capacitance due to use of high-k spacer on circuit performance is evaluated. Using the optimized TFETs with dual k spacers, the static and dynamic circuit performance is analyzed. The static performance is evaluated using inverter and SRAM circuit. The dynamic performance is evaluated using inverter and ring oscillator circuit. Inverter simulation of the underlap TFET with dual-k spacer confirmed the device level optimization results.

We also show that the ON current of tunnel FET is affected by the the channel transport. When the tunneling generation rate is enhanced to reach ON current values of approximately few $\mu A/\mu m$, then the ON current becomes sensitive to the electron velocity in the channel. This is because, at large tunneling rates, the charge due to the generated electrons tends to modify the potential in the channel in such a way that limits the generation rate at the source. Such an electrostatic feedback decreases with increase in the electron velocity resulting into higher tunneling rate and ON current values.

Contents

List of Figures

List of Tables

List of Abbreviations

Al_2O_3	Aluminum oxide
BTBT	band-to-band tunneling
CMOS	complementary metal oxide semiconductor
CNT	carbon nanotube
CN-TFET	carbon nanotube tunnel field effect transistor
DD	drift diffusion
dec	decade
DG-nMOS	double gate metal oxide semiconductor field effect transistor
DG-nTFET	double gate n channel tunnel field effect transistor
DG-pTFET	double gate p channel tunnel field effect transistor
EOT	equivalent oxide thickness
FinFET	fin-shaped field effect transistors
GAA	gate all around
Ge	Germanium
GeOI	Germanium on insulator
HfO_2	Hafnium dioxide
hk	high k spacer
H-nTFET	hetero junction n-channel tunnel field effect transistor
LDD	lightly doped drain
lk	low k spacer
LUT	look-up table
MOSFET	metal oxide semiconductor field effect transistor
nMOSFET	n channel metal oxide semiconductor field effect transistor
nTFET	n channel tunnel field effect transistor
pMOSFET	p channel metal oxide semiconductor field effect transistor
pTFET	p channel tunnel field effect transistor
SG-nMOS	single gate metal oxide semiconductor field effect transistor
Si	Silicon
SiGe	Silicon Germanium
SiGeOI	Silicon Germanium on insulator
SiO_2	Silicon dioxide
SOI	Silicon on insulator
SS	sub-threshold slope
SSOI	strained Silicon on insulator
TFET	tunnel field effect transistor
ul	underlap
VLSI	very large scale integrated circuits

List of Symbols

ϵ_{si}	dielectric permittivity of Silicon
ϵ_o	dielectric permittivity of air
μ_e	mobility of electrons
μ_h	mobility of holes
k	dielectric constant
C_{d_ch}	depletion capacitance
C_{gd}	gate to drain capacitance
C_{gg}	gate capacitance
C_{gs}	gate to source capacitance
C_{if}	inner fringe capacitance
C_L	load capacitance
C_{of}	outer fringe capacitance
C_{ox}	gate oxide capacitance
E_G	forbidden bandgap
G_{b2bt}	band-to-band tunneling generation rate
I_D	drain current
I_{OFF}	OFF state current
I_{ON}	ON state current
K	Boltzman constant
L_G	gate length
N_D	drain doping
N_S	source doping
P_t	tunneling probability
q	electronic charge
T	Temperature
t_{Ge}	thickness of Germanium
t_{ox}	thickness of the gate oxide
t_{si}	thickness of Silicon
t_{SiGe}	thickness of Silicon Germanium
t_{SOI}	thickness of Silicon on oxide
t_f	fall time
T_p	time period
t_r	rise time
V_{DD}	supply voltage
V_{DS}	gate to drain voltage
V_{GS}	gate to source voltage
v_{sat}	velocity saturation
V_{TH}	threshold voltage

Chapter 1

Introduction

Silicon Complementary Metal Oxide Semiconductor (CMOS) has dominated the microelectronics industry over the last more than two decades. The concept of device scaling has been consistently applied over many technology generations to achieve low power, high speed, high packing density and low cost per unit function. The scaling of metal oxide semiconductor field effect transistors (MOSFETs) has been following the famous Moore's law which is often stated as the doubling of transistor performance and quadrupling of the number of devices on the chip every three years. Device dimensions have surpassed the micrometer scale and are now into the nanometer regime.

The continuous downward scaling to improve the performance of CMOS technology has reached the fundamental limits of material and fabricating technology. It is hindered due to various short-channel effects like drain induced barrier lowering, gate induced drain leakage, gate leakage and OFF state leakage current problems. A fundamental challenge to MOSFET scaling in the nanoscale regime is the non scalability of room temperature subthreshold swing (SS) [1] which limits the ratio of ON current (I_{ON}) to OFF current (I_{OFF}). This stems from the thermal injection mechanism responsible for the carrier injection from the source to channel in the MOSFET and SS is limited to 60 mV/dec at room temperature of 300 K. [2].

Novel device structures and material options are explored to overcome this hurdle and enhance performance. Advanced structures like the 3-D multiple-gate fin-shaped field effect transistors (FinFET) with very thin mesa [3, 4] and silicon-on-nothing [5] are proposed. The strong gate coupling results into SS which is close to the 60 mV/dec value at room temperature of 300 K. To achieve a sub 60 mV/dec subthreshold slope, Schottky barrier Tunnel FETs [6, 7], impact ionization MOSFETs [8, 9] and tunnel FETs (TFET) are proposed. The Schottky barrier Tunnel FETs have the problem of high leakage. Impact ionization MOSFET has the advantage of very low subthreshold slope ($<$ 10 mV/decade) [8], but faces severe reliability issues. The novel and simple device structure of the TFET is explored in this thesis.

1.1 Tunnel FET

The TFET is fast emerging as an attractive alternative to MOSFETs for the nanoscale regime. Since the current depends on band to band tunneling, the TFET exhibits SS less than 60mV/dec at T = 300 K. This permits low standby leakage currents and enables scaling of the supply voltage (V_{DD}) which has come to a crawl in the nanoscale regime. Most widely explored TFET structure is a gated p-i-n structure shown in Fig. 1.1. The structural similarity of this p-i-n structure to MOSFETs also offers the ease of fabrication using standard CMOS technology.

The TFET has many advantages over the MOSFETs, namely:

- Suitability for low standby power application due to lower subthreshold swing.
- Better scalability compared with MOSFETs.
- Unlike MOSFETs, the tunneling effects enhance the performance of TFETs.
- Much lower V_T rolloff as V_T depends on the smaller tunneling region and not on the entire channel.
- Channel region is intrinsic thereby suppressing the V_T fluctuations caused due to random distribution of dopant atoms.

1.2 Scope of the Present Work

Although the earliest TFET transistor proposed was way back in 1987, most of the research in TFET has been reported from 2000 onwards. This is because as the performance improvements by scaling of CMOS started diminishing, interest in TFET as an alternate device technology gained momentum. Since TFET is a relatively new device, many issues need to be sorted out before it becomes a mature technology which is commercially viable. After Reddick et al. [10] published paper on lateral TFET and Bhuwalka et el. [11] published paper on vertical TFET, there has been many reports on fabricated TFET and their variants. Most of these lateral TFETs use Silicon on insulator (SOI) substrate and vertical TFET including silicon nanowire use bulk substrate. The detailed description of these are covered in chapter 2.

Even though TFETs have been experimentally demonstrated with superior SS and subthreshold leakage compared to MOSFETs of comparable gate length, the ON state current remains significantly low, especially for silicon TFETs [2, 12, 13]. Also sharp doping profile [14] along with high source doping concentration [15, 16] is very important for the obtaining high performance TFET.

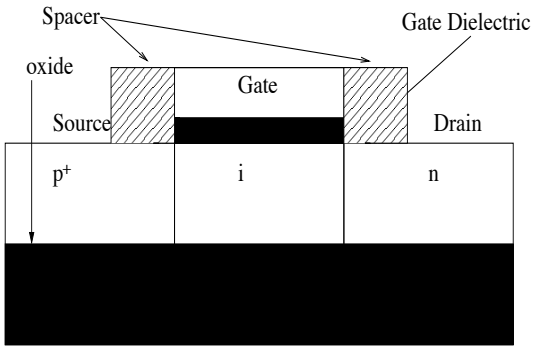


Figure 1.1: Schematic of gated p-i-n TFET structure built on SOI substrates.

In order to replace CMOS technology with TFET device, both n channel TFET (nTFET) and p channel TFET (pTFET) need to be optimized in order to achieve performance comparable to n-channel MOSFET and p-channel MOSFET respectively. The present work deals with various aspects of device design and optimization of TFETs with extensive device simulations. The performance improvement is also evaluated at circuit level with mixed mode simulations.

To increase the I_{ON} of the TFET, innovative solution involving use of high k spacer and dual k spacers are proposed for decreasing the barrier width. Use of high k material in spacers increases the I_{ON} without affecting the I_{OFF} whereas the use of high k material in gate dielectric increases the I_{ON} along with an increase in I_{OFF}. The performance improvement is studied for various gate dielectric namely silicon oxide (SiO_2), Aluminium oxide (Al_2O_3) and Hafnium oxide (HfO_2). A more realistic gate dielectric case of HfO_2 layer on SiO_2 layer is also studied. An underlap TFET structure with dual k spacer is presented for the first time which gives further improvement in I_{ON}.

The effect of high k spacer on the device capacitances of TFET were studied and fringe capacitances were extracted. Finally to evaluate the performance improvement at circuit level, mixed mode simulation of inverter and ring oscillator were done. The analysis of circuit performance improvement was also done using results of Look-Up Table (LUT) based simulations of inverter, ring oscillator and SRAM cell.

As the tunneling generation rate increase with application of various technology boosters, the impact of the channel transport on I_{ON} becomes significant. Hence the channel transport in TFET was studied. Unlike in MOSFET, the drain side field is low in TFET. This results into carrier accumulation near the drain spacer thereby modifying the channel potential in such a way that generation rate reduces. This type of electrostatic feedback effect reduce with increase in saturation velocity. As a result the I_{ON} improves with increase in velocity saturation.

1.3 Organization of the Report

The report is organized into the following chapters. In chapter 2, a literature survey on TFETs is presented. The chapter 3 gives the design considerations and details of the simulation setup. Chapter 4 covers the optimization of TFET with single high k spacers. Chapter 5 covers the optimization of silicon TFET with dual k spacers. Chapter 6 covers the study of device capacitances in the optimized TFET. Chapter 7 contains the results of the circuit simulation using the optimized TFETs. Chapter 8 covers the channel transport in TFET. Conclusions are drawn in Chapter 9.

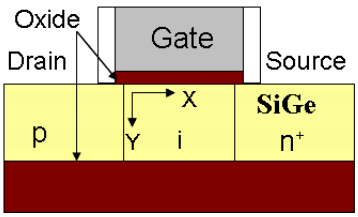
Chapter 2

Literature Survey on Tunnel FETs

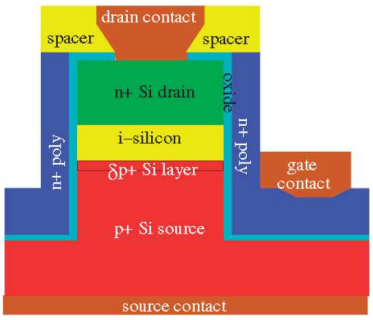
2.1 History of Tunnel FET

In 1965, the first TFETs were discussed in the literature as parasitic devices in early MOSFET technology [17]. In 1987, Banerjee et al. [18] proposed for the first time that the TFET could be a potential candidate to replace MOSFETs in VLSI applications. Banerjee et al. observed a zener effect in a trench transistor cell used in Texas Instruments DRAM. From this observation they fabricated a three terminal MOS tunneling device. Takeda et al. [19] proposed the band to band tunneling MOSFET which uses the band to band tunneling (BTBT) effect in the gate-drain overlap region to operate the device. Baba et al. and Uemura et al. [20, 21] proposed the first gated p-i-n TFET structure named as surface tunnel transistor in III-IV compound material. Reddick et al. [10] and Koga et al. [22] demonstrated the lateral interband tunneling in silicon tunnel transistor. The TFETs were later demonstrated in vertical gated p-i-n diode grown by molecular beam epitaxy [23, 24]. Royer et al. and Mayer et al. [25, 26] demonstrated TFET implemented using Silicon on insulator (SOI), Silicon Germanium on insulator (SiGeOI) and Germanium on insulator (GeOI). Fulde et al. [12] have reported experimental results of double gate nTFET (DG-nTFET) with FinFET structure. Recently TFET has also been implemented in novel materials like Carbon Nano-Tube (CNT) [27] and graphene ribbon [28]. Bjork et al. [29], Chen et al. [30] and Moselund et al. [31] have reported experimental results of silicon vertical nanowire. Some of the common architectures of TFET implemented in literature are shown in Fig. 2.1 including nanowire TFET [32].

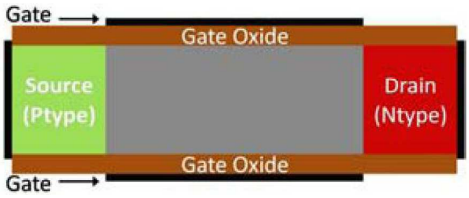
Recently Koswatta et al. [33] have presented a comparative simulation study of CNT TFET with conventional MOSFETs where it is reported that TFETs can exhibit faster switching at larger I_{ON}/I_{OFF} ratios as smaller amount of charge needs to be provided to the channel. Landsiedel et al [34] have also compared TFET with MOSFETs and proposed circuits with a mix of TFETs and MOSFETs thereby projecting TFETs as promising candidates for future low standby power applications.



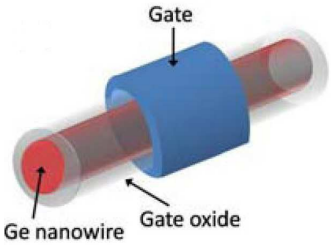
(a) Lateral Tunnel Transistor in SOI[35]



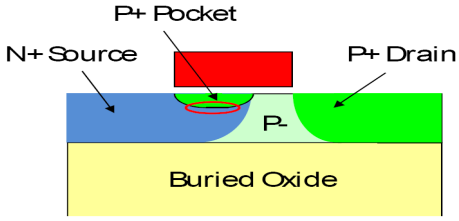
(b) Vertical Tunnel FET [23]



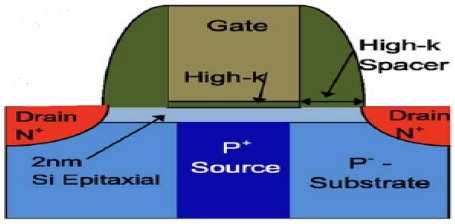
(c) DG-Tunnel FET [36]



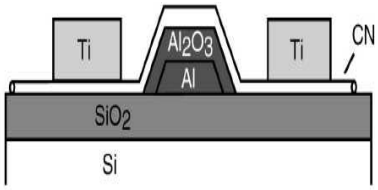
(d) Nanowire Tunnel FET [36]



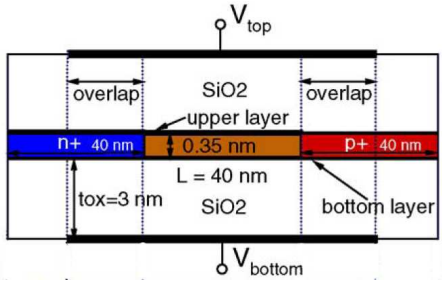
(e) Green TFET [37]



(f) Sandwich Tunnel Barrier FET [38]



(g) CNT Tunnel FET [27]



(h) Graphene ribbon Tunnel FET [28]

Figure 2.1: The commonly encountered architectures of TFET in literature.

2.2 Principle of Operation of TFET

As illustrated in Fig. 1.1, a nTFET is a three terminal device with a p^+ doped source and n doped drain. A pTFET has similar structure with a n^+ doped source and p doped drain. The channel is intrinsic for both nTFET and pTFET. Fig. 2.2 shows the band diagram of both the nTFET and pTFET under different bias conditions. Due to the application of positive gate bias, the bands in the channel are bend downwards for nTFET. Conversely, due to the application of negative gate bias, the bands in the channel are pulled up for pTFET. With sufficient magnitude of gate bias, the filled valence band states aligns with the empty conduction band states resulting into flow of the band to

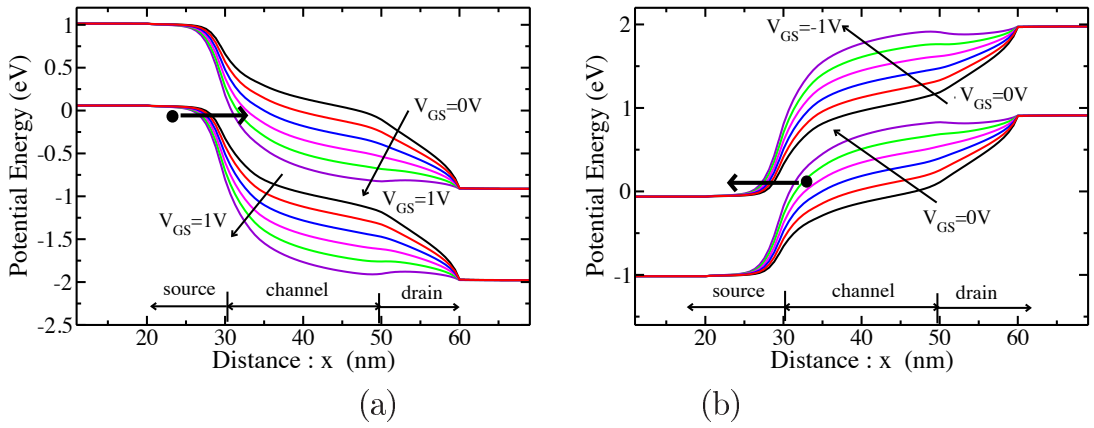


Figure 2.2: Band diagram of TFET for various gate bias. (a) nTFET (V_{DS} = 1 V) and (b) pTFET (V_{DS} = -1 V).

band tunneling (BTBT) currents. In nTFET, the electrons tunnel from source to channel and are transported through the channel to the drain. In pTFET, electrons tunnel from channel to source, the resultant holes in channel are transported through the channel to the drain. The I-V characteristic of the nTFET and pTFET are shown on Fig. 2.3 and Fig. 2.4 respectively.

The computation of the electrical parameter of threshold voltage (V_{TH}) and SS have been described by Bhuwalka et al. [23]. They have used the constant current method in determining the V_{TH}. This approach has been used in majority of the published papers. The SS is defined as the average of SS computed at every decade from V_{TH} to I_{OFF}.

In addition to the low BTBT currents in TFET, the other drawback of this device is the exponential nature of the output characteristic as seen in Fig. 2.3(b) and 2.4(b). Shen et al. [39] have explained this exponential nature and saturation of the output characteristic

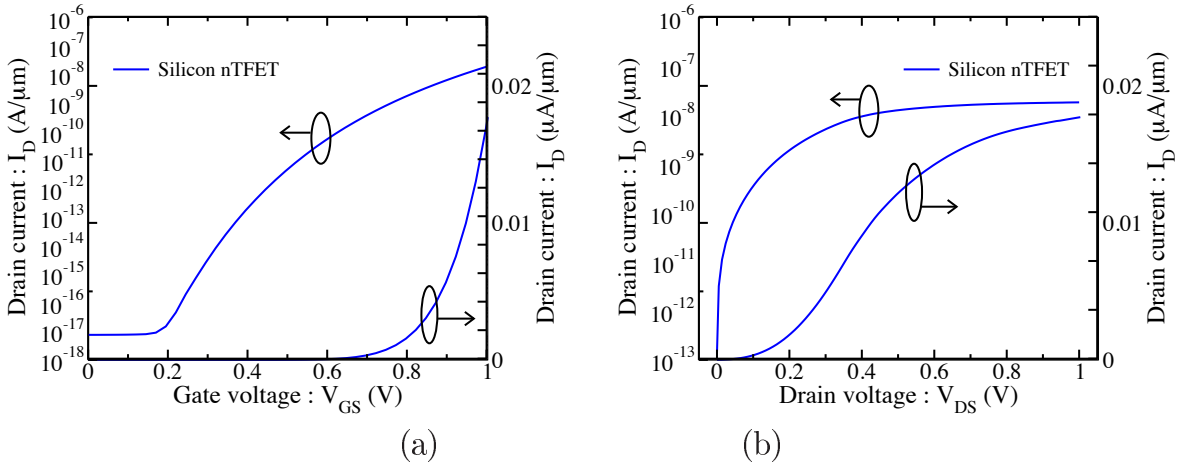


Figure 2.3: (a) The I_D-V_{GS} characteristic at V_{DS} = 1 V and (b) the I_D-V_{DS} characteristic at V_{GS} = 1 V for nTFET.

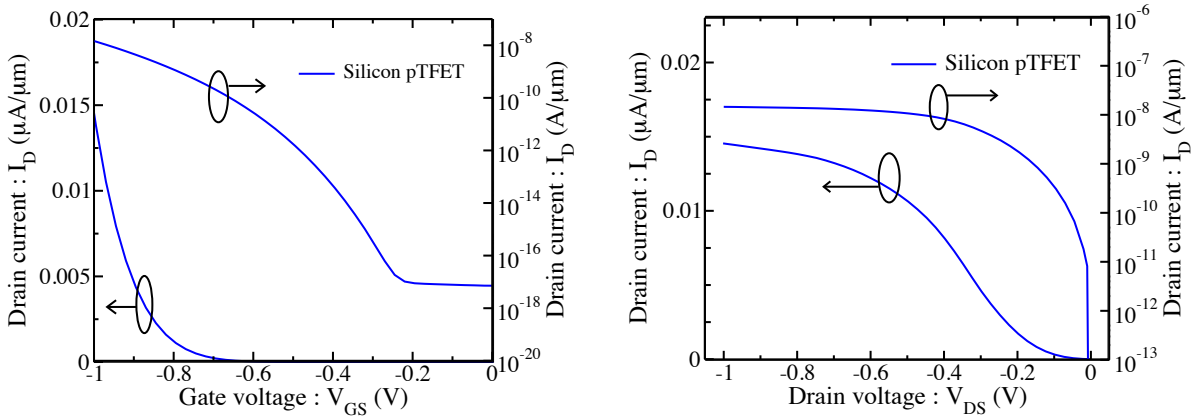


Figure 2.4: (a) The I_D-V_{GS} characteristic at V_{DS} = -1V and (b) the I_D-V_{DS} characteristic at V_{GS} = -1 V for pTFET. Magnitude of I_D is ploted on the Y-axis.

of TFET. At V_{DS}=$V_{DD}/2$, the V_{GD} is high, resulting into inversion carrier near the drain. The conduction band in the channel can not be much lower than that in the drain due to the large amount of inversion electrons. Hence, the E_c in channel is effectively pinned by the drain voltage. This limits the rise of the tunneling currents at lower V_{DS} giving the exponential nature of the output characteristic. However at high V_{DS}, the V_{GD} reduces and inversion charge starts reducing thereby permitting full band bending at the source -channel junction and the output characteristic goes into saturation. More discussions on nTFETs and pTFETs are given in section 2.4 and section 2.5 respectively.

Koswatta et al. [40] have shown that the output characteristic improve by use of broken gap structure in gate all around CNT TFET. The improvement in exponential nature at low V_{DS} part of output characteristic, also referred as "dead zone", can greatly improve the switching characteristic of TFET. Ashish Pal et al. [41] also suggest that to improve circuit performance of TFETs, just optimizing the I_{ON} is not sufficient. The output characteristic should also be improved.

2.3 Physical Models used for Band to Band Tunneling

The Kane's model [42] implemented in MEDICI has been widely used in the earlier published papers [11, 23, 35, 37, 43–48]. This models assumes a triangular tunneling barrier. It uses the local electric field at beginning of the tunneling path (point A in Fig. 2.5) and assumes this field to be uniform throughout the tunneling path. It therefore computes smaller tunneling distances ($W_{T-local}$) as seen in the illustration given in Fig. 2.5. This results into an over estimation of the tunneling currents. Hence the simulated currents in the reported work [15, 37, 45, 47, 48] were greater in magnitude than the experimentally reported tunneling currents [12, 25, 26, 29, 49, 50] .

If the entire potential profile along the tunneling path is taken into account, then the

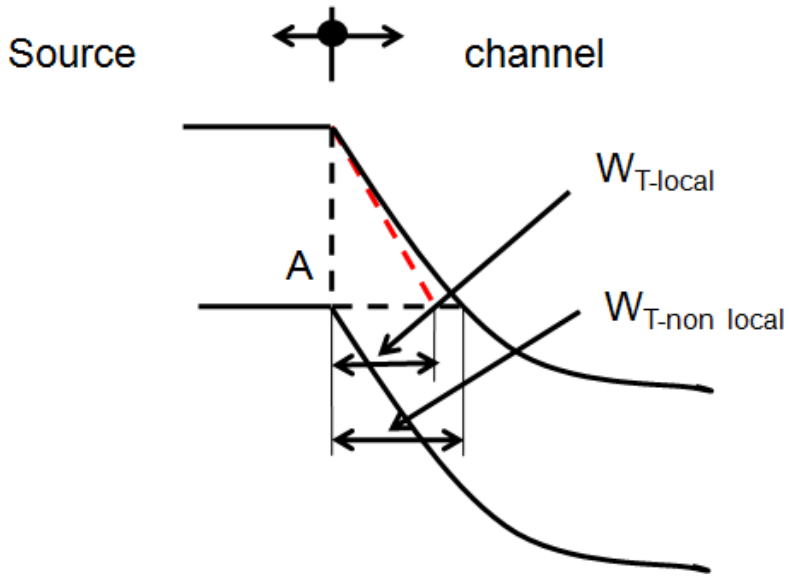


Figure 2.5: The local model for band to band tunneling computes smaller tunneling width ($W_{T-local}$) as compared to that of non local model ($W_{T-nonlocal}$).

tunneling distance ($W_{T-nonlocal}$) computed is larger (Fig. 2.5) giving a more accurate representation of the BTBT currents. In 2009, this approach of computation was implemented as the non local model for tunneling in SENTAURUS TCAD suite and also in SILVACO TCAD suite. Hence, research work reported from 2009 onwards extensively uses this non local model.

Table 2.1 indicate the vast differential in the reports of the simulated tunneling currents of nTFET. The experimental values are also shown in this table. This is because of the use of non calibrated models and use of local tunneling models which over estimates the tunneling currents. Further details of these two models are explained in chapter 3.

2.4 N-channel Tunnel FETs

Although TFETs have been experimentally demonstrated with superior SS and sub-threshold leakage compared to MOSFETs of comparable gate length, the ON state current remains significantly low, especially for silicon TFETs [12, 13, 51].

Drain current in nTFET is due to the tunneling of valance band electrons from the source to the conduction band of the intrinsic channel region. This tunneling current depends on the height and the width of the tunnel barrier. Various techniques for enhancing the ON state current, theoretically studied in the literature, can be classified into two categories namely:
(i) tunnel barrier height engineering and
(ii) tunnel width engineering.

Table 2.1: Comparison of results of n-channel TFETs reported in the literature.

Ref	structure	Exp. (E) Sim. (S)	model	L_G (nm)	t_{ox} (nm)	V_{DS} (V)	V_{GS} (V)	I_{on} (μA/μm)	SS (mV/dec)
[2]	lateral SOI	E	-	70	4.5(SiO_2)	1	5	~0.5	-
[13]	lateral SOI	E	-	70	2(SiO_2)	1	1	1.21	52.8
[25, 26]	lateral GeOI	E	-	400	3(HfO_2)	0.8	2	1	-
[30]	Si nanowire	E	-	200	4.5(SiO_2)	1.2	1.5	53	~70
[49]	gated Si p^+-n diode	E	-	50	4(SiO_2)	-3	3	0.002	≈50
[50]	DG TFET (strained Ge channel)	E	-	1000	-	3	4	300	~ 50
[52]	Ge source	E	-	5000	3(SiO_2)	0.5	0.5	0.42	13
[53]	$In_{0.53}Ga_{0.47}As$ TFET	E	-	100	10(Al_2O_3)	0.75	2.5	20	-
[15]	Ge TFET	S	L	50	5(HfO_2)	1.2	1.2	1800	~30
[16]	Si DGTFET	S	L	100	3(HfO_2)	1	1.5	~140	52
[35]	$Si_{0.5}Ge_{0.5}$ source	S	L	20	1(SiO_2)	1	1.2	300	27
[36]	Ge nanowire	S	L	100	2(SiO_2)	1	1.5	800	~12.5
[37]	p^+pocket-doped source	S	L	40	1(EOT)	1	1	776	-
[44]	Si DGTEFT	S	L	100	6(HfO_2)	1	3	~300	-
[45]	$Si_{0.3}Ge_{0.7}$ source	S	L	100	2(SiO_2)	1.2	1.2	580	13
[46]	n^+pocket-doped channel	S	L	100	2.5(-)	1	1	~850	~40
[47]	$Si_{0.8}Ge_{0.2}$ DGTFET	S	L	53	3(HfO_2)	1.2	1.2	800	32.4
[54]	$Si_{0.5}Ge_{0.5}$ source	S	L	100	2(SiO_2)	1	2	800	~50
[55]	Si TFET	S	L	50	2(k=100)	1	2	730	36
[56]	n^+pocket-doped channel $Si_{0.2}Ge_{0.8}$ source	S	L	90	2.5(-)	1	1	~250	~40
[57]	$Si_{0.5}Ge_{0.5}$ source	S	L	70	1.5(SiO_2)	1	1.2	120	20
[58]	InAs DGTFET	S	NL	30	2(SiO_2)	0.25	0.25	~100	-
[59]	Si DGFET	S	NL	30	2.5(HfO_2)	1	1	~100	-
[60]	Si DGFET	S	NL	50	3(HfO_2)	1	1.6	~1500	15
[61]	Si DGFET	S	NL	50	1(EOT)	1	1.2	~800	-
[62]	Strained Si DGTFET	S	NL	50	3(-)	1	1.75	~1000	-
[63, 64]	Strained Si DGTFET	S	NL	50	1.2(SiO_2)	1	1.2	220	-

L $\longrightarrow$ Local model, NL $\longrightarrow$ Non local model

2.4.1 Tunnel Barrier Height Engineering

Tunnel barrier height can be lowered by using a lower bandgap semiconductor for the entire structure or for a particular region in the device (hetero junction TFET) [11, 15, 27, 35, 36, 45, 47, 48, 58, 65–67]. As illustrated in Fig. 2.6, when lower bandgap material E_{G2} is used in place of the larger bandgap material E_{G1}, the tunneling barrier height reduces. These decreases the tunneling width for a given V_{DD}, thereby yielding larger tunneling currents.

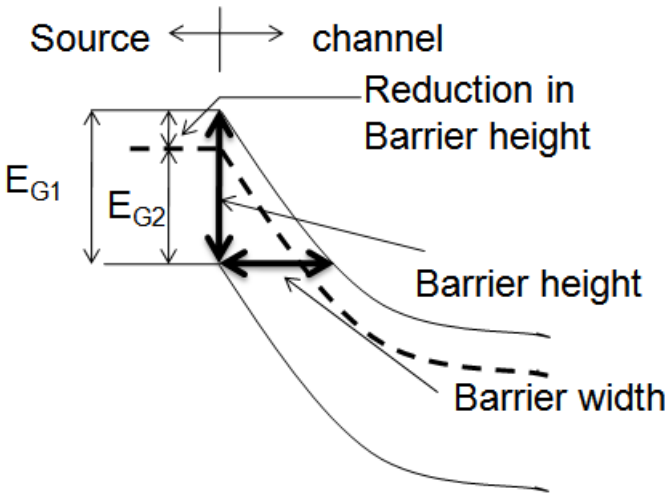
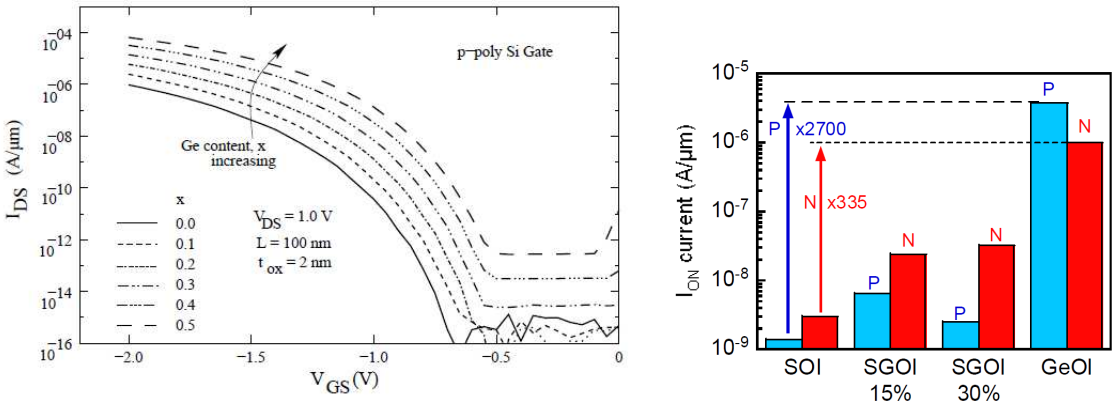


Figure 2.6: Reduction in tunneling barrier height. E_{G1} and E_{G2} are forbidden bandgap of material 1 and material 2.

2.4.1.1 Low Bandgap Material TFET

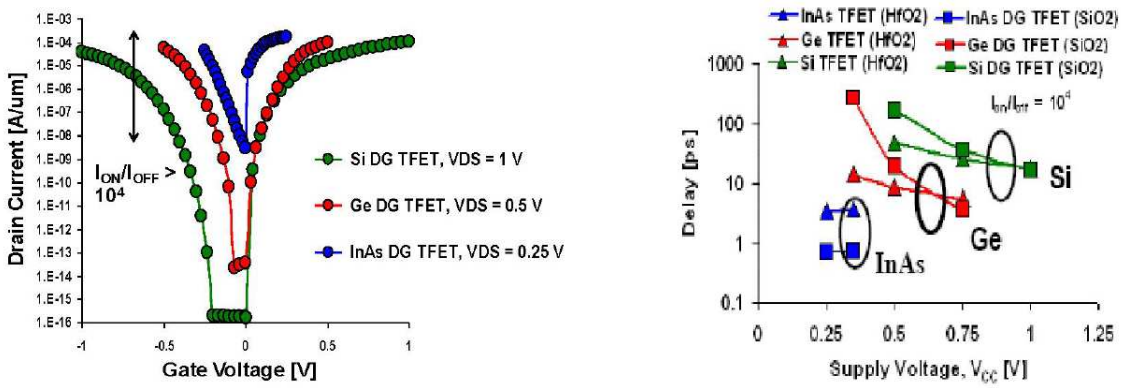
K. K. Bhuwalka [2] has presented simulated results of use of SiGe in vertical nTFET. He has shown that as Ge mole fraction (γ) increases the I_{ON} increases with increase in I_{OFF}. Nikam et al. [35] have shown similar simulation results using $Si_{0.5}Ge_{0.5}$ for complete TFET on SiGeOI.

Toh et al. [15] and Woo et al. [48] have compared the Si TFET with Ge TFET in a simulation study. Jain et al. [36] have simulated germanium p-i-n TFETs in the single (SG), double (DG), and nanowire gate-all-around (GAA) geometry and shown that GAA structure gives maximum I_{ON} due to the superior electrostatic control. Zhang et al. [14] have used gated n^+-p^+ Ge TFET on 2 nm GeOI. Kim et al. [52] have reported



(a) (b)

Figure 2.7: Simulated I_D-V_{GS} of nTFET (a) for Ge mole fraction variation from 0 to 0.5 [2] and (b) Extracted TFET ON current (at $V_{DS} = \pm 0.8$ V, $V_{GS} = \pm 2$ V) for 400 nm gate length TFETs on $Si_{1-x}Ge_xOI$ (x_{Ge} = 0-15-30%, t_{SiGe} = 20 nm) and GeOI (t_{Ge} = 60 nm) substrates (in p & n modes) [25].



(a) (b)

Figure 2.8: (a) Simulated I_D-V_{GS} of TFET made up of Si, Ge and InAs. (b) Intrinsic gate delay as a function of power supply for Si, Ge and InAs. Narrow bandgap semiconductor allows the scaling of power supply to 0.25 V while simultaneously lowering the intrinsic gate delay [69].

experimental results of high I_{ON}/I_{OFF} ratio (10^6) for low-voltage (0.5 V) operation using Ge nTFET. Junghyo Nah et al. [68] have shown that by using flash-assisted rapid thermal process (fRTP) for dopant activation, an abrupt type profile can be achieved in Ge nanowire. This gives improvement of I_{ON} by an order of magnitude. Mayer et al. [25] and Royer et al. [26] have demonstrated a TFET on SOI, SiGeOI and GeOI wafer and have experimentally proved that there is an improvement in ON current as the band gap of the material used is reduced. This experimental study uses upto 0.3 Ge mole fraction. This is because although the simulation results discussed above uses upto 50% of Ge in SiGe, integrating the same in the CMOS fabrication process is a technology challenge. A bar graph showing this comparison is shown in Fig. 2.7. A comparative simulation study between Si, Ge, InAs materials for TFET has been done [32, 58, 67, 69] and it has been shown that use of InAs and Ge have a clear advantage in terms of switching performance as well as in the delay reduction as the device power supply is progressively scaled (Fig. 2.8). Mookerjea et al. [53] have reported experimental results of $In_{0.53}Ga_{0.47}As$ TFET with 100 nm channel length and high-k metal gate stack with high I_{ON}/I_{OFF} ratio (10^4). Due to small bandgap, high I_{ON} of 20 μA/μm was obtained.

Novel materials like the carbon nano tube and graphene ribbon are also used as low band gap material. Carbon nanotubes (CNTs) are candidate materials for future integrated circuits owing to their unique properties including 1-D near-ballistic transport, high mobility for both electrons and holes, chemical robustness, lack of surface dangling bonds and sustained electrical properties when integrated into realistic device structures. Appenzeller et al. [27] have reported the experimental and simulation results of a dual gated carbon nanotube TFET (CN-TFET). Koswatta et al. [65] have made a simulation study of 20 nm gate length CN-TFET (E_G = 0.8 eV) with high-k gate (HfO_2) of 2 nm

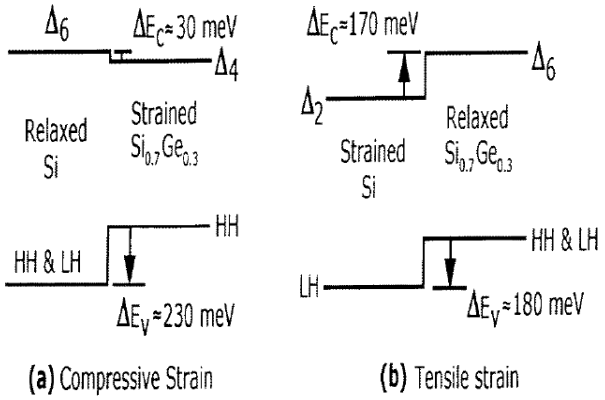


Figure 2.9: (a) Band alignments between Si and $Si_{0.7}Ge_{0.3}$ on two substrates: (a) Si (Type I staggered junction) and (b) $Si_{0.7}Ge_{0.3}$ (Type II staggered junction) [73].

thickness. Zhang et al. [70] have discused the fabrication methodology for CN-TFET and demonstrates a 25 mV/dec subthreshold swing. Poli et al. [66] have done the scaling study of CN-TFET. The CN-TFET simulations in literature has been performed using the non equilibrium Green's function formalism for a sub 1 V power supply. Knoch et al. [71] have shown that, one-dimensional systems of CN-TFET offer the possibility to combine a high ON-state performance with steep inverse subthreshold slopes.

Fiori et al. [28] have shown that for graphene TFET, I_{ON}/I_{OFF} ratios of 10^3 can be obtained for an ultra low V_{DD} of 0.1 V. Luiser et al. [72] have shown that the performance of graphene TFET is limited by the line edge roughness (LER). The I_{OFF} increases due to LER and I_{ON}/I_{OFF} ratio gets limited.

Although the tunneling currents improve by use of the above technology boosters, the introduction of Ge, III-V compounds, carbon nanotube and graphene ribbon in VLSI technology remains a significant challenge.

2.4.1.2 Hetero Junction TFET

Using the low bandgap material for the entire TFET implementation has the drawback of increase in I_{OFF} which is mainly due to the thermal generation of carriers in the intrinsic channel region. Workfunction engineering can be used to reduce I_{OFF}, but this tends to also reduce the I_{ON} for a given V_{DD}. Hence to control the increase in I_{OFF} without sacrificing the improvement achieved in I_{ON}, hetero structures made up of a combination of low band gap and high band gap material are used. Usually the source is made of low bandgap material while the channel and drain are made of high bandgap material. Since the bandgap of channel is now larger, I_{OFF} do not increase. Growing a SiGe structure on relaxed silicon results into type I staggered hetero junction shown in Fig. 2.9(a) and has been used in most of the following literature studies. The valence band discontinuity is large and the conduction band discontinuity is small. Thus using this hetero junction

in TFET reduces the tunneling height. Bhuwalka et al. [11] have used a δp^+ layer of SiGe between source and channel to create a hetero junction and improve I_{ON} of vertical TFET using device simulation. Fabricating such a small layer in lateral TFET is difficult, hence the full source made of SiGe or Ge is used in most of the literature study for planar TFET.

Nikam et al. [35] have studied nTFET with SiGe source for various values of Ge mole fraction using device simulation. His work predicts that the hetero junction TFETs (H-TFET) can satisfy ITRS HP and LSTP specifications by an appropriate choice of Ge fraction, EOT and work function. Patel et al. [45] have reported simulation study of Si/SiGe H-TFET wherein only the top layer of source is made up of SiGe. They predict that the BTBT generation rate is maximum at the surface and extends upto 20 nm depth. Hence the optimal thickness of this top level needs to be 20 nm which gives performance similar to a full source made of SiGe. This reduced thickness of SiGe layer would reduce the strain on the channel which can increase/decrease the mobility in the channel (study not presented and effect of strain on Si due to SiGe source is not considered). Toh et al. [47] have reported simulated I_{ON} of 800 $\mu A/\mu m$ for double gate H-TFET with $Si_{0.8}Ge_{0.2}$ source. Verhulst et al. [74] have shown the improvement in I_{ON} by using low band gap material in the source of nTFET using analytical calculations.

Yoon et al. [75] have shown that the carbon hetero-junctions could provide much larger I_{ON} compared to homo junction CN-TFETs due to the effective small bandgap for the injected carriers.

Koswatta et al. [40] have used a broken gap CN-TFET to boost the I_{ON} of CN-TFET in his simulation study and showed that the performance is better than hetero junction and homo junction TFETs. Konch et al. [76] have suggested the use of III-V compound semiconductors (InAs/$Al_xGa_{1-x}Sb$ hetero junction nanowire) to obtain type II hetero-interfaces with a staggered or even broken band line-up. Bjork et al. [77] have fabricated Si/InAs hetero junction p-n diode and demonstrated boost in the tunneling currents. A broken line-up is particularly attractive since in this case the BTBT barrier tends to zero and optimal device performance can be expected. Luiser et al. [78] have compared TFET made of InSb, Carbon, and GaSb-InAs Broken Gap hetero structures using an atomistic and full-band quantum transport solver. The performances of 2-D single-gate and double-gate devices as well as 3-D gate-all-around structures has been presented. Graphene nanoribbons, carbon nanotubes, and InSb transistors exhibit too low ON-currents and poor performances compared to GaSb-InAs hetero structures. However, carbon-based TFETs can operate at lower supply voltages (0.2 V) than the III-V semiconductors.

Although Ge mole fraction of 0.3 [79] and 0.4 [49] are currently integrated in CMOS technology , Ge mole fraction required in TFET source to achieve drive currents competitive to state of the art CMOS devices is predicted to be 0.6 or higher [35, 45]. Fabricating SiGe mole fraction greater than 0.4 remain a significant challenge.

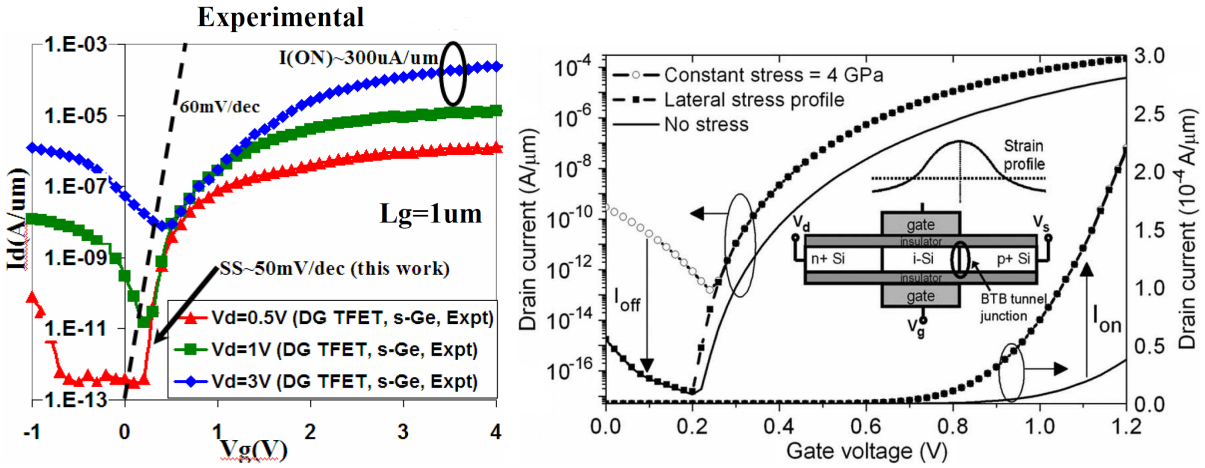


Figure 2.10: (a) Experimental I_D-V_{GS} of strained germanium nTFET [50]. (b) Simulated I_D-V_{GS} of strained silicon nTFET [63].

2.4.1.3 Strained TFET

Nayfeh et al. [49] have reported experimental results of strained $Si_{0.6}Ge_{0.4}$ diodes. Using this results, they have further done a simulation study of strained staggered type II H-TFET [80]. Since conduction band discontinuity is also large for staggered II hetero junctions as seen from Fig. 2.9, less gate bias is required for channel band bending thereby improving the I_{ON} for a given V_{DD}.

Krishnamohan et al. [50] have experimentally demonstrated a double-gate (DG), strained-Ge, H-TFET exhibiting very high drive currents and SS $\leq$ 60 mV/dec. Due to small bandgap of Ge and the electrostatics of the DG structure, record high drive current of 300 μA/μm along with a subthreshold slope of 50 mV/dec has been reported (Fig. 2.10(a)). Guo et al. [81] have performed experimental studies on the effect of strain on DG-nTFET by applying mechanical stress along the [110] direction of the wafer strip using a four-point wafer bending tool. They reported that the bandgap narrowing due to uniaxial tensile stress leads to I_{DS} enhancement and uniaxial compressive stress reduces I_{DS}.

Saurabh et al. [62] have reported simulated results of strained DG-nTFET using single-layer strained-silicon-on-insulator (SSOI) technology. SSOI is a novel SiGe-free material system that has the advantages of strained silicon while improving the scalability of thin-film SOI. The amount of strain in an SSOI is controlled by varying the mole fraction of Ge in the relaxed SiGe buffer layer that is used during its fabrication. Due to uniform strain throughout the device, the I_{ON} improves along with increase in I_{OFF}. To overcome this increase in I_{OFF}, Boucart et al. [63, 64] have proposed the use of Gaussian type of non uniform profile for strain on nTFET with the maximum strain at the source-channel tunneling junction (Fig. 2.10(b)). Pratik et al. have used strained Si over Ge to improve

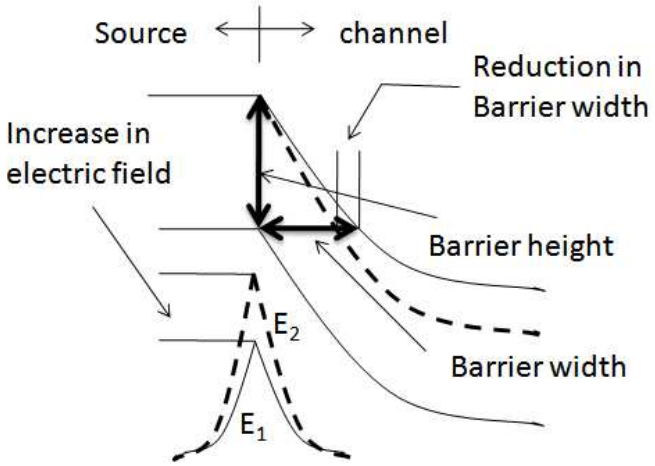


Figure 2.11: Reduction in tunneling barrier width when the electric field at the source-channel junction is enhanced from E_1 to E_2.

currents for the novel TFET structure with bubble doping below the source-gate overlap [82]

Using self-consistent quantum transport simulations, Yang Lu at al. [83] have shown that with local strain applied at the tunneling junction between the source and the channel in a graphene nanoribbon tunneling FET, the on-current can be significantly improved by over a factor of 10 with the same off-current.

2.4.2 Tunnel Barrier Width Engineering

The second option to enhance drain current is tunnel width engineering. This is achieved by increasing the electric field at the source-channel junction say from E_1 to E_2

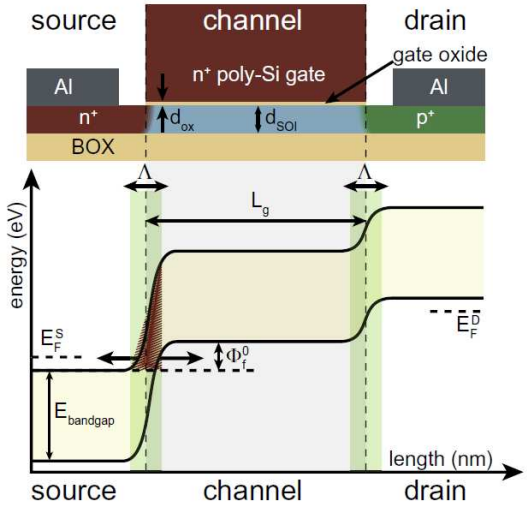


Figure 2.12: Structure of a TFET on SOI substrate and the band profile along current transport direction. The extent of the tunneling barrier is given by Λ, the screening length for potential variations. The barrier is approximated by the hatched triangular shape. [84].

as illustrated in Fig. 2.11. The width of the tunneling barrier is described by the natural length scale for potential variations [76, 84] as shown in Fig. 2.12.

$$\Lambda = \lambda_{dop} + \lambda_{ch} \tag{2.1}$$

where λ_{dop}, the screening length in the source is given by the Debye-length

$$\lambda_{dop} = \sqrt{\frac{\epsilon_0 \epsilon_{si} KT}{q^2 N_D}} \tag{2.2}$$

and λ_{ch} is the length in the channel region resulting from a parabolic expansion of the vertical potential distribution [85] given by

$$\lambda_{ch} = \sqrt{\frac{\epsilon_{si}}{\epsilon_{ox}} t_{SOI} t_{ox}} \tag{2.3}$$

Hence using heavily doped source will reduce the λ_{dop} and reducing the oxide thickness t_{ox}, SOI body thickness t_{SOI} and increasing gate dielectric constant ϵ_{ox} would reduce λ_{ch}. This enhances the p-i junction electric field, reduces the tunneling width and increasing the current.

2.4.2.1 Gate Dielectric Scaling

Boucart et al. [86] and Toh et al. [47] have used 3 nm of HfO_2 to boost the ON current of double gate TFETs using simulations. Specifically Toh et al. reported that ITRS specifications for I_{ON} can be met using double gate tunnel FETs down to gate length of 10 nm. However the EOT corresponding to the dielectric layer used by them is very small ($\sim$ 0.5 nm). Nikam et al. [35] have reported an improvement of $\sim$ 5 times in ON currents as gate dielectric EOT is scaled from 1.8 nm to 0.8 nm [35].

Use of high k gate dielectric material to increase ON currents results in increase of OFF currents. To resolve this issue, Mahdi et al [87] have proposed a dual k gate dielectric structure to reduce OFF currents. The high k dielectric at the tunneling junction increases the ON current while the low k dielectric over the rest of the channel keeps the OFF state current under control. But integrating this dual k gate dielectric into VLSI process flow increases the fabrication complexity and cost. Choi et al. [88] have also proposed a similar dual-k gate structure and shown that I_{OFF} and ambipolarity reduces. Saurabh et al. [89] have shown that using similar dual-k gate with strained DG-TFET, the output characteristic and average SS is improved. Ning Cui et al. [90] have used a hetero metal gate (dual workfunction gate) with HfO_2 gate dielectric to improve the I_{ON} and SS of nTFET.

2.4.2.2 Realization of Devices on Ultra Thin SOI

Aydin et al. [43] have reported experimental results using Si TFET with 40 nm SOI film thickness with $I_{ON} \sim 1\ \mu A/\mu m$ for V_{DS}=1.8 V and V_{GS}=5 V. Zhang et al. [14] have reported simulated I_{ON} of 440 $\mu A/\mu m$ for 2 nm GeOI n^+-p^+ gated TFET. Luisier et al. [91] have studied a 5 nm thin body $In_xGa_{1-x}As$ TFET using an atomistic, full-band quantum transport simulator based on the nearest neighbor sp^3d^5s tight binding method with spin-orbit coupling and self-consistent solutions of 2-D Schrodinger and Poisson equations.

Although technologies for ultra thin SOI and source-drain doping engineering are extensively being developed for aggressive scaling of VLSI technology, these techniques themselves are not adequate to obtain target I_{ON} for the future requirements [92].

2.4.2.3 Non-Overlap Structure

These structure uses an underlap between the gate and drain to reduce the OFF state currents and control the ambi polarity in TFETs [25, 26, 44, 50]. The I_{ON} is not affected by drain side underlap. These structures would improve the I_{ON}/I_{OFF} ratio but has the disadvantage of increasing the layout area of the device.

Poli et al. [66] have proposed the use of 1 nm source/drain to gate underlap to enhance ON current of CNT TFET with 3.2 nm HfO_2 gate dielectric and metal gate. However there is no mention of the spacer used and the gate dielectric covers the entire CNT tube. Chattopadhyay et al. [61] have predicted that a source/drain to gate underlap TFET with high k spacers improves the I_{ON}. These underlap structures offers an interesting compromise between layout density and parasitic capacitance.

2.4.2.4 Fringe Field Effects of High k Dielectric

Wang et al. [93] have explored the design consideration of TFET using III-IV compound semiconductors for ultra low power applications (0.3 V). When the gate is perfectly aligned to the tunneling junction (Fig. 2.13), a fraction $C_{ox}/(C_{ox} + C_{d\_ch})$ of V_{GS} gets translated in change in conduction band energy. C_{ox} is the oxide capacitance and C_{d_ch} is the depletion capacitance of the channel. An Intrinsic channel would provide maximum coupling of the V_{GS} by reducing the C_{d_ch}. An underlap results into coupling through the fringe field, which effectively reduces the C_{ox}. An overlap results into coupling of V_{GS} to both source and channel. This results into pulling down of the channel and source bands (below the overlap) which increases the tunneling distance, reduces the I_{ON} and SS. A gate edge perfectly aligned to the tunneling junction, bandgap of source low enough to give higher I_{ON} without increasing I_{OFF}, lightly doped channel and appropriate source doping are projected as critical factors to preserve sharp turn on characteristic. Koswatta et al. [33] have also explained that the gate oxide over the doped source region for CN-

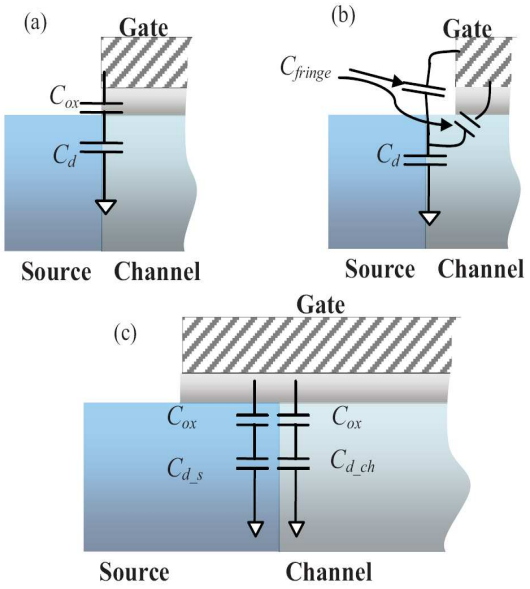


Figure 2.13: (a) Direct gate to channel coupling with aligned gate, (b) gate to channel coupling via fringing capacitance with gate-source underlap, and (c) gate coupling to both source and channel with gate source-overlap. [93].

TFET enhances the source-channel fringing fields that increases band-bending distance at that junction. This reduces the I_{ON}.

Schlosser et al. [55] propose the use of fringe field of high-k gate dielectric to improve the I_{ON}. They use a structure without side spacers. Due to use of local model, high I_{ON} $\sim 10\ \mu A/\mu m$ for SiO_2 gate dielectric and even higher $I_{ON} \sim 1.154$ mA/μm for high-k gate dielectric ($k = 200$) is reported. This value reduces when a SiO_2 sidewall is present next to gate dielectric (in spacer position). However the value of the high-k dielectric required to take advantage of the fringe field effects is very high in the range of 100 or more. At such high k-values the band gap of the dielectric is expected to be low, leading to very high gate leakage current [94].

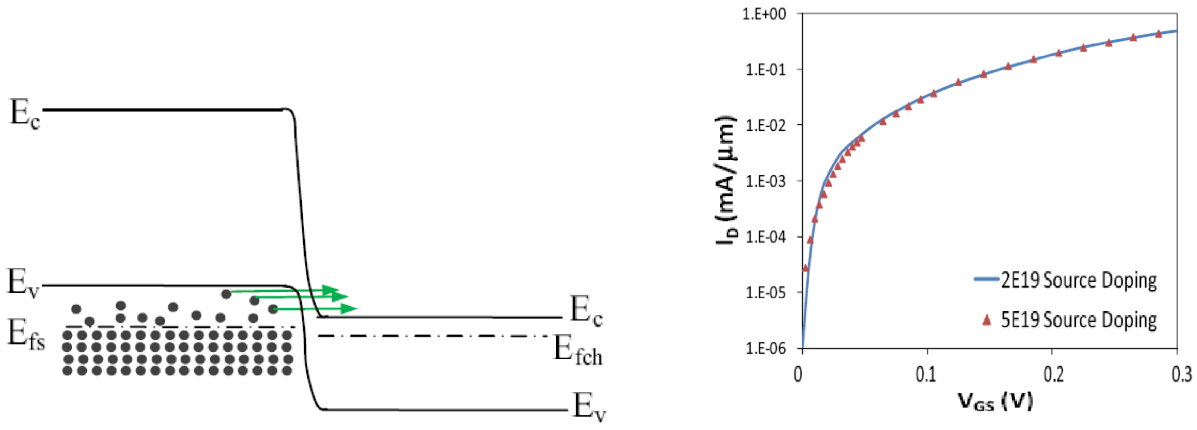
Anghel et al. [60] have reported impact of spacer dielectric constant on nTFET with high-k gate dielectric. They have studied DG-TFET with 3 nm HfO_2 gate dielectric and spacer-k of (a) 3.9 (SiO_2) and (b) 21 (HfO_2). They conclude that use of the low-k spacer (fixed width of 20 nm) and high-k gate dielectric leads to a higher I_{ON} by a factor of 3.8 and reduced SS by factor of 2. However the fringe field coupling through the spacer depends on the dielectric constant k as well as the width of the spacer, which is large in this case. Also the impact of the variation in spacer k and spacer width has not been studied. In case (b), where the gate dielectric and spacer dielectric used are same, increase in spacer-k over and above the k value of gate dielectric has not been studied. This could improve the fringing field through the spacer and could have favorable impact on I_{ON}.

A. Chattopadhyay and A. Mallik [61] have studied effect of spacer-k (width = 50 nm)

on nTFET (EOT = 1 nm). They reports that low-k dielectric of spacer gives performance improvement in I_{ON} with HfO_2 gate dielectric while use of HfO_2 spacer reduces the I_{ON}. They have studied the effect of high-k spacer width variation. As spacer width (HfO_2 with k = 21) for nTFET with SiO_2 gate dielectric is increased from 0 nm (no spacer) to 50 nm in steps of 10 nm, the I_D-V_{GS} characteristic deteriorates. They conclude that a minimum possible spacer width produces the best device performance for high k spacers. Studies for spacer width variation from 1 to 10 nm is not done. They have also reported a study of gate-source/drain overlap and underlap. A gate source overlap reduces the spacer dependence of the device characteristics as the internal field dominates over the fringe field. A gate source underlap structure improves the fringing through the spacer as detailed above. Hence TFET with a high-k spacer and 5 nm underlap shows improved performance. However if underlap is increased to 10 nm, I_{ON} reduces. Studies of underlap < 5 nm is not done. The entire work has been done using abrupt junction which does not give a realistic increase/decrease observed in tunneling currents.

2.4.2.5 Source Doping Engineering

Optimizing the source doping along with sharp source-channel doping profile increases the ON state currents. Yeo et al. [95] have shown by simulations that I_{ON} increases with source doping. Wang et al. [93] have proposed use of optimum doping for source. For heavy doping of the source, the Fermi level lies below the valance band as seen in Fig. 2.14. Hence, at the onset of tunneling current and in the subthreshold region, the carrier density in the source available for tunneling reduces and subthreshold slope increases. They proposed the use of lower doping near the channel (LDD concept) and higher doping away from the tunneling junction to reduce the source resistance. This concept of using



(a) (b)

Figure 2.14: (a) Effect of source doping on the Fermi level in the source and (b) I_D-V_{GS} of nTFET for different source dopings [93].

LDD has been implemented by Mayer et al. [25]. Konch et al. [76] also suggests that the source doping should be such that Fermi level should not be beyond the conduction band for n^+ source of pTFET.

Zhang et al. [14] have shown that electric field at the tunneling junction reduces as the doping gradient increases from 0 (abrupt) to 4 nm/dec. Hence sharp doping profiles are desired for higher tunneling currents. Smith et al. [96] have used Excimer Laser Annealing in silicon nanowire to obtain abrupt box type doping profile and shown an improvement in SS of 9%. Gandhi et al. [97] have used low-temperature dopant-segregated silicidation for the source-side dopant activation in silicon nanowire to obtain SS of 30 mV/decade and I_{ON}/I_{OFF} =10^5. Jeon et al. [98] have used nickel silicide to create a special field-enhancing geometry and a high dopant density by dopant segregation at source-channel interface. It produces steep subthreshold swing (SS) of 46 mV/dec and high I_{ON}/I_{OFF} =10^8.

2.4.2.6 Doping Implants in Channel: Tunneling Source MOSFET

Nagavarapu et al. have reported a novel silicon structure using a PNPN-tunneling source nMOSFET giving higher on currents with improved subthreshold slope [46]. A 4 nm wide pocket is implanted between the source-channel of nTFET with doping of 5 x 10^{19} cm^{-3}. Since the pocket is fully depleted due to small width, band structure similar to nTFET and improved SS is demonstrated by simulations with box type abrupt doping profile. Experimental results are also presented for 10 nm pocket implant using bulk substrate. As the implant width increases, it is no longer fully depleted and characteristic become similar to that of conventional MOSFET. Jhaveri et al. [99] have used same structure on SOI and shown experimentally that spike anneal improves the tunneling currents. Chang et al. [56] have reported SiGe heterojunction PNPN-tunneling source nMOSFET with Gaussian profiles using simulations. The n^+ pocket in tunnel source region can induce lateral electric field and enhance the carrier tunneling. Therefore the PNPN tunnel FET has better performance than PIN tunnel FET. Heigi et al. [100] have used a Zener diode in series with TFET in vertical structure which is similar to the PNPN structures described above. In this case the n layer/implant is not fully depleted thereby yielding a Zener diode + MOSFET configuration. An improvement of 1 decade in I_{ON} is reported with this structure over the similar vertical PNP MOSFET structure.

2.4.3 Vertical Tunneling Phenomena

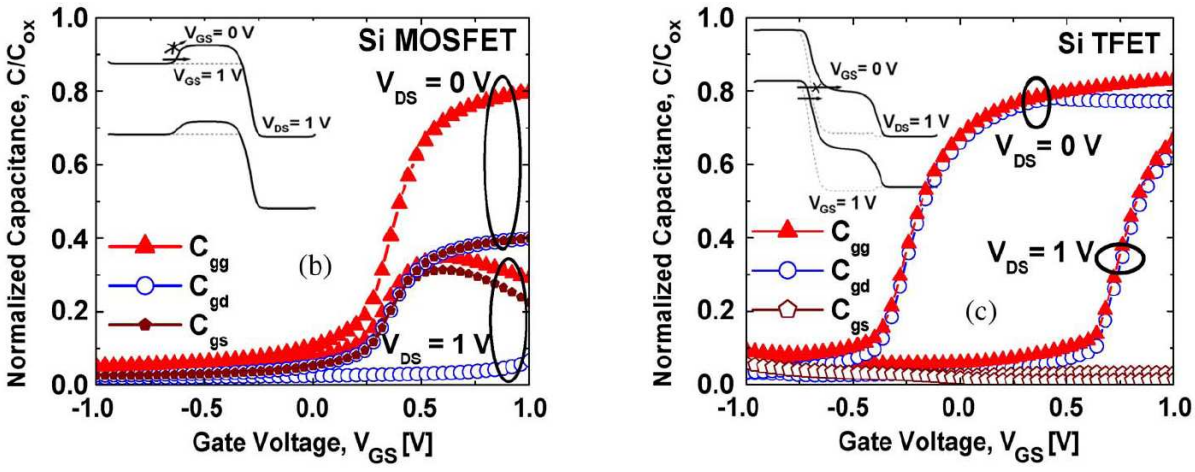
Attempts have been made to modify the simple p-i-n structure to explore the possibilities of increasing the interband tunneling current. One such modified structure, called green TFET (Fig. 2.1(e) showing green pTFET) reports higher ON current of 776 μA/μm for V_{DS} = 1 V and V_{GS} = 1 V using a n^+ bubble doping under the gate for nT-

FET [37, 82, 101]. In this case tunneling occurs vertically underneath the bubble region which improves the area over which tunneling occurs thereby improving the tunneling currents. The depth of the bubble is kept small to ensure that it is fully depleted.

Kim et al. [102] have proposed a raised source (Ge) silicon TFET. In this device the tunneling occurs at the gate-source interface due to band banding of the Ge source resulting into vertical tunneling. The tunneling currents are now no longer dependent on the source-channel doping profile thereby simplifying the fabrication of TFET. Hans et al. [103] have published the experimental characteristic of such a raised Ge source TFET. Asra et al. [38, 104] have simulated a sandwich tunnel barrier FET (Fig. 2.1(f)) which also uses similar vertical tunneling concept. Due to the unique design, the area of tunneling is over almost the entire channel thereby giving high I_{ON} =1.4 mA/μA.

2.5 P-channel Tunnel FETs

For TFET to replace MOSFET based CMOS technology, both n and p-channel TFETs should provide significant competitive advantages over conventional MOSFETs in terms of performance and leakage. A lot of work has been reported on the performance enhancement of the nTFET as stated above. However relatively few reports have been published on pTFET. Bhuwalka et al. [51] have reported experimental results about the ambipolar working of vertical nTFET with negative gate bias, as a pTFET device. Knoch et al. have reported simulation results of a CNT pTFET [105]. Mayer et al. [25] and Royer et al. [26] have reported experimental results of SOI, SiGeOI and GeOI pTFET with 3 nm HfO_2 gate dielectric. Due to low EOT and low band gap material (Ge), higher ON currents of 8 μA/μm is reported. Moselund et al. [106] have reported experimental results of silicon nanowire with SiO_2 and HfO_2 gate dielectric. They report I_{ON} of 0.01 μA/μm for V_{GS}=V_{DS}=-1 V with 5 nm HfO_2 gate dielectric wire diameter of 50 nm. With 20 nm SiO_2 gate dielectric and wire diameter of 40 nm, I_{ON} of 0.005 μA/μm is obtained for similar bias conditions. Toh et al. [15] have reported simulated data of a Ge based double gate pTFET with 3 nm HfO_2 gate dielectric with an ON state current of 800 μA/μm. Verhulst et al [74] have reported $In_xGa_{1-x}As$ source p-channel TFET with currents comparable to n-channel TFET using simulations with semi-analytical model. The gate bias required in all the above cases for operation except [15, 106], is more than the supply voltage due to high threshold voltage. This makes integration of this pTFET into circuit application very impractical. Except for Mayer et al. [25], Royer et al. [26], Verhulst et al [74] and Moselund et al. [106], many other pTFET reports have used negative V_{GS} and positive V_{DS} (i.e. nTFET with negative gate bias). For use of pTFET in circuit applications, there is a strong need of optimization of pTFET with negative V_{DS} and V_{GS} to ensure consistency with CMOS type biasing.



(a) (b)

Figure 2.15: Capacitance voltage characteristics showing the gate (C_{gg}), gate-to-source (C_{gs}), and gate-to-drain (C_{gd}) capacitances as a function of gate-to-source voltage V_{GS} for (a) Si MOSFET and (b) Si TFET [107].

2.6 Performance of Tunnel FETs in Circuits

The structure of nTFET with p^+-i-n^+ doping is similar to that of nMOSFET which has n^+-p-n^+ doping. However TFET have different capacitance behavior as compared to that of MOSFET which has a profound impact on dynamic performance of circuits. Mookerjea et al. [107] have made a comparison of the C-V characteristics of these devices (Fig. 2.15). For TFET I_{ON} is limited by the BTBT compared to thermionic emission over the barrier for MOSFET. This results on much lower I_{ON} in TFETs compared to that of MOSFETs resulting into very low gate-to-source capacitance (C_{gs}) in TFETs in the ON state ($V_{GS} = V_{DS} = 1$ V). However the gate-to-drain capacitance (C_{gd}) in TFETs is large as potential drop between the channel and the drain is low in TFETs compared to the large reverse bias that exists between the channel and the drain in MOSFETs. Even in the OFF state ($V_{GS} = V_{DS} = 0$ V), the C_{gd} is larger as the source-to channel barrier resistance is large while the channel-to-drain barrier resistance is low. In MOSFETs there is equal barrier on both sides of the channel resulting in equal C_{gs} and C_{gd}. The gate capacitance C_{gg} is entirely dominated by C_{gd} in TFETs under all bias conditions in contrast to MOSFETs, where both C_{gs} and C_{gd} contribute. This increased Miller capacitance (C_{gd}) effect in TFETs over MOSFETs, coupled with low ON currents, has important implications for their dynamic performance. For example the overshoots in inverter transient response are enhanced due to higher C_{gd}.

2.6.1 Static Performance

The earliest circuit simulations were reported by Nirschl et al. [108] using tunneling source MOSFET. They simulated NOR gate, NAND gates and SRAM cell using LUT approach. The device used had a MOSFET type behavior. Fulde et al. have proposed a reference voltage circuit with a mix of multiple gate TFETs and MOSFETs [12, 34]. However this reference voltage circuit has not been simulated. Hu et al. [37] have published the DC transfer characteristic of a inverter. However it is not clear whether they have used mixed mode simulation (MEDICI) or LUT based circuit simulation. Zhang et al. [14] have reported inverter transfer characteristic using thin body Ge TFET. Mookerjea et al. [107, 109] have published mixed mode simulation results using Si TFETs. The DC transfer characteristic using calibrated non local model has been reported. They have used double gate TFET with 2.5 nm HfO_2 gate oxide to boost the currents of Si TFETs. The ON state current ($\sim$ 0.1 mA/μm) and shape of the output characteristics of TFETs are reported to influence the noise margins of TFET inverters.

Khatami et al. [57] have reported LUT based inverter transfer characteristic using cylindrical gate all round vertical TFET with undoped SiGe layer between the source and channel and high k gate dielectric. The device optimization reported is with MEDICI TCAD tool. The static performance of the TFET based inverter is compared to the 45 nm CMOS based inverter. A gain of $\sim 10^6$ is achieved in static power consumption for the TFET based inverter.

The static performance is also evaluated by computing the noise margins (NM) of SRAM cell. The SRAM cell design using TFETs have the problem of uni-directionality [110]. Hence the conventional design of 6T-SRAM cell cannot be used. To overcome this hurdle of uni-directionality for SRAM realization, Kim et al. have proposed a 7T SRAM cell with separate read and write ports [110]. The new 7T SRAM design achieves 7-to-37x reduction in leakage power compared to the respective CMOS circuits for different V_{DD}. Singh et al. [59] have proposed a new 6T TFET SRAM cell with unique design features and write assist techniques. They have used a DG-TFET with thin 2.5 nm HfO_2 gate dielectric for simulation of new 6T-SRAM cell using verilog-A lookup table thereby reducing 1 transistor as compared to the design of Kim et al. They show a leakage reduction improvement of 700x and 1600x over traditional CMOS SRAM designs at V_{DD} of 0.3 V and 0.5 V respectively. Mookerjea et al. [53] have reported $In_{0.53}Ga_{0.47}As$ TFET SRAM simulation with the same 6T SRAM design used by Singh et al.

2.6.2 Dynamic Performance

Mookerjea et al. [107] have reported transient simulation of inverter highlighting the increase in overshoots due to enhanced miller capacitance. The unidirectional current flow and miller capacitance are the two major difference between TFET and CMOS which

affects the circuit implementation with TFET. Kim et al. [110] have used type II hetero junction TFET (HETT) with abrupt doping profile at $V_{DD} = 0.5$ V for circuit simulation of ring oscillator. They have used verilog-A look up table for the simulations and showed that the HETT-based ring oscillator gives a 9-to-19x reduction in dynamic power.

Wan et al. [111] have done experimental studies of the low frequency noise (LFN) behavior in silicon fully depleted SOI TFET. In large TFETs, the LFN is dominated by random telegraph signal noise characterized by 1/f slope. This is because drain current in TFET is controlled by the local tunneling junction involving a small area with small number of traps.

2.7 Discussion

In this chapter, the principle of operation of TFET is discussed. Various techniques, which are reported in the literature to increase the tunneling currents of TFET are reviewed. The tunnel barrier height can be reduced by using low bandgap material like SiGe, Ge etc or by using strain. These methods have the drawback of increased leakage currents. Hetero-junction are preferred to this method as the I_{OFF} does not increase because the channel is made of high bandgap material. Lateral stress profiles are also used to selectively reduce barrier height near source-channel junction thereby improving I_{ON} without increase in I_{OFF}. Novel materials like CNT, Graphene and III-IV compounds are also used to optimize the I_{ON} of TFET. The tunnel barrier width can be reduced by enhancing the source-gate electric field. This can be achieved using high-k gate dielectric which increase I_{ON} as well as I_{OFF}. Another method is to use halo type doping implants. The electric field can also be enhanced using fringe field coupling through the spacers. This improves I_{ON} without deterioration of I_{OFF}. This techniques has been reported only in three recent papers and scrutiny of these papers reveal that there is still scope for a complete study. Another interesting approach is to use vertical tunneling at the source-channel or gate-channel interface by raised source structure or other architectural innovations. This methods make the tunneling currents independent of the doping profiles in the TFET.

Chapter 3

Simulation Setup and Calibration of models

3.1 Introduction

In literature review (chapter 2), we had discussed the importance of choosing the correct model in order to simulate accurate tunneling currents. This chapter reviews the process of band-to-band tunneling (BTBT), in which electrons tunnel across the energy gap of a semiconductor (i.e., valance to conduction band). Details of these models used for the interband tunneling, namely the local tunneling model using tool MEDICI and non local tunneling model using tool SENTAURUS are described. The calibration results of these models with experimental data is presented. The local model was used only in the initial simulation work for optimization of TFET, since the non local model implementation in SENTAURUS TCAD suite was not available at that time.

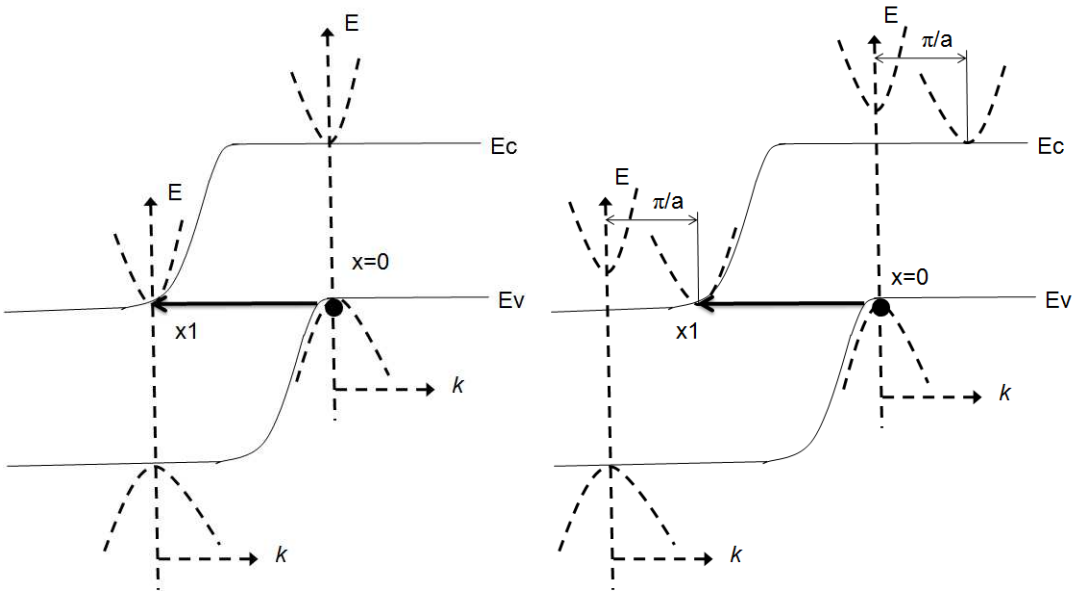
3.2 Tunneling Theory

The tunneling probability P_t can be given by the WKB (Wentzel-Kramers-Brillouin) approximation [112]:

$$P_t \approx exp\left[-2\int_0^{x_1} |k(x)|\right] dx \tag{3.1}$$

where $|k(x)|$ is absolute value of the wave vector of the carrier inside the barrier, and x=0, x_1 are the classical boundaries shown in Fig. 3.1

To calculate the tunneling probability from the WKB approach, an accurate expression of the imaginary wave vector throughout the electron path must be known. The tunneling of an electron through a forbidden band is formally the same as a particle tunneling through a potential barrier. If we approximate this potential barrier as a triangular barrier as shown in Fig. 3.2, then the wave vector inside the triangular barrier is given



(a) Direct tunneling (b) Indirect tunneling

Figure 3.1: Direct and indirect tunneling processes demonstrated by E-k relationship superimposed on the classical turning points (x = 0 and x_1) of the tunnel junction. (a) Direct tunneling process with $k_{min} = k_{max}$ (b) Indirect tunneling process with $k_{min} \neq k_{max}$ [112].

by [112] :

$$k(x) = \sqrt{\frac{-2m^*}{\hbar^2}(qFx)} \tag{3.2}$$

where

F = magnitude of the electric field

m^* = carrier effective mass

$\hbar$ = Planck's constant$(h)/2\pi$

q = charge of an electron

substituting eq. 3.2 in eq. 3.1 we obtain

$$P_t \approx exp\left[-2\int_0^{x_1}\sqrt{\frac{2m^*}{\hbar^2}(qFx)}dx\right] \tag{3.3}$$

For a triangular barrier with uniform field, $x_1 = E_G/Fq$, hence we get

$$P_t \approx exp\left(-\frac{4\sqrt{2m^*}E_G^{3/2}}{3q\hbar F}\right) \tag{3.4}$$

where E_G = energy bandgap.

To obtain large tunneling probability, both effective mass and bandgap must be small and electric field must be large.

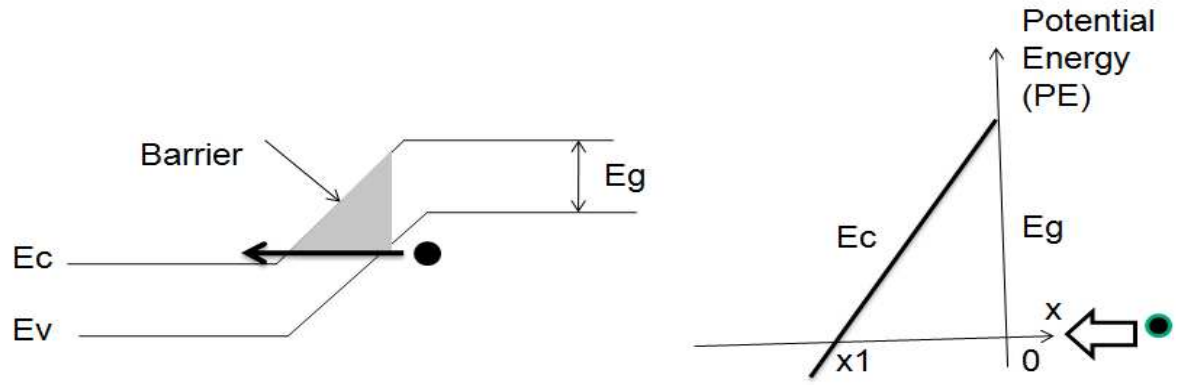


Figure 3.2: Tunneling in a tunnel diode can be analyzed by a triangular potential barrier [112].

3.3 Simulation Tools and Models

The 2-D simulations were performed using the Synopsis TCAD suite. The models used were local and non local model which are described in this section along with the calibration of these models.

3.3.1 Local Model for Tunneling

The Synopsis TCAD tool MEDICI 2006v was used for local tunneling model simulations. Models which compute the tunneling probability by assuming constant electric field along the tunneling path are generally called as LOCAL tunneling models.

3.3.1.1 Kane Model

The process of band to band tunneling of electrons from the valance band to the conduction band is phonon assisted for indirect bandgap material such as silicon (Fig. 3.1 (b)). Keldysh et al. presented the first calculation of the probability of the band to band transition in 1958. Keldysh's results were later adapted and improved by Kane et al. [42]

The Kanes model for tunneling implemented in MEDICI was used which is based on the WKB approximation of the current tunneling through the triangular barrier (the height of the triangle is the bandgap). The tunneling generation rate for this model is given by:

$$G_{btbt} = A_{kane}\frac{F^C}{E_G^{1/2}}exp(\frac{-B_{kane}E_G^{3/2}}{F}) \tag{3.5}$$

$$A_{kane} = \frac{q^2\sqrt{m^*}}{18\pi\hbar^2} \tag{3.6}$$

$$B_{kane} = \frac{\pi\sqrt{m^*}}{2q\hbar} \tag{3.7}$$

where
A_{kane} = 3.5x10^{21} $eV^{1/2}$/cm-s-V^2
B_{kane} = 22.5x10^6 V/cm-$eV^{3/2}$
C = 2

3.3.1.2 Calibration of Kane Model

Krishna et al [2, 23] have shown that the experimental results of vertical TFET match the simulated characteristic with default parameters listed above.

$$F = DV_{GS} \tag{3.8}$$

where D=f(V_{DS},t_{ox},doping,L_G), t_{ox} is gate oxide thickness and L_G is gate length.

$$I_{DS} \propto G_{btbt} \tag{3.9}$$

using eq. 3.5, 3.8 and 3.9 we get:

$$I_{DS} = A_{kane}\frac{D^2}{E_G^{1/2}}exp(\frac{-B_{kane}E_G^{3/2}}{DV_{GS}}) \tag{3.10}$$

$$log(\frac{I_{DS}}{V_{GS}^2}) = log(\frac{A_{kane}D^2}{E_G^{1/2}}) - \frac{B_{kane}E_G^{3/2}}{DV_{GS}} \tag{3.11}$$

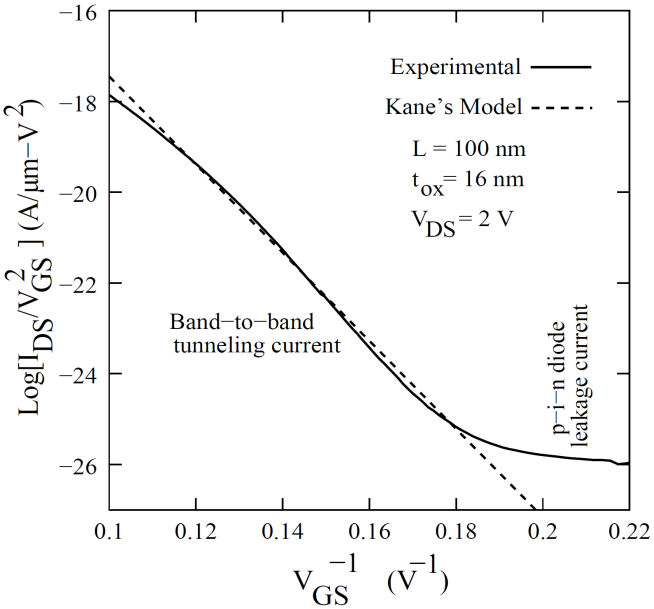


Figure 3.3: Modified Kane's model equation fit with experimental data [2, 23].

From Fig. 3.3, it can be seen that the modified Kane's model (Eq. 3.11) fits very well to experimental data in the saturation region.

The parameter BT.MODEL is set to 2 which implies that the average electric field along the tunneling path are used. Due to heavy doping in the source, Fermi Diarc statistics and band gap narrowing model are used.

Although this model is computationally efficient, the main disadvantage is that it computes high currents particularly at $V_{DS} = V_{DD}$ and V_{GS}=0. As a result the mixed mode simulations do not converge. However this model was widely used for TFET optimization [11, 23, 35, 37, 43–48] since it was calibrated as detailed above and the non local model implementation was not available in the TCAD suite.

A limitation of MEDICI implementation of Kane's band-to-band-tunneling model is that the true E-k relation along the tunneling path is not used. Instead a less accurate implementation given by Eq. 3.2 is used whereby the value of the k-vector increases with the square-root of the energy-barrier [112] (the energy barrier is given by the integral of the local electric field along the tunnel path). The use of the local field along the tunneling path results in inaccuracies for computing band-to-band tunneling currents (Fig. 2.5) which can be quite significant because only the energy barrier which has to be bridged is considered and therefore there is no dependence on the actual band gap at the start and end point of the tunnel path. The band alignment is not a necessary condition for tunneling in this model.

In version 2007.12v of MEDICI, an additional multiplying factor D_{tunnel} was added to Eq. 3.5 which takes into account the probability of having a filled state to tunnel from and an empty state to tunnel to.

$$D_{tunnel} = \frac{1}{1 + exp\left(\frac{E_{V,1} - E_{Fp,1}}{KT}\right)} - \frac{1}{1 + exp\left(\frac{E_{C,2} - E_{Fn,2}}{KT}\right)} \tag{3.12}$$

where

$E_{V,1}$,$E_{Fp,1}$ $\rightarrow$ valence band and the hole Fermi energy on one side of the tunnel barrier

$E_{C,2}$,$E_{Fn,2}$ $\rightarrow$ conduction band and the electron Fermi energy on the other side of the tunnel barrier.

Hence D_{tunnel} is a non local quantity requiring the evaluation of band energy levels on both sides of the tunneling barrier. This ensures the band alignment requirement, but the dependence on the local field still results in computation of higher tunneling currents. Hence this model was used only in the initial simulation work for optimization of TFET due to non availability of non local model implementation in SENTAURUS TCAD suite.

3.3.2 Non Local Model for Tunneling

The Synopsis TCAD tool SENTAURUS was used for non local tunneling model simulations. The inter-band current in the TFET depends on the potential profile along the entire path between two points connected by tunneling. The non local model accounts for the actual spatial charge transfer across the tunnel barrier by considering the actual potential profile along the entire path connected by tunneling.

The key feature of this model is that the tunneling current through the barrier is converted into a local generation rate G_{btbt} which depends on the local Fermi level ϕ and the potential profile along the tunneling path. At the tunneling junction, a tunneling path is extracted from the 2-D domain using a carefully constructed mesh. This mesh called the non local mesh is a special purpose 1-D mesh required by the simulator to implement the non local physical model. It consists of non local lines, each non local line is subdivided by non local mesh points, to allow for the discretization of the equations that constitute the physical models. Simulator performs this subdivision automatically to obtain optimal interpolation between the non local mesh and the normal mesh.

The local generation rate at r is given by:

$$G_{btbt}(r) = gA\frac{T}{K_B}F(r)P_t(r)ln\left[\frac{1+exp(E(r)-E_{ch})/KT}{1+exp(E(r)-E_S)/KT}\right] \tag{3.13}$$

where
F(r) = Electric field
E(r) = -qψ=carrier energy
E_{ch} = -qϕ_{ch} = quasi fermi energy of carriers in channel
E_S = -qϕ_{source} = quasi fermi energy of carriers in source
g = As/A, As is the Richardson constant for carriers in semiconductor
A is the Richardson constant for carriers in free space
P_t(r) is WKB approximation for the tunneling probability given by [113]:

$$P_t(r) = exp\left[-\frac{2}{\hbar}\int_0^r \sqrt{2m(\phi_{channel}/q+\phi_{source}-\psi(x))dx}\right] \tag{3.14}$$

The P_t(r) is computed accurately based on the potential profile $\psi(x)$ variation throughout the tunneling barrier, whereas this computation is approximated in Kane's model.

3.3.2.1 Calibration

The SENTAURUS non local model was calibrated using experimental data of reversed biased tunneling diode data from Fair and Wivell [114]. Since the I-V characteristic as well as the SIMS doping profile has been reported in [114], the same were preferred for use as experimental data. The experimental data of the I-V characteristic along with SIMS data of TFET was not available, hence the above referred diode data was used for

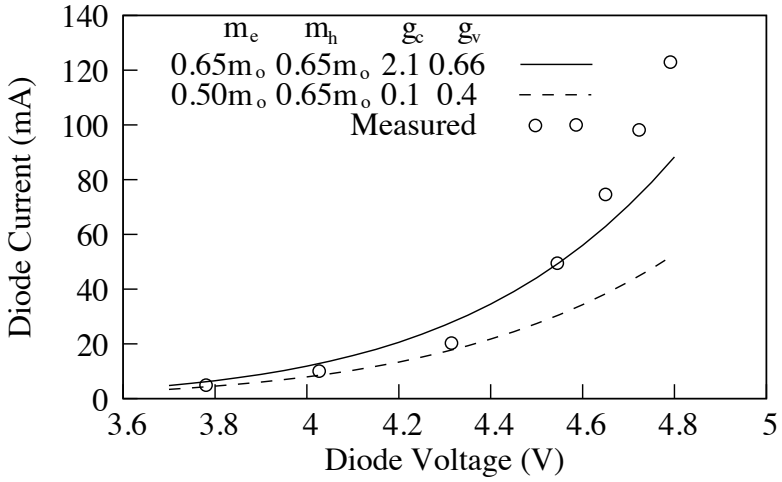


Figure 3.4: The simulated Si Zener diode characteristic fitted to experimental data from Fair and Wivell [114]. The characteristic generated with the calibration reported in [109] is also shown with dashed lines.

calibration. The measured and simulated diode characteristic are shown in Fig. 3.4. The simulated characteristic shows a good match with the experimental data.

The tunneling masses m_e and m_v were tuned to obtain a match between the experimental and simulated data. The g_c and g_v values, which sets the effective Richardson constant were kept unchanged to their default values of 2.1 and 0.66 respectively. A good match is obtained with experimental data for $m_e = 0.65m_o$ and $m_h = 0.65m_o$.

Mookerjea et al. [109]. have used the same data for calibration and the same is included in the Fig. 3.4 for comparison. The calibration in this work is a better match to the experimental data than the reported calibration as seen in Fig. 3.4.

3.4 Device Structure

The lateral p^+-i-n structure for nTFET and n^+-i-p structure for pTFET shown in Fig. 3.5 are used throughout this chapter. The structure is suitably modified to optimize the I_{ON} using gate stack engineering, hetero junctions and doping engineering in subsequent chapters. The gate length (L_G) and equivalent oxide thickness (EOT) were selected to be

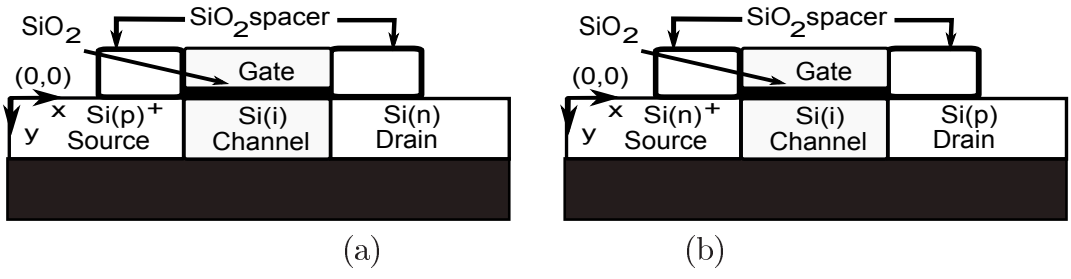


Figure 3.5: Lateral TFET structures. (a) n-channel TFET and (b) p-channel TFET.

20 nm and 1.1 nm, respectively, to be relevant for modern CMOS technology.

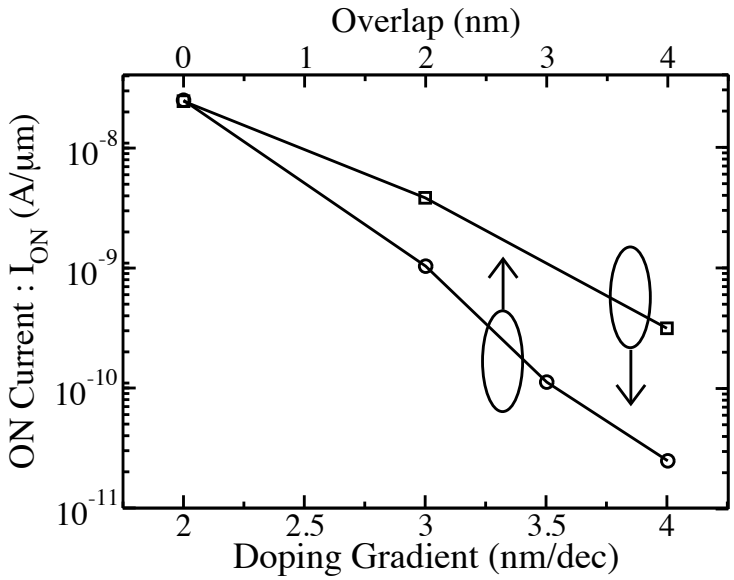


Figure 3.6: Reduction in ON currents with (a) increasing gate-source overlap and (b) increasing doping gardient at the source-channel junction.

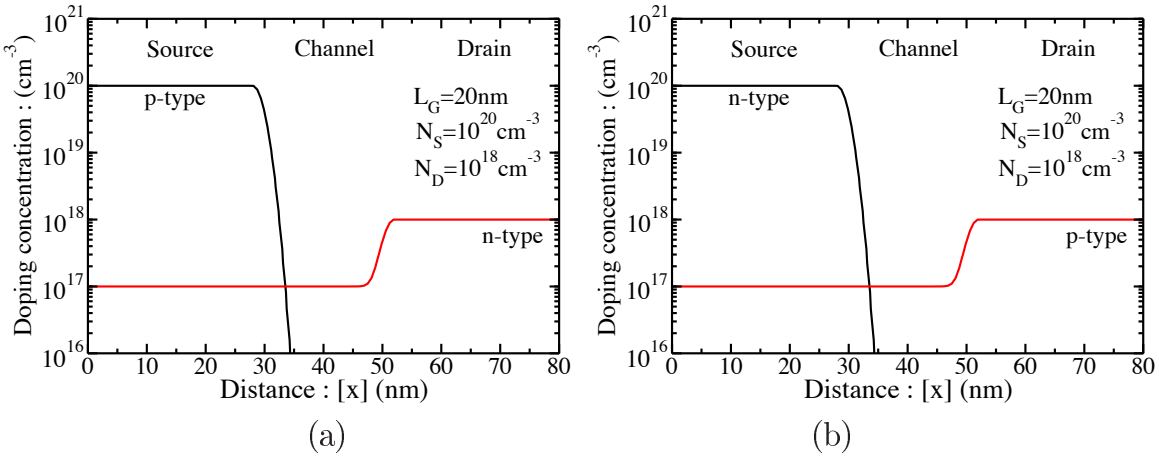


Figure 3.7: (a) The doping profile of p^+ source and n drain with $N_S = 10^{20}$ cm^{-3} and $N_D = 10^{18}$ cm^{-3} for the n-channel TFET. The channel is uniformly doped with n type dopant with concentration of 10^{17} cm^{-3}. (b) The doping profile of n^+ source and p drain with $N_S = 10^{20}$ cm^{-3} and $N_D = 10^{18}$ cm^{-3} for the p-channel TFET. The channel is uniformly doped with p type dopant with concentration of 10^{17} cm^{-3}.

The tunneling currents are sensitive to the doping profile of the tunneling junction [14]. Fig. 3.6 shows the I_{ON} for 2 nm/dec, 3 nm/dec and 4 nm/dec doping profile. I_{ON} decreases as the doping profile slope increases. The tunneling currents are also sensitive to the gate alignment to the tunneling junction [93]. Fig. 3.6 shows the I_{ON} for 0, 2, 3 and 4 nm of gate source overlap. The I_{ON} decreases with increase in overlap. Hence nil

gate-source overlap is preferred [33, 93]. The source doping is kept at 1x10^{20} cm^{-3}. Lower source doping in source such that Fermi level is at conduction band edges (n^+ source) for pTFET and valence band edge (p^+ source) for nTFET is proposed to maximize the carrier density in source available for tunneling in subthreshold region. This improves the SS but the I_{ON} reduces due to the reduction of the electric field at the junction. Hence a higher doping is used to maximize the I_{ON} at the cost of small degradation in SS. The drain doping is kept low ($\leq$1e18) cm^{-3} and the channel is intrinsic ($\leq$1e17cm^{-3}).

Abrupt doping profiles were used for the MEDICI simulations with Kane's local tunneling model and Gaussian doping profiles with gradient of 2 nm/decade were used for the SENTAURUS simulation with non local tunneling model. The p^+-i-n doping profile used for nTFET are shown in Fig. 3.7. Similar n^+-i-p doping profile are used for pTFET.

3.5 Summary

The models used for simulation with the TCAD tool MEDICI and SENTAURUS were described. The calibration of the tunneling models used was detailed. The structure details of TFET were outlined and the the simulation setup was explained.

The next chapter covers the simulation of TFET with high-k spacers using the models and simulation setup described in this chapter.

Chapter 4

Optimization of Tunnel FET with High k spacers

4.1 Introduction

In this chapter, we propose the use of a high k spacer engineering to improve the performance of n-channel TFETs. Unlike use of high k gate dielectric, which increases both ON and OFF state currents, use of high k spacers enhances ON state current without deterioration of OFF state currents. High-k spacers have been studied in conventional MOSFETs to electrically induce extension regions and this technique was found to suppress short channel effects [115]. In this chapter, we have shown that by replacing the SiO_2 spacer with a high k spacer for nTFET, the ON current and subthreshold swing of nTFET with 1.1 nm SiO_2 gate dielectric are enhanced, without deterioration of OFF currents.

We also propose the use of high k spacer engineering to improve the ON state currents of pTFET. Negative values of V_{GS} and V_{DS} have been used in this work and hence the results are CMOS bias compatible.

This work, like many other published work, was initially done in tool MEDICI with Kane's tunneling model since non local model implementation in TCAD suite was not available. Later, when more physical and accurate non local model was implemented in SENTAURUS TCAD suite, the same was used and the results were reconfirmed.

4.2 Effect of High-k spacer on Tunneling Current of n-channel TFET

We simulated hetero junction nTFETs (H-nTFETs), the generic structure of which is shown in Fig. 4.1. For the simulations reported in this chapter, the device parameters are as follows. The p^+ source region is made of $Si_{0.6}Ge_{0.4}$ and the intrinsic channel region and

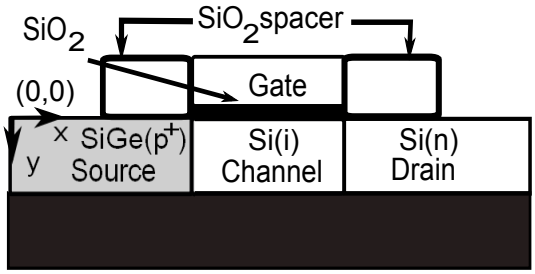


Figure 4.1: Schematic of gated p-i-n structure built on SOI substrates and used as TFET. The source is made of $Si_{0.6}Ge_{0.4}$ and the channel and drain regions are made of Si.

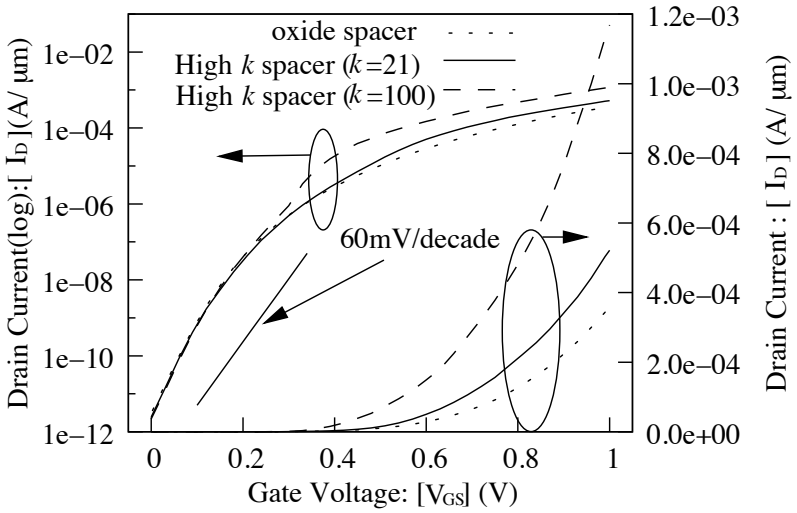


Figure 4.2: I_D-V_{GS} characteristics of hetero junction nTFETs with spacer of various dielectric constants. Gate length = 20 nm, Ge mole fraction = 0.4, spacer thickness = 3 nm and V_{DS} = 1 V.

the n-doped drain region were made of Silicon. The gate length is 20 nm. The physical thickness of the spacer was kept constant at 3 nm. Abrupt doping profiles are used for both source and drain. A 1.1 nm thick SiO_2 is used as the gate dielectric and the gate workfunction at 4.4 eV. The 2-D device simulations were performed with Kane's model using Synopsis TCAD tool MEDICI [116].

Fig. 4.2 shows the I_D-V_{GS} characteristics of the H-nTFET at V_{DS} = 1 V as the spacer dielectric constant is varied through 3.9 (SiO_2), 21 (HfO_2) and 100. It is seen that the ON state current ($V_{DS} = V_{GS} = 1$ V) improves as the dielectric constant of the spacer is increased. However the OFF state current ($V_{DS} = 1$ V, $V_{GS} = 0$ V) is not dependent on the k value of the spacer material. The average SS is nearly independent of the spacer k value and is better than 60 mV/dec in all the three cases. For calculating the average SS, we have computed SS for every decade decrease from $1 \times 10^{-7}\mu$A/μm to I_{OFF} and then taken the average [2]. Also the threshold voltage, which is defined as the gate voltage at which the drain current is $1 \times 10^{-7}\mu$A/μm, does not change significantly. Fig. 4.3 shows

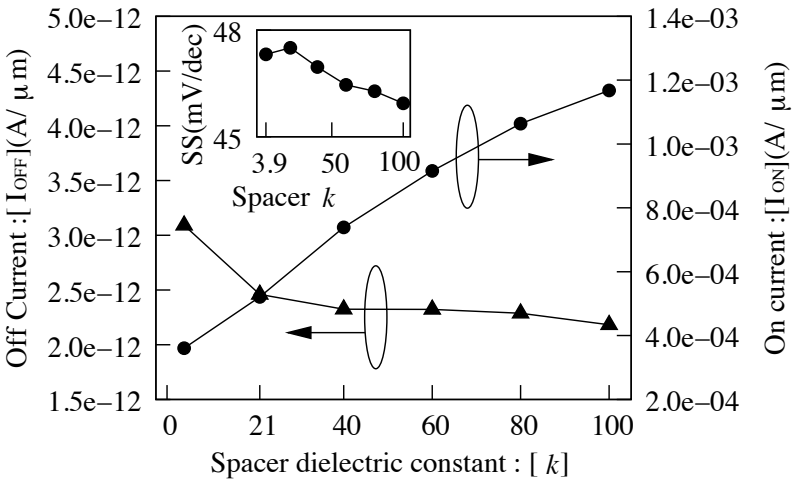


Figure 4.3: Effect of spacer dielectric constant on I_{ON}, I_{OFF} and average SS of nTFET.

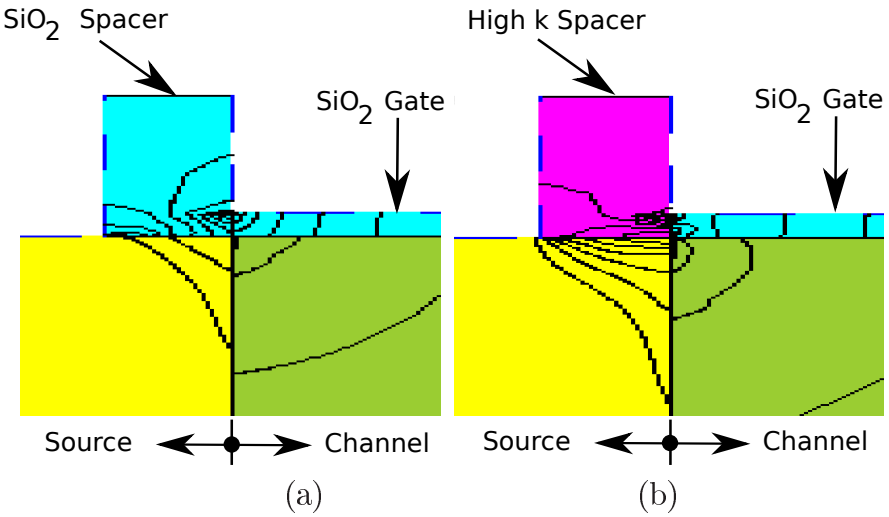


Figure 4.4: Fringe field coupling ($V_{DS} = 1$ V and $V_{GS} = 1$ V) through spacer for (a) oxide ($k = 3.9$) and (b) high-k ($k = 100$) spacers. The gate dielectric is SiO_2 with a thickness of 1.1 nm.

the variation of I_{ON}, I_{OFF} and SS as a function of spacer k value. I_{ON} is seen to increase 45% as k is increased from 3.9 to 21 and 225% as k is increased from 3.9 to 100.

The physics behind the I_{ON} improvement can be understood by analyzing the field lines near the source-channel junction and the band-diagram from source to drain close to the gate dielectric interface. Fig. 4.4 shows the electric field lines in the device close to the source-channel junction. The figure on the left is for spacer k of 3.9, and the right figure is for spacer k of 100. Higher k of the spacer result in denser field lines at the junction, which leads to higher field at the junction. The corresponding band-diagrams are shown in Fig. 4.5. It is seen that the band-bending start at the outer edge of the spacer. As the spacer k is increased, the fringing fields through the spacer cause a larger bending of the bands closer to the spacer as shown. Consequently the tunneling width decreases leading

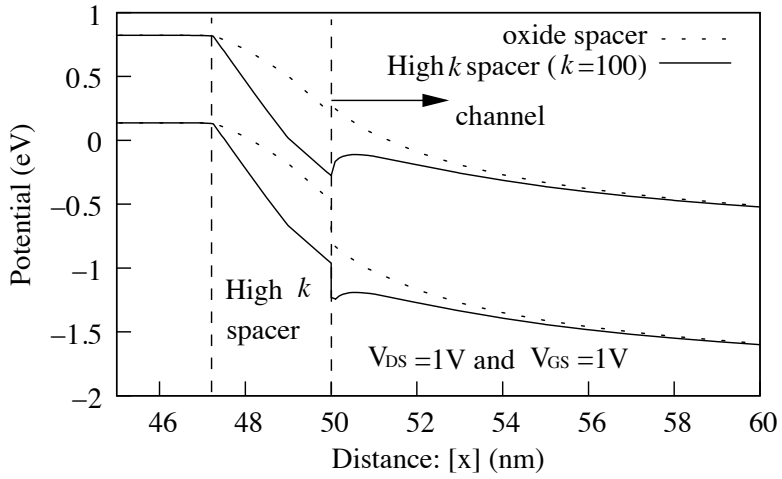


Figure 4.5: Band diagram showing the reduction of tunneling width in $Si_{0.6}Ge_{0.4}$ hetero junction nTFET when a high-k spacer ($k = 100$) is used. A small bump (upward shift) is seen in the band diagram on the "i" side of the junction when a high-k spacer is used.

to higher current. The tunneling would happen from the valance band at the outer edge of the spacer to the conduction band in the channel or the source itself, depending on the spacer k and the gate bias. In the channel region further from the source-channel junction, the bands for the various spacer k values seems to merge.

The tunnel current is seen to increase with spacer k only when the gate bias is typically beyond 0.25 V, depending on the spacer k, see Fig. 4.2. Below $V_{GS} = 0.2$ V, I_D-V_{GS} is seen to be independent of spacer k. This can be explained as follows. It may be noted that at the source-channel junction, the band-diagram shows an upward shift for a short distance when the spacer k is different from the k of the gate dielectric. Fig. 4.6 shows the band-diagram for spacer $k = 100$ at $V_{DS} = 1$ V and $V_{GS} = 0$, 0.3 and 1 V. When V_{GS}

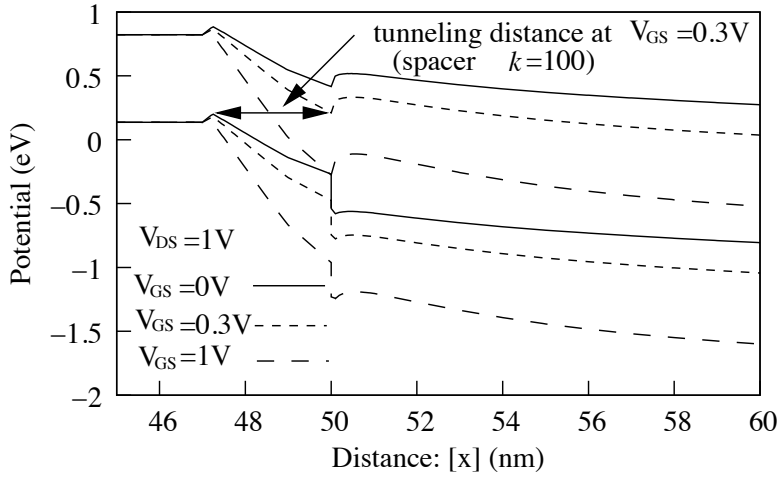


Figure 4.6: Band diagram of the hetero junction nTFET with spacer k of 100 for various values of V_{GS}.

= 0, electrons tunnel from valance band at the outer edge of the spacer to the conduction band in the channel region. This is seen to continue till V_{GS} is close to 0.3 V. However at V_{GS} = 0.3 V, the tunneling would occur to the conduction band at the source-channel junction and the tunneling width decreases abruptly, leading to an abrupt change in the tunneling current seen in Fig. 4.2. As a consequence the OFF state current and the subthreshold slope of the devices do not change with spacer k. But the ON state current is significantly enhanced.

Schlosser et al. have reported that the use of high k materials as gate dielectric would improve the ON state current due to the enhancement of fringe fields at the gate edges [55]. However, the OFF state current for a given gate voltage and gate work function was also reported to degrade as the k value was increased. This might be due to the fact that the internal fringe fields also increase as the k value is increased [117], resulting in increased current at all gate voltages. As a result, both the I_{ON} and I_{OFF} tends to increase simultaneously. They also reported that the ON current improvement was not significant when the k was varied from 3.9 to 21 and it was significant only for very large values of k. Use of high-k spacer provides improvement in tunneling currents at comparatively lower k values without significant increase in I_{OFF}.

4.3 Comparison with Simulation Results using Non Local Model

Since the local tunneling model overestimates the tunneling currents, the work was reconfirmed by performing simulations with non local model. As seen in Fig. 4.7, we

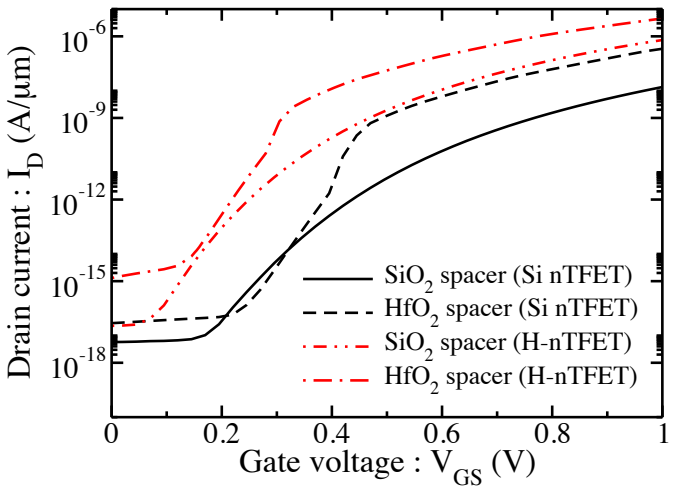


Figure 4.7: I_D-V_{GS} characteristics of Si nTFET and H-nTFET ($Si_{0.6}Ge_{0.4}$ source) with 5 nm spacers made of SiO_2 and HfO_2 (k=25).

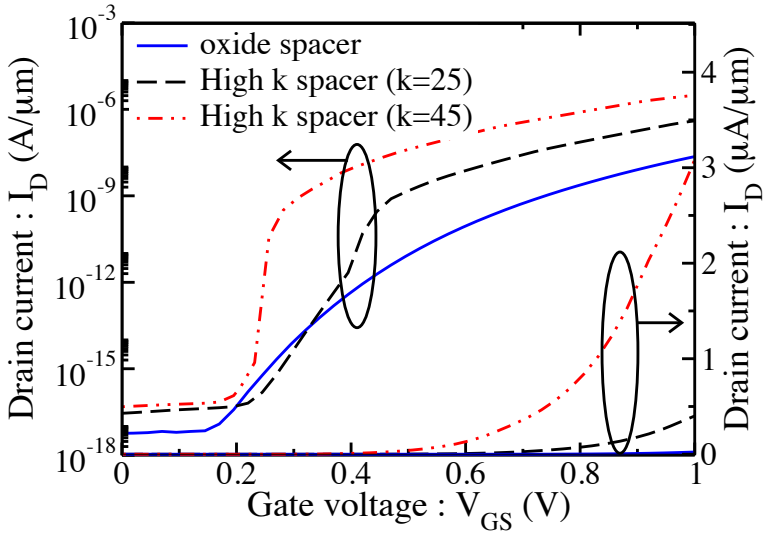


Figure 4.8: I_D-V_{GS} characteristics of Si nTFETs with spacer of various dielectric constants. Gate length = 20 nm, spacer thickness = 5 nm and V_{DS} = 1 V.

obtain similar improvement trends (I_{ON} increases as the spacer k increased) in I_D-V_{GS} characteristic for silicon nTFET as well as H-nTFET (source made up of $Si_{0.6}Ge_{0.4}$). We note that the tunneling currents obtained for H-nTFET are smaller in magnitude as compared to Fig. 4.2 and are similar to the magnitudes of the experimental data of TFET currents.

The non local model was calibrated for tunneling in silicon as detailed in chapter 3. However the data on Si/SiGe hetero junction tunneling was not available for calibration. Hence the following work in this chapter and rest of the work in this thesis was done using homo-junction silicon TFET.

4.3.1 Effect of Spacer Dielectric on Tunneling Current of n-channel TFET

Silicon TFETs with structures shown in Fig. 3.5 was used. The gate length is 20 nm. Gaussian doping profiles with slopes of 2 nm/decade were used for both source and drain (Fig. 3.7). A 1.1 nm thick SiO_2 is used as the gate dielectric and the gate workfunction is 4.1 eV.

The impact of spacer dielectric constant was studied by keeping the spacer width at 5 nm and varying the spacer k. Fig. 4.8 shows the I_D-V_{GS} characteristics of the device at V_{DS} = 1 V as the spacer dielectric constant is varied through 3.9 (SiO_2), 25 and 45. It is seen that the ON state current ($V_{DS} = V_{GS}$ = 1 V) improves as the dielectric constant of the spacer is increased. However the OFF state current (V_{DS} = 1 V, V_{GS} = 0 V) is not dependent on the k value of the spacer material. The average SS improves with increase in spacer dielectric constant. Since the non local model computes

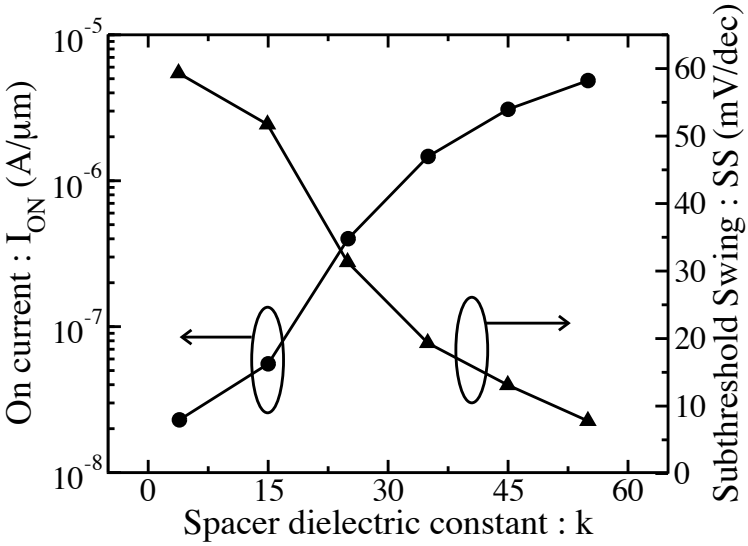


Figure 4.9: Effect of spacer dielectric constant on I_{ON} and average Subthreshold Swing of nTFET.

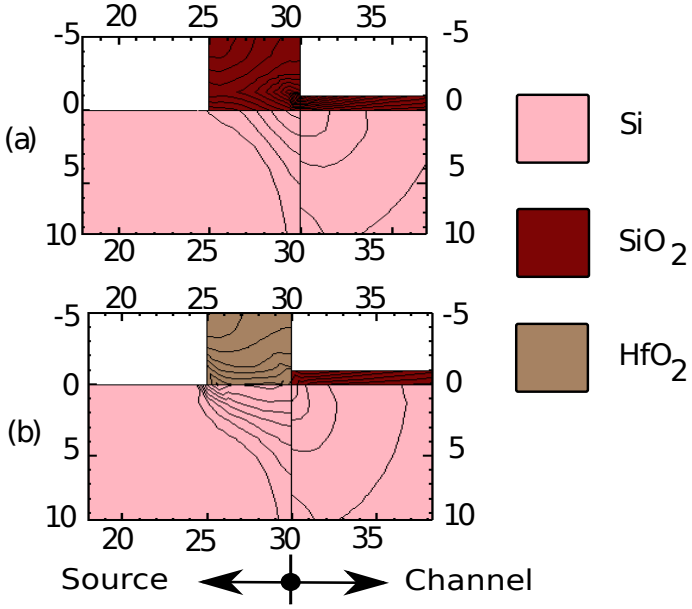


Figure 4.10: Fringe field coupling (V_{DS} = 1 V and V_{GS} = 1 V) through spacer for (a) oxide (k = 3.9) and (b) high-k (k = 45) spacers. Dimensions are in nanometers.

smaller tunneling currents as compared to local model, we need to redefine V_{TH} and SS. For calculating the average SS, we have computed SS for every decade decrease from $1 \times 10^{-10}\mu$A/μm to $1 \times 10^{-16}\mu$A/μm and then taken the average [2]. Also the threshold voltage is defined at a drain current of $1 \times 10^{-10}\mu$A/μm. Fig. 4.9 shows the variation of I_{ON} and SS as a function of spacer k value. I_{ON} is seen to increase by one decade as k is increased from 3.9 to 25 and by more than 2 decades as k is increased from 3.9 to 45.

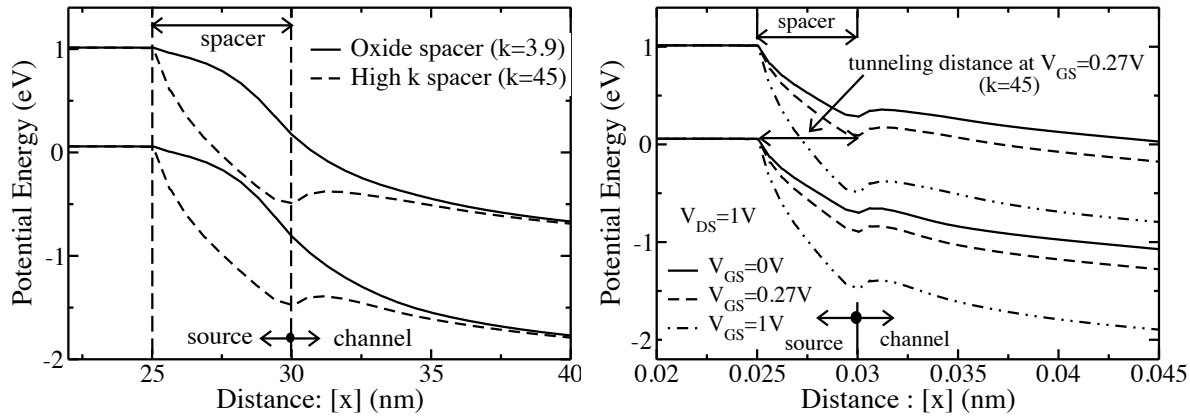


Figure 4.11: (a) Band diagram showing the reduction of tunneling width in nTFET when a high-k spacer ($k = 45$) is used. $V_{GS} = 1$ V and $V_{DS} = 1$ V. (b) Band diagram of the nTFET with spacer k of 45 for various values of V_{GS} ($V_{DS} = 1$ V).

This results are similar to that obtained with Kane's model and is due to increased fringe field through the high-k spacer as seen in Fig. 4.10. The increased electric field at the source-channel interface results into higher band bending (Fig. 4.11 (a)).

The tunnel current is seen to increase with spacer k only when the gate bias is typically beyond 0.25 V, depending on the spacer k, see Fig. 4.8. Below $V_{GS} = 0.2$ V, I_D-V_{GS} is seen to be independent of spacer k. This effect is also similar to the results obtained with Kane's model and can be explained in similar way as follows. It may be noted that at the source to channel junction, the band-diagram shows an upward shift for a short distance when the spacer k is different from the k of the gate dielectric. Fig. 4.11 (b) shows the band-diagram for spacer $k = 45$ at $V_{DS} = 1$ V and $V_{GS} = 0$, 0.27 and 1 V. When $V_{GS} = 0$, electrons tunnel from valance band at the outer edge of the spacer to the conduction band in the channel region. This is seen to continue till V_{GS} is close to 0.27 V. However at $V_{GS} = 0.27$ V, the tunneling would occur to the conduction band at the source to channel junction and the tunneling width decreases abruptly, leading to an abrupt change in the tunneling current seen in Fig. 4.8. As a consequence the OFF state current of these devices do not change significantly with spacer k. But the ON state current is significantly enhanced and the subthreshold slope decreases.

4.3.2 Effect of Spacer Dielectric on Tunneling Current of p-channel TFET

The p-channel TFET show a similar improvement in tunneling current as observed in Fig. 4.12. Geometry of the structures used is similar to Fig. 3.1 and doping is n^+-i-p with similar doping level and doping profile. Workfunction is 5.2 eV.

The enhancement of the fringe field enhancement improves the band bending as seen

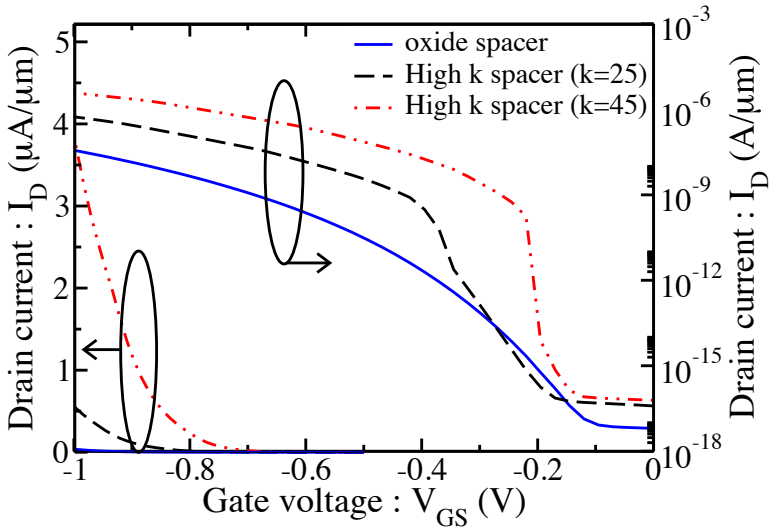
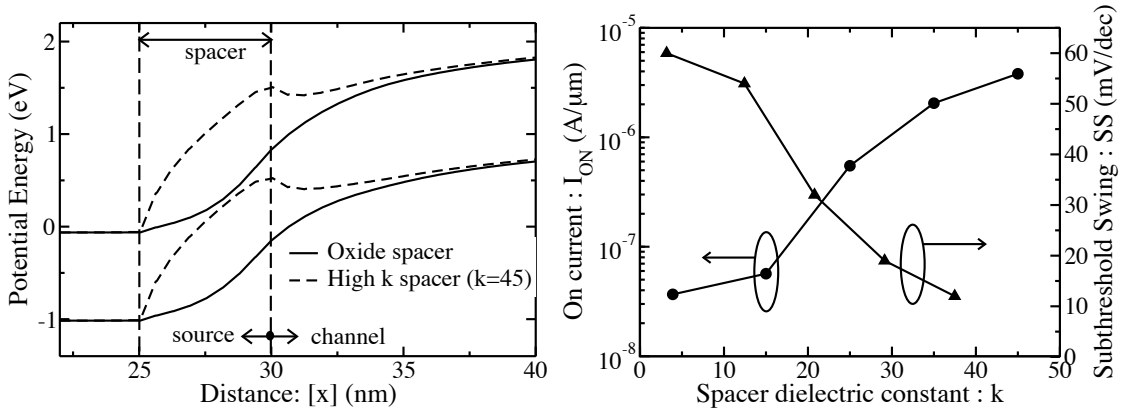


Figure 4.12: I_D-V_{GS} characteristics of Si pTFETs with spacer of various dielectric constants. Gate length = 20 nm, spacer thickness = 5 nm and V_{DS} = -1 V.



(a) (b)

Figure 4.13: (a) Band diagram showing the reduction of tunneling width in pTFET when a high-k spacer (k = 45) is used. V_{GS} = -1 V and V_{DS} = -1 V. (b) Effect of spacer dielectric constant on I_{ON} and average Subthreshold Swing of pTFET.

in Fig. 4.13 (a) giving higher tunneling currents. The I_{ON} increases and with increase in spacer dielectric constant (Fig. 4.13 (b)). This is consistent with the trend observed for nTFET.

4.4 Effect of High k Spacer Width

Even though the use of a high-k spacer seems to enhance the I_{ON}, a 5 nm spacer made of high-k material also increase the parasitic gate-drain and gate-source capacitance. We have studied the impact of spacer width on I_{ON} of nTFET. The results are shown in Fig. 4.14. It is seen that a narrow spacer result in better improvement of I_{ON}. As the spacer

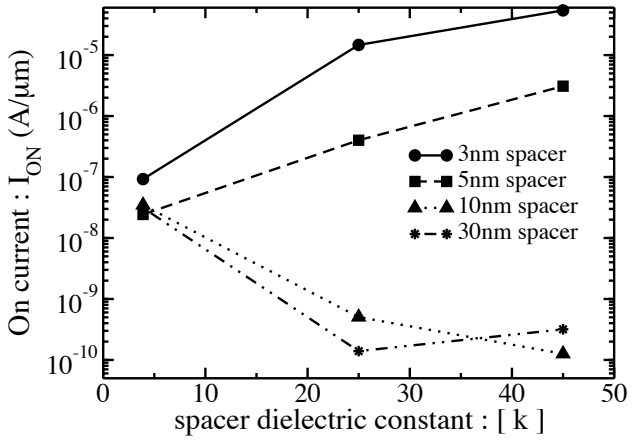


Figure 4.14: Impact of spacer width on I_{ON} of nTFET with the spacer k variation.

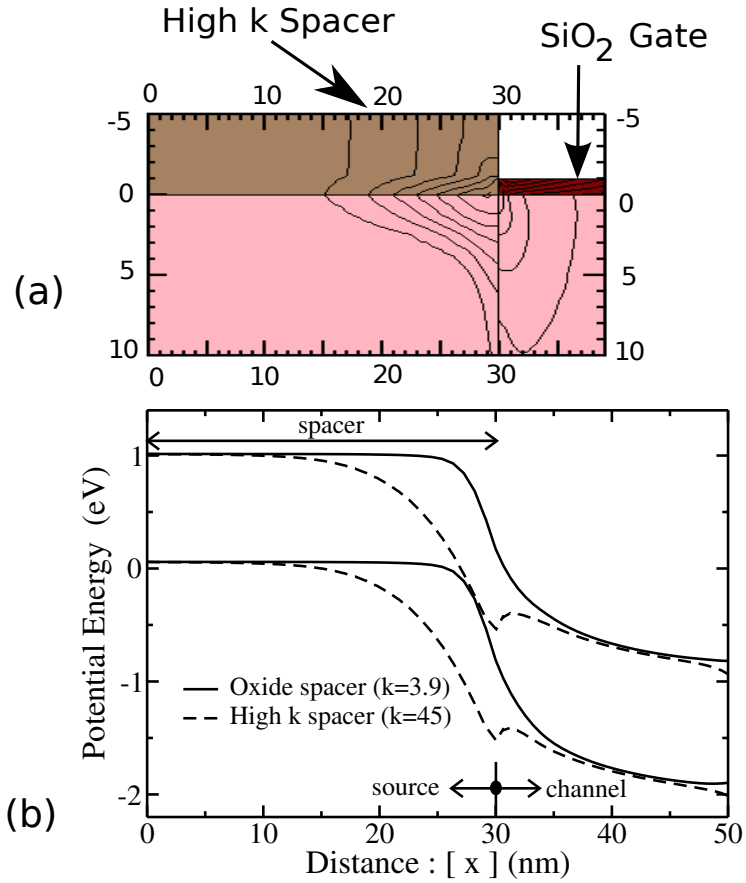


Figure 4.15: (a) Fringe field coupling through spacer (dimensions are in nanometers) and (b) band diagram for nTFET with high-k ($k = 45$) spacer of 30 nm width. $V_{GS} = 1$ V and $V_{DS} = 1$ V.

width is increased, I_{ON} is seen to reduce but is greater than nTFET with SiO_2 spacer upto spacer width of 5 nm. Beyond the spacer width of 5 nm, I_{ON} decreases below the

value for the Si nTFET with oxide spacers.

For the case of nTFET with 30 nm HfO_2 ($k = 25$) spacer, we observe from the band diagram (Fig. 4.15(b)) that the tunneling distance has increased as compared to nTFET with 30 nm SiO_2 spacer. This is because for larger spacer width, the fringe field through the spacer gets spread (Fig. 4.15(a)) and the band bending under the spacer occurs over a larger lateral distance as seen in Fig. 4.15 (b). This increases the tunneling width with increase in spacer width and tunneling currents decrease.

4.5 Conclusion

A novel concept of increasing the tunneling currents of a H-nTFET and silicon nTFET using high k spacer engineering is presented. The tunneling currents obtained for H-nTFET with local model is higher than that obtained with non local model. For the simple p-i-n structure with $t_{ox} = 1.1$ nm, replacing the oxide spacer with HfO_2 gives improvement in tunneling currents due to increased fringe field coupling through the high k spacers. Higher the k value of the spacer used, better is the I_{ON} and the subthreshold slope. Similar improvement in performance is obtained for pTFET. However this improvement is observed only for spacer width ≤ 5 nm. For spacer spacer width ≥ 5 nm, the fringe field through the high k spacer spreads resulting into decrease in tunneling currents.

In CMOS, the gate and source/drain contact are separated by a pre-metal isolation layer of SiO_2. Therefore, we would have a SiO_2 layer next to the proposed thin (≤ 5 nm) high-k spacer effectively forming a dual-k spacer. The effect of this dual-k spacer on nTFET is explained in the next chapter.

Chapter 5

Optimization of Tunnel FET with Dual k spacer

5.1 Introduction

The use of a thin layer of high-k (hk) spacer improves the performance of TFET as explained in the earlier chapter. In the conventional process flow of VLSI, the gate metal contact is isolated from the source/drain contacts by a pre-metal dielectric layer, usually made of SiO_2. When only a thin layer of high-k spacer is used, this pre-metal dielectric layer of SiO_2 will be located next to the thin high-k spacer as shown in Fig. 5.1. This gives us an effective configuration of a TFET with dual-k spacer which is explained in this chapter.

Dual-k spacer has been used with MOSFET to suppress short channel effects. The MOSFET structure proposed by Miyashita et al. [118] have a high-k off-set spacer formed prior to extension implants and a low-k (lk) spacer formed subsequent to extension implants. Lee et al. [119] have proposed the design of T shaped Gate MOSFET underlap

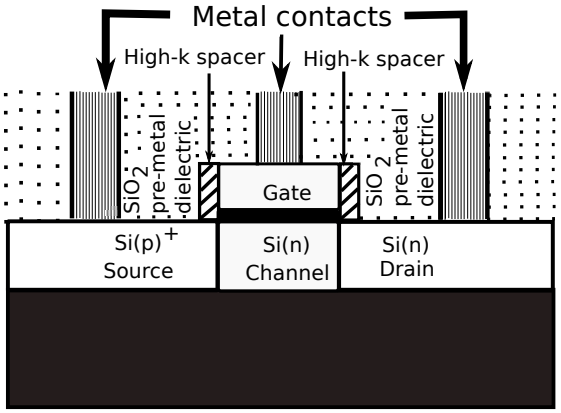


Figure 5.1: Si nTFET with thin layer of high-k spacer. The SiO_2 pre-metal dielectric layer isolates the gate contact from the source/drain contacts giving a dual-k spacer configuration.

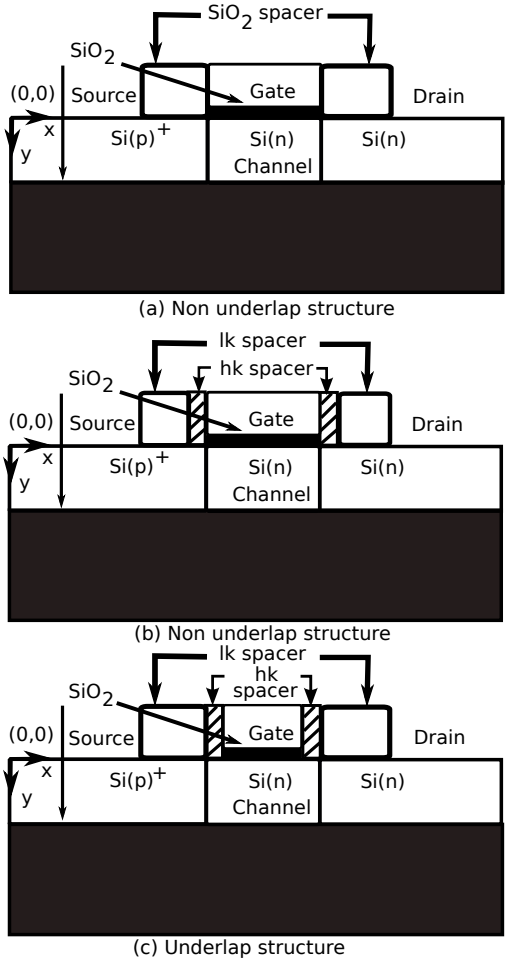


Figure 5.2: Silicon nTFET structures with dual-k spacer investigated in this chapter. (a) Non-underlap structure with SiO_2 spacer, (b) Non-underlap structure with dual-k spacer and (c) Underlap structure with dual-k spacer.

structure with dual-k spacer.

In this chapter, we have explored the use of dual-k spacer, similar to the approaches of Miyashita et al. and Lee et al., in TFETs to improve the performance. A dual-k spacer concept is also evaluated in underlap silicon nTFETs for the first time. The impact of the thickness and dielectric constant of the hk spacer along with the k of the gate dielectric on performance is investigated. The physical origin of this improvement is explained. Detailed explanation for nTFET is given first followed by the explanation for pTFET.

5.2 Optimization of n-channel TFET with Dual-k Spacers

5.2.1 Device Structure and Simulation Setup

Fig. 5.2 shows the structures of silicon n-channel TFET with dual-k spacer. The gate length is 20 nm for non-underlap structure and 16 nm for underlap structure. For non-underlap structure, an optimized thin hk layer is placed on either sides of the gate. On either side of this first spacer is another 8 nm SiO_2 layer (lk spacer). For the underlap structure, the optimized hk spacer is positioned over the intrinsic channel region creating an underlap at the source and drain. The width of this spacer is computed from the edge, which is common with the low-k spacer, to the edge closer to the gate. Hence the underlap created is equal to the hk spacer width. Next to the hk spacer is the lk spacer of 10 nm positioned on either side of the gate. An optimized hk spacer width of 2 nm is used and the spacer widths are kept fixed for entire work except for the study of spacer width variation.

The distance between the two outer edges of the lk spacers in both the structures described above is 40 nm. This ensures that both implementations would result in identical integration density, unlike the underlap schemes proposed in [44, 50] which comes with a significant integration penalty.

A two layer spacer using a thin SiO_2 inner layer and a thicker Si_3N_4 outer layer are common in state of the art CMOS technology, for example see Fig. 9 in [120]. The proposed spacer is similar, except for the dielectric constants of the materials used. Lee et al. [119] have proposed the design of T shaped gate MOSFET underlap structure with dual-k spacer along with the process flow for the fabrication of the same. Such spacers can be easily integrated in planar TFETs made by typical process flows reported in the literature, for example [50].

Gaussian doping profiles (Fig. 3.4 in chapter 3) with a peak density of 10^{20} cm^{-3} for source region and 10^{18} cm^{-3} for drain region, followed by doping gradients of 2 nm/dec are used. The channel is n-type doped with a concentration of 10^{17} cm^{-3}. The gate workfunction is fixed to 4.1 eV. The EOT of gate dielectric is fixed to 1.1 nm. A dielectric constant of 25 is used for the material HfO_2 for the entire results in this chapter.

5.2.2 Effect of Spacer Engineering using High k Material

Fig. 5.3 shows the I_D-V_{GS} characteristics at $V_{DS} = 1$ V for (a) single spacer with $k = 3.9$ (SiO_2) and non-underlap structure, (b) HfO_2 inner spacer and SiO_2 outer spacer with non-underlap structure and (c) HfO_2 inner spacer and SiO_2 outer spacer with underlap structure. The gate dielectric is 1.1 nm SiO_2. As V_{GS} increases from 0, we observe that

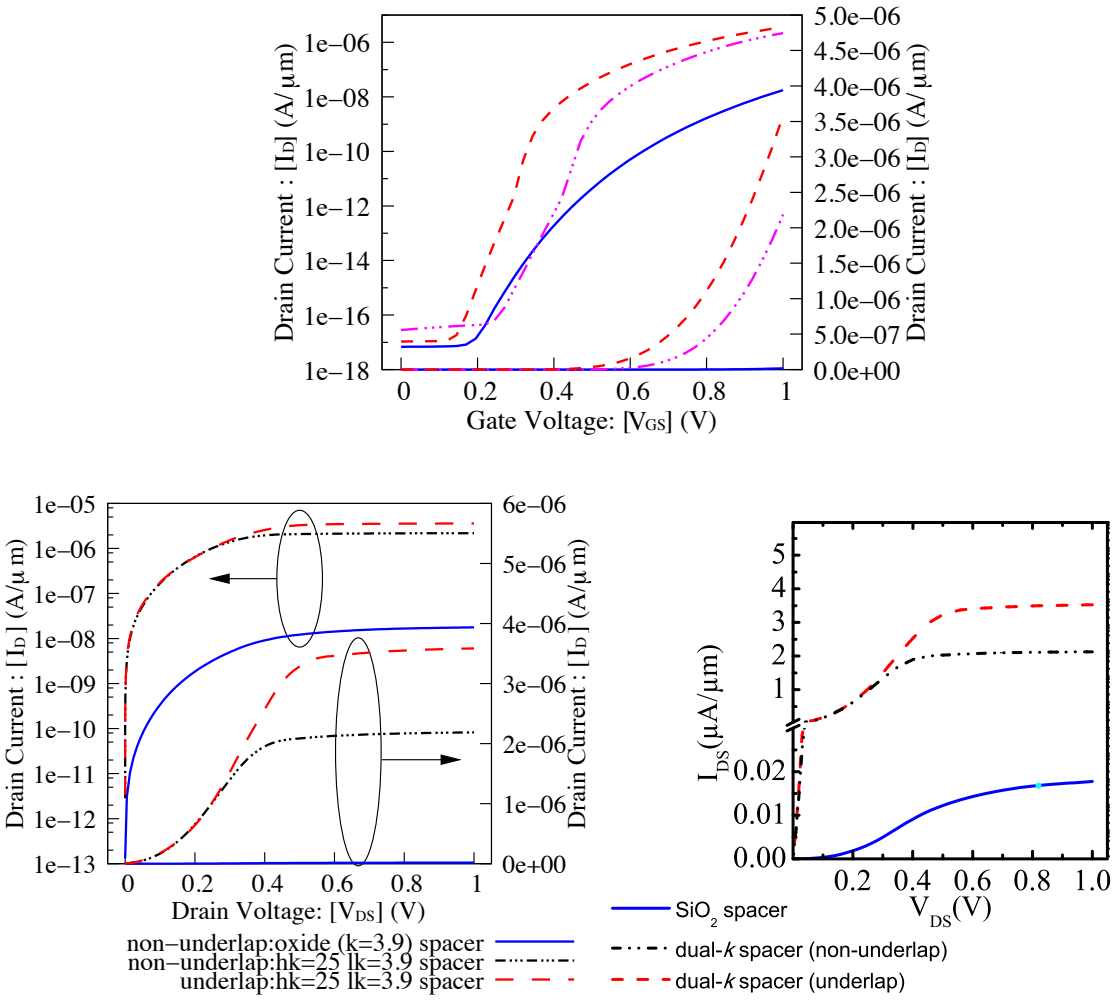


Figure 5.3: I_D-V_{GS} characteristic ($V_{DS} = 1$ V) and I_D-V_{DS} characteristic ($V_{GS} = 1$ V) for (a) non-underlap nTFET structure with SiO_2 spacer, (b) non-underlap nTFET structure with dual-k spacer made of HfO_2 and SiO_2 and (c) underlap nTFET structure with dual-k spacer made of HfO_2 and SiO_2. The gate dielectric is SiO_2 of 1.1 nm thickness.

the drain current, I_D, remains nearly flat till a certain V_{GS} and then it increases. The flat region of the characteristics gives us the OFF state current, I_{OFF} , of the device. We observe that the I_{OFF} is less than 10^{-16} A/μm in all the three cases. In fact the I_{OFF} is in this range for all the devices reported in this work. For most of the applications, the I_{OFF} specifications are much higher than this value and I_{OFF} is not discussed further for the same reason.

The I_{ON}, defined as the I_D at $V_{DS} = V_{GS} = 1$ V, is seen to increase consistently and substantially as we move from case (a) to (c). The improvement from a lk single spacer to a dual-k spacer is by more than two orders of magnitude. For the non-underlap structure of case (b), it may be noticed that the I_D-V_{GS} shows improvement in tunneling currents beyond 0.45 V. However for the underlap structure, the I_D-V_{GS} start to deviate from the other two cases for V_{GS} beyond 0.1 V.

Fig. 5.3 also shows the I_D-V_{DS} characteristics at $V_{GS} = 1$ V for the three cases considered. We observe identical improvement in the tunneling currents at low V_{DS} for case (b) and (c) as compared with the case (a). The shape of the I_D-V_{DS} characteristics also does not change at low V_{DS}. However, we observe an improvement in I_D-V_{DS} characteristics at high V_{DS}. We note that saturation is reached earlier in case (b) compared to case (c). The underlap structure gives the best output characteristic at higher V_{DS}.

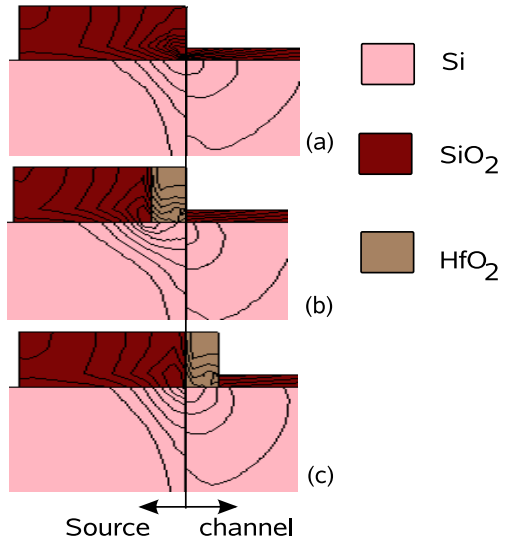


Figure 5.4: Fringe field coupling through spacer for the three cases shown in Fig. 5.3. $V_{DS} = V_{GS} = 1$ V.

Fig. 5.4 shows the electric field contours near and around the source-channel junction for the three cases described above. Considering the non-underlap structures with dual-k spacer, the gate fringe field coupling to the source-channel junction increases as compared to nTFET with oxide spacers. See Fig. 5.4(a) and Fig. 5.4(b). However the field lines are denser just outside of the p-i (source-channel) junction. The field lines can be made denser near the junction by shifting the hk spacer towards the channel as in the underlap structure, Fig. 5.4(c). These trends are consistent with the I_{ON} seen in Fig. 5.3.

The impact of gate field coupling on the tunneling process is further illustrated by the band diagrams shown in Fig. 5.5. The figure shows the band diagram just below the dielectric - semiconductor interface near the source - channel junction. In the figure, w_s and w_{dk} refer to tunneling width for the SiO_2 single spacer and dual-k spacer in non-underlap structures respectively. The same is referred in underlap structure with dual-k spacer by $w_{dk,ul}$.

Fig. 5.5(a) shows the comparison of single spacer (oxide) against the dual layer spacer in non-underlap structure. The electron tunneling distance from the source valance band to conduction band decreases from 6.3 nm to 5.7 nm as the single layer spacer is replaced with dual-k spacer. In fact, when a dual-k spacer is used, the tunneling happens within

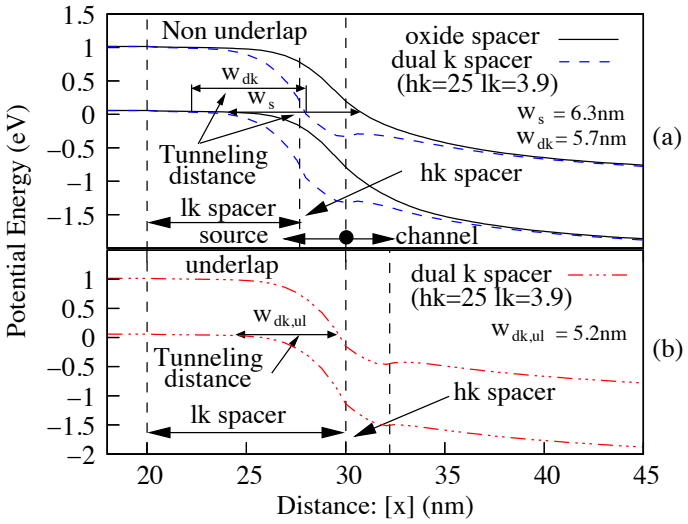


Figure 5.5: Band diagram for nTFET with (a) SiO_2 spacer and dual-k spacer in non-underlap structure and (b) dual-k spacer in underlap structure. The tunneling width is indicated by w_s and w_{dk} for the SiO_2 single spacer and dual-k spacer non-underlap structures respectively. The same is referred in underlap structure with dual-k spacer by $w_{dk,ul}$. $V_{DS} = V_{GS} = 1$ V.

the source region itself. Fig. 5.5(b) shows that the tunneling distance can be further reduced to 5.2 nm with dual-k spacer in an underlap structure.

In Fig. 5.3, we had also noticed that the I_D-V_{GS} with the dual-k material in the spacer shows a marked deviation compared to the I_D-V_{GS} of nTFET with single SiO_2 spacer case. For the dual-k spacer in non-underlap structure, the I_D-V_{GS} shows a prominent deviation beyond $V_{GS} = 0.45$ V. The reason for this deviation can be understood by studying the band diagram shown in Fig. 5.6. The band diagrams are plotted for $V_{GS} = 0$, 0.45 V and 1 V. Additional band bending in the conduction band and valance band can be noticed at the source-channel junction. This is due to the fact that the source doping is 10^{20}cm^{-3} and the bandgap narrowing in the source shows up as a lowering of the band energy level. For low values of V_{GS}, the tunneling is from the valance band in the source to conduction band in channel silicon. However as the V_{GS} is increased, the tunneling distance decreases and as it approaches 0.45 V, the tunneling happens from the valance band in the source to the conduction band at the junction. Just below 0.45 V, the tunneling would be to the channel and the deviation in I_D-V_{GS} marks the beginning of tunneling to the source itself. The gate voltage at which the destination of tunneling changes from channel to source happens at lower gate voltages for the underlap structure, resulting in a significant improvement in the SS as well.

In Fig. 5.3, as the drain current start increasing beyond I_{OFF} , it may be noticed that for the single spacer device, the SS is the minimum for low I_D. SS is seen to decrease as V_{GS} is increased further. This is consistent with literature data, where low values of SS ($<$ 60 mV/decade) are experimentally observed only for low values of I_D and not the

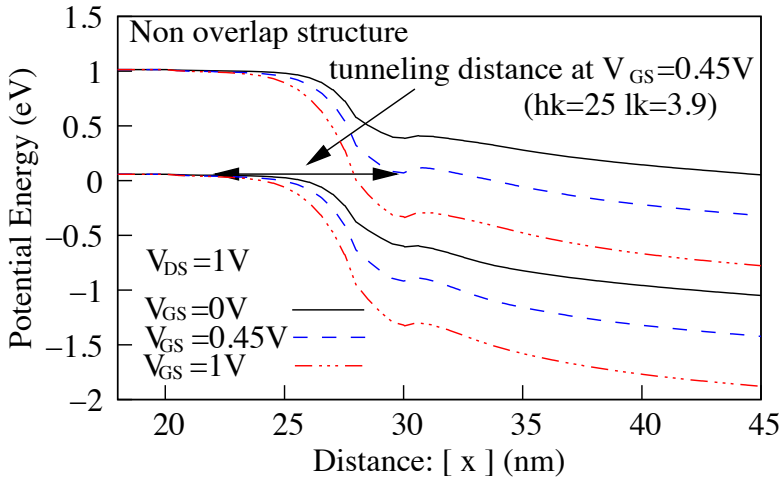


Figure 5.6: Band diagram of the nTFET with dual-k spacer and non-underlap structure. The spacer k is 25 and the band diagrams are shown for various values of V_{GS}. The gate dielectric is SiO_2 of 1.1 nm thickness.

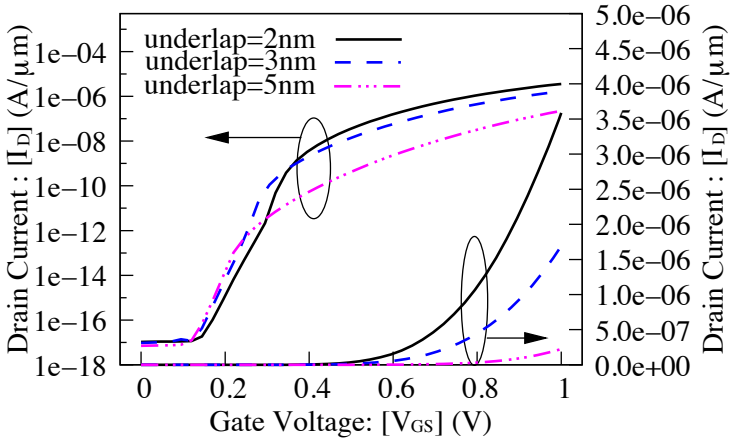


Figure 5.7: Effect of hk spacer width variation on I_D-V_{GS} characteristic of the underlap structure (V_{DS} = 1 V). The gate dielectric is SiO_2 of 1.1 nm thickness.

entire subthreshold regime [13, 25, 50, 70]. This results in a high average SS, even though the spot SS is better than 60 mV/decade at low currents. It may be noticed that the dual-k spacer result in low SS for a larger V_{GS} range. The SS improves further beyond I_D of 10^{-12} A/μm before it tapers off. This results in better average SS for the devices with dual-k spacer. We have further investigated this observation by simulating the underlap structure with different values for the underlap (or the width of the hk spacer).

Fig. 5.7 shows the I_D-V_{GS} plot for the underlap device as the underlap is varied from 2 nm to 5 nm. HfO_2 is used the hk material. For an underlap of 3 nm, the behavior of the curve is similar to that for the 2 nm case, which was described above. However the subthreshold slope improves compared to the 2 nm case, whereas the I_{ON} decreases. As we increase the underlap further to 5 nm, the subthreshold slope for low I_D is seen

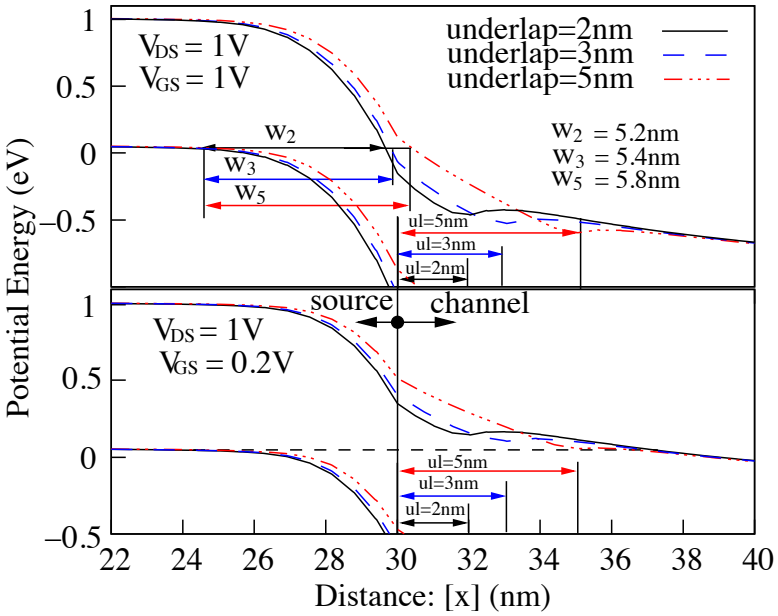


Figure 5.8: Band diagram corresponding to the I_D-V_{GS} shown in Fig. 5.7 for two gate voltages. Tunneling width is indicated by w and ul refers to the the underlap. For V_{GS} = 0.2 V, the tunneling path is indicated by the horizontal broken line.

to improve further. However the I_D tapers off beyond 10^{-12}A/μm. The I_{ON} decreases substantially.

Fig. 5.8 shows the band diagram for various underlap (ul = underlap length) values discussed above. The band diagrams are shown for V_{GS} = 0.2 V (lower half) and V_{GS} = 1 V (upper half). For V_{GS} = 0.2 V, a typical value for which $I_D < 10^{-13}$ A/μm, the tunneling width indicated by the horizontal discontinuous line, is the lowest for ul = 5 nm. The tunneling width increases marginally as the ul is reduced. This is consistent with the trend in I_D and SS seen at such low voltages in Fig. 5.7. It may be also noticed that the tunneling is from the source to channel region in this bias range for all the ul values shown.

For V_{GS} = 1 V, the lowest tunneling width, indicated by w, is seen for ul = 2 nm and the tunneling width increases as we increase the ul. This is consistent with the trend in I_{ON}. The observations and discussions so far can be summarized as follows. The use of a dual-k spacer as proposed, result in concentration of the fringe fields through the spacer in the region under the interface between the two spacers. For large values of V_{GS}, this field can be enhanced as we reduce the width of the hk layer in the dual-k spacer.

5.2.3 Device Optimization

In this section we would investigate device optimization by varying the k and width of the spacer layers, the underlap length and the k of the gate dielectric.

In Fig. 5.3 we had seen that the underlap structure gives better I_{ON} than the nonun-

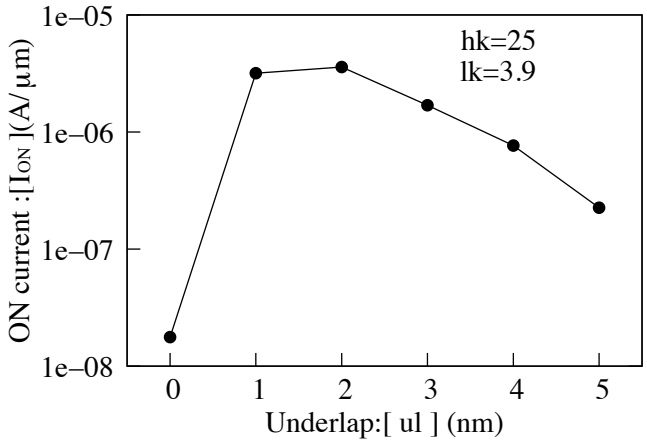


Figure 5.9: Effect of hk spacer width on I_{ON}. The hk spacer has a k of 25 (HfO_2). The gate dielectric is SiO_2 of 1.1 nm thickness.

derlap structure without any significant degradation in I_{OFF}. This was seen consistently and hence only the underlap structure is explored further for performance optimization.

Fig. 5.9 shows the effect of variation in width of hk layer (k = 25) on the I_{ON} for the underlap structure. The hk spacer width is equal to the gate-source/drain underlap. As the hk spacer width is increased, the gate length decreases. For example ul = 2 nm, L_G = 16 nm and for ul = 5 nm, L_G = 10 nm. The lk spacer is SiO_2 with a fixed width of 10 nm. The optimum value of underlap for hk = 25 is seen to be 2 nm. Even though other values of ul may give better SS in a limited range (Fig. 5.7), the best I_{ON} is observed for ul = 2 nm.

For underlap length of 0 (corresponds to a single layer spacer (Fig. 1.2(a))as the hk spacer thickness would be zero), the fringe field is spread through the lk dielectric. As

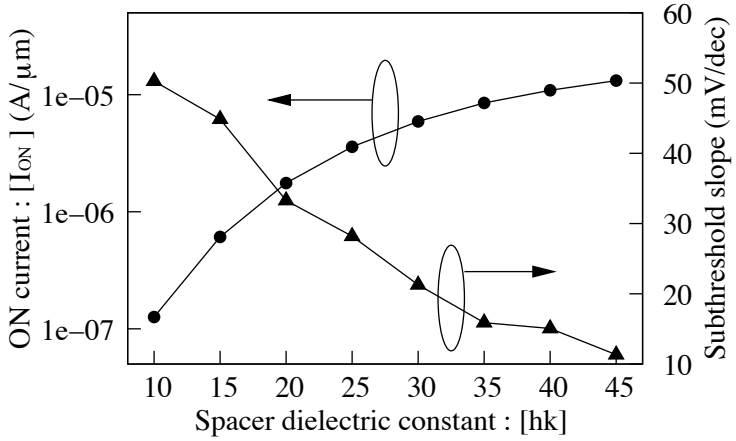


Figure 5.10: Effect of the k of the hk spacer on DC characteristics of the underlap nTFET with dual-k spacer. The lk spacer is made of SiO_2. Thickness of the hk spacer is 2 nm and the thickness of the lk spacer is 10 nm. The gate dielectric is SiO_2 of 1.1 nm thickness.

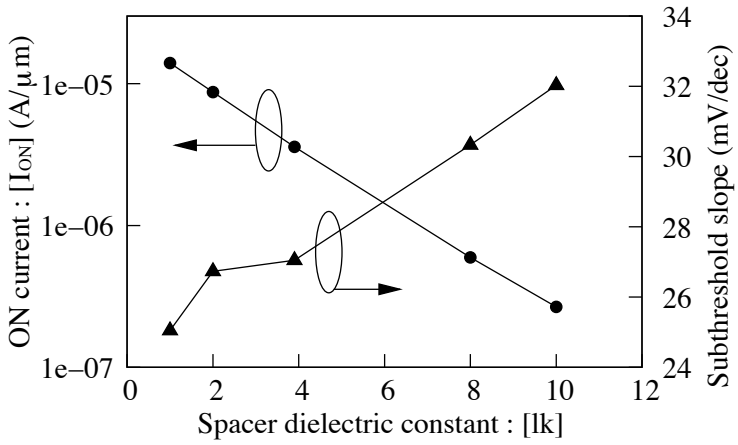


Figure 5.11: Effect of the k of the lk spacer on DC characteristics of underlap nTFET with HfO_2 ($k = 25$) inner spacer of width 2 nm. The gate dielectric is SiO_2 of 1.1 nm.

the hk spacer is introduced, there is a significant concentration of the fringe field near the junction. Hence the I_{ON} increases as the hk spacer width increases upto a spacer width of $\sim$ 2 nm. As the hk thickness is further increased, the fringe field coupling through it spreads reducing the electric field at the source-channel junction. This results in an optimum value for the hk spacer width.

Fig. 5.10 shows the effect of the k of the hk spacer on the I_{ON} and SS of the underlap structure. The hk spacer thickness is fixed to 2 nm and the lk spacer thickness is fixed to 10 nm. It is seen that the I_{ON} increases consistently. The SS is found to decrease consistently as the k increases from 10 to 45.

Fig. 5.11 shows the effect of the k of the lk spacer on the I_{ON} and SS of the underlap structure. It is seen that the I_{ON} decrease consistently with increase in lk value. The SS is found to increase consistently as the k is varied from 1 to 10. The optimal performance is for lk = 1 which represents the case of air spacer [121].

5.2.4 Impact of Gate Dielectric on n-channel TFET with Dual k Spacer

A SiO_2 gate dielectric with a thickness of 1.1 nm was used in all the simulations presented so far. However for this range of EOT, use of high-k dielectrics in the gate stack is inevitable due to the high leakage current in thin SiO_2. However using a high-k gate dielectric could change the fringe field distribution in MOSFETs [117] and in TFETs [55].

In this section we consider the impact of hk gate dielectric on the performance of underlap TFET with dual-k spacer. Effective oxide thickness of the gate dielectric is fixed to 1.1 nm and four different scenarios are considered for the gate dielectric: (i) SiO_2 with dielectric constant of 3.9 (ii) Al_2O_3 ($k = 9.6$) (iii) HfO_2 ($k = 25$) and (iv) a stack of

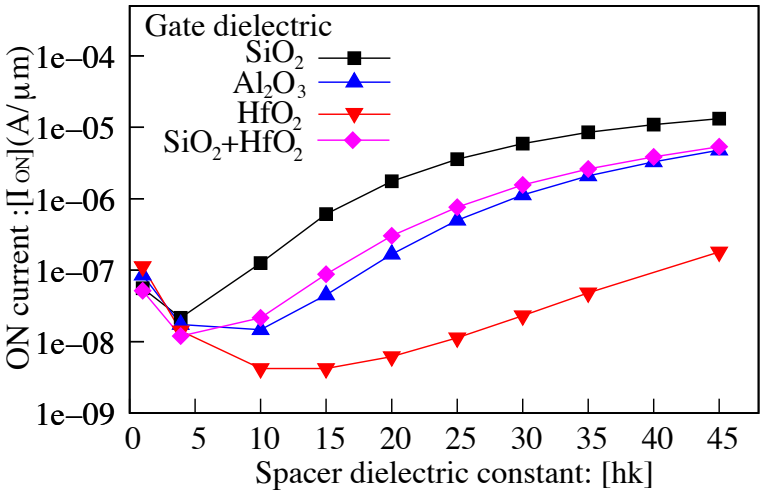


Figure 5.12: Effect of variation of hk spacer dielectric on I_{ON} of an underlap nTFET with dual-k spacer and gate dielectric (EOT = 1.1 nm) of (i) SiO_2 (ii) Al_2O_3 ($k = 9.6$) (iii) HfO_2 ($k = 25$) and (iv) SiO_2 (physical thickness = 0.8 nm) + HfO_2 (physical thickness = 1.9 nm). The physical thickness of hk spacer is 2 nm and the k is varied. The lk spacer is 10 nm of SiO_2.

0.8 nm SiO_2 and 1.9 nm of HfO_2. Case (iv) corresponds to a more realistic scenario for silicon technology and has an effective k value of 9.6 (same as Al_2O_3). The lk spacer is 10 nm SiO_2 and the thickness of the hk spacer is fixed to 2 nm and the k is varied.

Fig. 5.12 shows the I_{ON} for the four cases versus the k of the hk spacer. The k is varied from 1 (air) to 45. For $k = 1$, the device with HfO_2 as gate dielectric is seen to have the highest I_{ON}. The I_{ON} decreases as the gate dielectric k decreases. As the k of the spacer high-k is increased beyond 1, the I_{ON} is seen to decrease for all the four gate dielectrics considered. The I_{ON} hits a minimum and subsequently increases as the k of the hk spacer is increased to high values. It may be noticed that the minimum value of I_{ON} is lower for higher gate dielectric k. Higher the k value of the gate dielectric, higher is the k value of the hk spacer for which the I_{ON} is minimum. For example, the I_{ON} for SiO_2 gate dielectric is minimum for a spacer hk around 3.9, whereas the minimum for HfO_2 gate dielectric occurs for a spacer hk of 15.

As can be seen in Fig. 5.12, for any given value of the dielectric constant of the gate dielectric, the performance improvement seem to saturate for very high value of the k of the hk spacer. For example, for SiO_2 gate dielectric, the performance is seen to saturate beyond a k of 40 for hk spacer. For higher gate dielectric constant, the saturation is seen to happen at higher k of the hk spacer.

Fig. 5.13 shows the electric field in the semiconductor along the channel direction and just under the level of the gate dielectric for all the four cases shown in Fig. 5.12, for a HfO_2 (k = 25) hk spacer. The field peaks just at the junction and it is seen that the peak field reduces as the gate dielectric is changed from SiO_2 to Al_2O_3 to HfO_2. The

peak field for SiO_2 + HfO_2 combination is lower than SiO_2 and higher than Al_2O_3. These observations are consistent with the trend in the I_{ON}.

We observe from Fig. 5.12 that the I_{ON} improvement obtained by use of high k spacer is least for the case (iii) of HfO_2 gate dielectric which is consistent with the observations by Anghel et al [60], A. Chattopadhyay and A. Mallik [61]. Depositing a high k gate dielectric directly on Si results into degraded mobility and poor reliability. To overcome this drawback, an interfacial layer of SiO_2 is formed before high k gate deposition. Such a scenario corresponds to case (iv) where an interfacial layer of 0.8 nm SiO_2 is formed, above which the high k layer of 1.9 nm HfO_2 layer is deposited thereby maintaining the same EOT of 1.1 nm. The use of this gate dielectric arrangement gives an improvement of more than two orders of magnitude in I_{ON} for hk = 45 (compared to case for hk=3.9) in contrast to low I_{ON} for gate dielectric of only HfO_2 layer.

We now compare our data with the published results of similar study of enhancing I_{ON} of TFET by enhancing electric field at source-channel junction [55, 60, 61]. Schlosser et al. [55] have predicted an increase in I_{ON} due to enhanced external fringe coupling from the side walls of the high k gate dielectric (no spacers were used). He noted that a spacer is not required in the case of a TFET as no extension or halo implants are required. Consequently most of their simulations were done using a structure without any spacer. Using such a structure, they reported a 2 orders of magnitude improvement in ON state current in n-channel TFETs as the k of gate dielectric is varied from 3.9 (SiO_2) to 200 for V_{GS} = 2 V, V_{DS} = 1 V and gate dielectric EOT of 2 nm. It was further noted that the drain current reduces by a factor of 2 when a SiO_2 spacer was used. This enhanced fringing field while degrading the scalability of conventional MOSFETs [117] was shown to improve TFET performance [55].

We would like to point out that a transistor used in an integrated circuit should

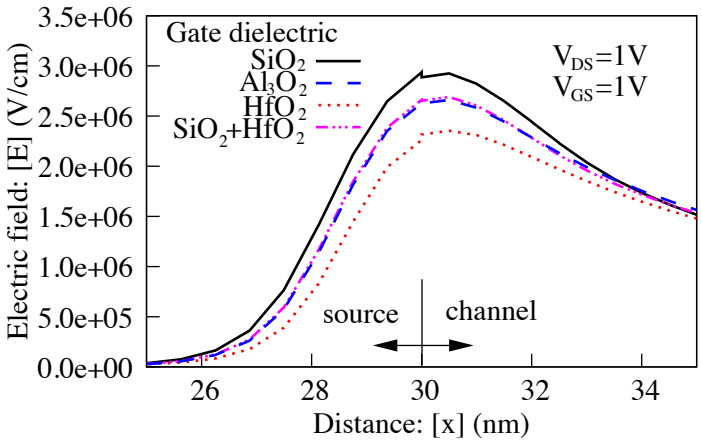


Figure 5.13: Effect of the gate dielectric on the electric field below the top surface of the semiconductor for an underlap nTFET with dual-k spacer for the four cases shown in Fig. 5.12. The hk spacer is HfO_2 with physical thickness of 2 nm and k of 25. The lk spacer is 10 nm of SiO_2.

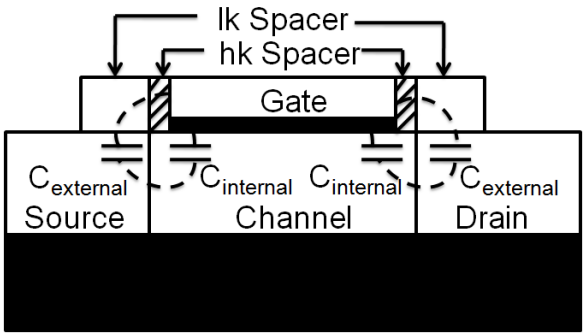


Figure 5.14: Conceptual model depicting electric field coupling through (a) external field (fringe field via the spacer) and (b) internal field (fringe field via gate dielectric).

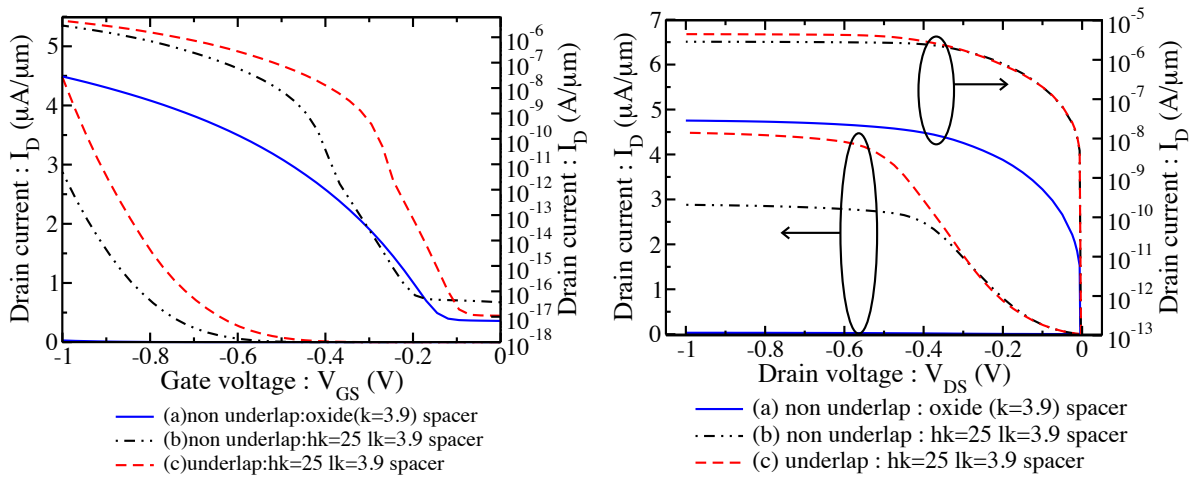
be isolated from on-chip wiring. For this purpose typically an isolation oxide, know as pre-metal dielectric is used in conventional CMOS technology. Fringe fields through such isolation dielectrics may not be completely ignored in a TFET, even though an intentional spacer may not be required in a TFET. An extreme case for the isolation dielectric would be air (k = 1).

Anghel et al. [60] and A. Chattopadhyay along with A. Mallik [61] have reported that using a low k spacer used along with high k gate dielectric (HfO_2) improves the I_{ON} whereas high-k spacer used with high-k (HfO_2) gate dielectric deteriorates the I_{ON}. Study of spacer with k value greater than that of (HfO_2) gate dielectric is not done.

In the underlap structure we have used, it is observed (Fig. 5.12) that the I_{ON} for a high-k spacer with $k = 1$, is higher for a HfO_2 gate dielectric than for a SiO_2 dielectric. This result is similar to the cases presented by Schlosser et al. [55] and Anghel et al. [60]. Consistent with these reported results [55, 60, 61], we also notice that the I_{ON} decreases as the spacer k is increased to 3.9 (SiO_2) for the HfO_2 gate dielectric. From Fig. 5.12, we observe that for HfO_2 ($k = 25$) gate dielectric, I_{ON} at spacer $k = 25$ is less than that at spacer $k = 1$ and at spacer $k = 3.9$. This is consistent with the observations of Anghel et al. [60], A. Chattopadhyay and A. Mallik [61]. An improvement is observed for the of case HfO_2 ($k = 25$) gate dielectric only at spacer k values much greater than that of the gate dielectric ($k = 25$) value.

A. Chattopadhyay and A. Mallik have also reported that a high k spacers improves the I_{ON} for an underlap TFET with SiO_2 gate dielectric consistent with the observation in Fig. 5.12

Our data and the results of Schlosser et al., Anghel et al., A. Chattopadhyay and A. Mallik can be explained consistently by the conceptual model shown in Fig. 5.14. The gate voltage is coupled to the source-channel junction and the region around it through the gate dielectric and the spacer (intentional or as demanded by the isolation requirements in an integrated circuit). The fringe fields through the gate dielectric may be termed as internal and that through the spacer external. When the dielectric constant and thickness



(i) (ii)

Figure 5.15: (i) I_D-V_{GS} characteristic ($V_{DS} = 1$ V) and (ii) I_D-V_{DS} characteristic ($V_{GS} = 1$ V) for (a) non-underlap pTFET structure with SiO_2 spacer, (b) non-underlap pTFET structure with dual-k spacer made of HfO_2 and SiO_2 and (c) underlap pTFET structure with dual-k spacer made of HfO_2 and SiO_2. The gate dielectric is 1.1 nm SiO_2.

of the spacer and the gate dielectric are such that the two fringe fields are balanced, the gate potential is coupled over a large distance. This would result in low electric field and hence low tunneling current. This would explain the minima seen in Fig. 5.12. When the internal fringing field is enhanced in comparison with the external fringe field by using a higher k for the gate dielectric than that used for the spacer, the gate potential is mainly coupled through the gate dielectric over a smaller distance than the scenario where the fringe fields are balanced. Correspondingly, the I_{ON} increases as we move to the left of the minima seen in Fig. 5.12. An extreme case of this scenario is to completely remove the spacer, confining all the field coupling through the gate dielectric, as considered in [55]. Similarly, when the spacer k is higher than that of the gate dielectric used, the gate potential is mainly coupled through the spacer to the source region just outside of the junction (see Fig. 5.8). This again leads to a higher field than the balanced case. Correspondingly the I_{ON} increases as we move to the right of the minima.

5.3 Optimization of p-channel TFET with Dual k spacers

The p-channel TFET show a similar improvement in tunneling current as observed in Fig. 5.15. Geometry of the structures used is similar to Fig. 5.2 and doping is n^+-i-p (source-channel-drain) with similar doping level and doping profile.

The mechanism of fringe field enhancement improves the band bending as seen in Fig. 5.16(i) giving higher tunneling currents. Optimal underlap is also 2 nm for pTFET with

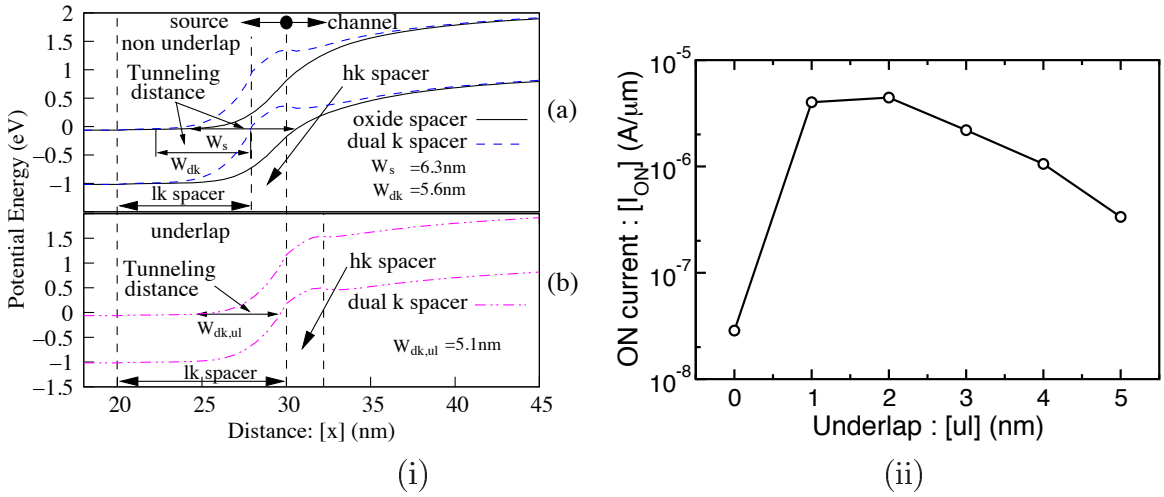


Figure 5.16: (i) Band diagram for pTFET with (a) SiO_2 spacer and dual-k spacer in non-underlap structure and (b) dual-k spacer in underlap structure. The tunneling width is indicated by w_s and w_{dk} for the SiO_2 single spacer and dual-k spacer non-underlap structures respectively. The same is referred in underlap structure with dual-k spacer by $w_{dk,ul}$. $V_{DS} = V_{GS} = 1$ V. (ii) Effect of underlap variation on I_{ON} of the underlap structure. The hk spacer has a k of 25 (HfO_2). The gate dielectric is 1.1 nm SiO_2.

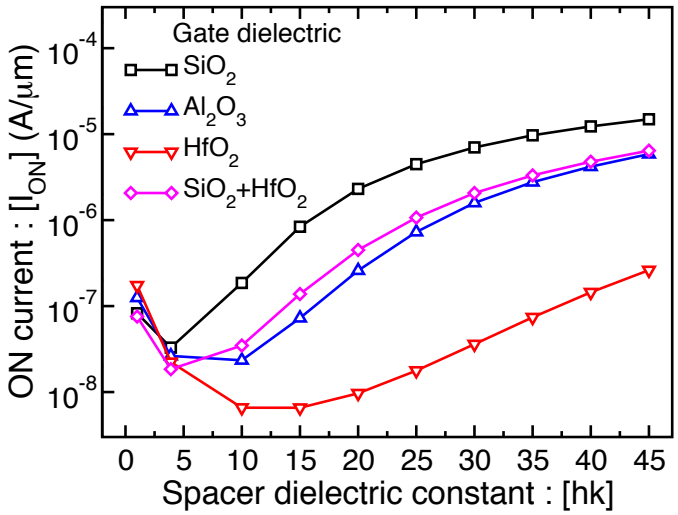


Figure 5.17: Effect of variation of hk spacer dielectric on I_{ON} of an underlap pTFET with dual-k spacer and gate dielectric (EOT = 1.1 nm) of (i) SiO_2 (ii) Al_2O_3 ($k = 9.6$) (iii) HfO_2 ($k = 25$) and (iv) SiO_2 (physical thickness = 0.8 nm) + HfO_2 (physical thickness = 1.9 nm). The physical thickness of hk spacer is 2 nm and the k is varied. The lk spacer is 10 nm of SiO_2

dual-k spacer as seen in Fig. 5.16(ii).

The effect of different gate dielectric on pTFET with dual-k spacer is also similar and has the same physical explanation as the nTFET as seen in Fig. 5.17.

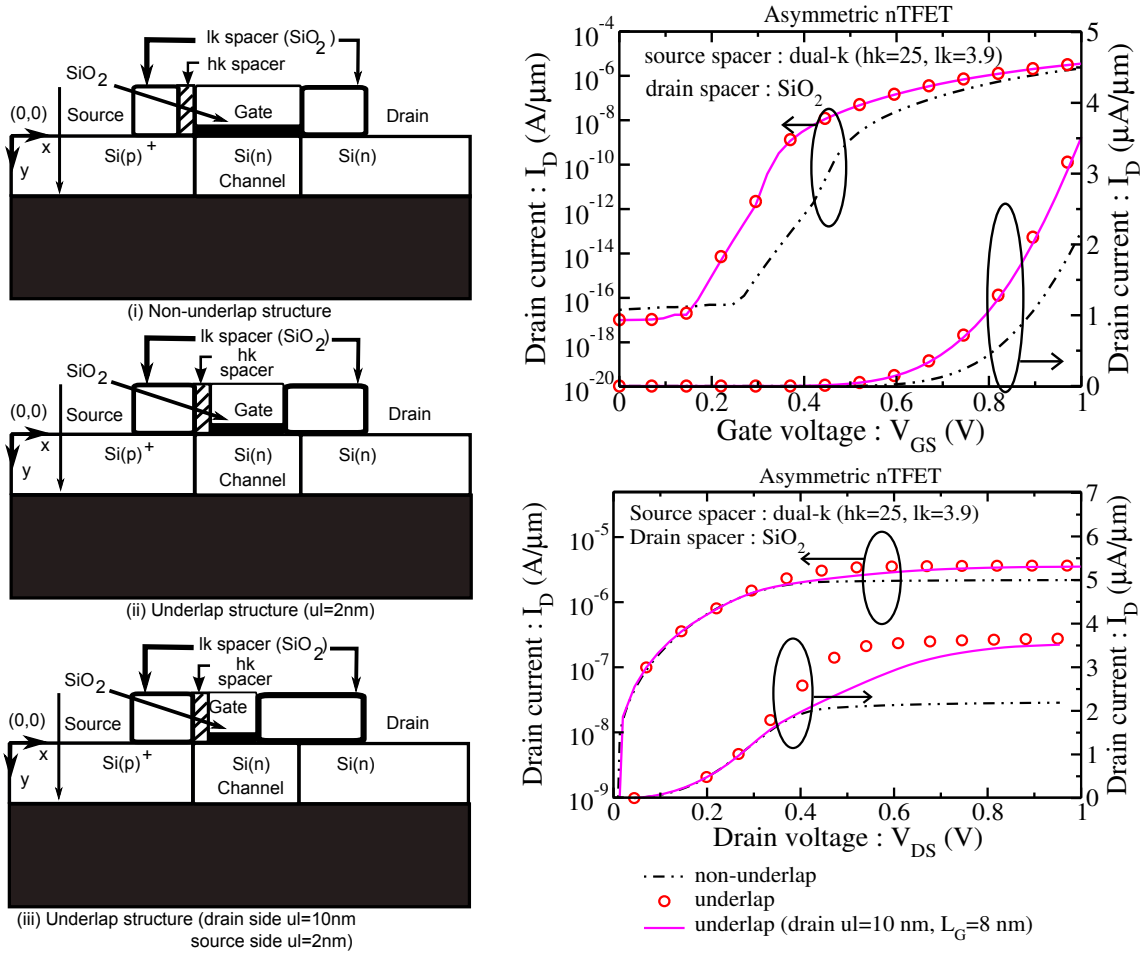


Figure 5.18: (a) **Asymmetric** nTFET structures with dual-k spacer. (i) Non-underlap structure, (ii) Underlap structure (drain side ul = 2 nm) and (iii) Underlap structure (drain side ul = 10 nm). (b) I_D-V_{GS} and I_D-V_{DS} characteristics of TFETs shown in (a).

5.4 Asymmetric TFETs with Dual k Spacers

The use of high k dielectric as spacer material increases the device parasitic capacitance. The I_{ON} in TFET is dominated by the electric field at source-channel region. Therefore using a shorter gate with a higher gate drain underlap or dual k material gate (high k at source side and low k at drain side) does not change the I_{ON}. Hence replacing the dual k spacer at the drain end would not substantially reduce the I_{ON}, but would reduce the device capacitance. This would give improved circuit performance at the cost of increasing the fabrication complexity. Such device structures are shown in Fig. 5.17 for both non-underlap and underlap case. One more underlap structure, similar to the structure in (ii) but with gate-drain underlap of 10 nm (gate length of 8 nm) is also shown. These devices are referred as asymmetric TFETs.

The I_D-V_{GS} and I_D-V_{DS} characteristics of these asymmetric TFETs are shown in Fig. 5.17. We observe that there is no significant change in I_D-V_{GS} characteristics compared

to symmetric TFET structures for case (i) and (ii). In case (iii) with 10 nm channel-drain underlap structure, the output characteristic shows saturation much later as compared to the 2 nm undelap structure and I_{ON} reduces marginally by about 4 %. Due to the small gate length of 8 nm over 20 nm channel, the band banding does not occur uniformly across the whole channel. The band banding near the source side is more due to the effect of the gate bias compared to band banding towards the drain side which has the SiO_2 spacer over it. The overall band banding is lesser than that for the full gate TFET (case(ii)). This results into higher tunneling distance and lower I_{ON}. Also at lower V_{DS}, due to lesser band bending compared to full gate TFET (case(ii)), the I_{DS} rise to saturation occurs at higher V_{DS}.

5.5 Conclusions

The fringe fields through spacer can be engineered to improve the performance of tunnel FETs. It is shown that the fringe fields coupling to the source - channel junctions can be improved by using a dual-k spacer with a high-k inner layer and a low-k outer layer, and by using a underlap structure. I_{ON} improves as the inner spacer k is increased and the outer spacer k is reduced. The gains due to the high-k in the spacer is diminished when a high-k material is used for the gate dielectric. Replacing the drain side dual-k spacer by SiO_2 spacer has no effect on the tunneling currents of non-underlap and underlap TFET (ul = 2nm). However for larger gate-drain underlap, a marginal reduction in I_{ON} and late saturation in output characteristic is observed.

The impact of high-k spacer on TFET capacitances are detailed in the next chapter.

Chapter 6

Capacitance of n-channel TFET with Dual k spacer

6.1 Introduction

The higher ON state current observed using dual-k spacer is attributed to the concentration of gate to source fringe fields near the junction. This could manifest as an increase in device capacitance. The capacitance of nTFET with dual-k spacer has been evaluated in this chapter for symmetric and asymmetric structures. The pTFET exhibits almost identical C-V characteristics.

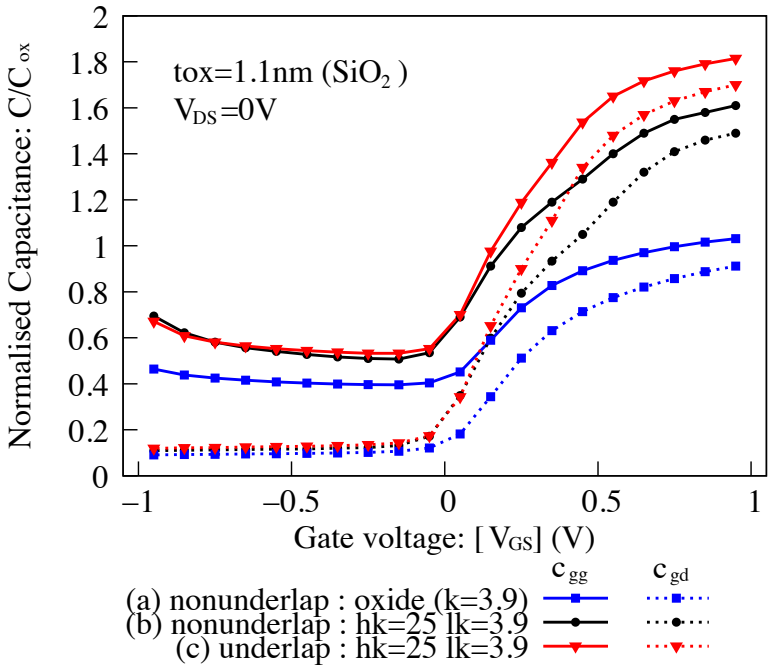


Figure 6.1: Capacitance - voltage characteristics for symmetric structures showing the gate and gate-to-drain capacitances as a function of gate-to-source voltage, V_{GS} for the three cases shown in Fig. 5.2. The gate dielectric is 1.1 nm SiO_2. $V_{DS} = 0$ V.

6.2 Capacitance of Symmetric n-channel Tunnel FET

The gate capacitance (C_{gg}) is entirely dominated by gate-to-drain (C_{gd}) capacitance in TFETs under all bias conditions in contrast to MOSFETs, where both C_{gs} and C_{gd} contribute [107]. For a symmetric spacer structure, both C_{gg} and C_{gd} could increase as we use a high-k material in the spacer. Since C_{gd} is also more important from a circuit perspective, it is extracted along with the gate capacitance, C_{gg}.

The C_{gg} and C_{gd} for the three cases considered in Fig. 5.2 are plotted in Fig. 6.1. The capacitances are normalized to C_{ox}, the capacitance of the gate dielectric (1.1 nm SiO_2) per unit area. As reported in [109], C_{gg} and C_{gd} have comparable values in TFETs. From Fig. 6.1, we observe that both C_{gg} and C_{gd} increases when dual-k spacer is used. For the non underlap structure with dual-k spacer both the capacitances are 1.6x that for the same structure with SiO_2 spacer. In the case of underlap structure, it is about 1.8x times higher compared to the structure with SiO_2 spacers.

The higher capacitances for the dual-k spacer could potentially degrade the circuit performance. However the I_{ON} increases by 2 orders of magnitude when the dual-k spacer is used, Fig. 5.2. This is significantly higher compared to the increase in capacitances. Both the I_{ON} and fringe capacitance would increase due to the increase in fringe electric field. However the tunneling current is exponentially dependent on the field, whereas

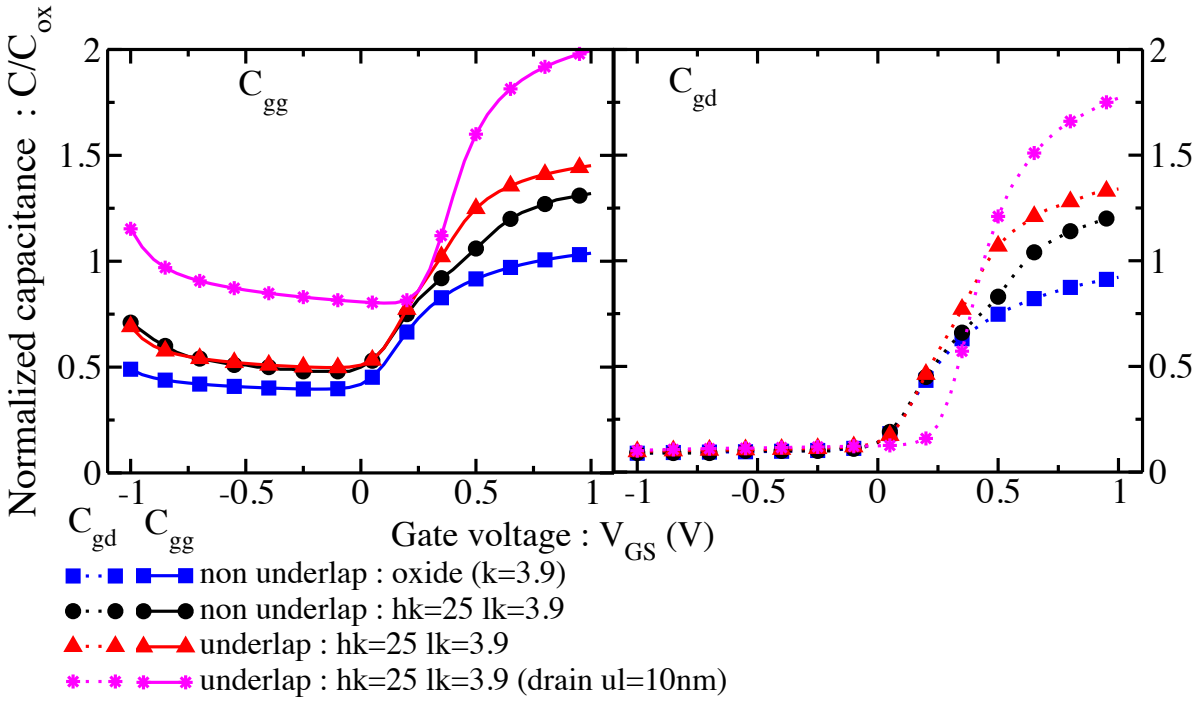


Figure 6.2: Capacitance - voltage characteristics for **asymmetric** structures showing the gate and gate-to-drain capacitances as a function of gate-to-source voltage, V_{GS} for the three cases shown in Fig. 5.18. The drain side spacer is replaced with a single SiO_2 spacer. The gate dielectric is 1.1 nm SiO_2. $V_{DS} = 0$ V.

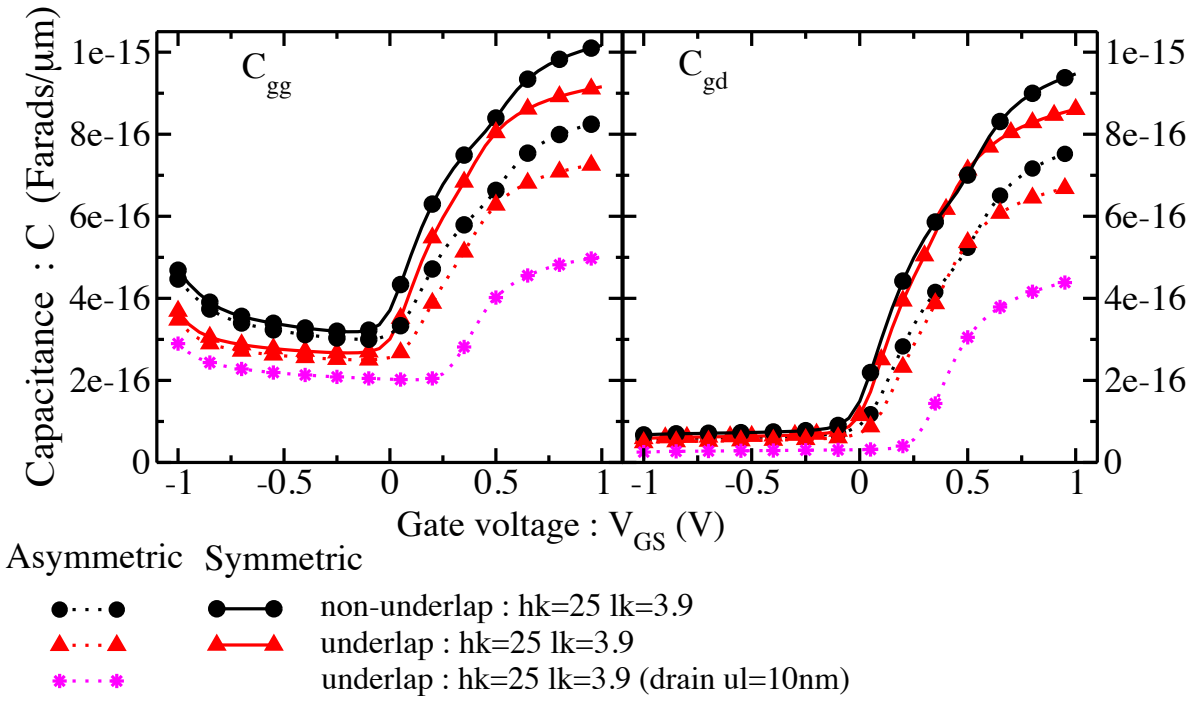


Figure 6.3: Capacitance - voltage characteristics showing a reduction in capacitance for asymmetric TFETs compared to that of symmetric TFETs. The gate dielectric is 1.1 nm SiO_2. $V_{DS} = 0$ V.

the capacitance is a weaker function of the field. We can expect that the overall circuit performance would only improve with a dual-k spacer as is shown in chapter 7.

6.3 Capacitance of Asymmetric n-channel Tunnel FET

The C_{gd} can be decreased by replacing the drain side spacer with oxide spacer which is being referred as asymmetric structure as explained in chapter 5. From Fig. 6.2 shows the C-V characteristic of the three asymmetric nTFET considered in Fig. 5.18(a) along with the reference case of nTFET with SiO_2 spacers. In Fig. 6.2, capacitance per unit area normalised to C_{ox} is plotted on Y axis. Since the area has reduced for the underlap TFETs due to smaller L_G, we observe an increase in C/C_{ox} ratio. However in Fig. 6.3 where the magnitude of capacitance is plotted on Y-axis, we observe a decrease in capacitance for the underlap TFETs compared to that of non-underlap. We further observe at least a 15 % decrease in the capacitance for the asymmetric TFETs as compared to symmetric nTFETs for both the non-underlap and underlap TFETs. With increase in gate-drain underlap to 10 nm (Fig. 5.18(a)-iii), there is further decrease in C_{gg} and C_{gd} due to the small gate length of 8 nm. This reduced capacitance would further reduce the delay and overshoots in inverter which are evaluated in the chapter 7.

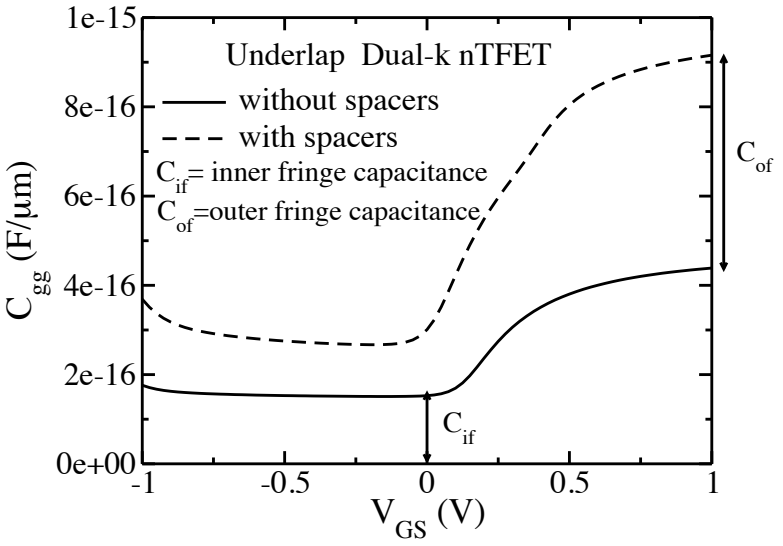


Figure 6.4: Capacitance - voltage characteristics for symmetric underlap TFET with dual-k spacer (Fig. 5.2(c)) illustrating the computation of the inner and outer fringe capacitance. The gate dielectric is 1.1 nm SiO_2. $V_{DS} = 0$ V.

6.4 Fringe Capacitance of n-channel Tunnel FET

To compute the inner fringe capacitance (C_{if}), C-V characteristics is simulated for structures of Fig. 5.2 without spacers for $V_{DS} = 0$ V. The capacitance value at $V_{GS} = 0$ V gives the inner fringe capacitance. Then the C-V characteristics is simulated with symmetric spacers for $V_{DS} = 0$ V. The difference in the capacitance value at $V_{GS} = 1$ V for these two characteristic gives the outer fringe capacitance (C_{of}), which represents the enhancement in the outer fringe capacitance due to use of spacers. This is illustrated for the underlap structure with dual k spacer in Fig. 6.4 and the computed values are given in Table 6.1. This method of computing the inner and outer fringe capacitances is only indicative and is used here purely for comparing the capacitances of the various TFET structures used in this work.

Table 6.1: Fringe capacitance for the symmetric TFET structures shown in Fig. 5.2.

structure	spacer	C_{if} F/μm	C_{of} F/μm
non-underlap	SiO_2	1.92e-16	1.07e-16
non-underlap	dual-k	1.92e-16	4.72e-16
underlap	dual-k	1.53e-16	4.77e-16

From Table 6.1, we observe that the external fringe capacitance increases for the nTFETs with dual k spacer which results into improvement in tunneling currents.

The pTFET exhibits similar C-V characteristics with identical increase and decrease in

capacitance due to use of dual-k spacer in symmetric and asymmetric pTFETs respectively and hence are not discussed here.

6.5 Conclusion

The use of high k material in the dual k layer spacer increases the device capacitance. The C_{gg} and C_{gd} increase for both non-underlap and underlap TFETs. The asymmetric dual k spacer TFET structures, where the drain side dual k spacer is replaced by an oxide spacer of same width, exhibit atleast a 15 % reduction in C_{gg} and C_{gd} compared to the symmetric structures. The increase in gate-drain underlap for asymmetric underlap TFET further reduces the device capacitances.

The effect of this increased capacitance due to use of dual k spacers is evaluated with inverter simulation in the next chapter for both symmetric and asymmetric TFETs.

Chapter 7

Impact of Dual k spacers on the Circuit Performance of Tunnel FETs

7.1 Introduction

The use of dual-k spacer in TFET, enhances the electric field at the source-channel junction resulting into improvement of the tunneling currents. However it also results into increased device capacitance as an undesirable and unavoidable side-effect as detailed in chapter 6. Hence the improved tunneling current is not a sufficient measure to determine the performance improvement. To obtain a complete evaluation of the performance improvement due to use of the dual-k spacers, a circuit level analysis needs to be done.

Unlike in conventional MOSFETs, (where the I_{ON} improvement is directly proportional to the capacitor scaling) in TFETs the increase in I_{ON} is way much higher than the increase in the capacitance. This significant difference between the two FETs can have profound implications in the device performances like power-delay characteristics, noise margin characteristics etc. We have investigated the static and dynamic circuit performance of the TFETs with dual-k spacers. The inverter delay and overshoot due to Miller capacitance were evaluated using mixed mode simulation. For larger TFET based circuits, mixed mode simulations is computationally expensive and is extremely cumbersome, inefficient and has a lot of convergence issues. Due to this issues, it is almost impractical to do elaborate circuit level simulation in TCAD. This necessitates new simulation models of TFETs for the circuit simulations involving the same.

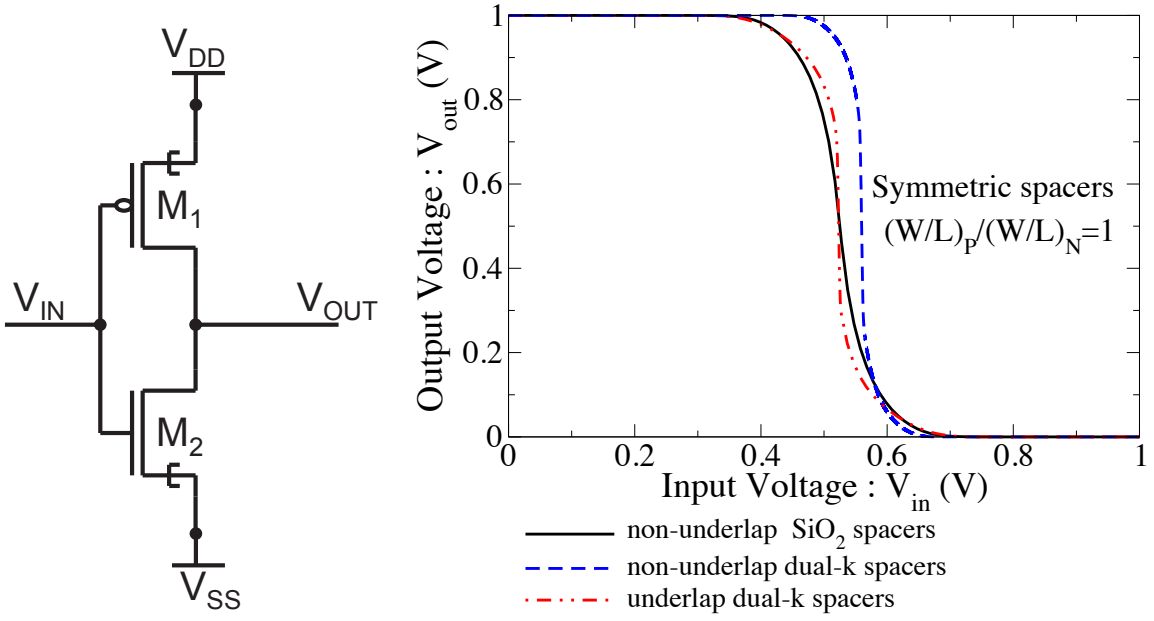
Unlike MOSFET, tunnel FETs do not have a well defined compact model for circuit simulation. In the absence of accurate compact analytical model, the Look-Up Table (LUT) based circuit simulation approach is an attractive option. Many researchers have investigated the LUT approach [122] and have used the same for circuit simulation with TFETs [59]. Using LUT simulations, the static noise margins were evaluated using SRAM cell and the power-delay analysis was performed using the 5-stage ring oscillator.

7.2 Device Structure

The symmetric structures of the silicon nTFET shown in Fig. 5.2 namely (a) non-underlap nTFET structure with SiO_2 spacer, (b) non-underlap nTFET structure with dual-k spacer and (c) underlap nTFET structure with dual-k spacer. In addition to these structures, we have used the asymmetric structures with dual-k spacer at source side and SiO_2 spacers at the drain side (Fig. 5.18) namely (d) non-underlap structure, (e) underlap structure (drain side ul = 2 nm) and (f) underlap structure (drain side ul = 10 nm). The pTFET structures have similar geometry with n^+-i-p (source-channel-drain) doping with same 2 nm/decade gradient. The gate dielectric is 1.1 nm SiO_2 unless specifically mentioned. Dual-k spacer is made up of HfO_2 (k = 25) inner layer and SiO_2 outer layer unless mentioned.

7.3 Mixed Mode Simulation

The static and dynamic performance was evaluated using the inverter circuit shown in Fig. 7.1(i). The circuit symbols which we are using to represent TFETs in a schematic is derived from the symbols used for MOSFETs. The devices M_1 and M_2 in Fig. 7.1(i) represent pTFET and nTFET respectively. The triangular arrow in the source terminal has been replaced by a rectangular arrow to differentiate it from a conventional MOSFET. The pTFET have a bubble in the gate electrode.



(i) (ii)

Figure 7.1: (i) Circuit schematic of inverter with TFET. (ii) Simulated DC Transfer characteristic of inverter using symmetric TFETs with (a) non-underlap oxide spacer, (b) non-underlap dual-k spacer, and (c) underlap dual-k spacer.

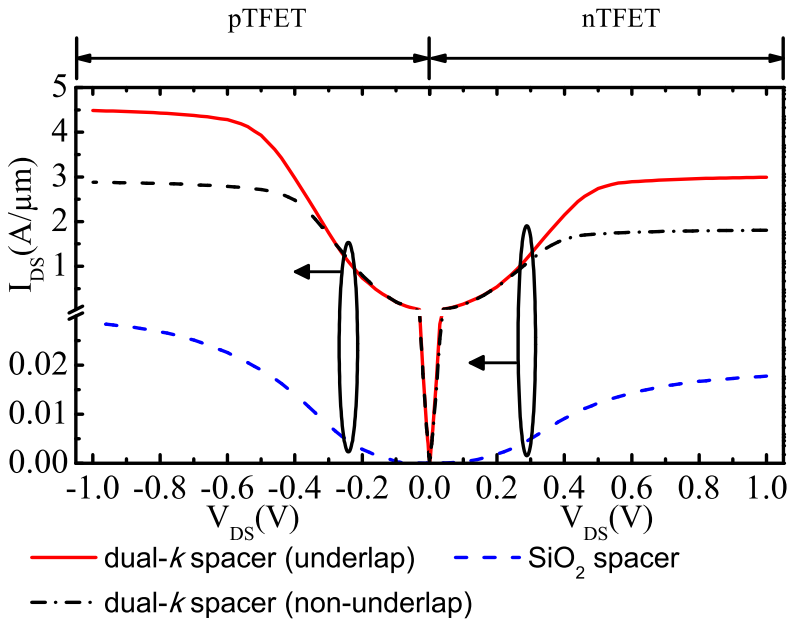


Figure 7.2: I_D-V_{DS} characteristic ($V_{GS} = 1$ V) for (a) non-underlap TFET structure with SiO_2 spacer, (b) non-underlap TFET structure with dual-k spacer made of HfO_2 and SiO_2 and (c) underlap TFET structure with dual-k spacer made of HfO_2 and SiO_2. The gate dielectric is SiO_2 of 1.1 nm thickness.

7.3.1 Static Performance

The transfer characteristic of the TFET inverter using the three symmetric structures of Fig. 5.2 is shown in Fig. 7.1 (ii). We observe that TFETs with dual-k spacer gives sharper transfer characteristic as compared with TFET with SiO_2 spacer. This is because the I_D-V_{DS} characteristic of the TFET with dual-k spacer is flatter at the saturation region than that of the TFET with SiO_2 spacer which is seen in Fig. 7.2. This superior saturation behavior of the the I_D-V_{DS} characteristics of the dual-k spacer TFET is the main reason for the sharper transition of the inverter transfer characteristics of the same which in turn has a positive effect on the digital circuit performance. Also I_D-V_{DS} characteristics of non-underlap TFET with dual k is more flatter than that of the underlap TFET with dual-k spacer (Fig. 5.3, 7.2), thereby exhibiting sharper transfer characteristic.

7.3.2 Dynamic Performance

The transient characteristics of the inverter using symmetric TFET structures for a pulse input voltage (V_{IN}) with 1 ns rise (t_r) and fall (t_f) time (time period (T_p) of 102 ns) are shown in Fig. 7.3. There is a large improvement in the transient characteristic for TFET inverter with dual-k spacer as seen in Fig. 7.3 (a). We observe that the delay for TFET with SiO_2 spacer is larger due to low I_{ON}, whereas the TFET with dual-k spacer gives lower delay due to higher I_{ON}. Although the use of dual-k spacer

increases the capacitances by almost 1.8x, the I_{ON} increase obtained is of more than two orders of magnitude. This large improvement obtained in I_{ON} masks the increased capacitance effect. The inverter using underlap TFETs shows improvement over the transient characteristic of inverter using non-underlap TFETs.

The TFET inverter has enhanced Miller capacitance [107] effect (C_{gd}) through which the input transitions are coupled to the output resulting into higher overshoots and undershoots compared to MOSFET inverter. The symmetric underlap structure which has lowest C_{gd} among the 3 cases considered, gives the lowest overshoot and undershoot.

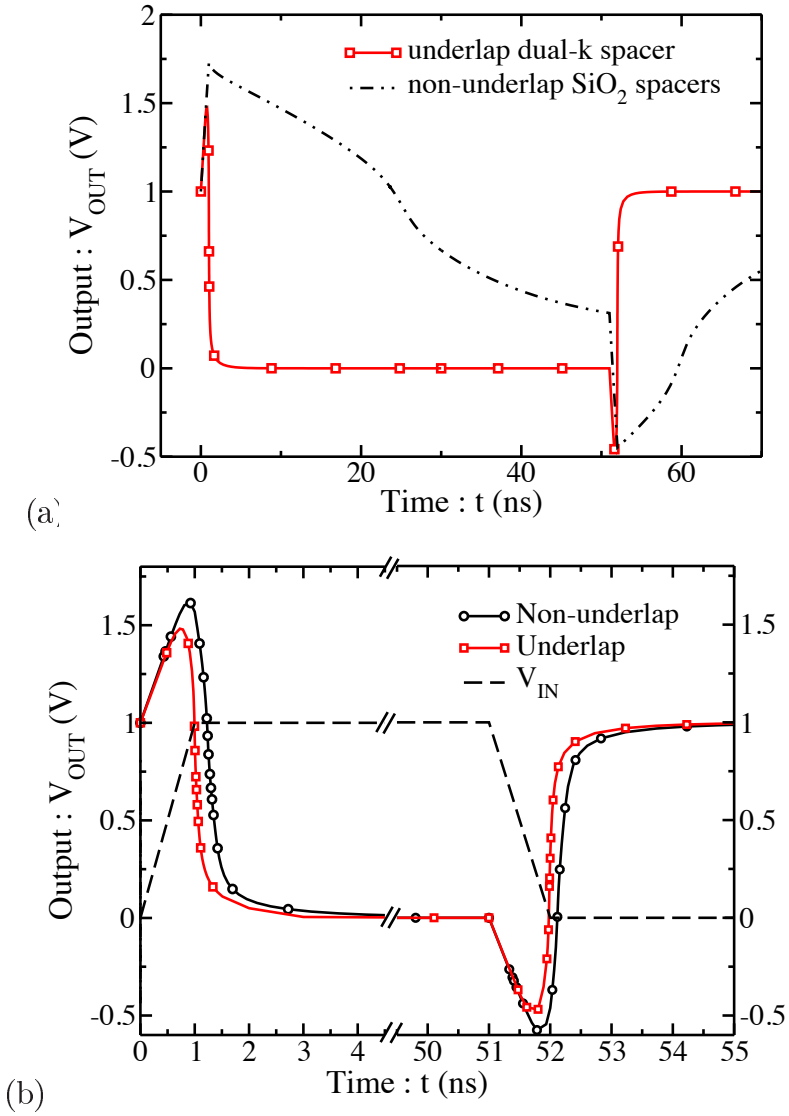


Figure 7.3: Transient characteristic of inverter using (a) symmetric non-underlap TFETs with SiO_2 spacer and symmetric underlap TFETs with dual-k spacer and (b) symmetric non-underlap and underlap TFETs with dual-k spacers. (For both (a) and (b), Vin: t_r = t_f = 1 ns, T_p = 102 ns and C_L = 0).

7.3.2.1 Effect on Delay and Overshoot for Different Loads

Fig. 7.4 shows the effect of spacer engineering on delay of the inverter using TFET with dual-k spacers for different load capacitance (C_L). The delay is defined as the average of the rise and fall delay times. The rise delay time is defined as the time delay between the instants at which input and the output crosses 50 % of V_{DD}. The fall delay time is defined in a similar fashion. The first order approximation of the inverter delay is given by $C_L V_{DD}/I_{ON}$ [14]. The delay is lesser for the TFET inverter using underlap structures as compared to TFET inverter delay when non underlap structures are used due to reduced gate length and higher I_{ON}. The underlap structure is seen to have lower sensitivity to load capacitance. This is due to the better current drive of the underlap structure

When asymmetric structures are used, the C_{gd} which is dominant component of C_{gg}, reduces. This reduces the effective intrinsic capacitance C_{EFF} of the inverter (output capacitance of the unloaded inverter comprising contributions from the intrinsic gate-to-drain capacitances (C_{gd}) of both the n and p channel TFETs) and hence the total load capacitance ($C_{L_{total}} = C_L + C_{EFF}$) reduces. Hence we obtain a reduction in delay as compared to inverter delay with symmetric structures.

The improvement obtained in inverter delay with asymmetric non-underlap TFET is more than that of asymmetric underlap TFET. This is because the I_{ON} is almost double for underlap TFET as compared with non-underlap case. The asymmetric structure with

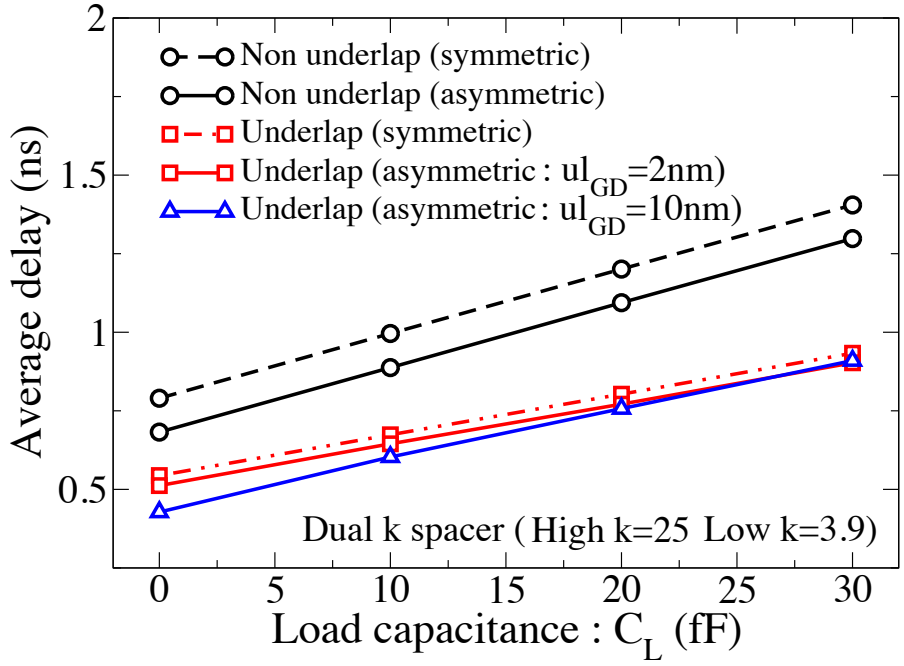


Figure 7.4: Effect of spacer engineering on delay of inverter for different C_L (Vin: $t_r = t_f$ = 1 ns and T_p = 102 ns). The gate-to-drain underlap is indicated by ul_{GD}.

10 nm drain gate underlap gives the least delay (Lg = 8 nm) due to smallest gate length, reduced capacitance and higher I_{ON} ($\sim I_{ON}$ of underlap TFET with dual-k spacer and ul = 2 nm). As the load increases, this improvement is seen to diminish as the load capacitance dominates over the C_{EFF}.

Fig. 7.5 shows the effect of spacer engineering on peak overshoot of the inverter for different C_L. Smaller overshoots are observed for underlap because C_{gd} for underlap TFETs is smaller than that of non-underlap TFETs. The inverter with asymmetric TFETs gives lower overshoots due to reduction in C_{gd}. The underlap TFET with drain to gate underlap of 10 nm gives the smallest overshoot as it has lowest C_{gd}. As load capacitance increases the overshoots reduce and the reduction obtained due to use of asymmetric spacers also diminish as the load capacitance dominates over the C_{gd}.

7.3.2.2 Effect on Delay and Overshoot for Fanout of One

The results of inverter simulation with fanout = 1 shown in Fig. 7.6 demonstrates similar improvement in performance. The symmetric underlap structure gives about 30 % lower delay compared with symmetric non-underlap structures due to lower gate length and higher I_{ON}. Asymmetric structure gives lower delays. Reduction in delay obtained for the non-underlap and underlap asymmetric structures are 11 % and 5 % respectively. Asymmetric underlap structure (L_G = 8 nm) with drain-channel underlap of 10 nm gives

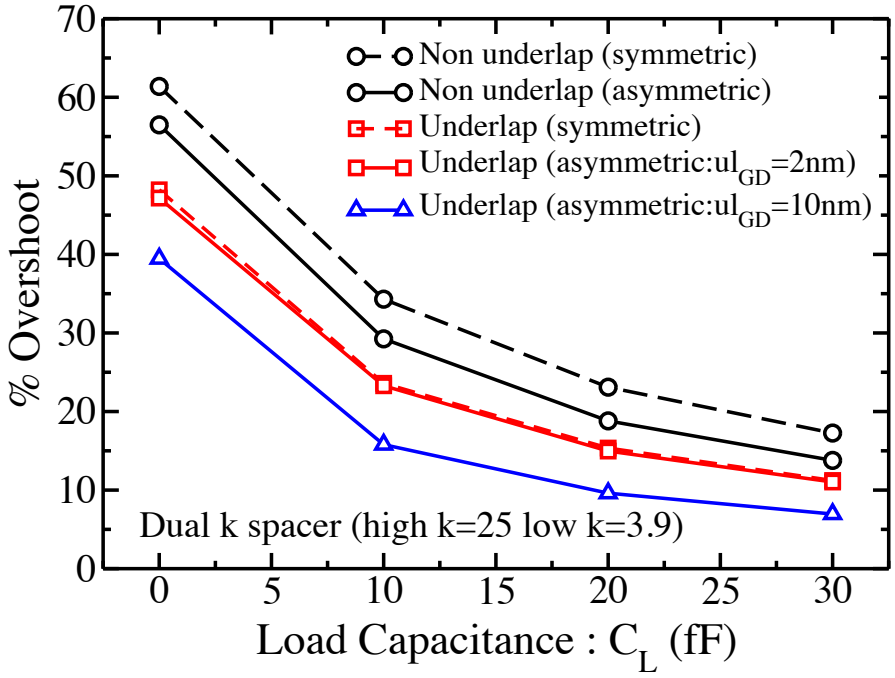


Figure 7.5: Effect of spacer engineering on peak overshoot of inverter for different C_L (Vin: $t_r = t_f$ = 1 ns and T_p = 102 ns). The gate-to-drain underlap is indicated by ul_{GD}.

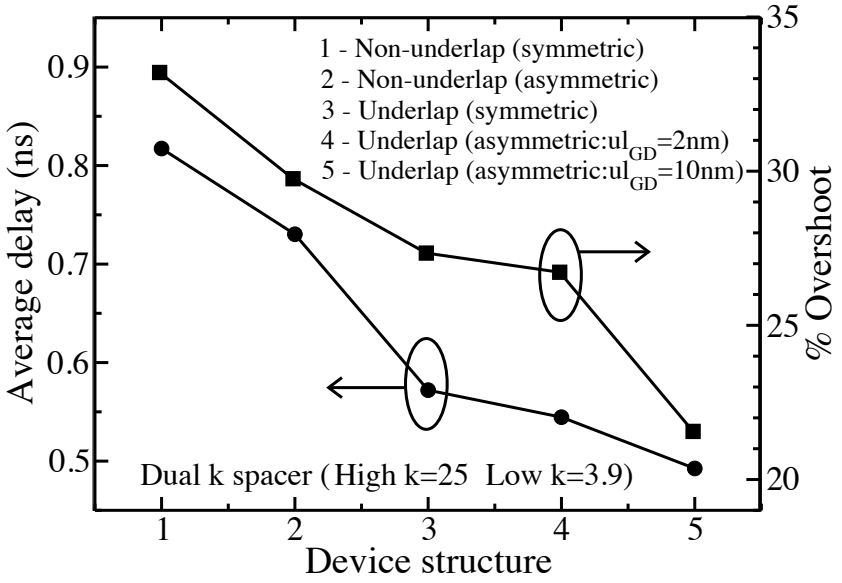


Figure 7.6: Effect of spacer engineering on delay and overshoot of inverter for fanout=1. The gate-to-drain underlap is indicated by ul$_{GD}$.

lowest delay due to the smallest gate length.

Symmetric underlap structures gives lower overshoots compared to non-underlap structure. Overshoots are reduced in asymmetric non-underlap and underlap structures by 3 % and 1 % respectively. Lowest overshoots are in asymmetric underlap structure with drain-channel underlap of 10 nm.

7.3.2.3 Ring Oscillator

The ring oscillator simulation has lot of convergence problems. Only the ring oscillator circuit using TFET with larger tunneling current converged. Fig. 7.7 shows the output of seven stage ring oscillator using symmetric underlap structure with dual-k structure (Fig. 5.1(c)) and stress = 4 GPa (Bandgap = 0.93 eV). The I_{DS}-V_{GS} characteristic is shown in Fig. 8.7 (chapter 8). The frequency of oscillations is 725 Mhz (Time period T = 1.38 ns and stage delay $\sim$ 0.2 ns).

We observe that the output waveform does not have a rail-to-rail swing from 0 to V_{DD} (1 V). This is because of the exponential nature of the output characteristic of TFET, see Fig. 5.3 and 5.15 (ii). Whenever the V_{DS} across TFET drops to $< \mid 0.2 \mid$ V, the charging or the discharging through the TFET slows down. Hence the output does not discharge or charge completely to 0 V or V_{DD} respectively.

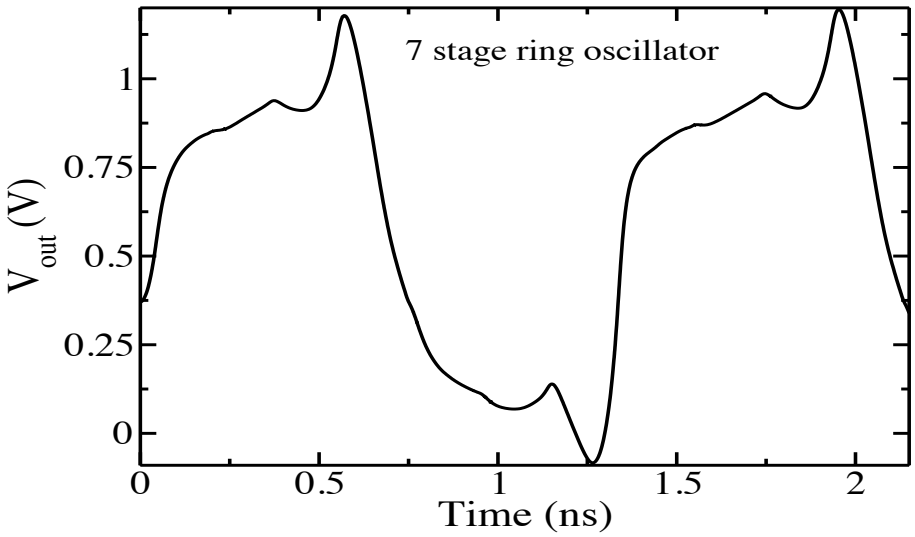


Figure 7.7: Output waveform of seven stage ring oscillator. The underlap structure with dual-k spacer and stress = 4 GPa have been used.

7.4 Look-Up Table based Simulation Setup

The TFETs which are used are 1) non-underlap TFET with SiO_2 spacer and 2) underlap dual-k spacer device which gives the highest I_{ON}. Both these structures have symmetric spacers. We have seen in chapter 5 that the underlap structure gives better I_{ON} than the non-underlap structure and hence only the underlap structure is considered here. A look-up table based simulator was built using Verilog-A for circuit simulation and evaluation. In this LUT based simulator, I-V and C-V characteristics of these TFET devices are extracted using calibrated SENTAURUS TCAD (detailed in chapter 3) simulations to form the look-up tables. The Verilog A module captures the quasi stationary behavior of the TFET by expressing the terminal currents in terms of the terminal voltages and the time rate of change of terminal voltages multiplied with the appropriate capacitance component. Also this method makes it easy to parameterize some of the design parameters for exhaustive experimentation. The cubic spline interpolation is used to obtain intermediate values as it provides smooth curves with continuous first and second derivatives. This efficient and accurate way of modeling is well suited for the emerging devices for which compact or SPICE models are not available [123, 124]. The LUT based circuit simulation work was performed jointly with Ashokanand N., Jawar Singh and Anil Kottantharayil [125]. This work has been used here to analyse the improvement in circuit performance of the dual-k spacer TFETs.

To validate the LUT based quasi stationary modeling, we have extracted the I_D-V_{GS} and I_D-V_{DS} characteristics of the above mentioned devices at $V_{DS} = 1$ V and compared

it with the TCAD data. Fig. 7.8 shows the I-V characteristics generated by LUT based simulator. One can observe that the LUT based simulator characteristics accurately match the characteristics generated by TCAD simulation and is as expected. The linear I_D-V_{DS} characteristics is plotted with a break in the I_D axis to highlight the shape of the output characteristics of the TFET with SiO_2 spacer which influences the DC performance of the digital circuits.

7.5 Circuit Simulation using LUT

7.5.1 Static Performance

SRAM cell Noise Margins (NM) were extracted using LUT based simulations to evaluate the performance improvement.

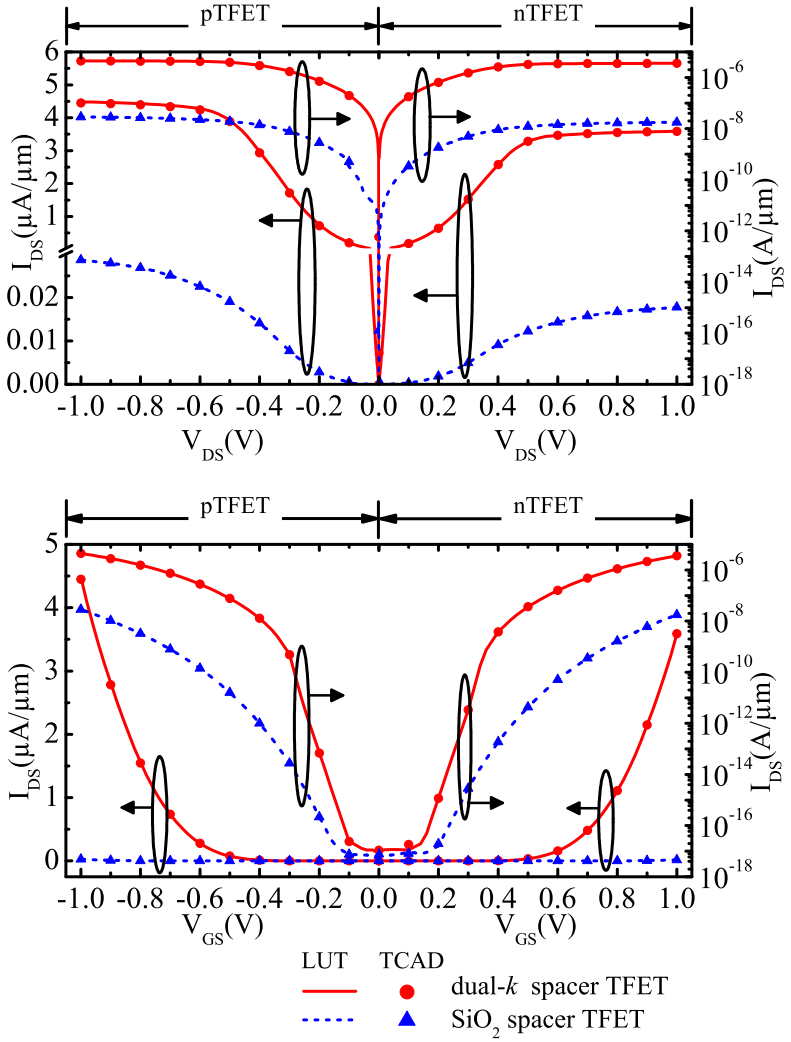


Figure 7.8: The I_D-V_{DS} characteristic at V_{GS} = 1 V and I_D-V_{GS} characteristic at V_{DS} = 1 V for nTFET and pTFET indicates an agreement with the TCAD generated characteristic.

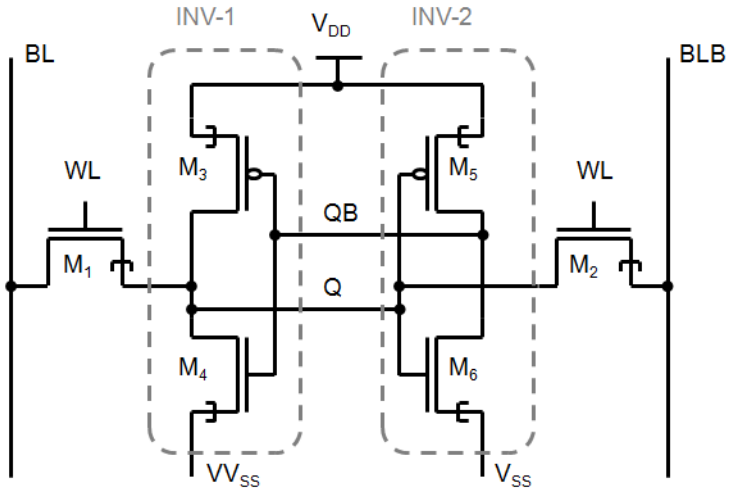


Figure 7.9: Si-TFET 6T SRAM bitcell design.

7.5.1.1 TFET based SRAM Designs and Challenges

Implementation of SRAM bitcell needs pass-gate access transistors to conduct either-way for successful read and write operations. Therefore, uni-directional current conducting TFETs based pass-gate transistor limits the viability of standard 6T SRAM bitcell, as reported in [110].The implications of uni-directional conduction behavior of TFET on SRAM bitcell and its viability have been explored recently in [59, 110]. Kim et al have proposed a hetero junction TFET based 7T SRAM bitcell. In this design, isolated read and write ports are employed to ensure adequate read and write noise margins. In [59], a new Si-TFET based 6T SRAM with adequate read and write noise margins ensured by its unique design features and biasing arrangements for read and write operations is proposed and has been used in this chapter.

The Si-TFET 6T SRAM bitcell consists of cross coupled inverters (INV-1 and INV-2) with the bit-lines BL and BLB connected to node Q through the access transistors M_1 and M_2 (Note that both the access transistors are connected to the same node Q), as shown in Fig. 7.9. It is a design strategy to connect both the bit-lines to node Q for writing either '1' or '0', and to provide the virtual ground (VV_{SS}) to INV-1 to assist the write operation. The VV_{SS} is raised to V_{DD} which decouples (or weakens the regenerative action) of the cross-coupled inverters while writing either 0 or 1. Once the Q and QB settle to the desired voltages, VV_{SS} is connected back to ground and the cross coupling is enabled. This makes the write operation easier and thereby improving the write noise margin. A detailed description of read and write operations and the equivalent circuits of the same are given in [59].

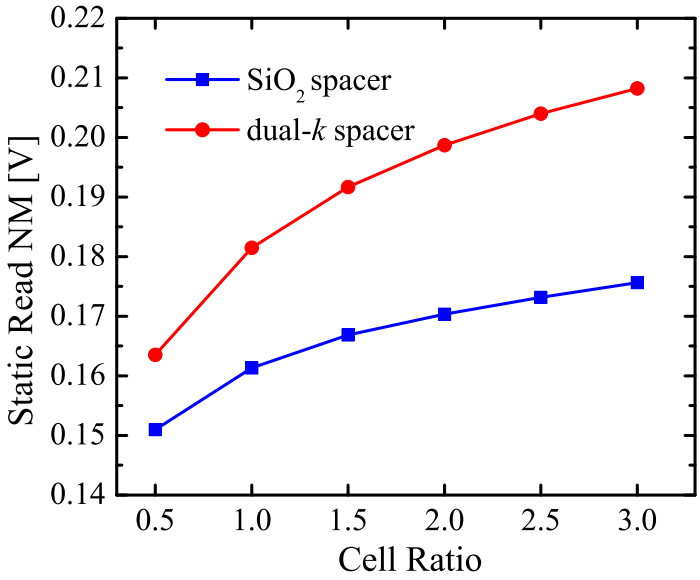


Figure 7.10: RNM vs cell ratios at fixed pull up ratio of 1.5

7.5.1.2 SRAM Bitcell Stability

Adequate read stability and write-ability of an SRAM bitcell are highly desirable for successful realization of robust and high performance cache memories. The Read Noise Margin (RNM) and Write Noise Margin (WNM) are the widely used metrics for stability analysis of a SRAM bitcell [126].

The static NM of SRAM bitcell depends on the value of the cell ratio, pull up ratio and supply voltage. The cell ratio (CR) for SRAM cell is defined as the sizing ratio of pull down transistor of the inverter to that of the access transistor. In the Fig. 7.9, it is the sizing ratio of M_4 to M_1. In conventional CMOS technology, higher the cell ratio, better is the read margin. The pull-up (PR) ratio is defined as the sizing ratio of pull up transistor of the inverter to that of the access transistor. In the Fig. 7.9 it is the sizing ratio of M_6 to M_2. In conventional CMOS technology, higher the pull up ratio, better is the write margin.

Fig. 7.10 shows the extracted RNM. Cell Ratio has been ramped from 0.5 to 3 with an interval of 0.5, while the pull-up ratio is fixed at 1.5. With increase in CR, the RNM also increases due to reduction in rise in potential at node Q. We observe that the RNM for the dual-k spacer TFET is superior to that of the SiO_2 spacer TFET. This is mainly because of the sharper inverter transfer characteristics of the inverter made of dual-k spacer TFET.

In order to demonstrate a successful write operation, the WNM of the proposed Si-TFET 6T SRAM is simulated using LUT based model for different Cell Ratios, and pull-up ratios. Due to the uni-directional conduction of the TFET pass transistor, writing a '1' is more difficult than writing '0', hence, we have only observed the WNM for writing a '1' into the bitcell.

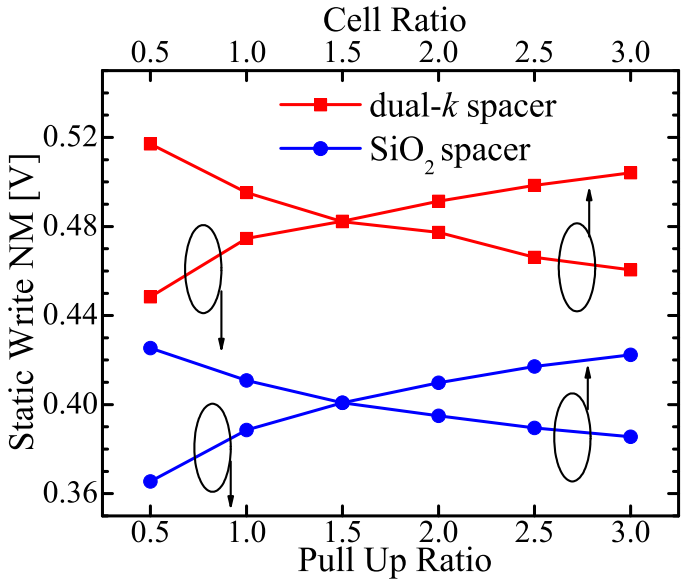


Figure 7.11: WNM of SRAM based on SiO_2 spacer and dual-k spacer TFETs for different cell ratios and pull-up ratios

Fig. 7.11 shows the WNM of both the devices for various cell ratios and pull-up ratios. The superiority of the dual-k spacer TFET based SRAM is evident from the graph. Higher ON-state resistance of the SiO_2 spacer TFET compared to the dual-k spacer TFET results in more voltage drop across the pass transistors. Hence the internal node voltage of Q slightly lags behind the bit-line voltage owing to the voltage drop across the series pass transistor whereas the voltage at Q closely follows the bit-line voltage in the dual-k spacer TFET based SRAM. Thus the writing of '1' on to node Q happens at a slightly higher voltage in the SiO_2 spacer TFET based SRAM compared to the dual-k spacer TFET based SRAM resulting in a higher write noise margin for the SRAM made of the dual-k spacer TFET.

7.5.2 Dynamic Performance

7.5.2.1 Inverter

From section 7.3.2 we observe a reduction in the inverter delay computed from the mixed mode simulations for TFETs with dual-k spacers. This trend was consistently observed for varying capacitive load and for fanout of one. Mixed mode simulations for fanout of 2 and more have severe convergence problems. Hence LUT simulation were performed for various fanouts (Fig. 7.12) which further confirms the superior performance of TFETs with dual-k spacer.

The power consumption of an inverter is a very important performance parameter particularly for TFETs because of their very low I_{OFF}. The static (leakage) power is

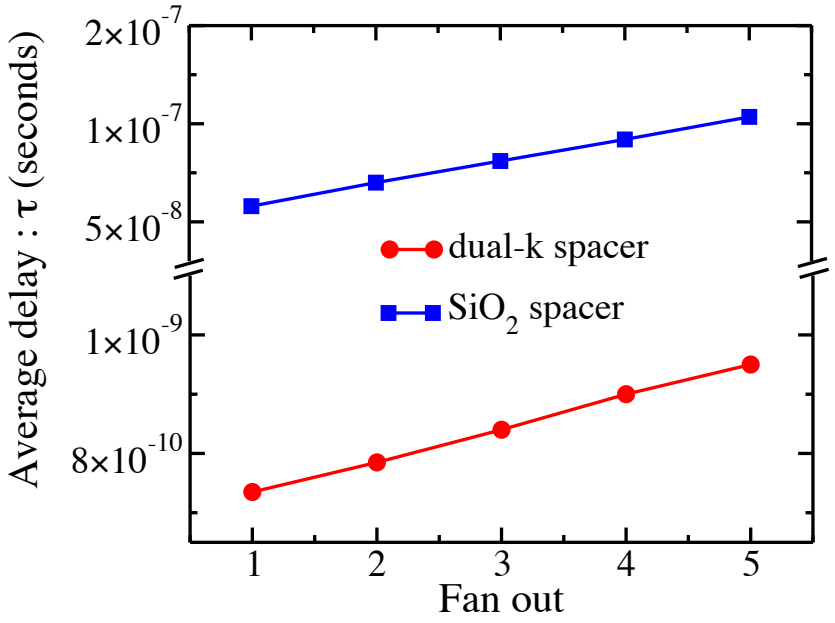


Figure 7.12: Average time delay as a function of fanout for inverter using (a) non-underlap TFET with SiO_2 spacer and (b) underlap TFET with dual-k spacer.

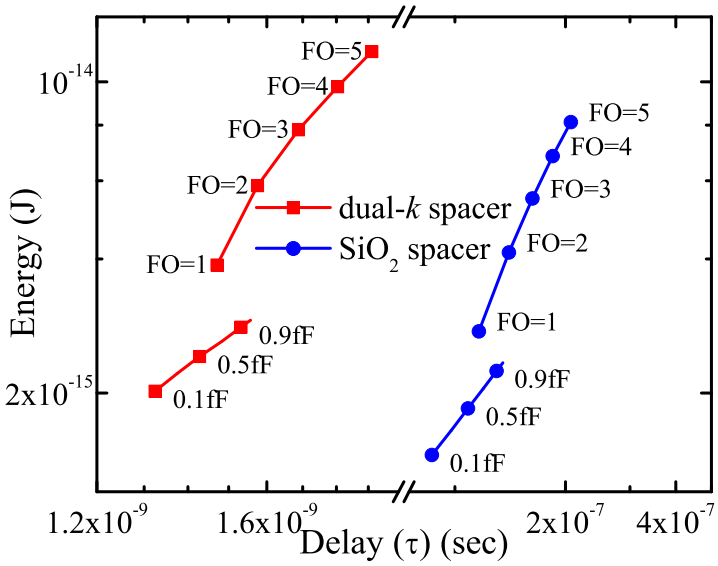


Figure 7.13: Energy vs Delay for different fan-outs and different load capacitances.

thus much less compared to the ordinary MOSFETs. For TFETs total power dissipation is mainly dominated by the Short Circuit Power Dissipation (SCPD) and the Dynamic Power Dissipation (DPD). Fig. 7.13 shows the Energy (per clock cycle) vs Delay for different load capacitances (1fF - 5fF which is an order higher than the intrinsic device capacitances) and Energy vs Delay for different fan-out (1 - 5). The DPD is simply given by CV^2f and hence is directly related to the fan-out or the load capacitance (C_L). But the SCPD might have a complex relation with the fan-out or the C_L. The fact that the delay is not increasing 5 times as we increase the fan-out 5 times clearly shows that the SCPD is more substantial than the DPD. This can be seen in another observation too.

The power dissipations of the 2 devices for the same load are different. The dual-k spacer TFET takes more power than the SiO_2 spacer TFET. This is because the dual-k spacer TFET has higher I_{ON} and hence more SCPD. Had that component been negligible we would expect same power for both the devices since it depends only on C_L (neglecting the device capacitances). In fact the peak short circuit current through the inverter with dual-k spacer TFET during a transition (either 0-1 or 1-0) is seen to be 48.81nA whereas the peak short circuit current through the inverter with SiO_2 spacer TFET is only 13.02 pA. This further explains the higher energy consumption of the inverter with dual-k spacer TFET than the one with SiO_2 spacer TFET.

7.5.2.2 Ring Oscillator

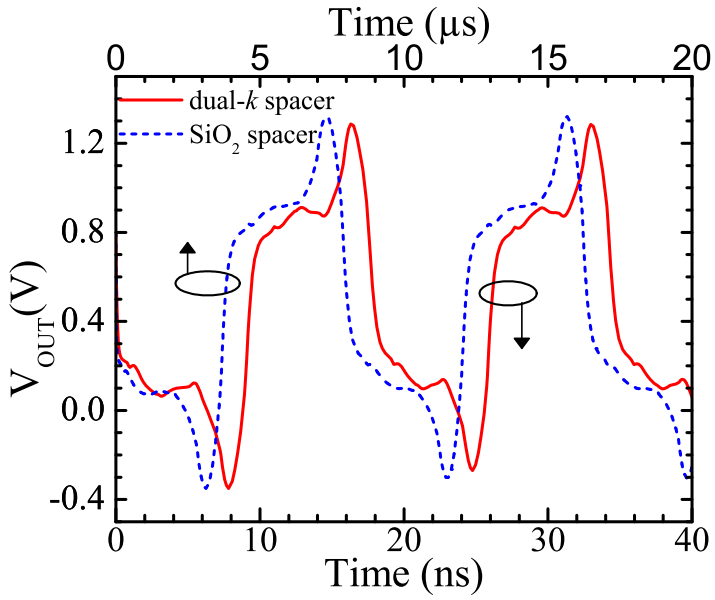


Figure 7.14: A five stage ring oscillator using (a) non-underlap TFET with oxide spacer and (b) underlap TFET with dual-k spacer.

Fig. 7.14 shows the outputs of the 5-stage ring oscillator circuit of (i) dual-k spacer TFET (ii) SiO_2 spacer TFET for $V_{DD} = 1$ V. The time periods of oscillation are 8 μs and 16 ns (which translates to stage delays of 0.8 μs and 1.6 ns) for the SiO_2 spacer case and dual-k spacer case respectively. We observe that the waveform generated are similar to that seen in Fig. 7.7 with difference in time period.

The power-delay analysis is carried out by plotting the "Average-Power" v/s "Stage-Delay" of the ring oscillator circuit for different V_{DD}. As the V_{DD} is increased the stage-delay reduces whereas the average-power increases. This results in a hyperbolic relation between the power and the delay which appears like a straight line with negative slope in a log (power) - log (delay) plot, Fig. 7.15. Due to convergence issues it was not possible to simulate the ring oscillators below 0.7 V. So it was required to extrapolate the power-delay graphs to do a fair comparison of the device. The solid lines in the graph represent

the real simulation output whereas the dotted portions of the graphs are extrapolation of the simulation results. As evident from the graph, for a fixed power consumption, the delay of the ring oscillator using dual-k spacer TFET is always lower than the ring oscillator using SiO_2 spacer TFET. Similarly, for a fixed delay, the power consumption of the ring oscillator using dual-k spacer TFET is always lower than the ring oscillator using SiO_2 spacer TFET. This undoubtedly proves that the dual-k spacer TFET device is also superior in terms of power to the SiO_2 spacer TFET device for any V_{DD}.

7.5.3 Comparison of the Mixed Mode and LUT simulations

The LUT based simulation are sensitive to the interpolation methods used to find out the terminal currents and capacitances at unspecified (in the LUT) bias points. As a result there is some loss in accuracy of the results obtained. From Fig. 7.12, we observe that for fanout of one, we obtain higher delay as compared to that obtained from mixed mode simulations (Fig. 7.6). However the trend in performance improvement remains intact.

7.6 LUT based Circuit Level Optimization of Tunnel FETs with Dual-k spacer.

For a pure comparison, the optimizations which are done in chapter 5 by considering the I_{ON} as the objective function have been redone with the consideration of delay (of an

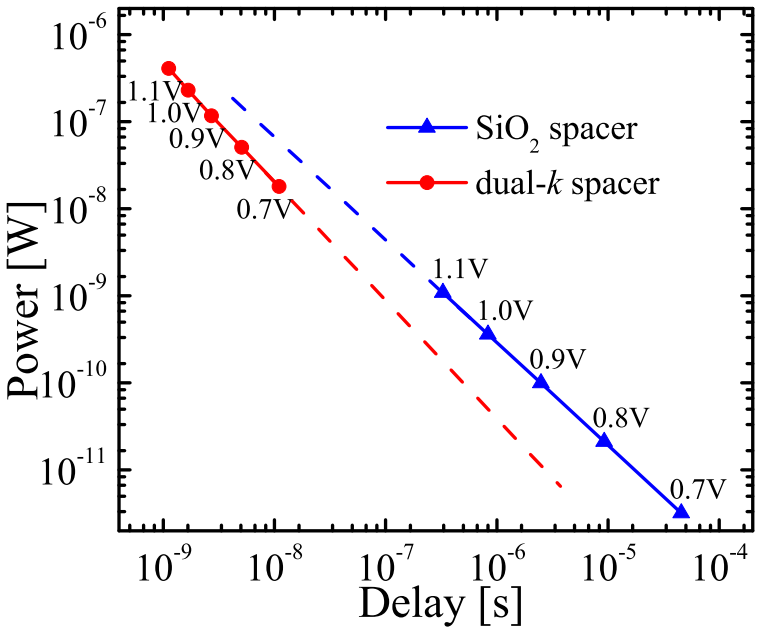


Figure 7.15: Power v/s Delay for ring oscillator circuit using TFET with (i) dual-k spacer (ii) SiO_2 spacer for different V_{DD}.

inverter made of such a device family driving another similar inverter) as the objective function. The results clearly validate the device level optimization results obtained in chapter 5.

Ring oscillator circuits are commonly used to compare delay performance of devices of different architectures or technologies. We have used delays computed using ring oscillator simulations for all LUT based results presented in this section.

Fig. 7.16 shows the result of the underlap width (width of hk layer) optimization. The width of SiO_2 lk spacer is fixed at 10 nm. The optimum value of underlap for hk = 25 is seen to be at 2 nm for which the I_{ON} is maximum and inverter delay is minimum confirming the device level optimization.

Fig. 7.17 shows the effect of k of the lk spacer on the I_{ON} and inverter delay of the underlap structure. It is seen that the I_{ON} decrease and inverter delay increases with increases in lk value consistent with the trend of device level optimization.

Fig. 7.18 shows the effect of k of the hk spacer on the I_{ON} and inverter delay of the underlap structure. The hk spacer thickness is fixed to 2 nm and the lk spacer thickness is fixed to 10 nm. It is seen that the I_{ON} increases consistently. The inverter delay is found to decrease consistently as k increases from 10 to 45 thereby reiterating the results of device level optimization.

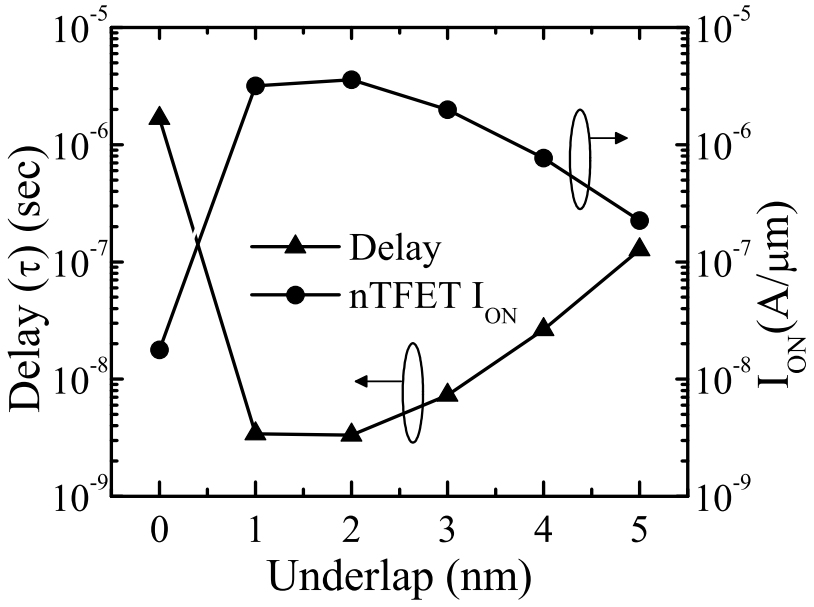


Figure 7.16: Effect of hk spacer width on I_{ON} and inverter delay for the underlap TFET with dual-k spacer. The hk spacer has a k of 25 (HfO_2). Gate dielectric is SiO_2 of 1.1 nm thickness.

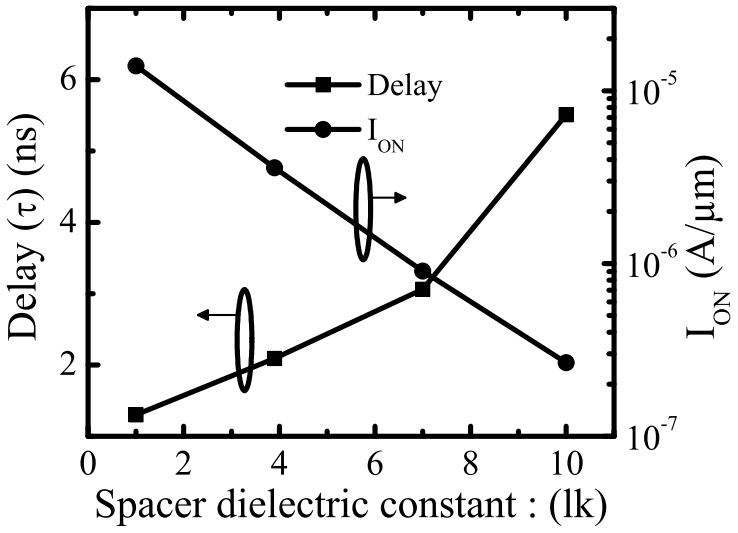


Figure 7.17: Effect of the dielectric constant of the lk spacer on performance of the underlap TFET with dual-k spacer. The hk spacer is made of HfO_2 ($k = 25$). The I_{ON} of nTFET with dual-k spacer is shown in the graph. The gate dielectric is SiO_2 of 1.1 nm thickness.

7.7 Conclusion

TFET inverter with dual-k spacer gives much better performance as compared to TFET inverter with SiO_2 spacers. Inverter with underlap structure gives lesser delay

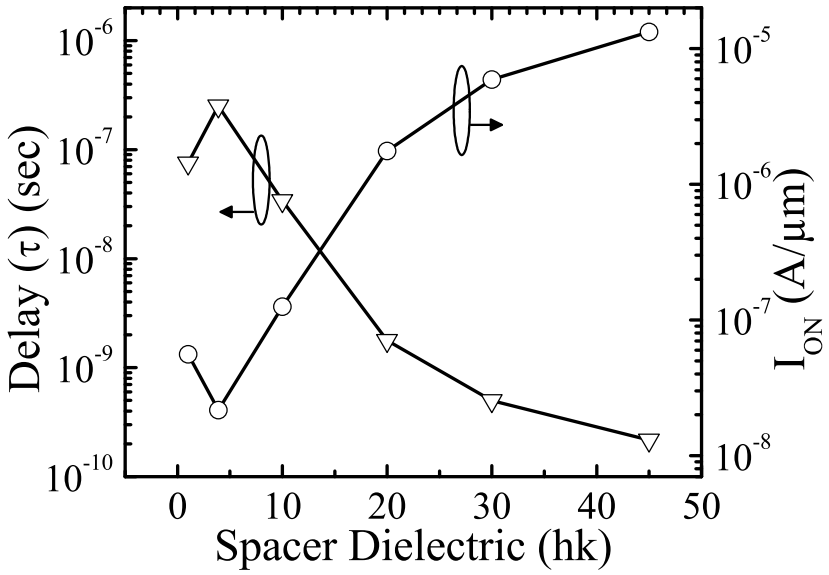


Figure 7.18: Effect of variation of hk spacer dielectric on DC characteristics of an underlap nTFET with dual-k spacer and gate dielectric is SiO_2 of 1.1 nm thickness. The hk spacer physical thickness is 2 nm and the k is varied. The lk spacer is 10 nm of SiO_2.

than the inverter with non-underlap structure. Use of asymmetric structure, reduces the C_{gd} and improves the inverter delay for the non-underlap and underlap structures. The overshoots are reduced in case of the asymmetric non-underlap structure. A small decrease in overshoot is observed for underlap structure (drain ul = 2 nm). However when the drain underlap is increased to 10 nm, best performance in terms of delay and overshoots is obtained due to reduced gate length of only 8 nm.

The LUT based SRAM simulation results also prove the better performance of the dual-k spacer structure over the single-k spacer structure. Frequency of oscillations increase for ring oscillator circuit with dual-k spacer TFET. For identical delays, the power consumed by the ring oscillator using TFET with dual-k spacer is lesser compared to ring oscillator with TFET with SiO_2 spacers. The LUT based inverter simulations confirms the device level optimization done in chapter 5.

The Impact of transport on the tunneling current is discussed in the next chapter.

Chapter 8

Channel Transport in Tunnel FET

8.1 Introduction

The various technology boosters used to optimize the tunneling currents focus on the improvement of the generation rate at the tunneling junction and little attention has been devoted to the possible role of the carrier transport in the channel. Koswatta et al. [127] reports that phonon scattering has moderate effect on the I_{ON} of carbon nanotube TFET. Saurab et al. [62] concludes that the mobility has negligible effect on I_{ON} for strained TFET.

In this respect, it is important to note that tunneling is a non local phenomenon that depends on the entire potential profile along the channel, which in turn is affected by the generation rate at the tunneling junction and also by how effectively the generated charge is swept along the channel to the drain contact. With the increase in tunneling generation rate, the transport in the channel may eventually influence the overall potential profile and hence the I_{ON}.

In this chapter, we present a study of the the channel transport in n-channel TFET which is significantly different from that of MOSFET. Using a toy model to increase the generation rate, we show that (i) the optimization of tunneling currents by the increase in generation rate is limited by electrostatic feedback due to non optimal channel transport and (ii) tunneling currents improve with increase in the velocity saturation and are relatively unaffected by mobility changes. We then verify the same by using the technology boosters. Similar results are obtained for p-channel TFETs.

8.2 Device Structure

The structures of the silicon n-channel TFET with dual-k spacer shown in Fig 5.1 are used in this work with same doping. The gate length has been increased to 50 nm for channel transport study using drift diffusion simulations. In addition to these structures,

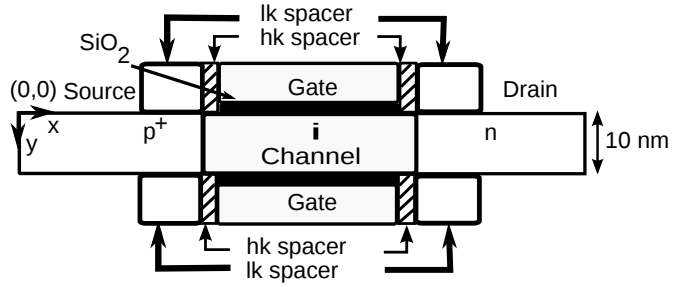


Figure 8.1: Underlap DG-nTFET structure (L_g = 46 nm). Body thickness is 10 nm.

a double gate nTFET (DG-nTFET) structure shown in Fig. 8.1, with same gate stack and doping of Fig. 5.1(c), has been used. The body thickness of 10 nm has been used.

8.3 Impact of the Channel Transport on the I_{ON} of n-channel TFET using a Toy Model

Various technology boosters has been used to enhance the carrier generation rate of Si TFET. However these large number of carriers generated are not transported efficiently to drain. Unlike MOSFET which have high electric field at the drain, TFET have low electric field at the drain. Due to these the transport of carriers in TFET tends to be different from that of MOSFET.

To gain an insight of the possible role of the carrier transport in nTFET as the generation rates are increased, initially we use a toy model wherein the prefactors g_c

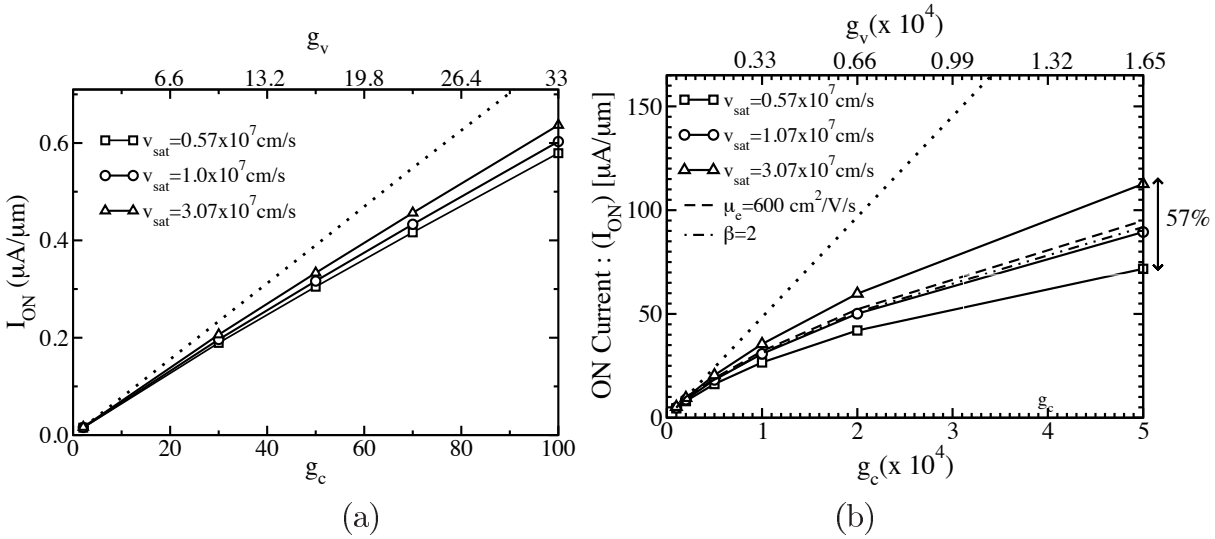
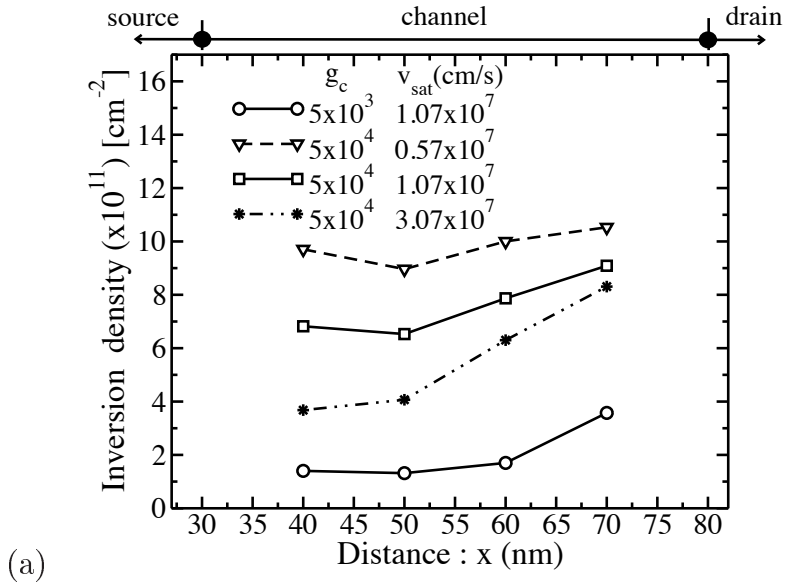
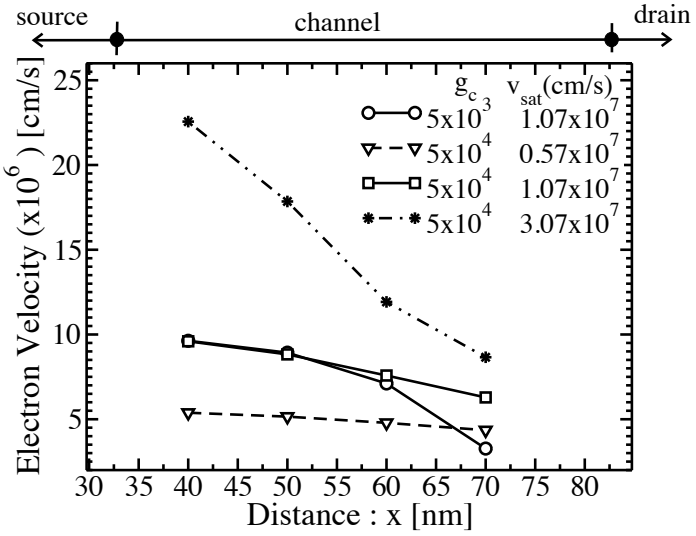


Figure 8.2: The effect of increasing the generation rate by increasing g_c and g_v in the non local tunneling model on I_{ON} for (a) low and (b) high values of g_c and g_v. I_{ON} for μ_e = 600 cm^2/V/s and $\beta = 2$ are computed for v_{sat} = 1.07x10^7 cm/s. The dotted straight line corresponds to an I_{ON} proportional to g_c.



(a)

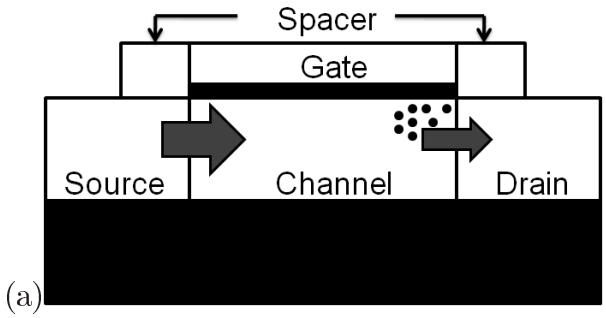


(b)

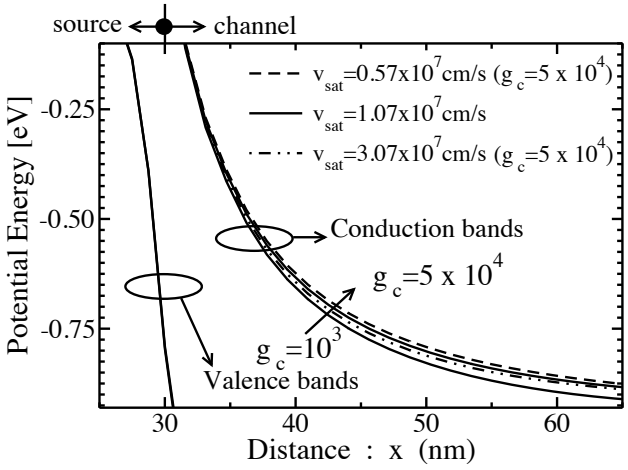
Figure 8.3: Effect of increasing the generation rate by increasing g_c and g_v in the non local tunneling model on (a) the inversion density and (b) the average velocity of electrons along the channel.

and g_v in non local tunneling model (Eq. 3.13) are increased to enhance the generation rate. These prefactors are ratios of Richardson constant for carrier in semiconductor to the same in free space. According to equations 3.9 and 3.13, which assume that the current is limited by the carrier generation due to tunneling, the I_{ON} would be proportional to g_c and g_v. The device structure of Fig. 5.1(a) with SiO_2 spacers (also shown in Fig 8.4(a)) is used.

Fig. 8.2 shows the I_{ON} versus the g_c and g_v, which are always varied by the same factor in this work. For low values of g_c and g_v the I_{ON} improves almost proportionately, as it is seen in Fig. 8.2(a). However for I_{ON} approximately larger than a few $\mu A/\mu m$, the



(a)



(b)

Figure 8.4: (a) Carrier accumulation near the drain. Thickness of the arrow is indicative of the magnitude of carriers moving in the direction of the arrow. (b) Effect of increasing the generation rate by increasing g_c and g_v in the non local tunneling model on the band diagram.

improvement in I_{ON} with increase in g_c and g_v reduces (Fig. 8.2(b)). The reason behind this behavior can be understood by examining the inversion density N_{inv} (Fig. 8.3(a)), the electron velocity (Fig. 8.3(b)) and the potential energy (Fig. 8.4(b)) along the channel. As the g_c value is increased, the generation rate and N_{inv} in the channel increase as well (solid lines in Fig. 8.3(a)). Due to large field at the source-channel tunneling junction, the carriers near the source have a large velocity close to the saturation value. However as the carriers move towards the drain, the velocity tends to decrease (solid lines in Fig. 8.3(b)) which is compensated for by the increase of N_{inv} (solid lines in Fig. 8.3(a)). Hence all the generated carrier are not swept to the drain, resulting into accumulation of carrier in channel near the drain (Fig. 8.4(a)). The increase of N_{inv} with g_c eventually tends to push up the conduction band edge in the channel, which in turn increases the tunneling distance (solid lines in Fig. 8.4(b)). Therefore the increase in tunneling current, which is exponentially dependent on the tunneling distance, gets limited by this electrostatic feedback effect.

In Fig. 8.2 we also observe that, as the velocity saturation value (v_{sat}) is increased (by use of alternate channel material), the I_{ON} for a given g_c value tends to increase. This is clearly explained by Fig. 8.3(a),(b) and 8.4(b). In fact, by increasing velocity saturation value, the average carrier velocity is enhanced throughout the channel (dot-dash line in

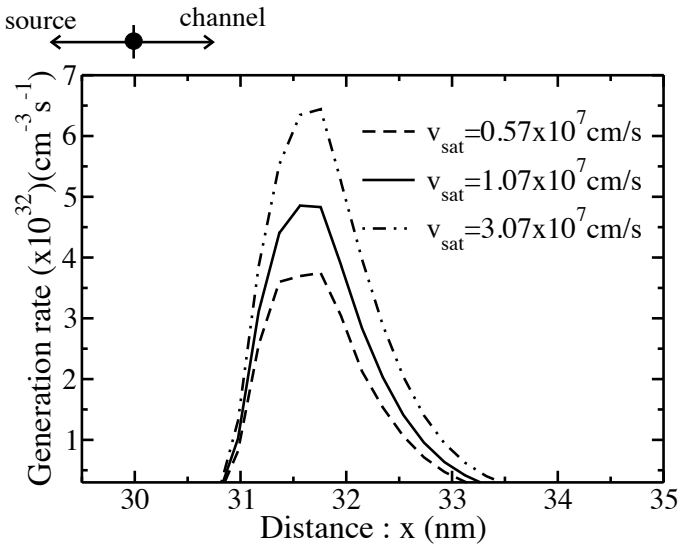


Figure 8.5: The electron generation rate along the channel.

Fig. 8.3(b)), so that a smaller N_{inv} is needed to sustain I_{ON} (dot-dash line in Fig. 8.3(a)) which in turn reduces the electrostatic feedback on the conduction band edge (dot-dash line in Fig. 8.4(b)). Hence, for a given g_c, the electrostatic feedback is weaker and the I_{ON} is larger for higher value of v_{sat}. This is clearly observed in Fig. 8.5 (dot-dashed line), which shows that, for a given g_c, the tunneling generation rate increases with v_{sat}. Conversely a decrease in v_{sat} value enhances the electrostatic feedback effect (dashed line in Fig. 8.3(a),(b) and 8.4(b)) resulting into decrease in generation rate (dashed line in Fig. 8.5) and I_{ON}.

In order to complete the analysis concerning the impact of the electron velocity on the I_{ON}, Fig. 8.2(b) also reports the I_{ON} obtained for $v_{sat} = 1.07\text{x}10^7$ cm/s by changing the low field mobility μ_o and the parameter β in the Caughey-Thomas velocity (v) versus field (F) relation:

$$v(F) = \frac{\mu_o}{\left[1 + (\frac{F\mu_0}{v_{sat}})^\beta\right]^{\frac{1}{\beta}}} \tag{8.1}$$

The curve labeled with $\mu_e = 600$ cm^2/V/s corresponds to simulations with a constant mobility (μ_o) value for electrons. The curve labeled $\beta = 2$, instead corresponds to a doubling of the default value $\beta = 1$. In both cases velocity saturation is included in the simulations. As it can be seen in Fig. 8.2(b), the effect of both μ_o and β is quite modest. This is because the electron velocity is very close to v_{sat} near the source-channel junction (Fig. 8.3(b)), so that the μ_o and β variations result in very small changes of the electron velocity and N_{inv} close to the tunneling region and thus in small changes of the band profile and of the tunneling generation rate.

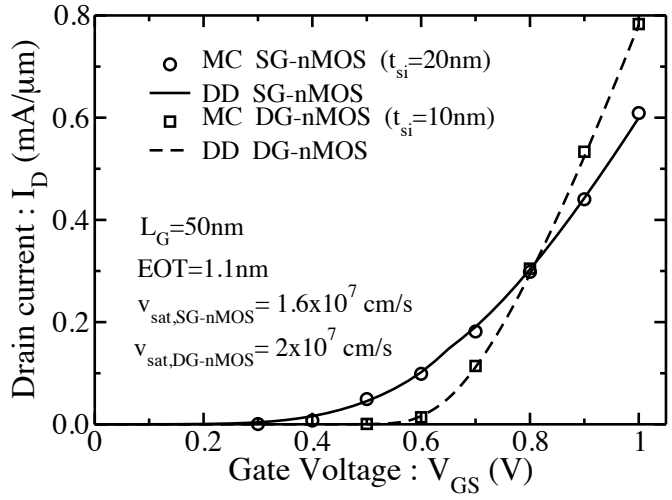


Figure 8.6: The simulated characteristic of SG-nMOS and DG-nMOS with v_{sat} = 1.6x10^7 cm/s and v_{sat} = 2x10^7 cm/s respectively. MSMC model as in [128]. t_{si} is the thickness of silicon.

8.4 Impact of Channel Transport on the I_{ON} of n-channel TFET using Technology Boosters

The use of the Drift Diffusion (DD) model for the channel transport is certainly simplistic for a channel length of about 50 nm. However, we verified that the use of the energy balance model dramatically deteriorates the numerical convergence on the simula-

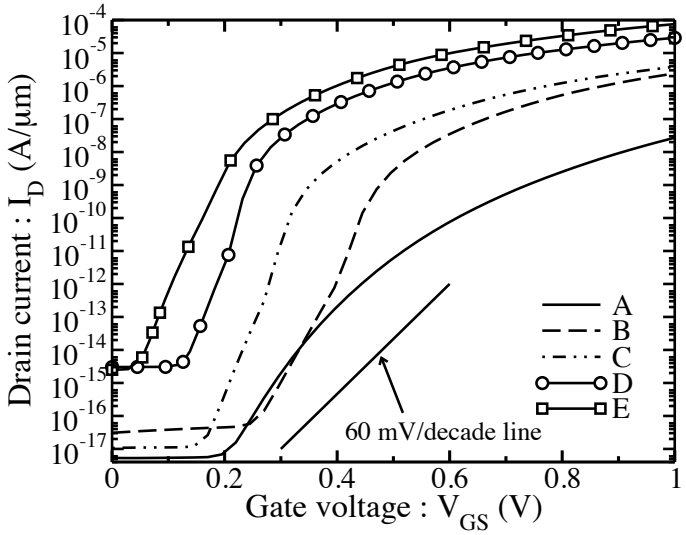


Figure 8.7: The I_D-V_{GS} characteristics for different technology boosters. (A) non-underlap nTFET with SiO_2 spacer (Fig. 5.2(a); (B) non-underlap nTFET with dual-k spacer (F1g. 5.2(b)); (C) same as B with underlap structure (Fig. 5.2(c)); (D) same as C with 4 GPa uniaxial tensile stress in the source/drain direction; (E) underlap DG-nTFET with dual-k spacer and 4 GPa uniaxial tensile stress in the source/drain direction (Fig. 8.1).

Table 8.1: Changes in the silicon band edges and corresponding value of the band-gap produced by a uniaxial stress in the ⟨110⟩ source-drain direction of a (100) TFET. The band edges are calculated according to [131–133].

Stress (GPa)	Conduction Band (eV)	Valence Band (eV)	Bandgap (eV)
0	1.170	0	1.170
1	1.149	0.027	1.122
2	1.121	0.054	1.067
3	1.085	0.081	1.004
4	1.043	0.108	0.935

tions, in spite of a disputable improvement of the physical accuracy [129]. To improve our confidence in the DD model we followed the approach proposed in [130] and adjusted the saturation velocity v_{sat} in the Caughey-Thomas velocity (v) versus field (F) relation of Eq. 8.1 to reproduce the $I-V$ characteristics of MOSFETs simulated with the multi-sub-band Monte Carlo (MSMC) simulator of [128]. To this purpose, we designed single gate MOSFET (SG-nMOS) and double gate MOSFET (DG-nMOS) with the same channel length and oxide thickness as the TFETs studied throughout this chapter. Fig. 8.6 shows that the DD can reproduce fairly well the MSMC results by increasing the v_{sat} to 1.6x10^7 cm/s for SG-nMOS and to 2x10^7 cm/s for DG-nMOS. The calibrated v_{sat} values are used only in the simulations of Fig. 8.7 to test the effectiveness of different technology boosters. The v_{sat} is instead varied as a parameter in most of the analysis presented below to study the impact of the electron velocity on I_{ON} of the TFETs.

Fig. 8.7 shows the effect of various technology boosters on Si nTFET. The use of dual-k spacer with Si TFET improves the I_{ON} with negligible impact on the I_{OFF} for non-underlap structure. Use of underlap along with dual-k spacer gives further improvement in the tunneling currents as detailed in chapter 5. The improvement in I_{ON} for DG-nTFET (Fig. 8.1(c)) is due to use of multi gate and ultra thin body.

A uniaxial tensile stress in the ⟨110⟩ source-drain direction of a (100) TFET can enhance the tunneling generation rate by lowering some of the silicon conduction band minima and by shifting upwards the valence band edge. We calculated the strain induced energy shifts of the conduction band Δ_z valleys according to [131] and the shifts of the valence band maxima by using the six bands $\mathbf{k}\cdot\mathbf{p}$ model [132, 133]; the results is reported in Table 8.1 and it has then been used in the TCAD simulations. The uniaxial tensile stress is also known to improve the electron mobility [134], however, lacking a reliable model for the stress dependence of the mobility in the TCAD framework and considering the negligible effect of the mobility on the I_{ON} shown in Fig. 8.2(b), the strain induced mobility improvements were not accounted for in the simulations of Figs. 8.7 to 8.9.

Fig. 8.8 shows the effect of saturation velocity on the I_{ON} for highest tunneling currents

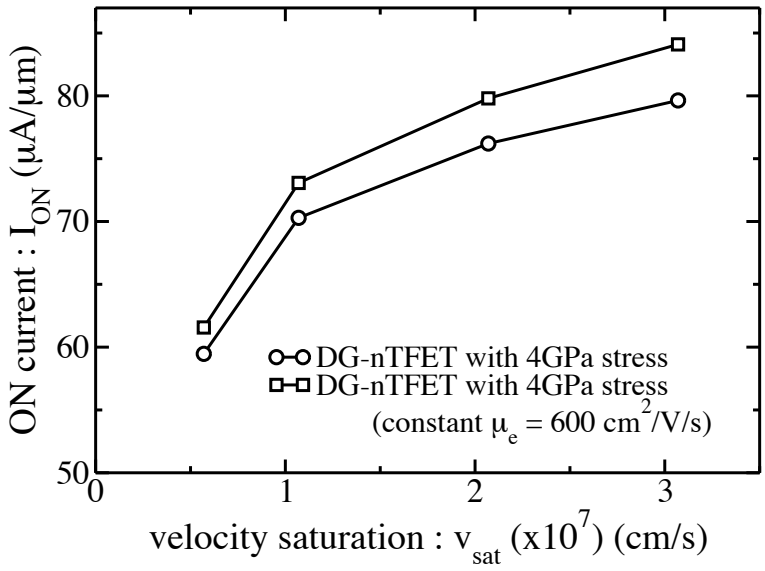


Figure 8.8: The ON current versus velocity saturation in DG-nTFET.

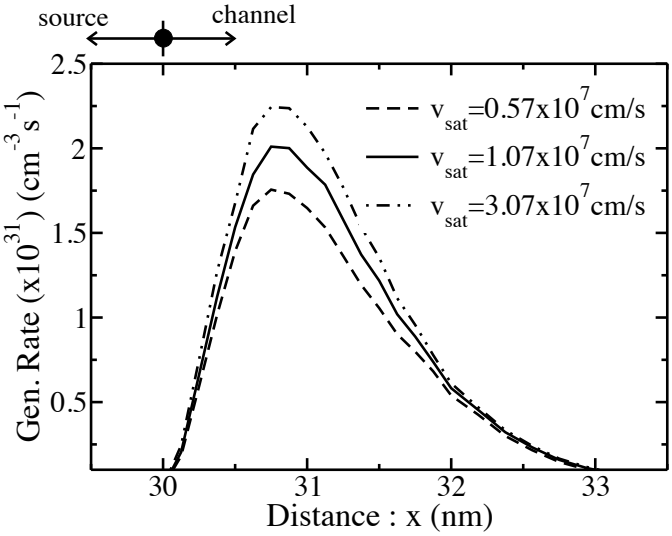
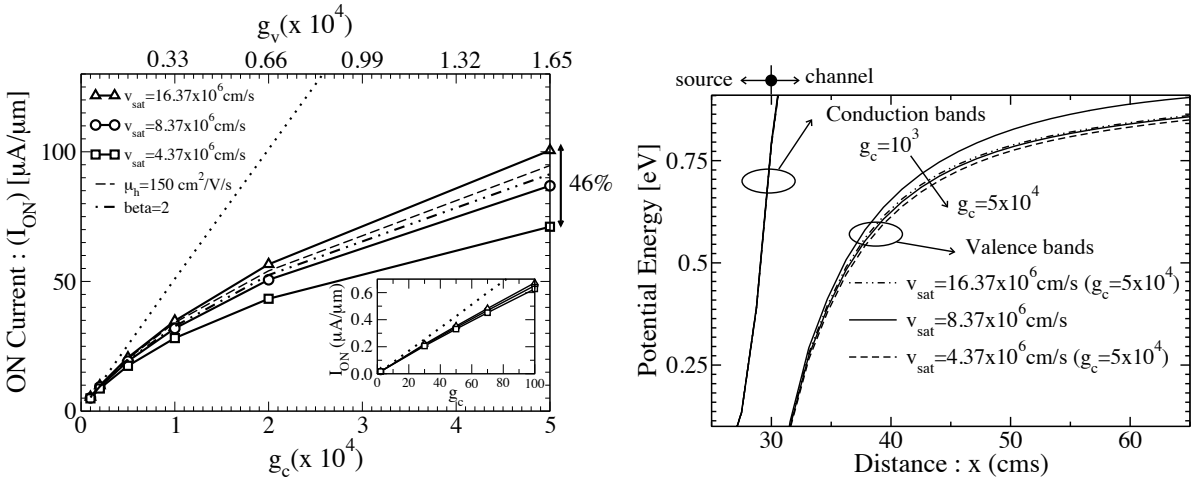


Figure 8.9: The generation rate along the channel in DG-nTFET.

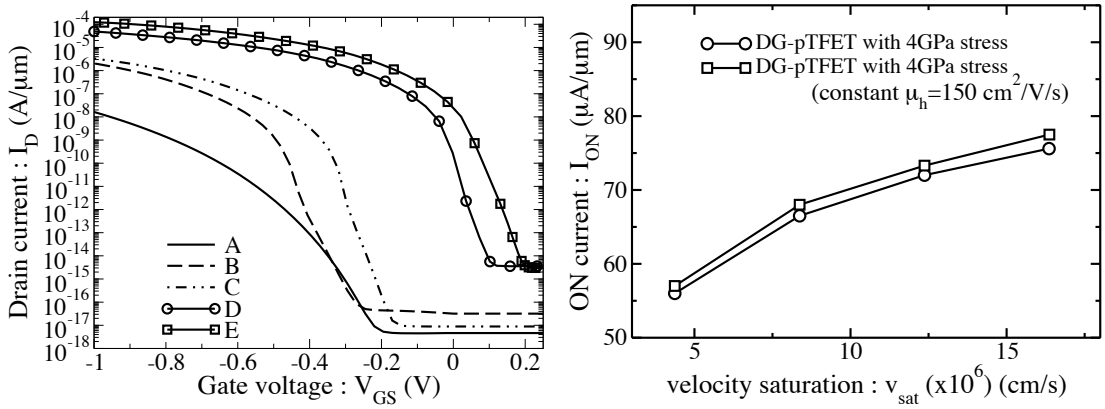
obtained for strained DG-nTFET with dual k spacer. We observe trends qualitatively similar to those observed in Fig. 8.2 for the toy model, namely I_{ON} increases with increase in the value of v_{sat}. The dependence of I_{ON} on v_{sat} has the same origin as illustrated in Fig. 8.3(a),(b) and 8.4(b), namely an increase of the carrier velocity reduces the inversion density in the channel and favors the band bending at the source junction that produces the tunneling. Hence the tunneling generation rate increases with v_{sat} as shown in Fig. 8.9.



(a) (b)

Figure 8.10: (a) The effect of increasing the generation rate on I_{ON} of pTFET by increasing g_c and g_v in the non local tunneling model. I_{ON} for constant hole mobility $\mu_h = 150$ $cm^2/V/s$ and $\beta = 2$ are computed for $v_{sat} = 8.37x10^6$ cm/s. The dotted straight line corresponds to an I_{ON} proportional to g_c. (b) The effect of increasing the generation rate on band diagram by increasing g_c and g_v in non local tunneling model.

8.5 Impact of the Channel Transport on the I_{ON} of p-channel TFET



(a) (b)

Figure 8.11: (a)The I_D-V_{GS} characteristics for different technology boosters. (A) non-underlap pTFET with SiO_2 spacer; (B) non-underlap pTFET with dual-k spacer; (C) same as B with underlap structure; (D) same as C with 4 GPa uniaxial tensile stress in the source/drain direction; (E) underlap DG-pTFET with dual-k spacer and 4 GPa uniaxial tensile stress in the source/drain direction. (b)The ON current versus velocity saturation in DG-pTFET with 4 GPa stress.

The p-channel TFET, where the carrier transport is by holes, also exhibit similar electrostatic feedback effect. The same technology boosters and structures (n^+-i-p doping

used with same doping level and profile) were used for the pTFET. The work function used is 5.16 eV. The study with the toy model using pTFET with SiO_2 spacers show similar reduction in the improvement of I_{ON} at higher g_c and g_v values as seen in Fig. 8.10(a). This is due the electrostatic feedback effect observed from the band diagram (Fig. 8.10(b)). The I_D-V_{GS} characteristics of pTFET with same technology booster as those used for nTFET are shown in Fig. 8.11(a). Considering the negligible effect of the mobility on the I_{ON} shown in Fig. 8.10(a), the strain induced mobility improvements were not accounted for in the simulations of Figs. 8.11(a) and (b). An improvement in I_{ON} with increase in saturation velocity for DG-pTFET with 4 GPa stress (bandgap = 0.935 eV from Table 1.1) is observed (Fig. 8.11(b)) consistent with the trend observed in DG-nTFET (Fig. 8.8).

8.6 Conclusions

We show that for I_{ON} values larger than few $\mu A/\mu m$, the BTBT generated carriers in TFETs tend to accumulate in the device channel and produce an electrostatic feedback which limits the I_{ON}. In this regime the I_{ON} becomes sensitive to the electron velocity and increases with it.

These results point out that the tunneling barrier may be the most important but certainly not the only element to be considered to achieve large I_{ON} in TFETs.

Chapter 9

Conclusions

In this work, we have attempted to optimize the device and circuit performance of Tunnel FET using 2-D TCAD simulations. In the initial part of the work (Chapter 4), a calibrated local model of tunneling was used as the non local model for tunneling was not available in the TCAD suite. However the results were later verified using non local model showing similar trends. It is observed that the local model computes higher magnitude of current as compared to the non local model under identical bias conditions particularly at $V_{GS} = 1$ V and $V_{DS} = 0$ V. The non local model in SENTAURUS, which takes into account the potential profile along the entire tunneling path, gives more accurate tunneling currents. This model was calibrated to experimental data from Fair and Wivell [114].

The TFET was optimized by using high-k dielectric material for the spacer. The nTFET with 1.1 nm SiO_2 gate dielectric was shown to exhibit higher tunneling current with high k spacers of width ≤ 5 nm. This is due to improved fringe field coupling through the high k spacer at the source-channel junction which reduces the tunneling width. This improvement in I_{ON} increases with increase in k of the spacer without deterioration in I_{OFF}. Similar results were observed for pTFET. However as the width of the high k spacer > 5 nm, the fringe field in the high-k spacer gets spread. This modifies the bands under the spacer in such a way that the tunneling width increases and the tunneling currents reduces. Hence only thin layers of high-k spacer improve the tunneling currents of TFET. However, when such thin high-k spacers are used, the SiO_2 pre-metal dielectric layer used for isolating the gate and source/drain metal contact would be located next to these thin high-k spacer. This gives the configuration of dual k spacer, where the thickness of the high k layer is smaller and the low k layer is higher. The performance of both nTFET and pTFET with dual-k was evaluated. A gate-source underlap structure was also proposed and the underlap value was optimized to 2 nm. This underlap structure reduces the gate length of the TFET thereby reducing the gate capacitance along with further improvement in I_{ON}.

Fabricating TFET with EOT of 1.1 nm would involve use of high-k dielectric. The

performance improvement is due to enhanced fringe coupling through the dual-k spacer which is also affected by the gate dielectric constant and it's thickness. Hence the performance improvement was studied for (i) SiO_2, (ii) Al_3O_2, (iii) HfO_2 gate dielectric and a more realistic case of (iv) HfO_2 gate dielectric with SiO_2 interfacial layer. The EOT was kept constant at 1.1 nm. It was found that for high k (HfO_2) gate dielectric, performance improvements occurs for lower spacer k values consistent with the trends reported in literature [55, 60]. As the spacer k value is increased a minima is obtained for I_{ON} beyond which the the I_{ON} increases for all the gate dielectric considered. Higher the k value of the gate dielectric, higher is the k value at which the minima occurs. The TFET with high k (HfO_2) gate dielectric gives the least improvement with dual-k spacers. However for case (iv) (HfO_2+SiO_2), an improvement of more than two orders of magnitude in I_{ON} for hk = 45 is obtained in contrast to low I_{ON} for gate dielectric of only HfO_2 layer.

The use of high k material in the spacer increases the device capacitance. It was found that replacing the drain side spacer with oxide spacer reduces the device capacitance without deteriorating the I_{ON}. Such an asymmetric structure improves the circuit performance by lowering the C_{gd}, but would increase the process complexity for fabrication.

The performance improvement of the dual-k TFET was evaluated at circuit level using mixed mode simulation of inverter. Although the capacitance increases due to increase in k value of the spacer, the magnitude of improvement in tunneling currents offsets this increase and better inverter performance is observed compared to TFET with oxide spacer. The underlap structure gives lower delay and lower overshoots compared with non-underlap structure. The asymmetric structure gives better performance than symmetric structure. The underlap structure with a gate-drain underlap ($L_G = 8$ nm) gives the best performance. Since the improvement obtained is < 10 % due to use of asymmetric TFET structure, the accompanied increase in process complexity and cost is not justified.

Mixed mode simulation of circuit with large number of TFETs has severe convergence issues. Hence the LUT base simulation were used. It was found that the inverter delay for various fanouts reduces and the ring oscillator frequency increases for underlap dual-k TFET. The static noise margins of SRAM also improve for underlap dual-k TFET. The LUT based inverter simulation validates the device level optimization results.

The conventional CMOS technology uses a two layer spacer made of a thin SiO_2 inner layer and a thicker Si_3N_4 outer layer. The proposed dual-k spacer is similar, except for the dielectric constants of the materials used. Lee et al. [119] have proposed the design of T shaped gate underlap MOSFET structure with dual-k spacer along with the process flow for the fabrication of the same. Such spacers can be easily integrated in planar TFETs made by typical process flows and is a feasible option for improving the performance of TFETs.

All the technology boosters reported in this work and in literature focus on the improvement of the generation rate at the tunneling junction and little attention has been

devoted to the possible role of the carrier transport in the channel. Since tunneling is a non local phenomenon which depends on the entire potential profile along the channel, it is affected not only by the generation rate at the tunneling junction, but also by how effectively the generated charge is swept along the channel to the drain contact. Using a toy model to artificially increase the generation rate by changing the prefactors in the tunneling model, we show that for I_{ON} values roughly larger than few $\mu A/\mu m$, the I_{ON} does not increase proportionally to the tunneling prefactors. This is essentially because carriers generated are not effectively swept across the channel due to the low electric field at the drain side. The accumulation of the carrier in the channel near the drain side modifies the potential profile in such a way so as to partly counteract the increase of the tunneling generation rate. Such an electrostatic feedback increases for smaller values of saturation velocity. Hence I_{ON} decreases for smaller value of velocity saturation (by use of alternate channel material) and vice versa. The use of various technology booster validate these results. A similar electrostatic feedback along with similar influence of velocity saturation value on I_{ON} was observed when the tunneling generation rate was increased by using the technology booster such as dual-k spacer, stress and multi-gate TFET.

9.1 Future work

One of the major challenge in fabrication of lateral TFETs is to obtain a sharp source doping profile. Silicidation of the source to achieve dopant segregation at source-channel junction [97, 98] and use of advanced anneal technique [96] have been used to achieve the same. The low temperature CVD technique to grow silicon epitaxial layer with sharp doping profile can also be explored for vertical TFET [135]. Improving the source-channel doping profile could be taken up as future work.

The use of raised source/drain [102, 103] and innovative architectures [38, 104] to introduce vertical tunneling component at the gate-source or gate/channel interface makes the tunneling currents independent of the source doping profile. Innovative arictectures in 2-D and 3-D incoporating both the lateral component and vertical component of tunneling can be developed and optimized.

The tunneling current are also sensitive to the gate alignment to source-channel junction in the non-underlap TFETs [93] and the source-gate underlap in the underlap TFETs. Process variation study can be done as part of the future work. However the tunneling currents are relatively unaffected by the gate-drain underlap which may be used as a parameter to reduce ambipolarity, I_{OFF} (specially in hetero junction TFETs) and the capacitance of TFET to improve circuit performance [25, 26, 44, 50].

The improvement in the exponential nature of I_D-V_{DS} characteristics of TFET at low V_{DS} can greatly improve the switching behaviour. Use of a broken bandgap source-channel hetero junction can improve this part of I_D-V_{DS} characteristics [40]. Such hetero

junction has been demonstrated using CNT [40] and III-V compound semiconductor [76]. The use of dual-k spacer TFET with broken bandgap hetero junction can be explored to improve I_D-V_{DS} characteristic at low V_{DS} and then demonstrate an improvement in digital circuit performance.

LUT based circuit simulation with innovative circuit architecture can also be done as part of the future work.

References

[1] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. pp 164-173, Cambridge University Press, 1998.

[2] K. K. Bhuwalka, "Novel tunneling devices for future CMOS technologies," Ph.D. dissertation, Universitaet der Bundeswehr, Munich, Germany, http://ub.unibw-muenchen.de/dissertationen/ediss/bhuwalka-krishna/inhalt.pdf, 2005.

[3] H. S. Wong, K. K. Chan, and Y. Taur, "Self-aligned (top and bottom) double gate MOSFET with a 25 nm thick silicon channel," in *Technical Digest of the International Electron Device Meeting*, December 1997, pp. 427–430.

[4] X. Huang, W. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. Choi, K. Asano, V. Subramanian, T. King, J. Bokor, and C. Hu, "Sub-50-nm FinFET:PMOS," in *Technical Digest of the International Electron Device Meeting*, December 1999, pp. 67–70.

[5] M. Jurczak, T. Skotnicki, M. Paoli, B. Tormen, J. Martins, J. Regolini, D. Dutartre, P. Ribot, D. Lenoble, R. Pantel, and S. Monfray, "Silicon on nothing (SON) - an innovative process for advanced CMOS," *IEEE Transactions on Electron Devices*, vol. 47, no. 11, pp. 2179–2187, 2000.

[6] J. Tucker, C. Wang, and P. Carney, "Silicon field effect transistor based on quantum tunneling," *Applied Physics Letters*, vol. 65, no. 5, pp. 618–620, 1994.

[7] M. Kimura and T. Matsudate, "A new tpye of Schottky tunnel transistor," *IEEE Transactions on Electron Devices*, vol. 15, no. 10, pp. 412–414, 1994.

[8] K. Gopalkrishnan, P. Griffin, and J. Plummer, "I-MOS: a novel semiconductor device with a subthreshold slope lower than KT/q," in *Technical Digest of the International Electron Device Meeting*, December 2002, pp. 289–292.

[9] K. Gopalakrishnan, P. Griffin, and J. Plummer, "Impact Ionization MOS (I-MOS)-Part I Device and Circuit Simulations," *IEEE Transactions on Electron Devices*, vol. 52, no. 1, pp. 69–76, 2005.

[10] W. M. Reddick and G. A. J. Amaratunga, "Silicon Surface Tunnel Transistor," *Applied Pysics letters*, vol. 47, pp. 494–496, May 1995.

[11] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Vertical tunnel field-effect transistor with bandgap modulation and workfunction engineering," in *Proceeding of the 34th European Solid-State Device Research conference*, September 2004, pp. 241–244.

[12] M. Fulde, A. Heigl, M. Weis, M. Wimshofer, K. Arnim, T. Nirschl, M. Sterkel, G. Knoblinger, W. Hansch, G. Wachutka, and D. Schmitt-Landsiedel, "Fabrication, Optimization and Application of Complementary Multiple-Gate Tunneling FETs," in *2nd IEEE International Nanoelectronics Conference (INEC 2008)*, March 2008, pp. 579–584.

[13] W. Y. Choi, B. Park, J. D. Lee, and T. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Letters*, vol. 28, no. 8, pp. 742–745, August 2007.

[14] Q. Zhang, S. Sutar, T. Kosel, and A. Seabaugha, "Fully-depleted Ge interband tunnel transistor: Modeling and junction formation," *Solid-State Electronics*, vol. 53, pp. 30–35, November 2009.

[15] E. H. Toh, G. H. Wang, G. Samudra, and Y. C. Yeo, "Device physics and design of germanium tunneling field-effect transistor with source and drain engineering for low power and high performance applications," *Journal of Applied Physics*, vol. 39, pp. 104 504(1–5), May 2008.

[16] K. Boucart and A. M. Ionescu, "Length scaling of the Double Gate Tunnel FET with a high-K gate dielectric," *Solid-State Electronics*, vol. 51, pp. 1500–1507, November 2007.

[17] S. R. Hofstein and G. Warfield, "The insulated gate tunnel junction triode," *IEEE Transactions on Electron Devices*, vol. 12, no. 12, pp. 66–76, February 1965.

[18] S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee, "A new three-terminal tunnel device," *IEEE Electron Device Letters*, vol. 8, no. 8, pp. 347–349, August 1987.

[19] E. Takeda, H. Hatsuoka, Y. Icura, and S. Asai, "A band to band tunneling MOS device (B^2T-MOSFET)," in *Technical Digest of the International Electron Device Meeting*, December 1988, pp. 402–405.

[20] T. Baba, "Proposal for surface tunnel transistor," *Japanese Journal of Applied Physics*, vol. 31, pp. L455–L457, April 1992.

[21] T. Uemura and T. Baba, "Characterization of Depletion type Surface Tunnel Transistors," *Japanese Journal of Applied Physics*, vol. 31, pp. L1727–L1729, December 1992.

[22] J. Koga and A. Toriumi, "Three-terminal silicon junction tunneling device for room temperature operation," *IEEE Electron Device Letters*, vol. 20, no. 10, pp. 529–531, 1999.

[23] K. K. Bhuwalka, J. Schulze, and I. Eisele, "A Simulation Approach to Optimize the Electrical Parameters of a Vertical Tunnel FET Template-based MOSFET device model," *IEEE Transactions on Electron devices*, vol. 52, no. 7, pp. 1541–1547, July 2005.

[24] S. Sedlmaier, J. Schulze, T. Sulima, C. Fink, C. Tolksdorf, A. Bayerstadler, I. Eisele, P. Wang, K. Hilsenbeck, and W. Hansch, "Phonon assisted tunneling in gated p-i-n diodes," *Materials Science and Engineering B*, vol. 89, pp. 116–119, February 2002.

[25] F. Mayer, C. L. Royer, J. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, "Impact of SOI, $Si_{1-x}Ge_xOI$ and GeOI substrates on CMOS compatible Tunnel FET performance," in *Technical Digest of the International Electron Devices meeting*, December 2008, pp. 163–166.

[26] C. L. Royer and F. Mayer, "Exhaustive experimental study of tunnel field effect transistors (tfets): From materials to architecture," in *10th International Conference on Ultimate Integration of Silicon, 2009*, March 2009, pp. 53–56.

[27] J. Appenzeller, Y. Lin, J. Knoch, and P. Avouris, "Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors," *Physical Review Letters*, vol. 93, no. 19, pp. 196 805(1–4), November 2004.

[28] G. Fiori and G. Iannaccone, "Ultralow-Voltage Bilayer Graphene Tunnel FET," *IEEE Electron Device Letters*, vol. 30, no. 10, pp. 1096–1098, October 2009.

[29] M. T. Bjork, J. K. ans H. Schmid, H. Riel, and W. Riess, "Silicon nanowire tunneling field-effect transistors," *Applied Pysics letters*, vol. 92, pp. 193 504(1–3), May 2008.

[30] Z. X. Chen, H. Y. Yu, N. Singh, N. S. Shen, R. D. Sayanthan, G. Q. Lo, and D. Kwong, "Demonstration of Tunneling FETs Based on Highly Scalable Vertical Silicon Nanowires," *IEEE Electron Device Letters*, vol. 30, no. 7, pp. 754–756, July 2009.

[31] K. E. Moselund, H. Ghoneim, M. T. Bjork, H. Schmid, S. Karg, E. Lortscher, W. Riess, and H. Riel, "VLS-grown silicon nanowire tunnel FET," in *Device Research Conference, 2009*, June 2009, pp. 23–24.

[32] S. Mookerjea and R. Krishnan and A. Vallett and T. Mayer and S. Datta, "Interband Tunnel Transistor Architecture using Narrow Gap Semiconductors," *Transactions of ECS*, vol. 19, no. 5, pp. 287–292, 2009.

[33] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Performance Comparison Between p-i-n Tunneling Transistors and Conventional MOSFETs," *IEEE Transactions on Electron devices*, vol. 56, no. 3, pp. 456–465, March 2009.

[34] D. Schmitt-Landsiedel and C. Werner, "Innovative devices for integrated circuits: A design perspective," *Solid State Electronics*, vol. 53, pp. 411–417, 2009.

[35] V. Nikam, K. K. Bhuwalka, and A. Kottantharayil, "N-channel heterojunction tunnel FET in sub 22nm regime," in *Technical Digest of the 66th Device Research conference*, June 2008, pp. 77–78.

[36] N. Jain, E. Tutuc, S. K. Banerjee, and L. F. Register, "Performance analysis of Germanium nanowire tunneling field effect transistors," in *Technical Digest of the 66th Device Research conference*, June 2008, pp. 99–100.

[37] A. Bowonder, P. Patel, K. Jeon, J. Oh, P. Majhi, H.-H. Tseng, and C. Hu, "Low-voltage green transistor using ultra shallow junction and hetero-tunneling," in *8th International workshop on Junction Technology, 2008*, May 2008, pp. 15–16.

[38] R. Asra, M. Shrivastava, K. Murali, R. Pandey, H. Gossner, and V. Rao, "A Tunnel FET for V_{DD} Scaling Below 0.6 V With a CMOS-Comparable Performance," *IEEE Transactions on Electron Devices*, vol. 58, no. 7, pp. 1855 –1863, July 2011.

[39] C. Shen, L. Yanga, G. Samudraa, and Y. Yeo, "A new robust non-local algorithm for band-to-band tunneling simulation and its application to Tunnel-FET," in *International Symposium on VLSI Technology, Systems and Applications*, April 2009, pp. 113–114.

[40] S. O. Koswatta, S. J. Koester, and W.Haen, "1D Broken-gap Tunnel Transistor with MOSFET-like On-currents and Sub-60mV/dec Subthreshold Swing," in *Technical Digest of the International Electron Device Meeting*, December 2009.

[41] A. Pal, A. B. Sachid, H. Gossner, and V. R. Rao, "Insights Into the Design and Optimization of Tunnel-FET Devices and Circuits," *IEEE Transactions on Electron Devices*, vol. 58, no. 4, pp. 1045 –1053, April 2011.

[42] E. O. Kane, "Theory of Tunneling," *Journal of Applied Physics*, vol. 32, pp. 83–91, January 1961.

[43] C. Aydin, A. Zaslavsky, and S. Luryi, "Lateral interband tunneling transistor in silicon-on-insulator," *Applied Pysics letters*, vol. 84, no. 10, pp. 1780–1782, March 2004.

[44] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Tunnel field-effect transistor without gate-drain overlap," *Applied Pysics letters*, vol. 91, no. 5, pp. 053 102(1–3), July 2007.

[45] N. Patel, A. Ramesha, and S. Mahapatra, "Drive current boosting of n-type tunnel FET with strained SiGe layer at source," *Microelectronics Journal*, vol. 39, pp. 1671–1677, February 2008.

[46] V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor," *IEEE Transactions on Electron Devices*, vol. 55, no. 4, pp. 1013–1019, April 2008.

[47] E.-H. Toh, G. H. Wang, L. Chan, D. Sylvester, C. H. Heng, G. S. Samudra, and Y. C. Yeo, "Device design and scalability of a double gate tunneling field effect transistor with silicon-germanium source," *Japanese Journal of Applied Physics*, vol. 47, pp. 2593–2597, April 2008.

[48] R. Woo, H.-Y. S. Koh, C. Onal, P. Griffin, and J. D. Plummer, "BTBT transistor scaling: can they be competitive with MOSFETs?" in *Technical Digest of the 66th Device Research conference*, June 2008, pp. 75–76.

[49] O. M. Nayfeh, C. N. Chleirigh, J. L.Hoyt, and D. A. Antoniadis, "Measurement of Enhanced Gate-Controlled Band-to-Band Tunneling in Highly Strained Silicon-Germanium Diodes," *IEEE Electron Device Letters*, vol. 29, no. 5, pp. 468–470, May 2008.

[50] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With Record High Drive Currents and < 60mV/dec Subthreshold Slope," in *Technical Digest of the International Electron Devices meeting*, December 2008, pp. 947–949.

[51] K. Bhuwalka, M. Born, M. Schindler, and M. Schmidt, "P-channel tunnel field-effect transistors down to sub-50 nm channel lengths," *Japanese Journal of Applied Physics*, vol. 45, pp. 13 106–3109, 2006.

[52] S. H. Kim, H. Kam, C.Hu, and T. K. Liu, "Germanium-Source Tunnel Field Effect Transistors with Record High I_{ON}/I_{OFF}," in *Symposium on VLSI Technology*, June 2009, pp. 178–179.

[53] S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom1, A. Liu, and S. Datta, "Experimental Demonstration of 100nm Channel Length $In_{0.53}Ga_{0.47}As$-based VerticalInter-band Tunnel Field Effect Transistors (TFETs) for Ultra Low-Power Logic and SRAM Applications," in *Technical Digest of the International Electron Devices meeting*, December 2009.

[54] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Scaling the Vertical Tunnel FET With Tunnel Bandgap Modulation and Gate Workfunction Engineering," *IEEE Transactions on Electron devices*, vol. 52, no. 5, pp. 909–917, May 2005.

[55] M. Schlosser, K. K. Bhuwalka, M. Sauter, T. Zilbauer, T. Sulima, and I. Eisele, "Fringing-Induced Drain Current Improvement in the Tunnel Field-Effect Transistor With High-k Gate Dielectrics," *IEEE Transactions on Electron Devices*, vol. 56, no. 1, pp. 100–107, January 2009.

[56] H. Y. Chang, V. Nagavarapu, A. Tura, R. Jhaveri, and J. Woo, "The SiGe heterojunction source PNPN n-MOSFET with SSOI for low power application," in *IEEE International SOI Conference, 2009*, October 2009, pp. 1–2.

[57] Y. Khatami and K. Banerjee, "Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits ," *IEEE Transactions on Electron devices*, vol. 56, no. 11, pp. 2752–2761, November 2009.

[58] S. Mookerjea and S. Datta, "Comparative study of Si, Ge and InAs based steep subthreshold slope tunnel transistors for 0.25V supply voltage logic applications," in *Technical Digest of the 66th Device Research conference*, June 2008, pp. 47–48.

[59] J. Singh, K. Ramakrishnan, S. Mookerjea, S. Datta, N. Vijaykrishnan, and D. Pradhan, "A Novel Si-Tunnel FET SRAM Design for Ultra Low-Power 0.3V VDD Application," in *Proceedings of 15th Asia South Pacific Design Automation Conference (ASPDAC)*, January 2010, pp. 181–186.

[60] C. Anghel, P. Chilagani, A. Amara, and A. Vladimirescu, "Tunnel field effect transistor with increased on current, low-k spacer and high-k dielectric," *Applied Physics letters*, vol. 96, pp. 122 104(1–3), March 2010.

[61] A. Chattopadhyay and A. Mallik, "Impact of a Spacer Dielectric and a Gate Overlap/Underlap on the Device Performance of a Tunnel Field-Effect Transistor," *IEEE Transactions on Electron Devices*, vol. 58, no. 3, pp. 677 –683, March 2011.

[62] S. Saurabh and M. J. Kumar, "Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor: Theoretical Investigation and Analysis," *Japanese Journal of Applied Physics*, vol. 48, pp. 064 503(1–7), 2009.

[63] K. Boucart and A. M. Ionescu, "Lateral Strain Profile as Key Technology Booster for All-Silicon Tunnel FETs," *IEEE Electron Device Letters*, vol. 30, no. 6, pp. 656–658, June 2009.

[64] K. Boucart, A. M. Ionescu, and W. Riess, "Asymmetrically strained all-silicon Tunnel FETs featuring 1 V operation," in *Proceeding of the 34th European Solid-State Device Research conference*, September 2009, pp. 452–456.

[65] S. O. Koswatta, D. E. Nikonov, and M. S. Lundstrom, "Computational Study of Carbon Nanotube p-i-n Tunnel FETs," in *Technical Digest of the International Electron Device Meeting*, December 2005, pp. 518–521.

[66] S. Poli, S. Reggiani, A. Gnudi, E. Gnani, and G. Baccarani, "Computational study of the ultimate scaling limits of CNT tunneling devices," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 313–321, January 2008.

[67] Q. Zhang and A. Seabaugh, "Can the interband tunnel FET outperform Si CMOS?" in *Technical Digest of the 66th Device Research conference*, June 2008, pp. 73–74.

[68] J. Nah, E. Liu, K. M. Varahramyan, D. Dillen, S. McCoy, J. Chan, and E. Tutuc, "Enhanced-Performance Germanium Nanowire Tunneling Field-Effect Transistors Using Flash-Assisted Rapid Thermal Process," *IEEE Electron Device Letters*, vol. 31, no. 12, pp. 1359–1361, December 2010.

[69] S. Datta, "Compound Semiconductor as CMOS Channel Material: Deja vu or New Paradigm?" in *Device Research Conference, 2008*, June 2008, pp. 33–36.

[70] G. Zhang, X. Wang, X. Li, A. Javey, and H. Dai, "Carbon Nanotubes: From growth, placement and assembly control to 60 mV/decade tunnel transistors," in *Technical Digest of the International Electron Device Meeting*, December 2006.

[71] J. Knoch, S. Mantla, and J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices," *Solid-State Electronics*, vol. 51, pp. 572–578, April 2007.

[72] M. Luisier and G. Klimeck, "Performance limitations of graphene nanoribbon tunneling fets due to line edge roughness," in *Device Research Conference, 2009. DRC 2009*, June 2009, pp. 201–202.

[73] C. K. Maitiy, L. K. Bera, and S. Chattopadhyay, "Strained-Si heterostructure field effect transistors," *Semiconductor Science and Technology*, vol. 13, no. 11, pp. 1225–1246, November 1998.

[74] A. S. Verhulst, W. G. Vandenberghe, K. M. Gendt, M. M. Heyns, , and G. Groeseneken, "Complementary Silicon-Based Heterostructure Tunnel-FETs With High Tunnel Rates," *IEEE Electron Device Letters*, vol. 29, no. 12, pp. 1398–1401, December 2008.

[75] Y. Yoon, S. H. Kim, and S. Salahuddin, "Performance analysis of carbon-based tunnel field-effect transistors for high frequency and ultra low power applications," *Applied Physics Letters*, vol. 97, no. 23, pp. 233 504(1–3), December 2010.

[76] J. Knoch, "Optimizing tunnel FET performance - Impact of device structure, transistor dimensions and choice of material," in *International Symposium on VLSI Technology, Systems and Applications*, April 2009, pp. 45–46.

[77] M. T. Bjork, H. Schmid, C. D. Bessire, K. E. Moselund, H. Ghoneim, S. Karg, E. Lörtscher, and H. Riel, "Si-InAs heterojunction Esaki tunnel diodes with high current densities," *Applied Physics Letters*, vol. 97, no. 16, pp. 163 501(1–3), October 2010.

[78] M. Luisier and G. Klimeck, "Performance Comparisons of Tunneling Field-Effect Transistors made of InSb, Carbon, and GaSb-InAs Broken Gap Heterostructures," in *Technical Digest of the International Electron Devices meeting*, December 2009.

[79] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. B. M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45 nm logic technology with high-k + metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning and 100 Pb-free packaging," in *Technical Digest of the International Electron Device Meeting*, December 2007, pp. 247–250.

[80] O. M. Nayfeh, C. N. Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt, and D. A. Antoniadis, "Design of Tunneling Field-Effect Transistors Using Strained-Silicon/Strained-Germanium Type-II Staggered Heterojunctions," *IEEE Electron Device Letters*, vol. 29, no. 9, pp. 1074–1077, September 2008.

[81] P. F. Guo, L. Yang, Y. Yang, L. Fan, G. Han, G. S. Samudra, and Y. Yeo, "Tunneling Field-Effect Transistor: Effect of Strain and Temperature on Tunneling Current," *IEEE Electron Device Letters*, vol. 30, no. 9, pp. 981–983, September 2009.

[82] A. Bowonder, P. Patel, K. Jeon, O. Jungwoo, P. Majhi, H. Tseng, and C. Hu, "Low-voltage green transistor using hetero-tunneling," in *IEEE Silicon Nanoelectronics Workshop*, June 2008, pp. 1–4.

[83] Y. Lu and J. Guo, "Local strain in tunneling transistors based on graphene nanoribbons," *Applied Physics Letters*, vol. 97, no. 7, pp. 073 105(1–3), August 2010.

[84] C. Sandowa, J. Knoch, C. Urbana, Q. T. Zhaoa, and S. Mantla, "Impact of electrostatics and doping concentration on the performance of silicon tunnel field-effect transistors," *Solid-State Electronics*, vol. 53, pp. 1126–1129, October 2009.

[85] R. H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *IEEE Transactions on Electron devices*, vol. 39, no. 7, pp. 1704–1710, July 1992.

[86] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-k gate dielectric," *IEEE Transactions on Electron devices*, vol. 54, no. 7, pp. 1725–1733, July 2007.

[87] M. Vadizadeh and M. Fathipour, "Using low-k oxide for reduction of leakage current in Double Gate Tunnel FET," in *10th International Conference on Ultimate Integration of Silicon, 2009*, December 2009, pp. 301–304.

[88] W. Y. Choi and W. Lee, "Hetero-Gate-Dielectric Tunneling Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 57, no. 9, pp. 2317–2320, September 2010.

[89] S. Saurabh and M. J. Kumar, "Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor," *IEEE Transactions on Electron Devices*, vol. 58, no. 2, pp. 404 –410, February 2011.

[90] N. Cui, R. Liang, and J. Xu, "Heteromaterial gate tunnel field effect transistor with lateral energy band profile modulation," *Applied Physics Letters*, vol. 98, no. 14, pp. 142 105(1–3), April 2011.

[91] M. Luisier and G. Klimeck, "Investigation of $In_xGa_{1-x}As$ Ultra-Thin-Body Tunneling FETs using a Full-Band and Atomistic Approach," in *Proceedings of the international symposium on Simulation of Semiconductor Processes and Devices*, September 2009, pp. 1–4.

[92] International technology roadmap for semiconductors (ITRS) 2009. [Online]. Available: http://www.itrs.net/links/2009ITRS/Home2009.htm

[93] L. Wang and P. Asbeck, "Design considerations for tunneling mosfets based on staggered heterojunctions for ultra-low-power applications," in *Proceedings of the IEEE*

International Conference on Nanotechnology Materials and Devices, June 2009, pp. 196–199.

[94] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics*, vol. 89, no. 10, pp. 5243–5275, May 2001.

[95] Y. C. Yeo, "Junction technologies for devices with steep subthreshold swing," in *Proceedings of the International Workshop on Junction Technology*, June 2009, pp. 11–14.

[96] J. Smith, C. Sandow, S. Das, R. Minamisawa, S. Mantl, and J. Appenzeller, "Silicon nanowire tunneling field-effect transistor arrays: Improving subthreshold performance using excimer laser annealing," *Electron Devices, IEEE Transactions on*, vol. 58, no. 7, pp. 1822 –1829, July 2011.

[97] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-Nanowire n-Type Tunneling FETs With Low Subthreshold Swing ($<$ 50 mV/decade) at Room Temperature," *IEEE Electron Device Letters*, vol. 32, no. 4, pp. 437 –439, April 2011.

[98] K. Jeon, W. Loh, P. Patel, C. Y. Kang, O. Jungwoo, A. Bowonder, C. Park, C. S. Park, C. Smith, P. Majhi, H. Tseng, R. Jammy, T. K. Liu, and C. Hu, "Si Tunnel Transistors with a Novel Silicided Source and 46mV/dec Swing," in *Symposium on VLSI Technology (VLSIT)*, June 2010, pp. 121–122.

[99] R. Jhaveri, V. Nagavarapu, and J. C. S. Woo, "Effect of Pocket Doping and Annealing Schemes on the Source-Pocket Tunnel Field-Effect Transistor," *IEEE Transactions on Electron Devices*, vol. 58, no. 1, pp. 80–86, January 2011.

[100] A. Heigl and G. Wachutka, "Simulation of Advanced Tunneling Devices," in *International Conference on Proceedings of the international symposium on Advanced Semiconductor Devices and Microsystems*, octomber 2006.

[101] C. Hu, D. Chou, P. Patel, and A. Bowonder, "Green Transistor - A V_{DD} Scaling Path for Future Low Power ICs," in *International Symposium on VLSI Technology, Systems and Applications*, April 2008, pp. 14–15.

[102] S. H. Kim, S. Agarwal, Z. A. Jacobson, P. Matheu, H. Chenming, and T. Liu, "Tunnel Field Effect Transistor With Raised Germanium Source," *IEEE Electron Device Letters*, vol. 31, no. 10, pp. 1107 –1109, october 2010.

[103] G. Han, P. Guo, Y. Yang, C. Zhan, Q. Zhou, and Y.-C. Yeo, "Silicon-based tunneling field-effect transistor with elevated germanium source formed on (110) silicon substrate," *Applied Physics Letters*, vol. 98, no. 15, pp. 153 502(1–3), April 2011.

[104] R. Asra, K. V. R. M. Murali, and V. R. Rao, "A Binary Tunnel Field Effect Transistor with a Steep Sub-threshold Swing and Increased ON Current," *Japanese Journal of Applied Physics*, vol. 49, no. 12, pp. 120 203(1–3), 2010.

[105] J. Knoch, S. Mantl, and J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices," *Solid-State Electronics*, vol. 51, pp. 572–578, 2007.

[106] K. E. Moselund, H. Ghoneim, M. T. Björk, H. Schmid, S. Karg, E. L. W. Riess, and H. Riel, "Comparison of VLS grown Si NW tunnel FETs with different gate stacks," in *Proceeding of the 34th European Solid-State Device Research conference*, September 2009, pp. 448–451.

[107] S. Mookerjea, R. Krishnan, S. Datta, and V. Narayanan, "Effective Capacitance and Drive Current for Tunnel FET (TFET) CV/I Estimation," *IEEE Transactions on Electron Devices*, vol. 56, no. 9, pp. 2092–2098, September 2009.

[108] T. Nirschl, P. F. Wang, C. Weber, J. Sedlmeir, R. Heinrich, R. Kakoschke, K. Schrufer, J. Holz, C. Pacha, T. Schulz, M. Ostermayr, A. Olbrich, G. Georgakos, E. Ruderer, W. Hansch, and D. Schmitt-Landsiedel, "The Tunneling Field Effect Transistor (TFET) as an Add-on for Ultra-Low-Voltage," in *Technical Digest of the International Electron Devices meeting (IEDM 2004)*, December 2004, pp. 195–198.

[109] S. Mookerjea, R. Krishnan, S. Datta, and V. Narayanan, "On Enhanced Miller Capacitance Effect in Interband Tunnel Transistors," *IEEE Electron Device Letters,*, vol. 30, no. 10, pp. 1102 –1104, Octomber 2009.

[110] D. kim, Y. Lee, J. Cai, I. Lauer, L. Chang, S. J. Koester, D. Sylvester, and D. Blaauw, "Low power circuit design based on heterojunction tunneling transistors (HETTs)," in *Proceedings of the 14th ACM/IEEE international symposium on Low power electronics and design*, 2009, pp. 219–224.

[111] J. Wan, C. L. Royer, A. Zaslavsky, and S. Cristoloveanu, "Tunnel field effect transistor with increased on current, low-k spacer and high-k dielectric," *Applied Physics letters*, vol. 97, pp. 243 503(1–3), December 2010.

[112] S. M. Sze, *Physics of Semiconductor Devices.* pp 418-428, Wiley publications, 2007.

[113] M. Ieong, P. M. Solomon, S. Laux, H. P. Wong, and D. Chidambarrao, "Comparison of raised and schottky source/drain mosfets using a novel tunneling contact model," in *Technical Digest of the International Electron Device Meeting*, December 1998, pp. 733–736.

[114] R. B. Fair and H. W. Wivell, "Zener and Avalanche Breakdown in As-Implanted Low-Voltage Si n-p Junctions," *IEEE Transactions on Electron Devices*, vol. 23, no. 5, pp. 512–518, May 1976.

[115] A. B. Sachid, R. Francis, M. S. Baghini, D. K. Sharma, K. Bach, R. Mahnkopf, and V. R. Rao, "Sub-20 nm Gate Length FinFET Design: Can High-κ Spacers Make a Difference?" in *Technical Digest of the International Electron Devices meeting*, December 2008, pp. 697–700.

[116] Synopsys sentaurus design suite. [Online]. Available: http://www.synopsys.com

[117] N. R. Mohapatra, M. P. Desai, S. G. Narendra, and V. R. Rao, "The effect of high-k gate dielectrics on deep submicrometer CMOS device and circuit performance," *IEEE Transactions on Electron Devices*, vol. 49, no. 5, pp. 826–831, May 2002.

[118] T. Miyashita, K. Ikeda, Y. S. Kim, T. Yamamoto, Y. Sambonsugi, H. Ochimizu, T. Sakoda, M. Okuno, H. Minakata, H. Ohta, Y. Hayami, K. Ookoshi, Y. Shimamune, M. Fukuda, A. Hatada, K. Okabe, T. Kubo, M. Tajima, T. Yamamoto, E. Motoh, T. Owada, M. Nakamura, H. Kudo, T. Sawada, J. Nagayama, A. Satoh, T. Mori, A. Hasegawa, H. K. K. Sukegawa, A. Tsukune, S. Yamaguchi, K. Ikeda, M. Kase, T. Futatsugi, S. Satoh, , and T. Sugii, "High-performance and low-power bulk logic platform utilizing FET specific multiple-stressors with highly enhanced strain and full-porous low-k interconnects for 45-nm CMOS technology," in *Technical Digest of the International Electron Devices meeting*, December 2007, pp. 251–254.

[119] H. Lee, H. Shin, and J. Lee, "Design of a 20 nm T-Gate MOSFET with a Source/Drain-to-Gate Non-Overlapped Structure," *Journal of the Korean Physical Society*, vol. 44, no. 1, pp. 65–68, January 2004.

[120] C. S. Park, M. M. Hussain, J. Huang, C. Park, K. Tateiwa, C. Young, H. K. Park, M. Cruz, D. Gilmer, K. Rader, J. Price, P. Lysaght, D. Heh, G. Bersuker, P. D. Kirsch, H. H. Tseng, and R. Jammy, "A scalable and highly manufacturable single metal gate/high-k CMOS integration for sub-32 nm technology for LSTP applications," in *Technical Digest of the Symposium on VLSI Technology*, June 2009, pp. 208–209.

[121] J. Park and C. Hu, "Air-Spacer MOSFET With Self-Aligned Contact for Future

Dense Memories," *IEEE Electron Device Letters*, vol. 30, no. 12, pp. 1368–1370, December 2009.

[122] B. Chawla, H. Gummel, and P. Kozak, "MOTIS - an MOS timing simulator," *IEEE Transactions on Circuits and Systems*, vol. 22, no. 12, pp. 901–910, December 1975.

[123] J. Lin, E. Toh, C. Shen, D. Sylvester, C. Heng, G. Samudra, and Y. Yeo, "Compact Hspice Model for IMOS device," *Electronics Letters*, vol. 44, no. 2, pp. 91–92, December 2008.

[124] A. Newton, "Techniques for the simulation of large-scale integrated circuits," *IEEE Transactions on Circuits and Systems*, vol. 26, no. 9, pp. 741–749, December 1979.

[125] N. Ashokanand, "Circuit Level Performance of Dual-k Spacer Tunnel FETs," *M.tech thesis, Indian Institute of Technology, Mumbai*, 2011.

[126] E. Seevinck, F. J. List, and J. Lohstroh, "Static Noise Margin Analysis of MOS SRAM Cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, October 1987.

[127] S. O. Koswatta and M. L. Lundstrom, "Influence of phonon scattering on the performance of p-i-n band-to-band tunneling transistors," *Applied Pysics letters*, vol. 92, pp. 043 125–1–3, January 2008.

[128] L. Lucci, P. Palestri, D. Esseni, L. Bergagnini, and L. Selmi, "Multisubband Monte Carlo Study of Transport, Quantization, and Electron-Gas Degeneration in Ultrathin SOI n-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 5, pp. 1156–1164, 2007.

[129] C. Jungemann, T. Grasser, B. Neinhuus, and B. Meinerzhagen, "Failure of moments-based transport models in nanoscale devices near equilibrium," *IEEE Transactions on Electron Devices*, vol. 52, no. 11, pp. 2404–2408, November 2005.

[130] J. D. Bude, "MOSFET modeling into the ballistic regime," in *Technical Digest of the International Electron Device Meeting*, December 2000, pp. 23–26.

[131] E. Ungersboeck, S. Dhar, G. Karlowatz, V. Sverdlov, H. Kosina, and S. Selberherr, "The effect of general strain on the band structure and electron mobility of silicon," *IEEE Transactions on Electron Devices*, vol. 54, no. 9, pp. 2183–2190, September 2007.

[132] M. V. Fischetti, Z. Ren, P. M. Solomon, M. Yang, and K. Rim, "Six-band k-p calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain, and silicon thickness," *Journal of Applied Physics*, vol. 94, no. 2, pp. 1079–1095, 2003.

[133] M. De Michielis, D. Esseni, Y. L. Tsang, P. Palestri, L. Selmi, A. G. O. Neill, and S. Chattopadhyay, "A Semianalytical Description of the Hole Band Structure in Inversion Layers for the Physically Based Modeling of pMOS Transistors," *IEEE Transactions on Electron Devices*, vol. 54, no. 9, pp. 2164–2173, 2007.

[134] S. Thompson, S. Suthram, Y. Sun, G. Sun, S. Parthasarathy, M. Chu, and T. Nishidas, "Future of Strained Si/Semiconductors in Nanoscale MOSFETs," in *Technical Digest of the International Electron Device Meeting*, December 2006, pp. 1–4.

[135] D. Lai, Y. H. Tan, O. Gunawan, L. He, and C. S. Tan, "Dopant profile control of epitaxial emitter for silicon solar cells by low temperature epitaxy," *Applied Physics Letters*, vol. 99, no. 1, pp. 011 102(1–3), July 2011.

List of Publications

[1] Hasanali G. Virani and Anil Kottantharayil, "Optimization of Hetero Junction n-channel Tunnel FET with High-k Spacers", in *Proceedings of the International Workshop on Electron Devices and Semiconductor Technology* , June 1-2, 2009.

[2] Hasanali G. Virani, Adari Rama Bhadra Rao and Anil Kottantharayil, "Investigation of Novel Si/SiGe Hetero Structures and Gate Induced Source Tunneling for Improvement of P-channel Tunnel FETs",in *Proceedings of the International Conference on Solid State devices and Materials*, 7-9 Oct 2009, Sendai, Japan.

[3] Hasanali G. Virani, Adari Rama Bhadra Rao and Anil Kottantharayil, "Optimization of P-channel Tunnel FETs using High k spacers," in *Proceedings of the 15th International Workshop on the Physics of Semiconductor Devices* , December 15-19, 2009.

[4] Hasanali G. Virani, David Esseni and Anil Kottantharayil, "Impact of Electron Velocity on the Ion of n-TFETs," in *Proceedings of the 40th European Solid State device research Conference* , pp 349 - 352, 13-17 Sept, 2010.

[5] Hasanali G. Virani, Suresh Gundapaneni and Anil Kottantharayil, "Optimization of Silicon p-channel Tunnel FET with Dual κ Spacer", in *Proceedings of the International Conference on Solid State devices and Materials* , 22-24 Sept 2010, Sendai, Japan.

[6] Hasanali G. Virani, Adari Rama Bhadra Rao and Anil Kottantharayil, "Investigation of Novel Si/SiGe Hetero Structures and Gate Induced Source Tunneling for Improvement of P-channel Tunnel FETs", in *Japanese Journal of Appled Physics*, vol. 49 , 04DC12 (1-6), April 2010.

[7] Hasanali G. Virani, Adari Rama Bhadra Rao and Anil Kottantharayil, "Dual-k spacer device architectures for the improvement of performance of silicon n-channel tunnel FETs," in *IEEE Transactions on Electron Devices* , vol. 57(10), pp 2410 - 2417, October 2010.

[8] Hasanali G. Virani, Suresh Gundapaneni and Anil Kottantharayil, "Double Dielectric Spacer for the Enhancement of Silicon p-Channel Tunnel FET Performance", in *Japanese Journal of Appled Physics*, vol. 50, 04DC04 (1-6), April 2011.

Acknowledgments

I would like to express my sincere gratitude to my thesis advisors, Prof. Anil Kottantharayil for giving me opportunity to work with him, and for providing me continuous and valuable guidance throughout the duration of my Ph.D. Programme. I am extremely grateful to him for the meticulous care with which he examined my work, which made it possible for this thesis to take its present shape.

I am also thankful to Prof. David Esseni of DIEGM, University of Udine, Italy for providing valuable guidance and advise during my research work (chapter 8) in Italy (May 2009 to April 2010) funded by the Italiani MIUR "Bando per borse a favore di giovani ricercatpri indiani".

I am highly obliged to Prof. V. Ramgopal Rao and Prof. Jayanta Mukherjee for their valuable suggestions during my progress seminars. Their valuable comments and feedback have been extremely useful. I would like to thank Prof. Dinesh Sharma for his moral support and advice. I also would like to thank the QIP coordinator, Prof. A. S. Moharir, and QIP staff member, Mr. Sudhir, for their support. I am also thankful to MCL system administrator Yogesh Save, Jainendra Singh and Almin Ansari for their technical help and support.

I also like to thank Synopsys, Inc. for providing the TCAD tools used for the simulations. This work was performed at the Center of Excellence in Nanoelectronics, Indian Institute of Technology Bombay, which is supported by the Department of Information Technology, Government of India. I am thankful to the IITB (Alumni fund) and Elecrical Engineering Department, IITB for funding my tours for the paper presentation at the conferences.

I would like to thank Adari Rama Bhadra Rao for the help in the initial simulation work. I am also thankful to Suresh Gundapaneni for his help in the calibration work of TFET. I owe to Ashokanand N. and Dr. Jawar Singh (Department of Electronics and Communication Engineering, Jaypee University of Engineering and Technology, Guna) for the development and implementation of the accurate LUT technique in Cadence verilog-A, which made it possible for the simulation of TFET-based circuits. It has been a wonderful experience to be part of the Microelectronics group and I thank my other colleagues and friends, Venkatnarayan Hariharan, Sudhakar Mande, Ramesh Navan Raju, Rajesh Thaker, Mayank Shrivastava, Angada Sachid, and many other, for the useful discussions, technical support, and making my stay enjoyable.

I take this opportunity to thank Ms. Tanvi Shelatkar, Ms. Jyoti, Ms. Madhu, Ms. Vaishali, Ms. Meenu, Ms. Shashi Anchan, and other staff members of the EE Department and Academic office for their support and timely help during the Ph.D. Programme.

I am also thankful to the ex-principal of my parent college, Prof. G. M. Gupt, for supporting my deputation at IIT Bombay for Ph.D research work. I am also thankful to Prof. R. B. Lohani, the Head of Electronics and Telecommunication Engineering Department at my parent college and my colleagues at parent college, Sebstian Mesquita, Anant Naik, Ameeta Chimulkar, Vanessa Colaco, Madhumita Tamhane, Chetan Desai, Shahajahan Kutty, and many others, for their help and co-operation during the tenure of my Ph.D work.

I want to thank my parents, wife, sons, sisters, and other family members for their continuous support, sacrifice, and motivation during the entire duration of my Ph.D. Programme. I would like to dedicate this work to all my family members.