Opto-Electric Characterization Of Dielectric Thin Films Using A Transparent Electrode

Thesis
submitted in partial fulfillment of the requirements for the degree of
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by

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This thesis is dedicated to my parents

Approval Certificate

This is to certify that the thesis entitled **"Opto-electric characterization of dielectric thin films using a transparent electrode"** by Kousik Midya (Roll No-06407014), is approved for the degree of Doctor of Philosophy.

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I declare that this written submission represents my ideas in my own words and where others ideas or words have been included; I have adequately cited and referenced the original sources. I also declare that chapter 4 of this thesis contains the work we have published in MRS Proceedings, Vol. 1447, pp. mrss12-1447. Cambridge University Press, 2012. Chapter 5 contains the work that has been published in Journal of Applied Physics, vol. 114, pp. 154101, 1-4, 2013. Chapter 6 contains the work that has been presented in the International Conference on Emerging Electronics 2016 conference and under the publication process.

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Abstract

There is a growing interest in the trap characteristics of wide band gap materials, like Silicon Dioxide (SiO_2), Silicon Nitride (Si_3N_4), Hafnium Oxide (HfO_2), Aluminum Oxide (Al_2O_3) and others due to their applications in different electronic devices. The quality of dielectric is of prime interest for better performance of the devices. The performance of electronic devices critically depends on type and density of defects (or traps) present in the semiconductor, amorphous dielectric and also at their interface. So, a detailed knowledge of trap characteristics is highly important. Trap is actually an impurity or charged point defect in semiconductor or dielectric where carrier can be captured for a period of time. Also, trap can be described as localized electronic state in forbidden gap originated from structural defect or extensive doping. From energy position of trap levels in the forbidden gap, they can be divided in two groups: shallow and deep traps. Depending on physical position of the traps they can be divided in three groups, interface, border and bulk traps.

Different methods have been proposed to retrieve information about different trap properties. It is easier to characterize interface traps compared to bulk traps as interface traps respond more easily to the applied signal. This study is mainly focused on bulk trap characterization. Among different proposed methods "flat band voltage monitored trap-depopulation" technique seems to be most promising, as it can measure maximum number of trap parameters accurately and also with a simple device structure. In this technique dielectric, embedded in Metal-Nitride-Semiconductor (MNS) structure, is first programmed electrically to fill all the trap levels by electrons. Then the device is illuminated by light of different energy. Photon energy is increased step by step. Depending on energy position of the trap levels, trapped electrons start to respond to some specific photon energies. The main difficulty associated with this technique is that, for optical study a transparent gate electrode is required. In previous works, thin metal layers (~ 15 nm) have been used as gate electrode. Low transmission coefficient of metal layer demands the illumination to be carried out for extended duration. Also, transmittance of metal layer falls beyond the wavelength of 600 nm (~ 2 eV). So, trap levels with energy position < 2 eV cannot be distinguished using metal electrode. Moreover, device with thin metal electrode is difficult to fabricate as annealing results in agglomeration of metal with such thickness. To address all these issues, in our work thick Indium Tin Oxide (ITO) layer with high transmittance up to near Infrared (NIR) region (up to ~ 3000 nm) has been used as the gate electrode. Also, in previous works the photon energy was scanned even above the mid-gap to obtain information about the trap levels lying below the mid-gap. However, for excitation with photon energy larger than $E_G/2$ (E_G is the band gap of the material), there is a probability of transfer of an electron from valance band to that trap level or some other empty state. This transition leads to erroneous result for the calculated trap density. Such drawback can be overcome by filling all the traps either by holes (-ve bias) or electrons (+ve bias) followed by wavelength dependent photo-detrapping experiment by using photon energy up to $E_G/2$.

The study was first focused on controlling the resistivity of the deposited ITO film, without compromising transmittance in the NIR region of the spectrum. It has been observed that, (222)

oriented film only shows high transmittance in NIR region. For optimization ITO films were deposited on quartz substrate using RF sputtering technique. In most cases, deposition was performed at elevated substrate temperature. The X-ray diffraction (XRD) analysis was performed for all the films. It was found that the samples deposited at elevated substrate temperature shows (222) crystal orientation even though the deposition ambient was oxygen free. For the films deposited at room temperature, significant presence of (400) peak has been observed even after post deposition annealing (PDA). It has been observed that, for all samples the average grain size is increased with subsequent annealing. Transmittance of the film has been measured for the wavelength range from 190 to 3300 nm. Average transmittance of 84.4%, 90.2% and 85.3% for wavelengths up to 800 nm, 2500 nm and 3300 nm respectively has been obtained. The resistivity in this case is found to be as low as ~ 10^{-3} Ω-cm. The transmittances of the samples do not vary substantially upon annealing, but the resistivity decreases by several factors.

The optimized ITO films have been used to establish modified trap spectroscopy technique. Energy levels of traps in Si_3N_4 are determined using a modified trap spectroscopy method, based on filling of traps using electrical stress followed by optical detrapping, in a MNS structure. Photon energy dependent shift in the flat band voltage is used to estimate type and energetic position of the traps. Here, we report detection of two prominent hole trap levels at 0.5 and 1.1 eV above the valance band edge. The study suggests that phonons hardly participate in the detrapping process of holes in Si_3N_4.

The optimized ITO film has also been used to characterize Al_2O_3 films. Al_2O_3 thin films are used for passivation of p-type Silicon surface in solar cells. In this work we investigate how atomic layer deposition (ALD) and pulsed-dc (p-DC) reactive sputtered Al_2O_3 films respond to UltraViolet (UV) illumination. UV exposure of the passivation is inevitable in the field and stability of the films to UV is an important criteria for solar cell application. We find that the negative fixed charge in the film increases upon UV illumination, which could lead to a better passivation. In conventional process, the film has to be annealed after deposition for the activation of the passivation. Fixed oxide charge density is found to be 5.8×10^{12} cm^{-2} and 9×10^{12} cm^{-2} for annealed and UV illuminated film respectively. So, it is proposed that annealing step can be replaced by UV illumination for activation of passivation.

List of Abbreviations

AC	Alternating Current
Al	Aluminum
ALD	Atomic Layer Deposition
Al_2O_3	Aluminum Oxide
a-Si:H	Hydrogenated Amorphous Silicon
Au	Gold
BiMOSFET	BJT-MOSFET
CV	Capacitance-Voltage
CP	Charge Pumping
CVD	Chemical Vapor Deposition
CMOS	Complementary Metal Oxide Semiconductor
IV	Current versus Voltage
DLTS	Deep Level Transient Spectroscopy
SiH_2Cl_2	Dichlorosilane
DC	Direct Current
DCIV	Direct-Current Current-Voltage
e-beam	Electron Beam
ESR	Electron Spin Resonance
FWHM	Full width at half maximum
GaN	Gallium Nitride
HfO_2	Hafnium Oxide
He-Cd	Helium-Cadmium
HFCV	High Frequency CV
HCl	Hydrochloric Acid
In	Indium
$InCl_3$	Indium Chloride
ITO	Indium Tin Oxide
LPCVD	Low Pressure Chemical Vapor Deposition
MOSCap	MOS Capacitor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MNOS	Metal-Nitride-Oxide-Semiconductor
MNS	Metal-Nitride-Semiconductor

NH_3	Ammonia
nMOSFET	n-Channel MOSFET
NIR	Near InfraRed
PMMA	Poly(Methyl Methacrylate)
PDA	Post Deposition Annealing
RCA	Radio Corporation of America
RF	Radio Frequency
RI	Refractive Index
RTS	Random Telegraphic Noise Signal
SEM	Scanning Electron Microscope
SiO_2	Silicon Dioxide
Si_3N_4	Silicon Nitride
SONOS	Silicon-Oxide-Nitride-Oxide-Silicon
TSC	Thermally Stimulated Current
TSD	Thermally Stimulated Depolarization
TSEE	Thermostimulated Exoelectron Emission Technique
Sn	Tin
$SnCl_4$	Tin Tetrachloride
TiN	Titanium Nitride
UV	Ultraviolet
XRD	X-ray Diffraction
XPS	X-ray Photoelectron Spectroscopy
Y_2O_3	Yttrium Oxide

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Chapter 1

Introduction

There is a growing interest in the trap characteristics of wide band gap materials, like Silicon Dioxide (SiO_2), Silicon Nitride (Si_3N_4), Hafnium Oxide (HfO_2), Aluminum Oxide (Al_2O_3) and others due to their applications in different electronic devices like Complementary Metal Oxide Semiconductor (CMOS) field effect transistors, semiconductor memory, solar cell etc. The quality of dielectric is of prime interest, as aggressive scaling continues in the CMOS technology. The performance of electronic devices critically depends on type and density of defects (or traps) present in the semiconductor, amorphous dielectric and also at their interface.

Trap is actually an impurity or charged point defect in semiconductor/dielectric where carrier can be captured for a period of time. Also, trap can be described as localized electronic state in forbidden gap originated from structural defect or extensive doping. So, position of trap refers to its location both in energy and physical space. Now, the question arises, what is the origin of such states in the band gap of semiconductor or dielectric.

Perfect crystal is simply a model or theoretical idea. In reality it is near to impossible to find a perfect crystal. Impurities and broken bonds are two main causes of imperfect crystal structure. Imperfections introduce electronic state in forbidden gap, which acts as trap for electron or hole. So, imperfection, either intentional or unintentional, plays important role to determine the suitability of the material (semiconductor/dielectric) for a certain application.

From energy position of trap levels in the forbidden gap, they can be divided in two groups: shallow and deep traps. Electronic states lying near valance or conduction band edge are shallow traps, whereas states nearer to the mid-gap are called deep traps. It is difficult to define the criteria for which shallow or bulk traps will be generated. In case of semiconductor, mostly substitutional impurities introduce shallow traps. But in some cases interstitial atoms may also introduce such type of traps. Impurities, which introduce shallow traps, are mainly used for doping to control carrier concentration, mobility and resistivity of the material. Deep traps can influence generation and recombination of electron and hole and optical or opto-electronic properties of the material.

Depending on physical position of the traps they can be divided in three groups, interface, border and bulk traps. Traps lying at interface of two layers (say, semiconductor/dielectric) in

device, originated mainly due to the disruption in the material structure at the interface, are called interface traps. Border traps are the traps situated near the interface. Bulk traps lie in the bulk of semiconductor or dielectric layer, originated from inherent structural imperfections. As structural defects mainly cause deep traps, bulk traps are also found to be deeper state compared to interface state. Interface traps are also known as fast traps as they are capable of exchanging charge rapidly compared to bulk traps. Border traps are slower than interface traps and faster than bulk traps.

So, due to dissimilar behavior, different types of traps affect the device performance in different ways. The device performance is also determined by different properties of traps lying in the material, like density, depth (both energy and positional depth), type (electron or hole trap), cross section etc. For example, for a Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) memory device, trap density defines memory window, trap depth and cross section defines retention and programming/erazing speed.

It is also interesting that different applications need different trap properties. CMOS applications look for dielectrics with low trap density. For SONOS-like devices, charge trapping layer should be trap rich to increase memory window. At the same time, tunnel and blocking dielectric should have bulk defect and interface state as low as possible because electron hopping through tunnel or blocking layer can increase leakage of stored charge. In case of solar cell, efficiency is significantly affected by carrier recombination at wafer surface. Introduction of a layer, at Silicon (Si) interface, with high fixed charge density can reduce electron or hole concentration at the interface. This leads to decrease in surface recombination. Such layer is called passivation layer. So, increase in trap density increases the efficiency of passivation layer by introducing more fixed charge density.

So, a detailed knowledge of trap characteristics is highly important. Different methods have been proposed to retrieve information about different trap properties. It is easier to characterize interface traps compared to bulk traps as interface traps respond more easily to the applied signal. This study is mainly focused on bulk trap characterization. So, first aim of the work is to find an efficient technique to extract different parameters of traps. The proposed techniques for characterization of bulk traps can be divided in two groups: electrical and opto-electrical methods.

Among different electrical techniques, thermostimulated exoelectron emission (TSEE) technique seems most efficient for characterization of bulk traps lying in wide band gap materials [1, 2]. But it is not a direct technique and also it needs complex experimental setup and mathematical modeling.

Comparative study shows that opto-electrical measurement based techniques are more efficient and need simpler device structure. Among different opto-electrical techniques, “flat band voltage monitored trap-depopulation” is most promising, as it can measure maximum number of trap parameters (e.g., energy position of the trap levels, density of traps at each level, capture and emission cross section) accurately and also with simple device structure [3–5]. In this technique, dielectric is embedded in Metal-Insulator-Semiconductor (MIS) structure. The device is first programmed

electrically or opto-electrically to fill all the trap levels by electrons. Then the device is illuminated by light of different energy. Photon energy is increased step by step. Depending on energy position of the trap levels, trapped electrons start to respond to some specific photon energies. The main difficulty is that, for this study a transparent gate electrode is required. Thin (10-15 nm thick) Aluminum (Al) and Gold (Au) films have been used as transparent gate electrode in different studies. So annealing cannot be performed after metalization, since the thin metal film would agglomerate during annealing. Also, it is reported that, transmittance of metal layer falls beyond the wavelength of 600 nm (2 eV). So, trap levels with energy position < 2 eV cannot be distinguished using metal electrode. Moreover, it is found that device needs to be illuminated for around 1 h at each excitation energy. So, the method is time consuming too. If the thin metal gate is replaced by a thick conducting electrode with high optical transparency in broad frequency range, then all the above mentioned issues can be overcome. Also, in the reported work excitation energy more than $E_G/2$ (E_G is the band gap) has been used to detrap electrons, which may lead to erroneous result in calculation of trap density.

Silicon Nitride is an important material in modern technology as it is widely used in CMOS, solar cell and memory devices. Many researchers have reported trap characterization of Si_3N_4 thin films. But comparatively less works have been reported on energy profiling of trap levels lying in nitride thin films [1, 2]. Again, the reported works were mainly focused on energy profiling of trap levels lying above mid-gap. Properties of hole trap levels in nitride films, lying near valance band edge, have not been explored well.

In recent years, Al_2O_3 films have drawn much attention in the field of solar cell, due to its excellent performance as passivation layer. Most interestingly, it has been found that after ultraviolet (UV) exposure, performance of Al_2O_3 film is improved [6], whereas opposite trend is observed for SiO_2 [7] and Si_3N_4 [8] films. As solar cells are bound to be exposed to illumination, the positive response of Al_2O_3 films to illumination has drawn much attention of current research. It is reported that, improvement comes due to photo-injection of electrons to Al_2O_3 layer from Si substrate [9, 10]. Unfortunately very less work is reported on stability of this photo-injected charge carriers [9].

1.1 Scope of the present work

Characterization of deep traps lying in bulk of wide band gap materials is a challenge of modern nanoelectronic technology. Flat band voltage monitored trap depopulation technique with novel gate material can be an efficient technique for this purpose. In this study Indium Tin Oxide (ITO) layer has been chosen as thick transparent electrode. Process optimization has been done to obtain an ITO layer even with higher transmittance in near infrared (NIR) region. Also, in the reported work based on this technique, excitation energy more than $E_G/2$ has been used to detrap electrons, which may lead to erroneous result in trap density calculation. Modification in methodology has

also been introduced to get more accurate result.

Silicon Nitride is an important material as it finds its application in various fields of modern electronics. Low pressure chemical vapor deposition (LPCVD) method is a widely used technique to produce high quality dielectric thin films. In this work, LPCVD Silicon Nitride thin films have been characterized by using modified trap spectroscopy (or modified flat band voltage monitored trap depopulation) technique.

Al_2O_3 film shows excellent performance as passivation layer in the field of solar cell. It shows some interesting property after illumination in UV light. Response of trap properties of Al_2O_3 film to UV illumination has been studied. Optimized ITO layer has been used as gate electrode for this case also.

1.2 Organization of the thesis

The rest of the thesis is organized as follows. In chapter 2 a detailed comparative study of different bulk trap characterization techniques has been described. The discussion leads to selection of most appropriate characterization technique for wide band gap materials. A review of reported literature on optimization of ITO films has been presented. Theoretical and experimental model proposed by different researchers to explain origin of traps in nitride film have been presented here.

A brief discussion on working principle of different fabrication and characterization techniques, used in this study, has been presented in chapter 3.

Chapter 4 details the development of ITO layer with high transparency in a wide spectral range. This is followed by the development of radio frequency (RF) sputtered ITO films.

In chapter 5, modified trap spectroscopy method is applied to the characterization of Si_3N_4 films deposited by LPCVD. This is followed by experiments and discussions.

In chapter 6, we present the impact of UV illumination on the fixed charges in the Al_2O_3 films deposited by pulsed direct current (p-DC) sputtering and atomic layer deposition (ALD). Fixed oxide charges play an important role in determining the passivation quality of Al_2O_3 films for applications in Silicon solar cells. It is demonstrated that films deposited by ALD can be improved significantly by UV illumination.

Thesis ends with chapter 7 reporting conclusion and future scope.

Chapter 2

Literature Review

2.1 Different trap characterization techniques

2.1.1 Trap characterization techniques based on electrical measurements

2.1.1.1 Charge Pumping Technique

Basic principle and measurement technique

Charge pumping (CP) effect was first reported by J. Brugler and P. Jespers in 1969 [11]. They proposed that, the effect can be used to characterize interface trap density in metal–oxide–semiconductor field-effect transistor (MOSFET). In 1984 Groeseneken et al. gave major breakthrough to this technique for characterization of interface states in MOSFET structure with more accurate explanation of the technique [12]. Fig. 2.1 shows basic experimental setup for charge pumping method with an n-channel MOSFET (nMOSFET).

The source and drain of the transistor are shorted and kept grounded or at certain reverse bias voltage with the substrate. A pulse voltage signal is applied at the gate. When the applied voltage is higher than threshold voltage (V_T), electrons start to flow from source and drain to the deeply depleted channel. During this process some of the electrons are captured by interface states. During negative slope of the pulse, the surface is driven again to accumulation and the mobile charges are driven back to source and drain due to the influence of reverse bias. But, the previously captured charges will now start to recombine with majority carriers of the substrate, resulting in a negative current to the substrate. This is called charge pumping effect. For a pulsed voltage signal with frequency f, the charge pumped per cycle Q_{SS} leads to a charge pumping current in substrate given by

$$I_{CP} = f.Q_{SS} \tag{2.1}$$

Now, as the frequency f is decreased mobile charges can get enough time to interact with the

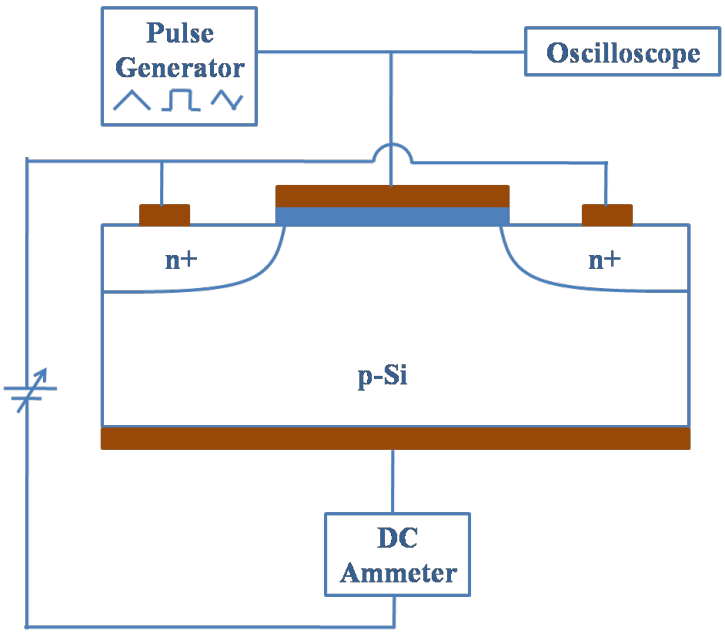

Figure 2.1: Experimental setup for CP technique.

deeper traps lying in dielectric, specially near interface. Paulsen et al. observed a 'breakpoint' frequency, below which Q_{SS} suddenly increases as near interface traps also start to contribute to total current [13]. Breakpoint frequency was found to be nearly equal to inverse of theoretically calculated trap-to-trap tunneling time constant. So, charge pumping is an efficient technique to characterize interface and near interface states.

Advantages:

1. It is a direct method for characterizing interface and border traps.
2. The technique is adequate for evaluation of type of degradation of MOS devices, e.g. due to hot carrier injection or FN tunneling.

Limitations:

1. The technique is not capable to characterize bulk traps lying far away from interface.
2. The interpretation of frequency and voltage amplitude dependencies of measured currents and the extraction of dielectric trap density in the case of ultra thin dielectric is not straightforward due to increase in parasitic leakage current [14].

2.1.1.2 Capacitance-Voltage Measurement

Measurement theory

Capacitance-Voltage (CV) characteristic of MOSFET or metal-oxide-semiconductor capacitor (MOSCap)

is the plot of capacitance versus gate voltage (V_G), as the device is driven from accumulation to inversion or in opposite direction. High frequency CV (HFCV) measurement has mostly been used for characterization of interface traps and to get an estimation of bulk trap lying in the dielectric. Interface charge and oxide charge can be calculated from shift in mid-gap voltage (V_{MG}) and threshold voltage (V_T) and flat band voltage (V_{FB}). Shift in mid-gap voltage (ΔV_{MG}) is influenced only by oxide charge density. But shift in threshold voltage (ΔV_T) and flat band voltage (ΔV_{FB}) are influenced by both interface and oxide charge density. So, combination of both can be used to calculate oxide and interface charge density following the formulas

$$Q_{OX} = -\triangle V_{MG} C_{ox} \tag{2.2}$$

$$\triangle V_{FB} - \triangle V_T = (-qD_{it} 2\phi_B / C_{ox}) \tag{2.3}$$

$$\phi_B = E_F - E_i \tag{2.4}$$

where, Q_{ox} - effective oxide charge (C/cm^2) localized at Si/dielectric interface, D_{it} - average interface state density ($cm^{-2}eV^{-1}$), E_i - intrinsic fermi level of Si (eV), E_F - fermi level after doped Si (eV), C_{ox} - oxide capacitance per unit area (F/cm^2).

But this method cannot be used for spatial profiling of the traps. To study physical distribution of traps in a dielectric lying in a Si/dielectric structure, etch back technique has been used [15]. In this technique top contact is made by mercury contact for such measurement. First, the dielectric is charged by electrons or holes. After that, oxide layer is etched back step by step and V_{FB} or V_{MG} is measured after each step. Change in mid-gap voltage ($\triangle V_{MG}$) due to oxide charge is given by

$$\triangle V_{MG} = -\left(Q_{ox}/\varepsilon_{ox}\right)\left(t_{ox} - \bar{x_1}\right) \tag{2.5}$$

where, Q_{ox} - total oxide charge (cm^{-2}), $\bar{x_1}$ - distance of the charge centroid measured from Si/dielectric interface and t_{ox} - dielectric thickness.

As long as the etching process does not affect the charge distribution, $\triangle V_{MG}$ versus t_{ox} remains a straight line and the intercept denotes $\bar{x_1}$. Woods and Williams used this technique to investigate hole trap distribution in a Si/SiO_2 structure [15]. For their experiment first the dielectric was treated by negative corona, which resulted in sufficient hole trapping in the oxide. By etch back experiment they found the hole traps are mainly distributed near the Si/SiO_2 interface, not in bulk of the oxide.

Advantages

1. This is easy to realize.

2. The technique does not need any complex device structure.

Limitations

1. In conventional CV measurement technique actually effective oxide charge density is measured. Effective oxide charge density is the sum of oxide fixed charge, mobile ionic charge and oxide trapped charge. These components cannot be distinguished by this technique. Also, it is here assumed that, the oxide charge is located at Si/SiO_2 interface. Therefore, conventional CV measurement technique is not a good option for detailed study of bulk traps.

2. With mercury probe setup, it is difficult to probe on exactly same area of the dielectric. So, non-uniformity in dielectric can lead to erroneous result.

3. Energy position of trap level cannot be obtained by this technique.

2.1.1.3 Statistical Random Noise Analysis

Measurement theory

Statistical random noise analysis is a comparatively new technique. The technique aims at study of statistical behavior of traps lying in a dielectric and their effect on device performance. In this method, the drain current of a MOSFET is measured under a fixed bias condition as a function of time. Consider a trap level lying at x_t from substrate/dielectric interface at energy level E_t. Now single electron can be captured by the trap from the substrate or can be emitted to the substrate with an average time τ_c and τ_e respectively, resulting in shift in V_T. The properties of trap responsible for random telegraphic noise signal (RTS) can be extracted from V_G dependance of τ_c and τ_e. Fig. 2.2 shows the trapping and detrapping phenomenon.

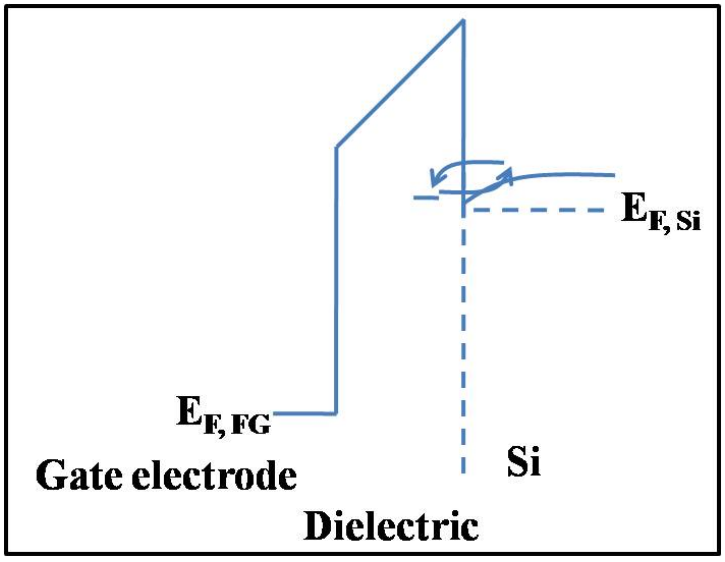

Figure 2.2: Conduction band profile explaining trap capture and emission process under +ve gate bias. The figure is adapted from [16].

Statistical model for RTS

For a single trap there are two possible states: filled (state 1) and empty (state 0). Consider a trap in state i (1 or 0) at time $t1$, which has been converted to state j (1 or 0) at time $t_2 = t_1 + T$. Here, T denotes the time period between two consecutive measurements. $Pij(i, j = 1, 0)$ denotes the probability of the trap to be converted from i to j state in time interval T. For example, if the trap is in filled state (state 1) at time t_1 then P_{10} is the probability of the trap to be in empty state (state 0) at time t_2. For a fixed V_G (i.e., fixed τ_c and τ_e), expression for P_{ij} are reported as [16]

$$P_{11} = \frac{1}{\tau_c + \tau_e}\left[\tau_c.exp\left\{-\left(\frac{1}{\tau_c} + \frac{1}{\tau_e}\right)T\right\} + \tau_e\right] \tag{2.6}$$

$$P_{10} = 1 - P_{11} \tag{2.7}$$

$$P_{00} = \frac{1}{\tau_c + \tau_e}\left[\tau_e.exp\left\{-\left(\frac{1}{\tau_c} + \frac{1}{\tau_e}\right)T\right\} + \tau_c\right] \tag{2.8}$$

$$P_{01} = 1 - P_{00} \tag{2.9}$$

τ_c and τ_c are the average time of the trap state to be in 1 and 0 states respectively.

These values can be used to compute probability of a trap causing positive or negative V_T shift. This model can be extended for multiple traps considering different RTS amplitude. Traps with different τ_c and τ_e, resulting from different x_t and E_t, should also be considered.

Advantages

1. It is a new concept of bulk trap characterization with very simple setup.
2. The technique can give information about both physical and energy position of the trap.

Limitations

1. The technique needs transistor structure.
2. The method is not direct and includes complex calculations.

2.1.1.4 Direct-Current Current-Voltage Technique

Measurement technique

Direct-Current Current-Voltage (DCIV) is a technique which can differentiate between interface

traps (D_{it}) and oxide traps (Q_{OX}) densities, which makes analysis of degradation mechanism more accurate and reliable. DCIV technique has got attention since it was proposed in 1995 [17], due to its wide range of applications [18–20].

DCIV was proposed and demonstrated by A. Neugroschel et al. in 1995 [17]. The method was described using a BiMOSFET (BJT-MOSFET) structure with nMOSFET in p-base well on an n epitaxy n^+ Si wafer with parasitic $n^+/p/n^+$ structure as shown in Fig. 2.3.

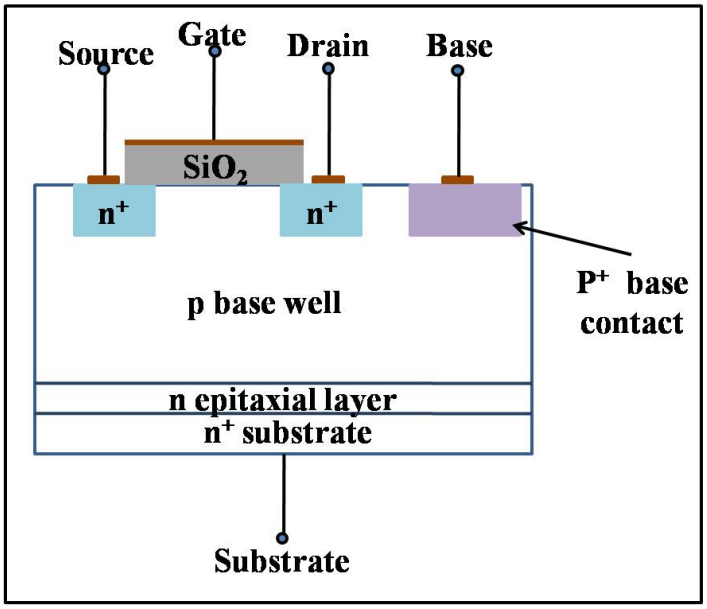

Figure 2.3: Cross sectional view of BiMOSFET structure. This figure is adapted from [17].

In this structure the base current (I_B) in vertical BJT can be measured in two configurations: top emitter and bottom emitter configurations with n^+-drain/p-base or n^+-substrate/n-epitaxy/p-base as forward biased emitter/base junction. In both configurations, D_{it} is measured from the shape of base current (I_B) versus gate voltage (V_G) graph and value of I_B at constant V_{EB} [21]. Stress induces a change in the base current, $\triangle I_B$, which arises from the recombination of electron - hole pairs at the stress induced interface traps. So, I_B is a function of $\triangle D_{it}$. But change (lateral shift) in collector current (I_C) versus gate voltage (V_G) curve is sensitive to both $\triangle D_{it}$ as well as $\triangle Q_{OX}$. So combination of both data would differentiate between two types of traps.

Advantage

1. This technique can differentiate interface and oxide traps directly. It can also distinguish the interface traps lying in channel region and drain region (not discussed here).

Limitations

1. The technique needs complex device structure.

2. As scaling progress, gate oxide becomes thinner, which results in parasitic tunneling current. The tunneling current adds up to the recombination current, leading to erroneous result.

2.1.1.5 Thermally Stimulated Current Spectroscopy

Measurement technique

Thermally Stimulated Current (TSC) is an useful method to study defect state in semiconductor or dielectric. The schematic diagram of the experiment is shown in Fig. 2.4.

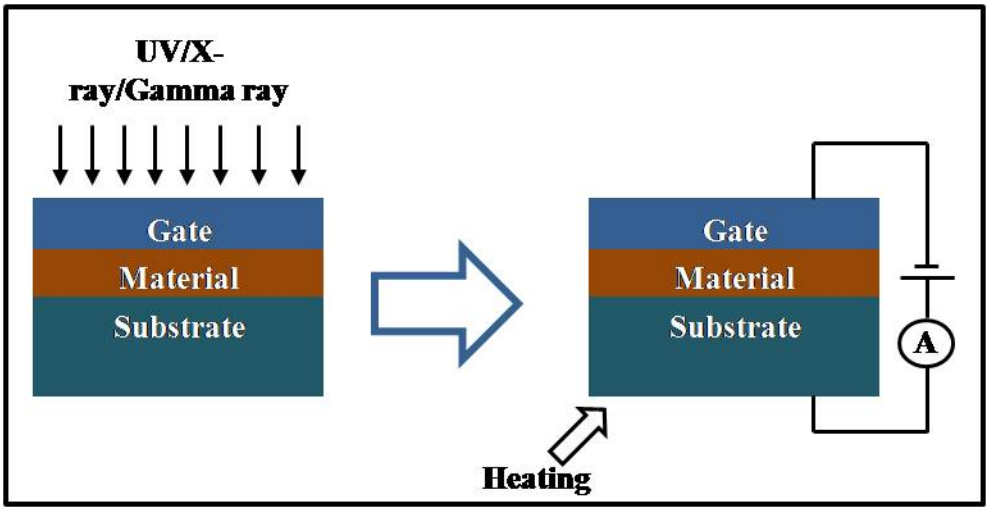

Figure 2.4: Schematic diagram of TSC measurement setup.

In this technique device is first excited by light or ultraviolet (UV) or X-Ray. So, traps are initially occupied by carriers. Next, the device is short circuited and its temperature is increased at a constant rate. The short circuit current is measured as a function of device temperature. Depending on energy position of the trap level at some specific temperature trapped carriers are excited enough to be released from the trap level. Excitation of carriers from the trap level results in increase in short circuit current. So, the peaks in current versus temperature graph indicates energy position of the trap level.

Consider temperature of the device at time t is

$$T = T_0 + \beta t \tag{2.10}$$

where, β is heating rate (K/s) and T_0 is the initial temperature (K). Then following relationship can be derived [22, 23]

$$E_C - E_t = T_m \left(1.92 \times 10^{-4} log_{10} \frac{v_{th} \sigma_n N_c}{\beta} + 3.2 \times 10^{-4} \right) - 0.015 \tag{2.11}$$

where, T_m - temperature at which peak in TSC current occurs (K), E_C - the energy of conduction band minima (eV), E_t - energy position of the trap level (eV), ν_{th} - thermal velocity of an

electron (cm/s), σ_n - capture cross section of the trap for electrons (cm^2), and N_c - density of states in conduction band (cm^{-3}). So, plotting the TSC characteristic as a function of temperature and then converting temperature scale to the energy scale using above equation, a direct image of the occupied trap distribution can be obtained.

Advantages

1. The technique needs simple device structure and comparatively simple mathematical modeling.

2. Comparatively less number of measurement techniques give information about energy position of bulk traps. TSC is one of them.

Limitations

1. Sensitivity depends on current measuring instrument.

2. With the increase in temperature mobility of the material also varies, which makes the result erroneous. The issue is more prominent for wide band gap materials, where traps are very deep and consequently carriers need quite high temperature to be excited from trap level.

3. The peaks in temperature scale may come both from electron and hole traps. So, differentiation is not possible here.

2.1.1.6 Thermostimulated Exoelectron Emission Technique

Measurement technique

In this measurement simplest device structure is required, dielectric or semiconductor deposited on substrate. Like TSC, in Thermostimulated Exoelectron Emission Technique (TSEE) also material is first irradiated by controlled electron gun or X-ray or UV ray. In both TSC and TSEE methods excitation should be done in a controlled way so that no trap would be generated due to excitation. The irradiated sample is then heated in a vacuum system. During heating, device is placed in front of an electron multiplier tube. Depending on position of the trap levels, at some specific temperatures trapped electrons would be excited enough to be emitted from the sample. The emitted electrons will be multiplied by electron multiplier, resulting in a measurable current at output. The schematic diagram of the experimental setup is shown in Fig. 2.5.

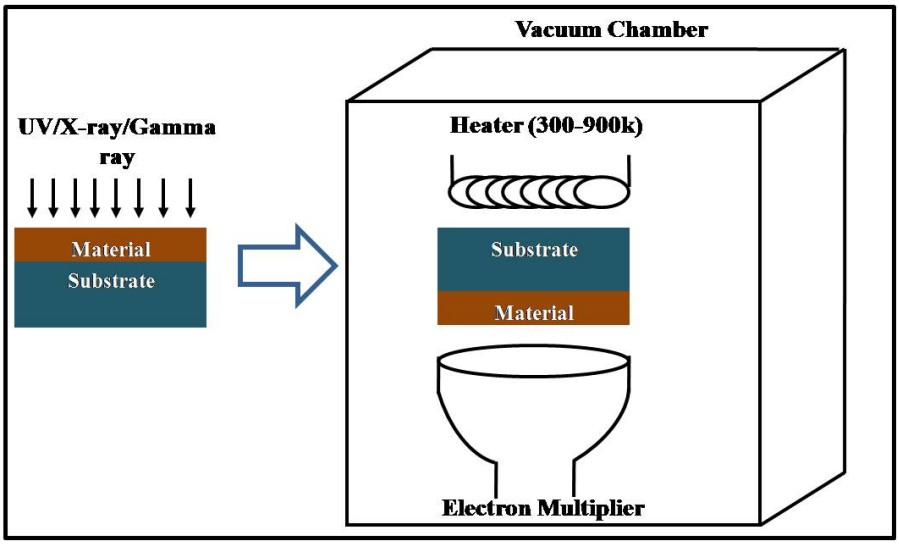

Figure 2.5: Schematic diagram of TSEE measurement setup.

Energy required by an electron to be emitted from the material is [1]

$$E_A = E_t + \chi \tag{2.12}$$

where, E_A is activation energy (eV), E_t is the energy of the trapping level (eV) and χ is electron affinity (eV).

Pure thermionic emission model is used for different materials to explain TSEE mechanism [24]. This mechanism is applicable for the materials with low electron affinity and shallow traps with $E_A < 1$ eV. But for materials like Si_3N_4, activation energy is quite high due to high electron affinity and presence of deep trap levels. For such cases thermionic mechanism is no longer applicable and emission can be explained by Auger recombination [1]. Then the technique includes complex mathematical modeling to retrieve energy level of the traps. Very few reported work is available on mathematical modelling of TSEE including Auger recombination process [2].

Advantages

1. The device structure required is simple.
2. Both energy position and density of trap levels can be obtained.
3. The technique is also applicable for wide band gap materials with proper mathematical modeling.

Limitations

1. Complex experimental setup is required.
2. More appropriate for III-V materials.

3. As discussed earlier, for wide band gap materials TSEE mechanism includes Auger recombination process, which is proportional to n^3 (n - carrier concentration). So, the technique is not sensitive for wide band gap materials with lower density of traps.

2.1.1.7 Summary of Electrical Characterization Techniques

All the techniques have some serious limitations. Most of the techniques are indirect and efficient for interface trap or shallow traps. Reported literature shows prominent trap levels exists even beyond 1 eV (from conduction band edge), in wide band materials. With proper mathematical modeling TSEE may be an efficient technique for trap rich dielectrics like Si_3N_4. But for dielectric like SiO_2, where trap concentration is relatively less TSEE is not so efficient. So, efficient technique to find properties of bulk trap in wide band gap material is not found from the above discussion.

2.1.2 Trap characterization techniques based on opto-electrical measurements

2.1.2.1 Photo-IV Measurement

Measurement theory

Current versus voltage (IV) measurement on a device under illumination is called photo-IV measurement. DeKeersmaecker and DiMaria studied SiO_2 layer by Photo-IV measurement technique [25]. In their study the device structure they have used is shown in Fig. 2.6.

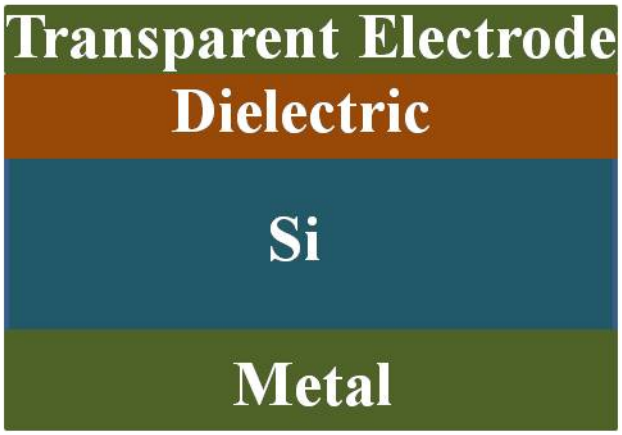

Figure 2.6: Device structure for photo-IV measurement.

10-15 nm Al layer was used as transparent electrode. In this technique trap levels in the dielectric are filled electrically or by internal photo-emission. In this technique IV measurement is performed under illumination, before and after trapping of the carriers in the dielectric. The theory is described below.

Photo-IV characteristic in MOS structure mainly depends on barrier height and distribution of trapped charge in the dielectric, which determines the internal field distribution in the dielectric. If x_0 is the position of the potential maximum including trapped space charge and metal-oxide interface is considered as origin, then field at x_0 can be expressed as [26, 28]

$$E\left(x_0\right) = \frac{V_G^- - \phi_{ms} - \psi_s^-}{L} - \frac{1}{\varepsilon}\left\{1 - \left(\bar{x}/L\right)\right\} + \frac{1}{\varepsilon}\int_0^{x_0^-} \rho\left(x\right) dx \tag{2.13}$$

when x_0 is near the metal-oxide interface and negative gate voltage;

$$E\left(x_0\right) = \left\{\left(V_G^+ - \phi_{ms} - \psi_s^+\right)/L\right\} + \bar{x}Q/\left(\varepsilon L\right) - \frac{1}{\varepsilon}\int_{x_0^+}^{L} \rho\left(x\right) dx \tag{2.14}$$

when x_0 is near the Si-oxide interface and positive gate voltage

where, V_G - applied voltage (V); ϕ_{ms} - work function difference between metal and Si substrate (V); ψ_s - Si surface potential (V); $\rho\left(x\right)$ - Trapped space charge density in the insulator (cm^{-3}); Q - integral of $\rho\left(x\right)$ over thickness L (C); $\bar{x}$ - position of centroid of the space charge (cm); ε - low frequency dielectric constant; - or + refers to polarity of the applied voltage at metal gate.

For a given photo-current level and voltage, $E\left(x_0\right)$ should be equal before and after bulk charging [25]. Using that condition and considering $\frac{1}{\varepsilon}\int_0^{x_0^-} \rho\left(x\right) dx$ and $\frac{1}{\varepsilon}\int_{x_0^+}^{L} \rho\left(x\right) dx$ are negligible and ψ_s^+ and ψ_s^- are negligible for degenerate Si or have not been changed significantly after charging (for non-degenerate Si), the following relations can be obtained

$$\triangle V_G^- = V_{GB}^- - V_{GA}^- = \frac{1}{\varepsilon}\left(L - \bar{x}\right)Q \tag{2.15}$$

when x_0 is near to the metal-oxide interface (for negative gate bias) and

$$\triangle V_G^+ = V_{GB}^+ - V_{GA}^+ = -\frac{\bar{x}}{\varepsilon}Q \tag{2.16}$$

when x_0 is near to the Si-oxide interface (for positive gate bias)

The subscripts A and B refer to the sample before and after charging of the device. Combining above two equations,

$$Q = \left(\frac{\varepsilon}{L}\right)\left(\triangle V_G^- - \triangle V_G^+\right) \tag{2.17}$$

and

$$\bar{x} = L\left[1 - \left(\triangle V_G^- / \triangle V_G^+\right)\right] \tag{2.18}$$

In their work, Dekeersmaecker and Dimaria analyzed Arsenic (As) doped SiO_2 layer in Si/SiO_2 structure. Photo-IV measurement were taken before and after charging of As-related traps by avalanche injection.

From the above result they found $\bar{x}$ = 64.7 nm and $\frac{Q}{e}$=-2.2$\times 10^{12}$ cm^{-2}.

D. Felnhofer et al. have performed experiments consisting of photo-IV and CV measurement [29]. That work is almost repetition of the work, done by D. Maria. But they also have not derived exact energy position of the trap level. In other work they have derived band gap offset by photo-IV and effective trap density by photo-CV measurement [27].

Advantages

1. Efficient technique to characterize bulk trap in dielectric.
2. Simple device structure required.

Limitation

1. Energy position of trap level cannot be found using the method.

2.1.2.2 Flat Band Voltage Monitored Trap-Depopulation Technique

Measurement theory

The technique can also be mentioned as optical detrapping technique. In this technique traps are first filled electrically or by internal photoemission. Then the device is illuminated by different excitation energy ($E_{excitation}$). Trap levels lying at a depth less than $E_{excitation}$, from bottom of the conduction band would respond to the excitation energy, i.e, trapped electrons from those levels would be excited and released to conduction band. CV measurement is taken before and after each excitation.

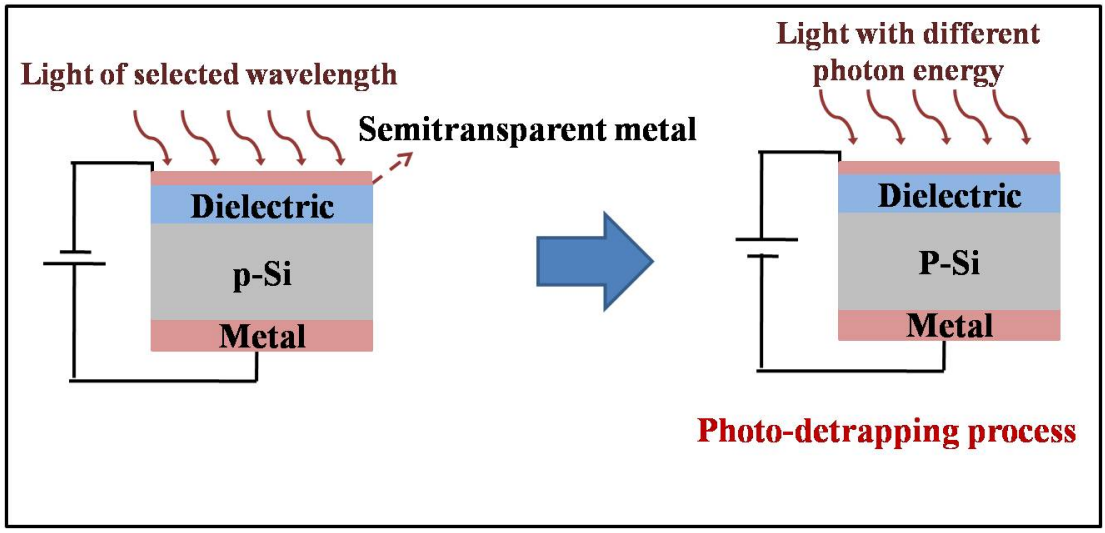

Figure 2.7: Pictorial description of the methodology for flat band voltage monitored trap-depopulation technique.

The change in flat band voltage (V_{FB}) indicates release of electron and amount of change in flat band voltage ($\triangle V_{FB}$) shows amount amount of electrons released. The device structure for this experiment is also same as shown for photo-IV measurement. The experimental steps have been schematically described in Fig. 2.7.

Kapoor and Turi studied (10 nm)Al/(110 nm) Si_3N_4/(100 nm)SiO_2/Si structure [3]. 10 nm thick Al layer was used as gate electrode. Electron trapping in the device was done by internal photoemission with excitation energy of 4.97 eV and +5V gate voltage. Excitation energy should be more than conduction band offset between Si and SiO_2 (4.2 eV) and less than Si_3N_4 band gap (~ 5.1 eV). It was observed from programing transient that, $\triangle V_{FB}$ saturates after around 70 min.

The same sample was then discharged with a photon energy of 4.14 eV and gate voltage of +5 V. Low gate voltage was used to avoid direct tunneling. They calculated amount of trapped charge using this technique.

In another work, Bibyk and Kapoor used same (10 nm)Al/(110 nm) Si_3N_4/(100 nm)SiO_2/Si structure for their experiment [4]. In this work they mainly focused on trap depopulation characteristic. First the electrons were photo injected from Al electrode by using 4.14 eV light energy and -80 V gate voltage. $\triangle V_{FB}$ was tracked by CV measurement. After charging of the device depopulation of trapped charge was performed. Depopulation was done with +10 V gate voltage and depopulating energy was varied from 2 to 3.4 eV with 0.1 eV increment.

From rate of depopulation of the trapped charge they calculated poto-ionization cross section of the deep trap centers lying in Si_3N_4 layer.

W. C. Wang et al. used the same technique to characterize Yttrium Oxide (Y_2O_3) layer deposited on Si wafer [5]. For their experiment they used 15 nm thick Gold (Au) as transparent top electrode in the Au/Y_2O_3/(2 or 5 nm)SiO_2/Si structure. Electron injected device was illuminated by photon and photon energy was varied from 1.3 to 4 eV with 0.3 eV increment. At each photon energy excitation was performed for 60 min. The experiment enables to calculate trap density from $\triangle V_{FB}$ at each 0.3 eV energy window.

Advantages

1. Needs simple device structure.

2. Various parameters like energy position of the trap levels, density of traps at each level, capture and emission cross sections can be calculated by this technique.

Limitations

1. During depopulation process excitation energy has been increased more than $E_G/2$, where E_G is the band gap of the dielectric. At such energy electron can be excited from valance band and trapped at some state which has been emptied before. So, population can even occur during depopulation process. Then trap density calculated from $\triangle V_{FB}$ would be erroneous.

2. Thin metal layers (10 - 15 nm thick) have been used as transparent gate electrode. So annealing cannot be done after metalization as the thin metal film would agglomerate during the annealing.

3. Use of metal layer introduce another difficulty. G. Hass and J. Waylonis measured transmittance of Al layer, for different thickness, as a function of wavelength [30].

Table 2.1: Tansmittance of Al film of different thickness as reported by G. Hass and J. Waylonis [30].

Film Thickness	**Transmittance (%T) at different Wavelength (nm)**				
(nm)	**220**	**300**	**400**	**500**	**600**
4	82	74	65	51	42
8	60	47	36	24	18
12	40	27	19	12	9
16	25	16	11	7	5
20	15.2	9.1	5.9	3.5	2.6
24	9.1	5.1	3.3	2.0	1.4

The result shows that transmittance decreases as wavelength increases or photon energy decreases. Consider the Al layer of thickness 12 nm (which thickness was used in the charge depopulation experiments in [3, 4]). At 650 nm (1.9 eV) transmittance reaches up to 9%. So, as photon energy is decreased below 2 eV, thin Al layer does not behave as transparent layer. So, depopulation of charged device can be started with minimum photon energy of 2 eV. That's why in all the reported work, where thin Al layer has been used as gate electrode, excitation energy starts from 2 eV. But, at this excitation energy all the trap levels lying up to 2 eV from conduction band edge, would start to respond. So, discrimination of the trap levels shallower than 2 eV would not be possible. Even, some of these trap levels may not respond to arbitrary higher energy (say, 2 eV) if phonon interaction is not so strong in that material (details discussed in chapter 5).

Wang et al. used 15 nm thick Au as gate electrode. Table 2.1 shows transmittance of Al layer as a function of wavelength.

Au shows better transmittance characteristic than Al. But for Au also transmittance decreases significantly as we move to higher wavelength. Also, Au is not a good candidate as a gate electrode, as it affects dielectric quality [31].

2.1.2.3 Other Techniques

Various techniques, frequently used to characterize wide band gap materials, have been discussed above. There are many other opto-electrical techniques that can be used for the characterization

of deep traps in different materials. Deep level transient spectroscopy (DLTS), photo capacitance, photoconductivity and photo-induced current transient spectroscopy are also used to retrieve information about deep traps. DLTS studies [32–34] can provide information about energy position of traps lying between 0.2 and 1.5 eV below the conduction band edge and density of traps with concentrations in the range of 10^{13}-10^{15} cm^{-3} range. Photo capacitance measurement [35, 36] can be used to detect deeper traps within the range of 0.8 to 2.5 eV below the conduction band edge. Optical absorption [37] and photoconductivity [38] are also able to characterize such deep levels. DLTS and photo-conductance methods are not applicable for samples with high resistivity (10^{12} Ω-cm). Photo stimulated current spectroscopy has been used for such high resistive materials like Gallium Nitride (GaN) [39]. Also Photo stimulated current spectroscopy technique do not have the ability to handle very high resistive material like Silicon Nitride (resistivity ~ 10^{14} Ω-cm).

2.1.2.4 Summary of Opto-Electrical Measurement Techniques

The discussion shows, proper study of bulk traps specially in dielectric is a difficult challenge. Every characterization technique has its own virtue and limitation. So, characterization method should be chosen depending upon the material under test and also which parameters need to be measured. From the above discussion it is clear that opto-electrical techniques have number of advantages over electrical techniques specially for characterization of bulk traps. Simpler device structure is required and also more number of trap parameters can be extracted from one technique. Techniques are more direct and deals with comparatively simpler mathematical modeling. Techniques are sensitive to low trap density also. For trap characterization of wide band gap materials (SiO_2, Si_3N_4, HfO_2 or Al_2O_3), "flat band voltage monitored trap-depopulation" technique seems to be most promising, as it can measure maximum number of trap parameters (e.g., energy position of the trap levels, density of traps at each level, capture and emission cross section) accurately and also with simple device structure. The main difficulty is that, for optical study a transparent gate electrode is required. The problem arises due to transparent thin metal layer has already been discussed in section 2.1.2.2. Annealing of the device with thin metal gate cannot be performed. Thin metal layer is not a good candidate as gate electrode when shallow traps need to be characterized. Also, it is found that device needs to be illuminated for around 1 hour at each excitation energy. So, the method is time consuming too. If the thin metal gate is replaced by a thick conducting electrode with high optical transparency in broad frequency range, then all the above mentioned issues can be solved.

In our work ITO has been used as a gate electrode to overcome the issues related to thin metal gate. To reduce duration of experiment and also to distinguish trap levels with energy position < 2 eV, we need ITO film with low resistivity and high transmittance even in NIR region.

2.2 Review of optimization of ITO films

Indium Tin Oxide is widely used in various optoelectronic devices and solar cells due to unique combination of very high transmittance and low resistivity. Extensive work is reported on optimization of transmittance and resistivity of the ITO layer. Till date, different techniques have been proposed to deposit ITO films. Chemical vapor deposition (CVD), evaporation technique, spray pyrolysis, ion beam sputtering, DC and RF sputtering are some common techniques, used for ITO deposition. Each of these processes have their own advantages and limitations. Resistivity and conductivity of deposited films depend on the deposition technique and process conditions. Here, different ITO deposition techniques have been discussed shortly with their advantages and shortcomings.

2.2.1 Different techniques for deposition of ITO films

In evaporation technique In_2O_3/SnO_2 powder is evaporated using electron beam (e-beam) or thermal evaporation. Another option is evaporation of In/Sn alloy in O_2 ambient. But in the later case due to differential evaporation rate, after few minutes concentration ratio of In and Sn alloy is changed. Hamberg et al. deposited ITO film in e-beam evaporation system using hot pressed pallets consisting of In_2O_3 + 9 mol% SnO_2. Deposition was performed in O_2 ambient and 310 °C substrate temperature [40]. ITO film with resistivity of 3×10^{-4} Ω-cm and approximately 90% transmittance was obtained in their experiment.

CVD method is relatively simple and cost effective as it does not require high vacuum. Volatile organometallic compound of metal is used in this method. Substrate is kept on a rotating hot plate reactor. For ITO deposition this technique involves vaporization of appropriate organic compound like Indium 2-Ethyl Hexanoate/Tin Chloride [41] or Indium/Tin Acetyl Acetonates [42]. Compound gas mixture along with carrier gas is allowed to flow in reaction chamber. Parameters of the deposited film can be monitored by controlling substrate temperature, composition of the gas, gas flow rate and rotating speed of the substrate. This technique generally faces difficulty, for ITO deposition, due to lack of thermally stable and volatile source materials. Uniformity of the film is another issue of this technique. Normally small size substrate is used to obtain the uniformity.

Spray pyrolysis is another technique which has been used for many years for ITO deposition. In this technique first Indium Chloride ($InCl_3$) and Tin tetrachloride ($SnCl_4$) are dissolved in appropriate solvent like Hydrochloric Acid (HCl), Propanol, water etc. The solution is sprayed on the heated substrate by an atomizer. Nitrogen (N_2), Argon (Ar) or air are normally used as carrier gas. ITO deposited by this technique can have very low resistivity (~ 5×10^{-4} Ω-cm) and about 90% transmittance in visible and near infra-red regions [43]. Very high deposition rate (200 to 400 nm/min) can be achieved by this technique. But film deposited, by this technique, has been found to have very rough surface. Homogeneous and reproducible film deposition is a challenge for this technique.

Sol-gel method is another cost effective technique. In this technique, dip-coating of the substrate in appropriate precursor sol is followed by heat treatment. Gallagher et al. deposited ITO films by dip coating of the substrate in an Acetylacetone solution of Indium and Tin Acetylacetonate [44]. The resistivity of the film was reported to be 1.1×10^{-3} Ω-cm.

Sputtering is one of the most extensively used techniques for ITO deposition. This technique offers high quality, homogeneity, better controlled composition and purity of the film throughout the wafer. This is a physical vapor deposition process where, target holder and surface holder are used as cathode and anode respectively. Ar is used as sputtered gas due to low reactivity. In this method target material is subjected to bombardment of accelerated Ar^+ ions. The bombardment results in ejection of target atom from cathode surface and subsequent deposition on the substrate. Due to conducting nature of In_2O_3-SnO_2 and In-Sn alloy, both DC [45] and RF [46] sputtering have been extensively used for ITO deposition. RF sputtering technique has some advantages over DC sputtering technique. In case of RF sputter system electrons gain energy directly from RF power (secondary electrons are not required to maintain plasma) and oscillating electrons are more efficient to ionize the gas. RF sputter is capable of maintaining plasma in lower pressure (1-15 mTorr) which results in fewer gas collisions and more line of sight deposition. In this study RF sputtering technique has been used for deposition of ITO film.

2.2.2 Reported work on optimization of different parameters

There are several sputtering variables, like RF power, sputtering pressure, substrate temperature and gas composition which affect the deposition rate considerably.

2.2.2.1 Deposition Rate Optimization

Work done by D. K. Maurya shows the variation of deposition rate as a function of O_2 percentage in the sputtering gas [47]. They observed that deposition rate decreases with increase in O_2 concentration in the reactive gas mixture. It is difficult to describe the exact mechanism responsible for the phenomenon because sputtering of a metallic alloy target involves many processes causing changes in the discharge conditions.

Work done by M. Chaung shows the effect of sputtering power on deposition rate [48]. As RF power increases from 30 to 60 W, deposition rate is enhanced from 0.8 to 3.3 nm/min. At higher RF power, more energized Ar ions pull more number of atoms and molecules out of the target. Therefore, amount of material, deposited on the substrate increases.

M. Chaung studied how deposition rate varies with the working pressure [48]. ITO was deposited in RF sputtering system in absence of oxygen flow. The deposition rate increases with working pressure, and the value increases from 2.1 to 2.6 nm/min.

According to M. Chaung, as working pressure increases total number of Ar ion increases resulting in more atoms (from target) being bombarded. So, deposition rate increases.

2.2.2.2 Resistivity Optimization

ITO is deposited both in Ar or Ar+O_2 environment. Yan-Kuin Su et al. studied the electrical resistivity of the deposited film as a function of O_2 concentration [49]. Their study indicates increase in resistivity with the increase in O_2 flow rate. The reason behind increment in resistivity has been explained by H. N. Cui et al. [50]. They proposed, defect density in the film increases with the increase in O_2 pressure. As a result, scattering of charge carriers is increased leading to rise in resistivity. In addition, as partial pressure of O_2 increases oxygen vacancy is decreased, which results in less carrier concentration (n_c) [50, 51].

Resistivity of ITO film strongly depends on annealing temperature. Annealing improves crystalline nature of the film which increases grain size. As grain boundary decreases mobility increases. D. K. Maurya observed in his study that, resistivity decreases with increase in annealing temperature and reaches at its minimum value for the film annealed at 400 °C [47]. At this temperature out-diffusion rate of oxygen atom from ITO becomes maximum. It has already been discussed that lack of oxygen results in better conductivity of ITO film.

Substrate temperature during deposition is another important parameter which can be used for controlling the resistivity of the deposited film. Ren Bingyan et al. observed that the resistivity decreases as substrate temperature is being increased [52]. Crystallinity of the film increases with substrate temperature and better crystallinity results in better conductivity. Their study show that, for a specific substrate temperature, the resistivity monotonically decreases with the increase in RF power. But study by M. Chuang shows resistivity initially decreases with deposition power and shows minimum value for deposition power of 40 W in their system [48]. Simultaneously, X-ray photoelectron spectroscopy (XPS) result shows Sn/In ratio is also maximum for 40 W. Explanation is straightforward, as discussed earlier each In atom replaced by Sn atom contribute one electron to conduction [53]. So, maximum Sn concentration at 40 W power leads to minimum resistivity.

Work done by D. H. Kim shows that the sheet resistance decreases as film thickness increases [54]. The reason were found by X-ray Diffraction (XRD) analysis of the samples. For the films with thickness below 80 nm, no characteristic peak was obtained except the broad peak for amorphous substrate Poly(Methyl Methacrylate) (PMMA). As thickness increases crystallinity improves and dominant peak for both (222) and (400) orientations are observed alongwith other peaks. It should be noted here that, PMMA substrate has been used in this work whereas for other reported investigations mostly glass or quartz substrates were used. So, for this case substrate temperature was maintained at relatively low temperature (70 °C) and no post deposition annealing (PDA) was performed. Annealing and higher substrate temperature may produce better crystallinity at comparatively lower thickness. High temperature treatment may result in better crystallinity at lower thickness.

2.2.2.3 Transmittance Optimization

Optical transmittance is an important parameter for the ITO film. ITO thin films, deposited by different techniques, have been studied by several authors [55–58]. Most of the reported works are focused on optical property of ITO films in the visible range [57–59]. However, there are few reports showing transmittance of these films in visible as well as in NIR region. Some studies have shown that the transmittance of ITO thin film falls sharply after around 1400 nm [60–62], while, others have shown good transmittance of the film beyond 1400 nm even with low resistivity [63–65].

Previous studies have shown that the ITO films have two dominant characteristic XRD peaks corresponding to the (222) and (400) planes. The XRD results for most of the reported ITO thin films with higher transmittance in NIR region show very high values for the intensity ratio I(222)/I(400). Hall measurement shows higher carrier concentration for (400) oriented film compared to (222) oriented film [55]. So, for higher carrier concentration transmittance decreases in NIR region. This can be explained following prediction of classical Drude's model [66]. According to this model, higher free carrier concentration results transition of material behavior from dielectric to metal type and transition point moves towards shorter wavelength as carrier concentration increases.

Benoy et al. have demonstrated how transmittance varies with wavelength for different film thicknesses. For the film of thickness 80 nm, nearly 85% transmittance up to 2600 nm and resistivity of 3.3×10^{-2} Ω-cm were obtained [63].

As thickness was increased to enhance the conductivity of the film, transmittance decreased sharply. The result can be explained in analogy of the work done by D. H. Kim et al., as discussed previously. (400) peak becomes more prominent as thickness increases. So, for higher thickness transmittance would decrease in NIR region.

Y. K. Su et al. observed that the transmittance of ITO film improves in visible range as O_2 flow rate decreases [49]. 90% transmittance was obtained for ITO film prepared in absence of oxygen. The explanation for such behavior has not been mentioned in their report.

Abd. El-Raheem et al. have studied properties of ITO films in different device structure [64]. First, SiO_2 layers of various thicknesses were deposited on glass substrates. After that, 200 nm ITO layers were deposited by thermal evaporation, on SiO_2, at various substrate temperature. The SiO_2 layer was used as buffer layer. They observed that the transmittance increases with the increase in buffer layer thickness. 92% average transmittance in visible region and 83% in NIR region (up to 2500 nm) were obtained in their case for ITO film deposited on 80 nm buffer SiO_2 layer with resistivity of 1.6×10^{-4} Ω-cm. In another work, transmittance of the ITO film deposited by thermal evaporation, in the wavelength range from 200 nm to 2500 nm, was found to decrease with the increase in thickness of the film [65].

To obtain better transmittance with lower resistivity H. M. Ali et al. annealed 150 nm thick film at different temperatures. Significant improvement was achieved after annealing of the film.

By annealing 150 nm thick ITO film at 400 °C for 120 min they obtained films with 82% and 85.5% average transmittance in visible region and in the NIR region (upper bound of 2500 nm) respectively and with resistivity of 2.8×10^{-4} Ω-cm .

2.2.2.4 Summary and Inferences

The above discussion indicates:

1. RF sputtering is a widely used technique for the deposition of ITO thin films due to good control on the film properties and industrial applicability of the process.
2. In RF sputtering, higher working pressure results in higher deposition rate.
3. In RF sputtering, deposition rate also increases as concentration of O_2 decreases. Better conductivity and optical property in visible range can be obtained in absence of O_2.
4. PDA results in lower resistivity and better transmittance.

As carrier concentration increases, transmittance starts to fall off at comparatively lower wavelength. On the other hand, increased carrier concentration results in lower resistivity of the film. Therefore, there is a trade-off between the transmittance at higher wavelength and conductivity of the film.

To get higher transmittance in NIR region there is no option other than (222) oriented film. After obtaining (222) oriented film resistivity can be controlled by decreasing grain boundary i.e., by using PDA.

Kim et al. proposed that only presence of O_2 in sputtering ambient causes change in preferential orientation from (400) to (222) plane [55]. But above discussion also indicates that the presence of O_2 severely degrades electrical property, deposition rate and transmittance in visible region. Aim of our work is to obtain ITO layer with less resistivity and higher transmittance in both visible and NIR region. So, if (222) oriented film can be produced without using O_2 in sputtering ambient then the goal can be achieved.

2.3 Modeling of energy distribution of trap levels in Nitride films

One aim of this study is trap characterization of Silicon Nitride thin films. Many experimental and theoretical studies have explored the origin and charge state of traps associated with a-Si_3N_4 films used in non-volatile memory devices [67–72]. Several different models have been proposed by various authors explaining charge trapping behavior in these films. Kirk [70] suggested that the Nitrogen dangling bonds are responsible for charge trapping in MNOS (Metal-Nitride-Oxide-Semiconductor) devices. On the other hand Robertson [69] and Ngai and Hasia [68] have argued

that a Silicon danging bond is responsible for charge trapping in Silicon Nitride. Kapoor et al. [71] have proposed that Silicon-Hydrogen bonds are the source of memory behavior in Silicon Nitride. Krick et al. [72] presented for the first time the conclusive evidence that paramagnetic neutral Si dangling bond defects in Silicon Nitride may capture either electrons or holes. This work is mainly focused on finding energy position of the trap levels in Silicon Nitride films. Here we will discuss some of the models which describes energy position of trap levels in Nitride film.

2.3.1 Model proposed by C. T. Kirk Jr. [70]

In 1975, Anderson presented negative U idea where doubly occupied localized gap state is more favorable than singly occupied state [73]. Kirk Jr. used that concept to find trap levels in Si_3N_4. In crystalline Si_3N_4 (c-Si_3N_4) each Silicon atom is coordinated with four Nitrogen atoms by sp^3 hybridization, where Nitrogen atom is associated to three Si atoms by sp^2 hybridization. Remaining p-orbital on each Nitrogen atom is non-bonding and occupied by lone pair of electrons. In ideal amorphous Si_3N_4 (a-Si_3N_4) although bonding distance and coordination are same as in c-Si_3N_4, but random distribution of bond angle occurs. In practice structural defects cannot be avoided in a-Si_3N_4. Due to such defects some broken bonds will exist which are called dangling bonds.

$$\equiv Si - \ddot{N} = \rightarrow \equiv Si \cdot + = \ddot{N} \cdot \tag{2.19}$$

$$2\left[\equiv Si - \ddot{N} =\right] \rightarrow \equiv Si - \left(N^+ - Si \equiv\right) = + = \ddot{N} :^- \tag{2.20}$$

Following the reported work on hydrogenated amorphous Silicon (a-Si:H), bonding and anti-bonding orbitals of Si-H and N-H are assumed to lie outside of gap i.e., not contributing to trap density. Accordingly, bond arrangement is considered as major source of gap state. The second equation can be rewritten as

$$2N_3 = N_4^+ + N_2^- \tag{2.21}$$

Here, N_3 is valance-bonded Nitrogen atom, N_4^+ is positively charged Nitrogen atom coordinated with four Si atoms and N_2^- is negatively charged nitrogen atom coordinated with two Si atoms. Now N_4 and N_2 can exhibit three charge states as occupied by none, one or two electrons. So, states are N_4^+, N_4^0, N_4^- and N_2^+, N_2^0, N_2^- for N_4 and N_2 respectively. Their calculation shows that N_4^+, N_4^0, N_4^-originates trap levels near conduction band edge, whereas N_2^+, N_2^0, N_2^- produces trap levels near valence band edge.

2.3.2 Model proposed by K. L. Ngai and Y. Hsia [68]

Kirk's model is based on the assumption that traps are originated from Nitrogen dangling bond. Ngai and Hsia also used negative U idea, but in their model traps are attributed to Si dangling bonds. In other work Ngai observed more shift in CV characteristic for an applied gate voltage in MOS device with (111) Si substrate compared to (100) Si substrate. For (111) substrate stress is more at interface leading to more number of Si dangling bond. So the result supports the assumption of Ngai and Hsia model, that Si dangling bond can be a source of trap level. They proposed traps in Nitride are amphoteric in nature, possessing either positive charged state with two holes (D^+) or negative charged state with two electrons (D^-) state. In energy scale the positively charged state D^+ lies above D_0 and near conduction band edge, whereas negatively charged state D^- lies below D_0 and near valance band edge.

If we consider memory application of MNOS structure, as they have used for their study, during writing electrons available at Si/SiO_2 interface move towards Nitride conduction band by tunneling through SiO_2. From conduction band electrons can be dropped to D^+ or D_0 state and converting them into D_0 and D^- state respectively.

$$D^+ + e \rightarrow D_0 \tag{2.22}$$

$$D_0 + e \rightarrow D^- \tag{2.23}$$

Opposite phenomena happen during erase operation. Electron released from D^- or D_0 state moves towards Si conduction band.

2.3.3 Model proposed by J. Robertson [69]

Contrary to the two models discussed above, J. Robertson argued that the dangling bonds in Si_3N_4 are expected to be positive U type. As Nitrogen is pnictide (Gr. 15 element in periodic table) and has $p\pi$ band, it is natural to expect dangling bonds to be negative U type. But dangling bond to be with negative U requires a $p\pi$ site to overcoordinate. But N has lower tendency to overcoordiate due to its small size. So, dangling bonds in Nitride are expected to be positive U type.

In that work, electronic energy spectra of dangling bonds, Si-Si, Si-H and N-H units have been calculated by recursion method. Local density of states (DOS) has been calculated by this method for regular and irregular clusters of atoms by expressing onsite Green's function as a continued fraction. DOS of N dangling bond, Si dangling bond, N-H, Si-H and Si-Si units were calculated.

Calculations were performed considering valence band edge at 0 eV. DOS of N dangling bond lies in the valance band at -2 eV. Si dangling bond is sp^3 hybridized producing state at 4.2 eV. The band gap of Si_3N_4 was obtained to be 4.3 eV. So, trap states generated from Si dangling bond lies

just below the conduction band minima. For N-H unit bonding (σ) and anti-bonding ($\sigma*$) state lies at -5.5 eV and 8.6 eV, which means N-H bond is not producing any trap level. So, according to the model, Hydrogen is an effective passivant for Nitrogen dangling bond. Si-H unit produces σ state at 0.5 eV and $\sigma*$ at 9.5 eV, i.e., not in the gap. So, this calculation indicates Hydrogen is not ideal passivant for Si dangling bond. σ state for Si-Si lies near mid-gap (at 3 eV) and $\sigma*$ state at 8 eV.

Robertson and Powel modified the calculation later by introducing self energy shifts in the Si center [74]. This work shows Si dangling bond produces deep trap level at 3.1 eV. They proposed that the $\equiv Si$ centers are responsible for long term charge trapping in Silicon Nitride.

2.3.4 Model proposed by D. T. Krick et al. [72]

Krick et al. performed electron spin resonance (ESR) and electrical measurements to determine the nature of traps in Silicon Nitride. In this case 550 nm Nitride was deposited on (111) Si substrate with 25 nm SiO_2 layer. Intermediate oxide layer is used to prevent unwanted charge injection in Nitride layer at moderate electric field. In this experiment the sample was first exposed to UV illumination which resulted in an increase in paramagnetic defect density and also annihilates previously trapped space charge in the Nitride layer. After that the device was first subjected to corona discharge under +ve and -ve bias. At each step CV measurement and ESR measurement were performed. Only paramagnetic bonds are detected in ESR measurement. CV measurements show the change in trapped charge density and ESR measurements show the change in paramagnetic density.

The g-value confirms that the Si dangling bonds are present in the Nitride layer. Strong correlation between change in density of paramagnetic dangling bond centers and space charge density indicates Si dangling bond is main source of traps in Nitride layer.

2.3.5 Model proposed by Y. Kamigaki et al. [67]

In this work Kamigaki et al. studied ESR result in more detail. Nitride, in MNOS structure, was deposited by LPCVD method at 760 °C using Dichlorosilane (SiH_2Cl_2) and Ammonia (NH_3) gas as the precursors. They found two ESR signals at g values of 2.005 and 2.002, which were attributed to $Si_3 \equiv Si^0$ (Si dangling bond with three neighboring Si atoms) and $N_3 \equiv Si$ (Si dangling bond with three neighboring N atoms) respectively. Increased partial pressure of Silane resulted in increase in the peak value of g at 2.005, which supports their assumption. But ESR result shows total spin density is only $2\times10^{17}\ cm^{-3}$, whereas programming window indicates 7×10^{18} cm^{-3} electron trap density and 1.2×10^{20} cm^{-3} hole trap density. This indicates that the majority of the traps are not paramagnetic, i.e. trap centers in Si dangling bonds are expected to be charged states where bond is either empty or filled with two electrons. They considered $Si_3 \equiv Si^+$ as electron trap centers and $N_3 \equiv Si^-$ as hole trap centers. They proposed in equilibrium three states are there at interface of Si cluster (A) $Si_3 \equiv Si{:}Si \equiv N_3$, weak covalent bond (B) $Si_3 \equiv Si^0$ and $N_3 \equiv Si^0$, relaxed bond and (C) $Si_3 \equiv Si^+$ and $N_3 \equiv Si^-$, split bond. Only group B can response to ESR measurement.

However, as from programming characteristic hole trap density is found to be more than electron trap density, some additional hole trap centers must be considered. They considered Nitrogen vacancy as source of additional hole traps. $N_3 \equiv Si : Si \equiv N_3$ acts as hole trap and capturing hole it becomes $N_3 \equiv Si^+$ and $N_3 \equiv Si^0$.

2.4 Silicon surface passivation using Al_2O_3

Crystalline Si solar cell is most important candidate in solar cell industry. There are several companies making close to 23% efficient cells. However they are not very successful commercially as the cost of the cells is quite high.

Different approaches have been implemented to increase the efficiency of crystalline Si solar cell. Among different limiting factors, surface recombination is a prominent drawback which results in reduced efficiency. The method of reduction of surface recombination is called surface passivation.

First it should be explained here, how passivation layer works in solar cell to increase efficiency by reducing surface recombination. Following Shockley–Read-Hall (SRH) recombination formalism, surface recombination rate $U_s(cm^{-2}second^{-1})$ can be expressed as [6]

$$U_s = \frac{(n_s p_s - n_i^2)\, v_{th} N_{it}}{\frac{n_s+n_1}{\sigma_p} + \frac{p_s+p_1}{\sigma_n}} = \frac{n_s p_s - n_i^2}{\frac{n_s+n_1}{S_p} + \frac{p_s+p_1}{S_n}} \approx \frac{n_s p_s}{\frac{n_s}{S_p} + \frac{p_s}{S_n}} \tag{2.24}$$

where, N_{it}: interface trap density (cm^{-2}), σ_n: electron capture capture cross section (cm^2), σ_p: hole capture capture cross section (cm^2), n_s: density of electrons (cm^{-3}), n_p: density of holes (cm^{-3}), v_{th}: thermal velocity of electrons (cm/s), n_1: electron concentration if trap energy level coincide with Fermi level (cm^{-3}), p_1: hole concentration if trap energy level coincide with Fermi level (cm^{-3}), n_i: intrinsic carrier concentration (cm^{-3}), $S_n = \sigma_n v_{th} N_{it}$ (cm/s) and $S_p = \sigma_p v_{th} N_{it}$ (cm/s).

The above equation shows, U_s is directly proportional to N_{it}. So, surface recombination can be decreased by decreasing interface state density. Another way to reduce recombination is by significant reduction of the density of one type of carrier. Since both a hole and an electron are required for recombination, U_s is reduced by this method. One method for achieving this is by applying an electric field to repel the carrier whose density has to be reduced. This type of passivation is called field effect passivation.

So, to reduce surface recombination research work is mainly directed to two ways. First one is to reduce interface state density at Silicon interface, which is called chemical passivation. Reduction in interface state density is mainly obtained by the passivation of Silicon dangling bonds with some dielectrics. Second is reduction in electron or hole concentration at interface by built-in electric field. The built-in-field can be obtained by choosing appropriate doping profile or by fixed charge at the Si interface.

In view of chemical passivation thermally grown SiO_2 is obviously the best candidate due to the low interface state density obtained [75]. But less amount of fixed charge in oxide layer results in reduced effective lifetime of carrier for SiO_2 layer [76]. Silicon Nitride (a-SiN_x :H/SiN_x) shows better field effect passivation compared to SiO_2 layer. The Silicon rich Nitride usually has higher content of Hydrogen. The chemical passivation is provided by Hydrogen. But as Nitrogen content is increased fixed positive charge density is also increased due to so-called k-center [77]. So, with higher Nitrogen content field effect passivation becomes dominant factor.

In modern solar cell technology, Al_2O_3 is considered as emerging material for passivation of c-Si surface, as it results in higher solar cell efficiency by decreasing surface recombination velocity significantly for surfaces of p type c-Si. Although passivation property of Al_2O_3 was reported in 1985 [78], but it has been mostly explored from 2005 when it was reported that Al_2O_3 deposited by ALD method shows excellent performance as passivation layer for both p-type and n-type c-Si [79, 80].

According to Lucovsky, presence of tetrahedrally coordinated Al in AlO_4^- unit and octahedrally coordinated Al in Al_3^+ unit in $3:1$ ratio results charge neutrality of Al_2O_3 film [81]. Kimoto et al. postulated that the presence of interfacial oxide layer results in higher population of tetrahedral coordination at interface. Tetrahedral coordination of Si in interfacial oxide film is responsible for that higher population. Therefore, interfacial oxide layer causes existence of significant amount of fixed negative charge in Al_2O_3 layer [82].

Also device goes through high temperature treatment during fabrication. Comparative study of SiO_2 and Al_2O_3 shows, firing significantly degrades effective lifetime for SiO_2 layer. For Al_2O_3 firing does not have such significant effect [76]. So, Al_2O_3 is more stable as passivation layer.

In case of solar cell it is obviously important to find response to illumination. Performance of SiO_2, SiN_x and Al_2O_3 as passivation layer under/after UV exposure is well reported. For both SiO_2 and SiN_x layer passivation is found to be degraded after UV illumination. In their work, P. E. Gruenbaum, R. A. Sinton, and R. M. Swanson have shown degradation of Si/SiO_2 interface after illumination. In that work, point contact solar cell was illuminated by concentrated sunlight at 56 W/cm^2. After illumination for various time period, efficiency was measured at 10 and 2 W/cm^2 [7].

T. Lauinger et al. observed same trend also for Silicon Nitride. Severe degradation in effective lifetime was observed specially for thinner Nitride film [8].

Opposite trend is observed for Al_2O_3 layer, where performance is improved after UV illumination. G. Dingemans et al. reported comparison of performance of Al_2O_3 and SiO_2 film as passivation layer under UV illumination [76]. They observed, effective lifetime is increased for Al_2O_3 and decreased for SiO_2 layer.

B. Liao et al. predicted that the main reason for such opposite effect is opposite polarity of fixed charge (positive for Al_2O_3 and negative for SiO_2 and SiN_x) [9]. As solar cell can't be avoided from exposure to illumination, the positive UV effect makes Al_2O_3 more acceptable in solar cell industry.

2.5 Summary of literature review

- Characterization of bulk trap levels, lying in wide band gap materials, is a challenging task. Techniques, based on opto-electrical measurements, seems to be better options as they are more direct and need simpler device structure. Among different opto-electrical techniques, "flat band voltage monitored trap-depopulation technique" is most efficient as it can retrieve maximum number of trap parameters [4, 5]. In the reported works, 10-15 nm thick semi-transparent metal layers (Al or Au) were used as gate electrode. But, to enhance efficiency of this technique and to make this technique appropriate also for shallow trap levels, semitransparent metal electrode should be replaced by a transparent electrode with high transmittance even in NIR region. Also, modification in methodology is required to ensure accuracy in calculation of trap density in a particular trap level.

- ITO is a frequently used transparent material in solar cells and opto-electronic devices. Reported works show, ITO films are mainly (222) and (400) oriented films. (400) oriented films are with higher carrier concentration and lower transmittance in NIR region [55]. So, (222) oriented films are required to obtain high transmittance in NIR region and (222) oriented films can only be obtained in presence of O_2 in sputtering ambient [55]. But presence of O_2 in sputtering ambient results in degradation of electrical property of the film and also decrease in transmittance in visible region [49]. So, our study was first focused on development of process conditions to produce (222) oriented ITO film in O_2 free sputtering ambient.

- Si_3N_4 is an important material in modern technology. Comparatively less works have been performed to retrieve information about energy position of trap levels, lying in nitride films. Different theoretical models proposed to explain trapping behavior, as discussed above, are conflicting. Kirk Jr. suggested that Nitrogen dangling bond is responsible for the trap levels in Nitride layer [70] whereas according to Ngai-Hsia model and Robertson's model Si dangling bond is responsible [68, 69]. Such contradiction highlights the need for experimental evidence. Krick. et al. performed ESR measurement and their result shows, Si dangling bonds are mainly responsible for presence trap levels in the Nitride films. But, Kamigaki et al. proposed that all bonds, originating trap levels, do not respond to the ESR measurement. The literature review indicates more work is needed on energy profilling of trap levels in the Nitride films.

- It is well reported that, UV illumination enhances the performance of Al_2O_3 films as passivation layer. During illumination photo-injection of electrons from Si substrate enhances the negative charge density in Al_2O_3 film. Very less works have been reported on nature and stability of these photo-injected charge carriers.

Chapter 3

Experimental Techniques

In this study, different experimental setup have been used for fabrication of the devices. Also different characterization techniques have been used to characterize deposited films or devices. Characterization techniques can be divided in two groups: physical characterization methods and electrical or opto-electrical characterization methods. Working principle of different fabrication and characterization techniques, used in this study, are discussed in this chapter [83, 84].

3.1 Device structure

The study is focused on the trap characterization of wide band gap materials. Dielectric is embedded in MIS structure.

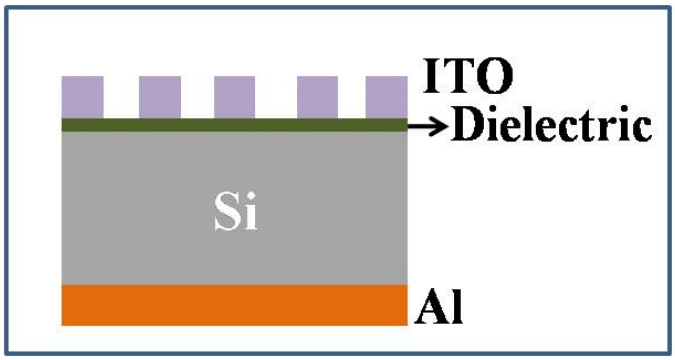

Figure 3.1: Schematic structure of device used in our study for trap characterization of dielectric films.

On RCA (abbreviation of Radio Corporation of America - where the process was first developed) cleaned Si wafer dielectrics (Si_3N_4 and Al_2O_3) were deposited using various deposition techniques (ALD, LPCVD and pulsed-DC sputtering). Films were annealed in different ambient conditions. After that, ITO film was deposited, using Si hard mask, by RF magnetron sputtering technique. Deposited ITO films were annealed in Ar ambient. At end, back side metalizations were

perfomed in thermal evaporation system. 100 nm thick Al was deposited at back of the device. The schematic structure of the device, used for dielectric characterization, is shown in Fig. 3.1.

3.2 Different fabrication techniques

3.2.1 Low pressure chemical vapor deposition technique

Low pressure chemical vapor deposition (LPCVD) technique is used widely to produce thin films. It is widely used to deposit Poly-Silicon, Silicon Dioxide and Silicon Nitride. Like other CVD processes, in LPCVD also gaseous species react with each other on or very near to a solid surface and produces solid phase material. Schematic diagram of the setup is shown in Fig. 3.2.

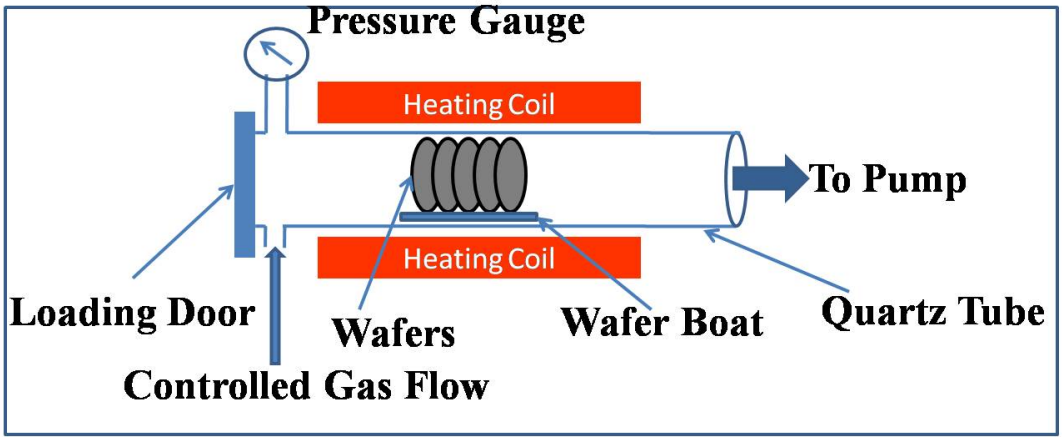

Figure 3.2: Schematic diagram of LPCVD setup.

In this technique, Si wafers are kept in a quartz tube. A spiral heater is placed around the quartz tube. There are three zones in the quartz tube: front zone, center zone and rear zone. The spiral heater actually covers the middle part of the quartz tube. The heater is designed in such a way that, the temperature of the center zone is definitely maintained at the desired temperature. After loading the sample into center zone, vacuum pump is switched on to create low pressure up to around 1×10^{-3} torr. Then, the tube is heated to the desired temperature. After attaining stabilized temperature, the gaseous species are allowed to flow into the chamber in a controlled manner. The gas flow rates are controlled using different flow meters. The process gas mixture consists of dilution gas and reactive gas. After deposition, temperature of the tube is slowly decreased to room temperature. After that, wafers are unloaded.

In our study, depositions of Silicon Nitride films were performed using Ultech LPCVD furnace. Nitrogen (N_2) was used as a dilution gas. Silane (SiH_4) and Ammonia (NH_3) were used as the reacting gases. The deposition was performed at 780 °C. At this process temperature, Si_3N_4 is deposited following the reaction

$$3\,SiH_4 + 4\,NH_3 \rightarrow Si_3N_4 + 12\,H_2 \tag{3.1}$$

To obtain uniform deposition, 10 dummy wafers were placed on each side of the main wafers, on which deposition was required.

3.2.2 Radio frequency sputtering system

To understand working principle of RF sputtering technique, first we need to discuss how basic DC sputtering system works. In DC sputtering system, sputtering is conducted in a closed system which is evacuated. After obtaining high vacuum level, heavy inert gas, e.g. Ar, is allowed to flow in the chamber in a controlled manner. Inside the chamber there are two electrodes as shown in Fig. 3.3. A high voltage is applied between two electrodes inside the chamber, to initiate electric discharge. Now the energetic emitted electrons hit Ar atoms and as a result Ar^+ ions are generated. As a result plasma is formed between cathode and anode. These Ar^+ ions are accelerated towards anode. The target i.e., the material which needs to be deposited, is placed on cathode. The accelerated Ar^+ ions hit the target which results in dislodgement and ejection of material in atomic or molecular scale and followed by deposition on the substrate, placed on anode. To increase efficiency a magnetic field is applied in parallel to the electric field. In presence of both electric and magnetic fields, electrons follow a spiral path. The increased path length results in more ionization.

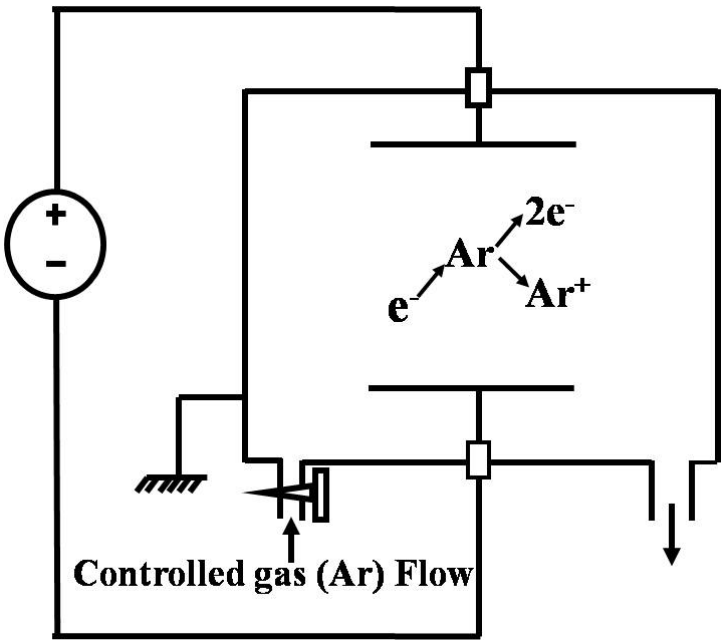

Figure 3.3: Schematic diagram of DC sputtering system.

Now fundamental problem with DC sputtering system is that, it cannot be used for non-conducting materials. If non-conducting target is placed on cathode then after hitting the Ar^+ ions will not be able to reach cathode electrode. Accumulation of Ar^+ ions on target material would actually stop

the further process. So, mainly for non-conducting materials RF sputtering technique was introduced. Schematic diagram of RF sputtering technique is shown in Fig. 3.4. In this technique in place of DC source, an alternating current (AC) power source is used. In one half cycle Ar^+ ions are accumulated on target and in next half cycle these ions move to another plate. As a result, the process is continued. In this case, actually in one half cycle current due to electron conduction occurs and in next half cycle current is obtained due to conduction of ions. Due to lower mobility, amplitude of ion current is obviously less than the electron current. A self bias method is used by introducing a capacitor to make total amount of charge equal in both the half cycles.

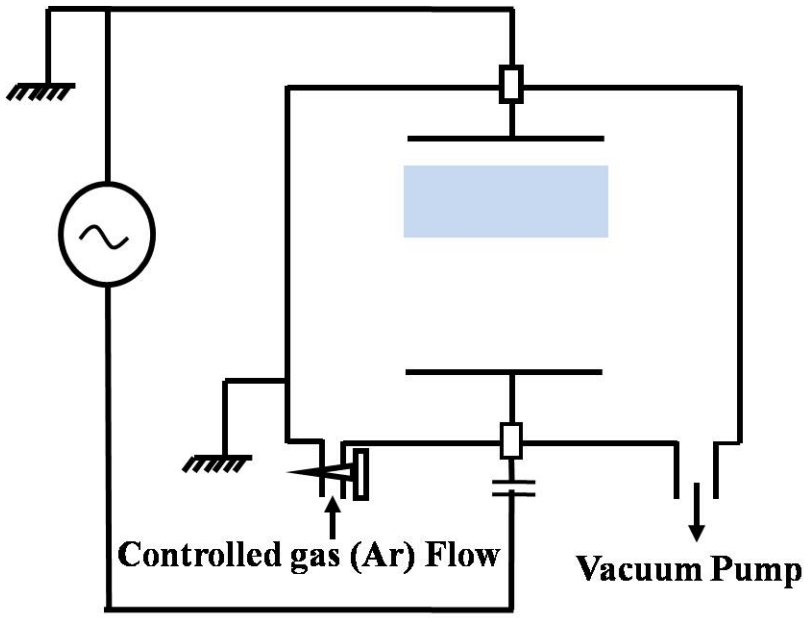

Figure 3.4: Schematic diagram of basic RF sputtering system with self bias configuration.

In our work, Nordiko RF sputtering system was used to deposit ITO films. A cryo pump is used to create vacuum level of 9×10^{-6} mbar. After that, vacuum valve is closed 80% and Ar gas is introduced in a controlled manner to maintain vacuum level at 2.6×10^{-3} mbar. After applying voltage between cathode and anode, vacuum valve is closed for few seconds. In that time Ar pressure goes high in the chamber and plasma is formed. After that, valve is again opened by 20%. A shutter is used in front of substrate. After 2-3 min of dummy deposition shutter is opened and deposition on substrate is started.

3.2.3 Pulsed-DC sputtering system

To avoid complexity in circuitry associated with RF sputtering technique, pulsed direct current (p-DC) sputtering technique was introduced. Pulsed DC power source actually provides DC with some chopping and interruption. So, normally it is in form of square or rectangular pulses. It is called mid-frequency because frequency used here is (~ 10-350 kHz) comparatively lower than

what is normally used in RF technique (13.56 MHz). Pulsed DC sputtering can be of different types depending on the shape of the applied pulse (Fig. 3.5).

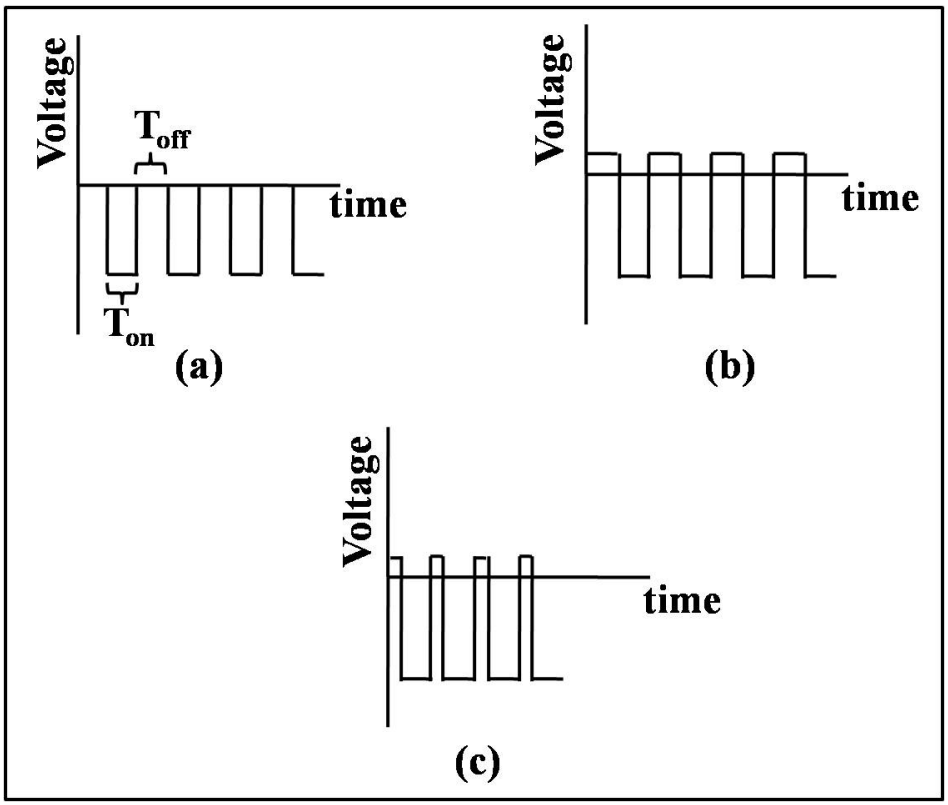

Figure 3.5: Voltage pulse for different types of pulsed-DC sputtering (a) unipolar pulsing (b) symmetric bipolar pulsing (c) assymetric bipolar pulsing.

(a) Unipolar Pulsing: In this case, voltage swings between 0 and some negative value with T_{on}=T_{off}. During Ton charge accumulation would be there. So, Ton should be chosen in such a way that, it would not lead to arc discharge.

(b) Symmetric Bipolar Pulsing: In this case, voltage level swings between small +ve value and large –ve voltage. In is ensured that charge accumulated in –ve cycle is totally neutralized by the +ve polarity.

(c) Asymmetric Bipolar Pulsing: In this case, T_{on} is not equal to T_{off}.

Endura Pulsed-DC sputtering system, made by Applied Materials, has been used in our study, for deposition of Al_2O_3 films. To obtain high quality film, chamber was first pumped down to 7×10^{-8} torr. Actual depositions were performed in Ar+O_2 ambient.

3.2.4 Thermal evaporation technique

Thermal evaporation is a physical vapor deposition technique. In this method, deposition is performed in a high vacuum chamber. An electric resistance heater (made of Tungsten) is used to evaporate a material, which needs to be deposited. Wafers are normally kept on a parabolic wafer

holder to get uniform deposition. At low pressure, the vapor cloud is originated. Low pressure also allows vapor particles to move directly to the substrate, the they are condensed back again in solid state. A crystal monitor can be used in the same plane of wafers, to monitor the thickness of the deposited film. Purity of the deposited film depends on the quality of vacuum and purity of the source material. The schematic diagram is shown in Fig. 3.6.

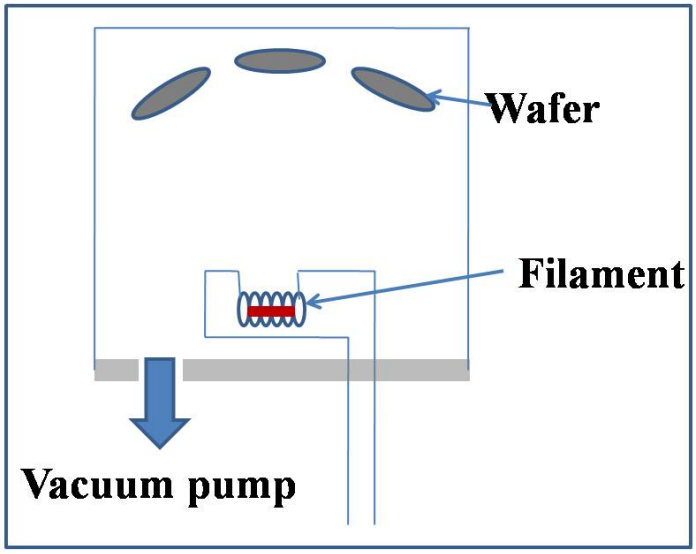

Figure 3.6: Schematic diagram of thermal evaporation system.

This system is restricted to low melting point materials. In our work, Al evaporations were performed using Hind Hivac thermal evaporation system. Depositions were performed at vacuum level of 4×10^{-6} mbar.

3.2.5 Annealing chamber

After deposition of the film, annealing is performed to improve the film quality. In annealing system, furnace is made of quartz. The quartz tube is wound by heating coils. First, user defines the set temperature in temperature controller. Temperature of the tube is increased slowly to the desired temperature. At high temperature, different atmospheric gases can react with the quartz tube. To avoid that, Nitrogen gas flow is maintained during heating of the quartz tube. Once the desired temperature is attained, Nitrogen flow rate is decreased slowly to zero and at the same time, flow rate of desired gas is increased. Flow meter is used to measure and control flow rate of the gas. After few minutes, required annealing ambient is established. After that, wafers are placed vertically on the quartz boat and the boat is placed at the loading end of the quartz tube. The boat is inserted into middle of the chamber, using a clean quartz rod. Then the loading end door is closed. After annealing, the boat is again taken out of the furnace slowly, using the quartz rod. After completion of annealing, again the annealing gas flow is slowly decreased to zero and simultaneously Nitrogen gas flow rate is slowly increased. Then the furnace is subjected to natural

cooling. After cooling of the furnace, Nitrogen flow is switched off. Fig. 3.7 shows schematic of the annealing chamber.

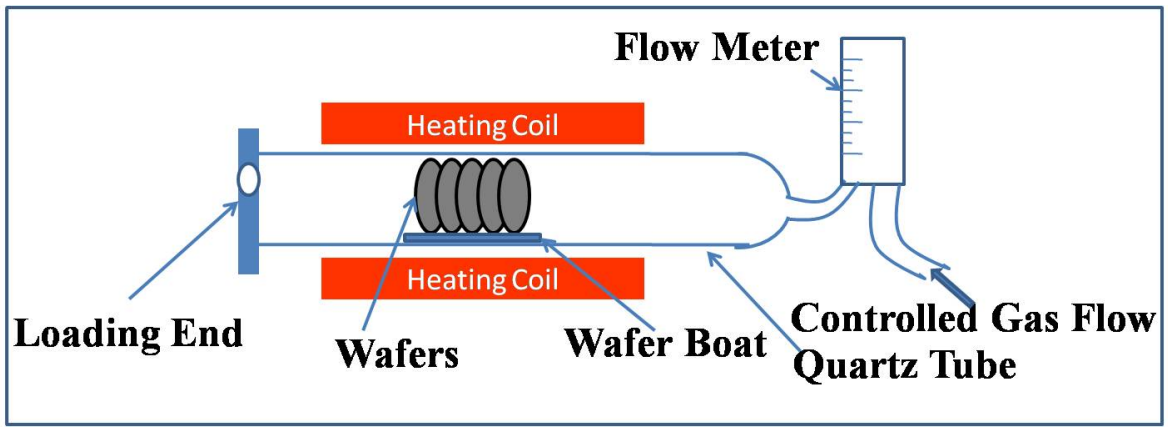

Figure 3.7: Schematic diagram of annealing chamber.

3.3 Different characterization techniques

3.3.1 Scanning electron microscopy

Scanning Electron Microscopy (SEM) is a physical characterization technique. Initially, light microscope was used for magnification. But the efficiency of a light microscope is limited by number and quality of the lens, as well as by wavelength of the light used. A modern optical microscope shows magnification 1000 X. Continuous decrease in device size demands instruments with higher resolution for better analysis of device structures and defects. Instruments with electron-based imaging can provide such high resolution. Very small electron wavelength (0.1 nm) is the secret of such high resolution. Scanning Electron Microscope is an instrument based on the principle of electron imaging. In SEM, a beam of electrons with energies typically 1-40 keV is used. The accelerated electrons with significant kinetic energy are incident on the sample. The energy is dissipated as a variety of signals consisting of secondary electrons, backscattered electron, and photons. Secondary electrons produce the SEM image. Back scattered electrons show contrast in the composition in multiphase samples. Up to 300,000 X magnification can be obtained in SEM. The schematic drawing of SEM system is shown in Fig. 3.8. Raith-150 Two, manufactured by Raith GmbH, was used in our work for SEM imaging of ITO films.

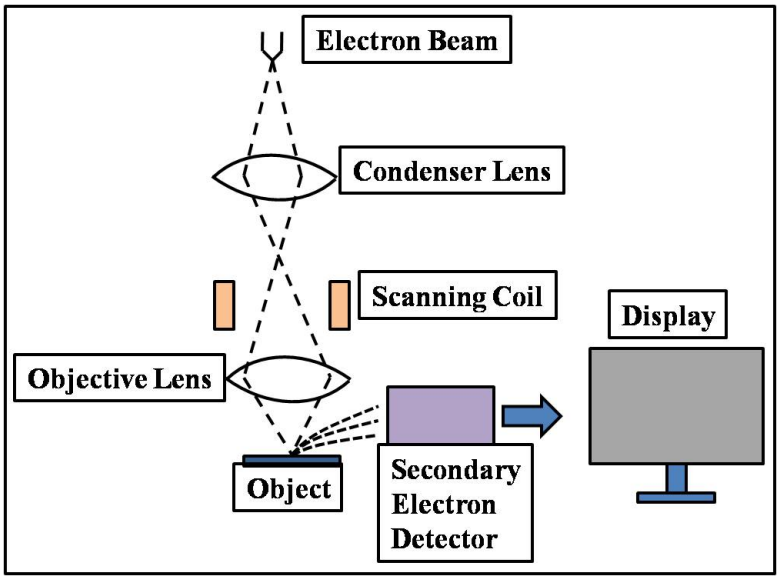

Figure 3.8: Schematic drawing of SEM system.

3.3.2 X-ray diffraction

X-ray diffraction (XRD), also known as X-ray crystallography, is a widely used technique to study the atomic and molecular structure of a crystal. Wavelength of X-ray is 0.1 nm, which is comparable to inter-atomic distance in crystalline materials. So, an array of atoms can create diffraction pattern of X-ray. In a crystal, atoms are arranged in a periodic manner as shown in Fig. 3.9.

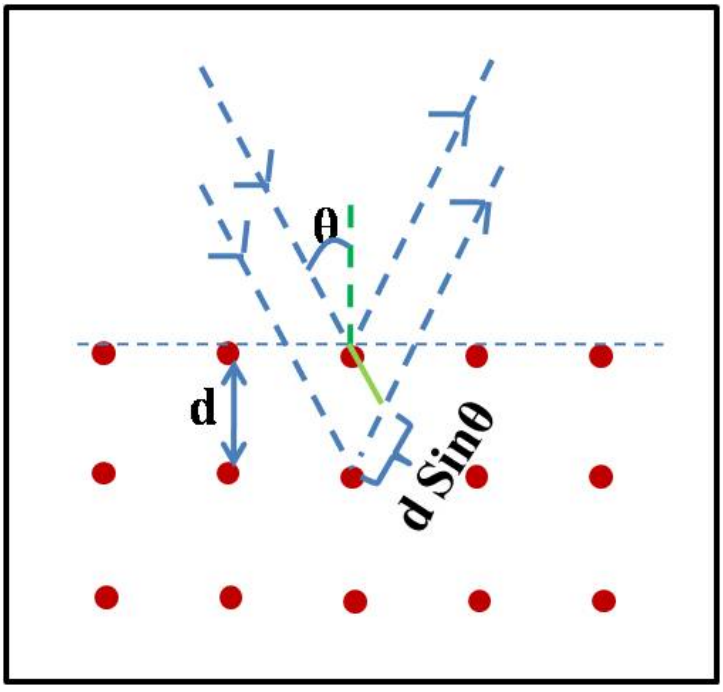

Figure 3.9: Pictorial description of working principle of XRD.

Now, consider two X-rays, parallel to each other makes an angle θ with the plane of the atoms.

After reflection, these two rays interfere constructively only when their path difference is an integer multiple of their wavelength. The equation is known as Bragg equation, after the name of the scientist who derived the formulae.

$$n\lambda = 2d\,Sin\theta \tag{3.2}$$

where, n is an integer, θ is the angle of incidence, λ is the wavelength and d is the inter-atomic distance. So, if θ and λ is known then inter-atomic distance can be calculated.

3.3.3 UV/Vis/NIR spectrometer

UV/Vis/NIR spectrometer is an instrument which measures the transmittance of a sample as a function wavelength, where wavelength varies from UV to NIR range. With specially designed sample holder, reflectance can also be measured by this instrument. The key components of a spectrometer are a light source, monochromator, detector and recorder. The suitable light sources are Deuterium lamp (160-375 nm), Tungsten lamp (800-2500 nm), Xenon arc lamp (190-800 nm) and Light-emitting diodes (LED) of lower and higher emission wavelengths. Fig. 3.10 shows schematic diagram of the spectrometer.

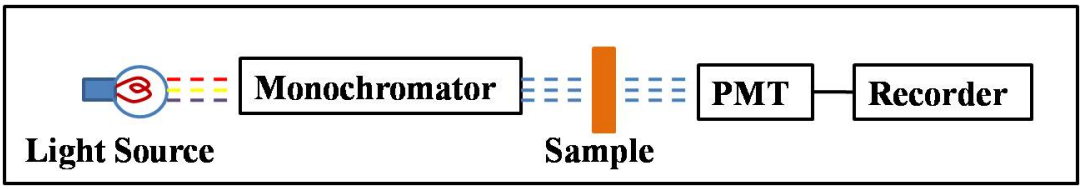

Figure 3.10: Schematic diagram of spectrometer.

The radiation emitted from the light source enters the monochromator through the entrance slit. The selected wavelength, of known intensity, is allowed to fall on the sample. The wavelength is changed step by step and the same process is repeated. If the sample is in liquid or powder form, it is kept in a quartz tube (as quartz is transparent in UV and visible region). Solid sample is kept vertically by a metallic sample holder. The light beam passed through the sample under study, is made to fall on the detector. Detector is an instrument which converts the optical signal into electrical signal. The intensities of respective transmitted beams are then compared over the whole wavelength range. In this study, we have used Perkin Elmer Lambda 750 UV/Vis/NIR spectrophotometer. The instrument consists of a dual source, Tungsten-Halogen and Deuterium lamps, providing a wide range of 190 nm to 3300 nm.

3.3.4 Optical capacitance-voltage measurement system

In Optical capacitance-voltage (optical-CV) measurement system, sample is placed in front of a light source of selected wavelength. The sample is kept vertically using a metal stand and Teflon

pin. A Tungsten probe is used to make front contact. A pressure contact is made between the back of the sample and metal stand, using the Teflon pin. Back contact is taken from the metal stand. Wavelength is changed step by step. A shutter is used in front of the light source. CV measurement is performed in dark condition. So, during CV measurement shutter is kept closed.

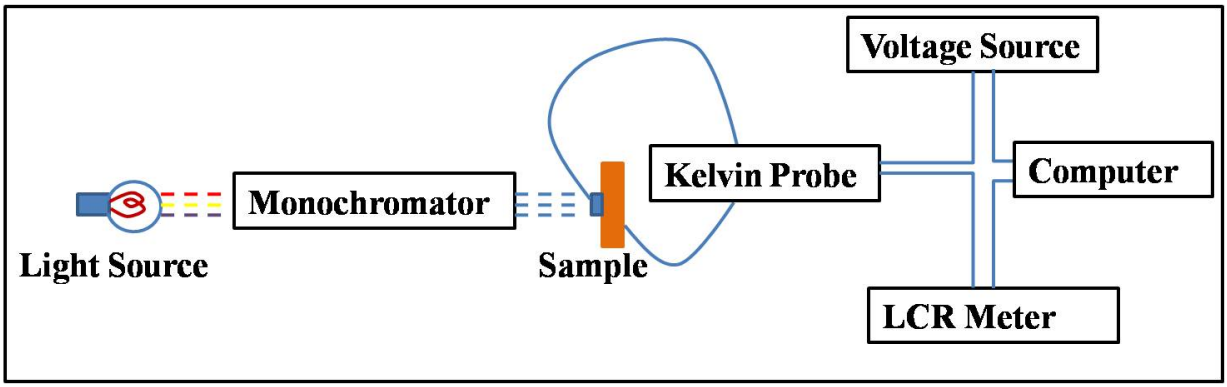

Figure 3.11: Block diagram of optical CV measurement system.

The block diagram of the setup is shown in Fig. 3.11. Device is connected to a voltage source and an LCR meter through Kelvin probe. The system is interfaced with a computer for data collection.

Chapter 4

Deposition and Optimization of ITO Films

Indium Tin Oxide (ITO) is an n-type semiconductor, which electrically behaves like a semi-metal but has a high optical transmittance. Now it is interesting to know the origin of high conductivity of ITO, although it has a band gap of approximately 4 eV. In ITO material, Tin (Sn) is tetravalent, whereas Indium (In) is trivalent. So, each Sn replacing In substitutionally, donates an electron for conductivity [53]. Oxygen vacancy is another source of electron in ITO film [51].

Due to such unique combination of electrical and optical properties, ITO has been widely used in different optoelectronic devices such as solar cells, optical coatings etc. High transmittance in infra red region can increase efficiency of dye-sensitized solar cell and IR emission devices.

As discussed in chapter 2, for "flat band voltage monitored trap-depopulation" technique duration of experiment is significantly higher due to less transmittance of metal gate electrode. In addition to that, as transmittance of metal layer falls rapidly beyond 600 nm (2 eV), trap levels lying within 2 eV from conduction or valance band edge cannot be distinguished with thin metal gate. In this chapter we would present our work focused on optimization of process parameters to produce highly conducting ITO film with high transmittance even up to larger wavelength range (~ 3000 nm).

4.1 Pre-processing of the ITO target

ITO target, made of 90% Indium Oxide (In_2O_3) and 10% Tin Oxide (SnO_2), has been used in this study. Thermal conductivity of ITO is not as good as metal. So, during deposition significant temperature gradient occurs between top and bottom surface of the ITO layer. Due to that, target can be cracked. To avoid this, in our work ITO target was first placed in circular Copper cap. In this study, ITO target of diameter 4" was used. So, a Copper cap with inner diameter slightly less than 4" was used. Back surface of ITO target was attached to Copper cap by Indium bonding. To perform the bonding, Copper cap was placed on a hot plate, heated at 200 °C. Small pieces of indium were spread on Copper cap and within few seconds Indium pieces were melted. Then ITO target was placed on Copper cap. Inner diameter of Copper cap was made same as outer diameter

of target. In heated condition, as diameter of Copper cap was increased, the target was inserted in the cap. After that, target with Copper cap was removed from the hot plate. To reduce pressure on the target due to shrinking of Copper cap (after cooling), four narrow cuts were made in the side wall of the Copper cap.

4.2 Experiment

Thin ITO films were deposited by RF sputtering method on 2.5 cm$\times$2.5 cm quartz sheet of 1 mm thickness. ITO was deposited in 99.999% Ar environment. The base pressure was 1.3×10^{-5} mbar in the vacuum system and working pressure was maintained at 2.6×10^{-3} mbar during deposition.

As discussed in section 2.2.2, work done by R. Bigyan et al. shows, the resistivity of the deposited films monotonically decrease with the increase in substrate temperature [52]. But, in that work substrate temperature was increased up to 200 °C only. It is also reported that at annealing temperature of 400 °C maximum rate of out-diffusion of O_2 is obtained, which results in minimum resistivity [47]. These two results indicate 400 °C can be optimum substrate temperature. Furthermore, before doing the actual experiments, to get an estimation films were deposited at 60 W and at three different substrate temperatures: 27 °C, 300 °C and 400 °C. Film deposited at 400 °C, was annealed in the sputtering chamber itself at 400 °C for 10 min in Ar ambient. The resistivity of the films was obtained to be 18000, 505 and 40 Ω/sq respectively. For the films deposited at 300 °C and 400 °C, thicknesses were measured to be 63 and 115 nm respectively. At a substrate temperature of 400 °C, reasonable resistivity was obtained. It should be mentioned that higher RF power can affect the quality of the dielectric, used in the actual device structure. So, actual study was mainly focused on the RF power of 40 W.

Deposition was performed at two different substrate temperatures, namely 120°C and 400°C. After deposition, samples were annealed for 20 min in Ar (99.999% purity) environment. Annealing temperature was varied from 400°C to 800 °C. Various process splits investigated are summarized in Table 4.1.

Table 4.1: Process splits, used in the experiment along with a summary of the key electrical and optical data.

Sample	RF Power (Watt)	Substrate Temp. (°C)	Annealing Temp. (°C)	Thickness (nm)	Sheet Resistance (Ω/sq.)	Resistivity ×10^{-4} Ω-cm	Average Transmittance (%)		Band Gap (eV)
							Visible (350 – 800 nm)	Vis-NIR (350 – 3300 nm)	
S1	40	400	NA	96	375	36.0	85.4	80.2	4.18
S2	40	400	400	100	187	18.0	85.1	83.7	3.96
S3	40	400	600	47	227	10.7	84.4	85.3	4.10
S4	40	400	800	115	797	91.7	87.4	82.3	3.98
S5	40	400	400	125	173	21.6	90.5	76.0	4.02
S6	60	120	NA	152	375	57.0	84.7	87.9	3.97
S7	60	120	600	104	260	27.0	84.5	85.5	4.02

The thicknesses of the films were measured by the profilometer. For this purpose steps were created, at the corner of the quartz sheets, using glass slide during deposition. So, measurements of thicknesses were not performed throughout the quartz sheet.

Sheet resistance of the films were measured by four probe method. Dektak XT profilometer, manufactured by Bruker Corporation, was used to measure the thickness of the deposited films. Perkin Elmer Lambda-750 spectrometer was used to measure the transmittance of the films. The spectrometer has dual source with two monochromators and can operate in the spectral range of 190 nm to 3300 nm.

The process conditions for different ITO films have been mentioned in Table 4.1.

4.3 Results and discussion

4.3.1 Grain size and crystal orientation

The discussion in section 2.2 shows, crystal orientation is the main deciding factor for transmittance in NIR region. Only (222) oriented film can produce high transmittance even in NIR region (beyond 1400 nm). The discussion also indicates resistivity of the film can be controlled by increasing grain

size and resultant decreasing grain boundaries. So, analysis of crystal orientation and grain size is important to optimize the process parameters. In our work, the methods used for estimating these properties are SEM and XRD.

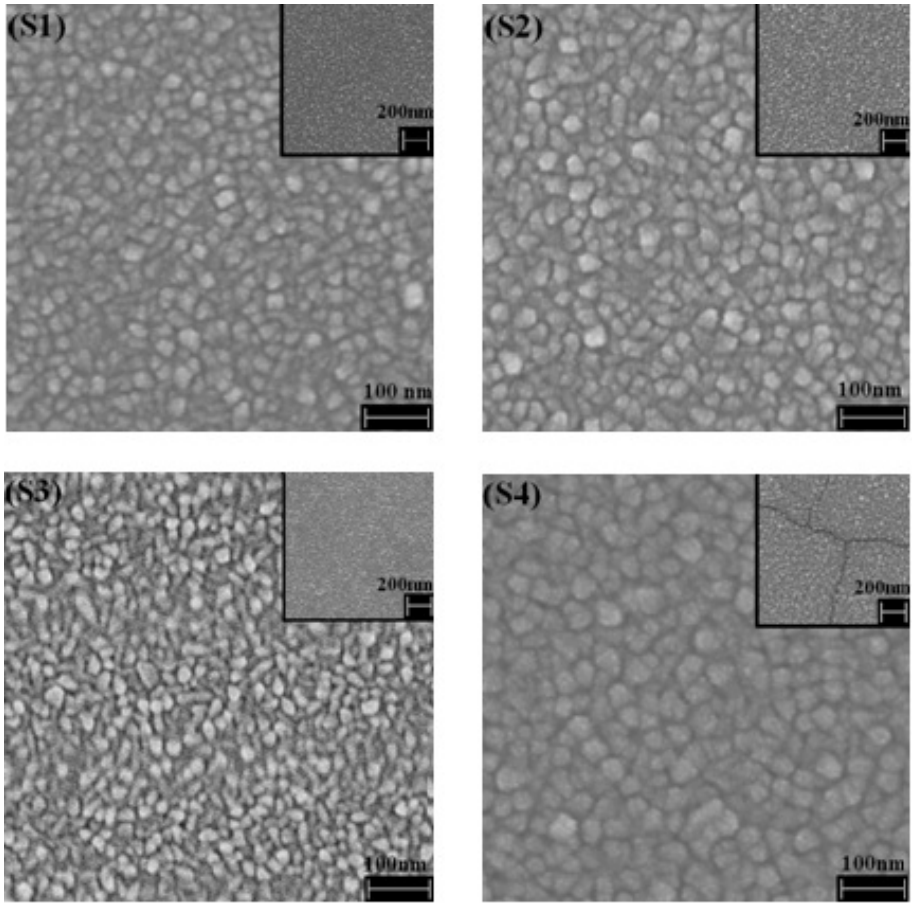

Figure 4.1: SEM images of ITO thin films; S1: substrate temperature 400 °C and no PDA, S2: substrate temperature 400 °C and annealing temperature 400 °C, S3: substrate temperature 400 °C and annealing temperature 600 °C, S4: substrate temperature 400 °C and annealing temperature 800 °C. Inset of S4 shows the cracks generated in the film during annealing process.

From S1 to S4 process conditions are same except annealing temperature. The result shows a decrease in resistivity as the annealing temperature is increased up to 600 °C. However the sheet resistance was higher for samples annealed at 800°C. The Scanning electron microscope (SEM) images of these samples are shown in Fig. 4.1.

Average grain sizes, measured by the linear intercept method (ASTM Standard E112), has been plotted in Fig. 4.4 as a function of annealing temperature. The result shows, grain size increases with the increase in annealing temperature. As grain size increases number of grain boundaries decreases, which results in better conductivity. SEM image in lower magnification shows cracks in sample annealed at 800 °C (inset of Fig. 4.1 (S4)). That might be the reason, why this sample shows higher resistivity despite having bigger grain size. These cracks are supposed to be generated due to different thermal expansion of ITO film and quartz. Fig. 4.2 (a) shows XRD pattern for all

the samples.

Comparison with JCPDS file shows that the film has cubic structure of In_2O_3 (JCPDS file: 06-0416) with a strong preferential orientation in (222) plane. Note that broad feature occurring at ~ 20° comes due to amorphous quartz substrate. Intensity of other peaks for (211), (400), (440), and (622) planes increases with the increase in film thickness. Full width at half maximum (FWHM) for the peak (222) was measured by profile fitting of pseudo-Voigt function using X'Pert HighScore software. FWHM as a function of anneal temperature is shown in Fig. 4.2 (b). The result suggests that the FWHM decreases i.e., crystalline quality of these films increases with the annealing temperature.

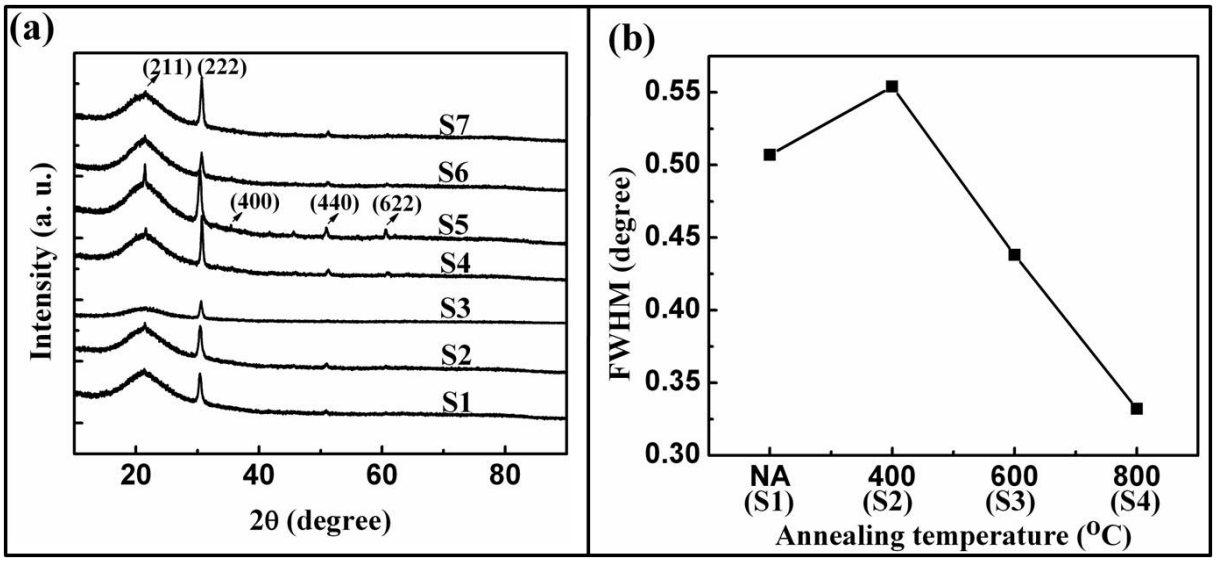

Figure 4.2: (a) X-ray diffraction pattern of various ITO thin films, (b) Variation of FWHM, for (222) peak, as a function of annealing temperature for the samples S1 to S4.

Fig. 4.3 shows the magnified (222) peak for S1 to S4.

Fig. 4.4 shows average grain size as a function of annealing temperature for these samples obtained from SEM as well as XRD. Both data sets show same trend in grain size with annealing temperature.

To understand the effect of substrate temperature on crystallinity more clearly, XRD measurements were taken for ITO thin films where, films are deposited at room temperature. After deposition one film was annealed at 400 °C for 20 min in Ar ambient (S9) and other was not annealed (S8) (not shown in Table 4.1). The XRD result is compared with the same of S1 and S2 in Fig. 4.5.

No characteristic peak is obtained for S8. Comparative study of XRD of S1 and S8 show, if PDA is not performed then characteristic peak or crystallinity can be obtained only if higher substrate temperature is used during deposition. XRD of S1:S2 and S8:S9 indicates, in presence of substrate temperature effect of annealing on crystallinity of the film decreases. Here one can also decide that absence of substrate temperature can be fully compensated by PDA. A careful observation of XRD graph for S1 and S9 indicates that (400) peak is more prominent (encircled

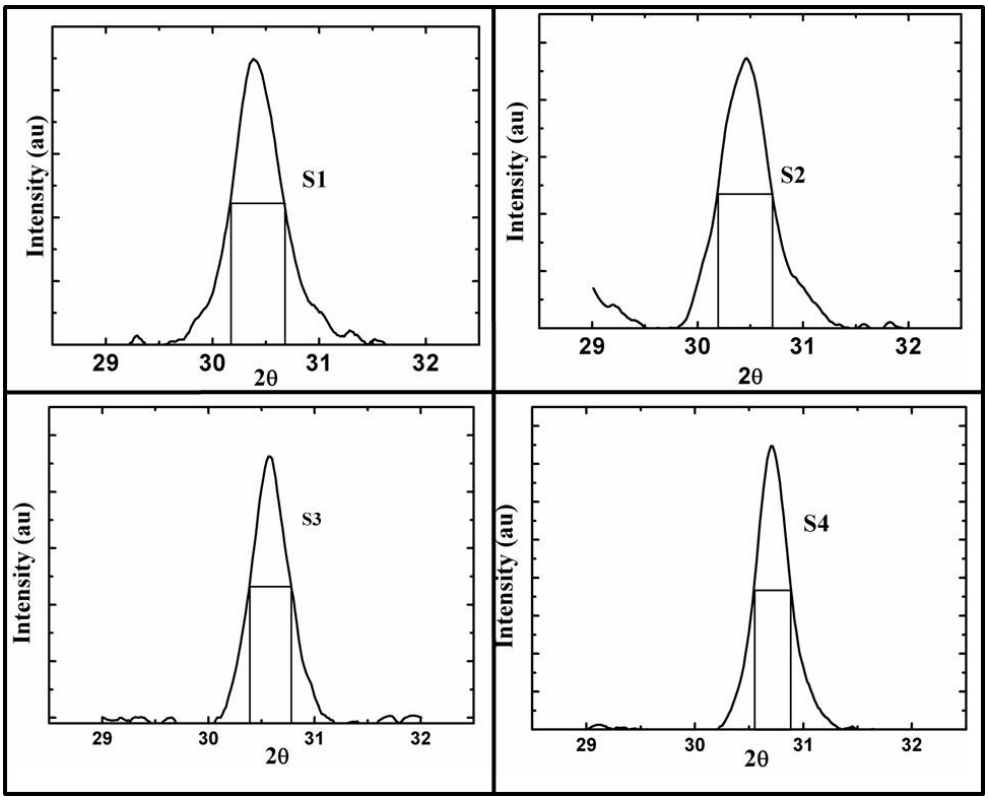

Figure 4.3: Magnified (222) peak and FWHM for S1, S2, S3 and S4.

in Fig. 4.5) for sample deposited at room temperature, although both are annealed at 400 °C. So, absence of substrate temperature cannot be fully replaced by PDA. In next section it will be shown that, even small signature of (400) peak affects transmittance significantly.

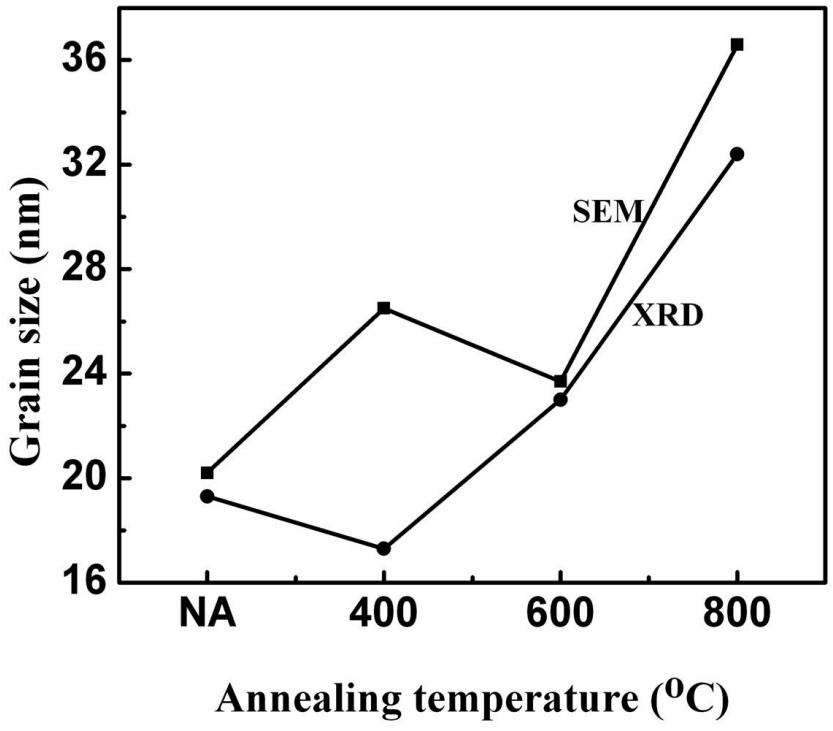

Figure 4.4: Grain size as a function of annealing temperature measured by SEM and XRD analysis.

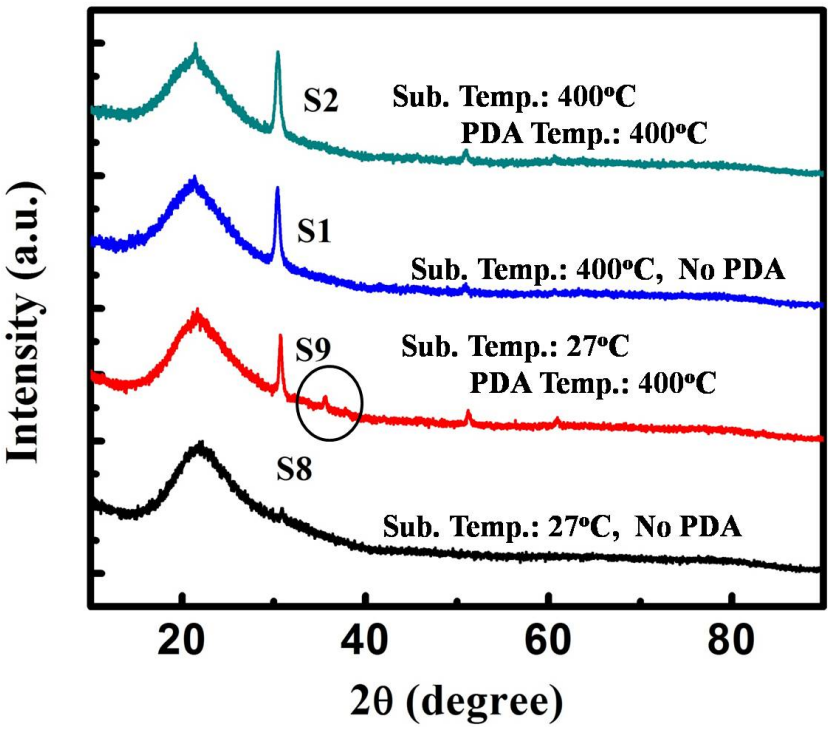

Figure 4.5: Impact of annealing on the crystallinity of the film. XRD pattern of the films grown with different substrate temperatures and post deposition anneal.

Kim et al. proposed that only presence of O_2 in sputtering ambient causes change in preferential orientation from (400) to (222) plane [55]. In a significant departure from the most of the reported

work on sputter deposited ITO, we have heated the samples during deposition. In this case even in 99.999% Ar ambient, (222) orientation has been obtained. Jung and Lee observed that the (400) peak intensity increases with the increase in film thickness [85]. In S5, where the thickness is 125 nm, a signature of (400) plane has been observed (Fig. 4.2 (a)), but far away from being a dominant peak.

4.3.2 Transmittance and optical band gap measurements

In this study, transmittance of the ITO film has been measured for the widest spectral range compared to previous studies. The results are presented in Fig. 4.6. For better understanding transmittance versus wavelength characteristics for all samples are splitted in two parts (Fig. 4.6 (a) and (b))

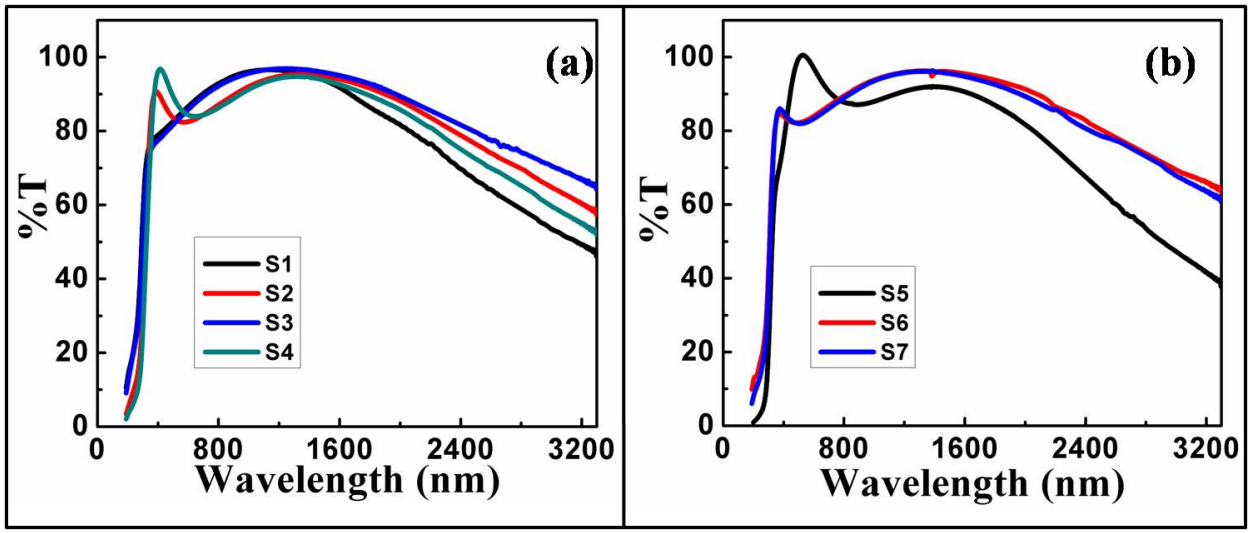

Figure 4.6: Transmittance as a function of wavelength for the samples (a) S1 to S4 (b) S5 to S7.

The transmittance is almost same for all samples, especially in visible region. Difference is observed in higher wavelength range. Transmittance of all sample, measured at 3000 nm is shown in Fig. 4.7. All samples show more than 80% transmittance up to 2000 nm.

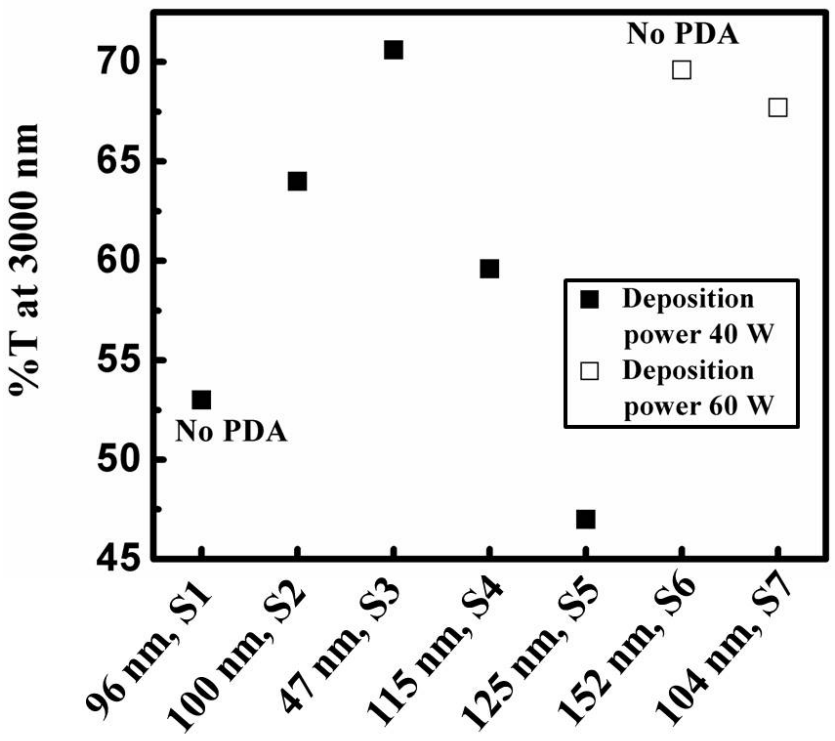

Figure 4.7: Transmittance for S1 to S7 at wavelength of 3000 nm.

Effect of Annealing

PDA was not performed for S1 and S6. Thickness of S1 and S2 is almost same. For both the samples, depositions were performed at substrate temperature 400 °C and RF power of 40 W. The only difference is that for S2 PDA, was performed at 400 °C. Transmittance at wavelength of 3000 nm is observed to be increased by 10% (from 53% to 63 %) after PDA. H. M. Ali et al. deposited ITO film of thickness 150 nm at room temperature and then the film was annealed at 400 °C [65]. Authors reported, at wavelength of 2500 nm, transmittance was increased by 50% (approximately from 25% to 75%) after annealing. Comparing the results with the reported literature, it can be remarked that effect of annealing on transmittance is not so significant for the films, deposited at elevated substrate temperature.

Comparison of S1:S2 and S6:S7 indicates, effect of annealing on transmittance is more significant for the films deposited at lower RF power. However, annealing substantially reduces the resistivity of the samples which is clear from Table 4.1.

Effect of Thickness and RF Power

Fig. 4.8 shows average transmittance (over the range of 350-3300 nm) versus resistivity and average transmittance versus sheet resistance characteristics. S4 (annealed at 800 °C) has not been considered in this plot, as it shows very high resistivity due to cracks. In order to study the effect of thickness on the optical and transport properties of the ITO film, two samples (S2 and S5) with

different thicknesses are deposited maintaining the same process conditions. XRD results show a signature of (400) plane for S5, which was not observed for S2 (Fig. 4.2 (a)). No significant improvement has been observed in the sheet resistance with the increase in thickness (Fig. 4.8 (b)). However the transmittance for S5 is clearly decreased specially for photon wavelength larger than 2000 nm (Fig. 4.6). Kim et al. reported that carrier concentration in the film increases with (400) orientation [55]. It is possible that decrease in transmittance for this case is arising due to increase in carrier concentration, but the fraction of (400) orientation is not high enough to reduce the resistivity significantly.

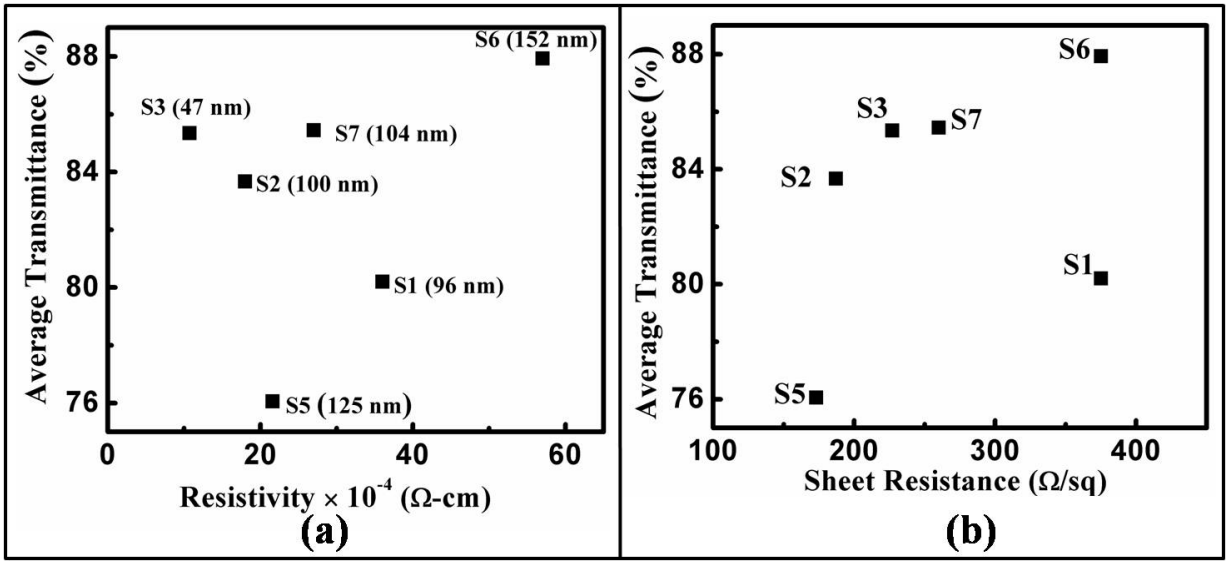

Figure 4.8: Average Transmittance (for the range of 350 - 3300 nm) versus (a) resistivity and (b) sheet resistance.

Previous studies show resistivity of the ITO film decreases with the increase in both substrate temperature [52] and RF power and reaches at minimum value at 40 W [48]. Comparison of resistivity between S1:S6 and S3:S7 shows good agreement with the reported result (Fig 4.8 (a)). S6 and S7 have almost same transmittance as S3, in both visible and NIR region, in spite of having higher thickness. So, ITO film optimized at higher power shows better optical property.

However, results shown in Fig. 4.8 (a) indicates, best combination of resistivity and transmittance has been obtained for S3, i.e., for sample deposited at substrate temperature 400 °C and annealed at 600 °C. Average transmittance of 83.3% and resistivity of 10^{-3} Ω-cm have been obtained the sample. Sample S2, deposited at substrate temperature 400 °C and annealed at 400 °C, also shows comparable result with S3.

Band Gap Measurements

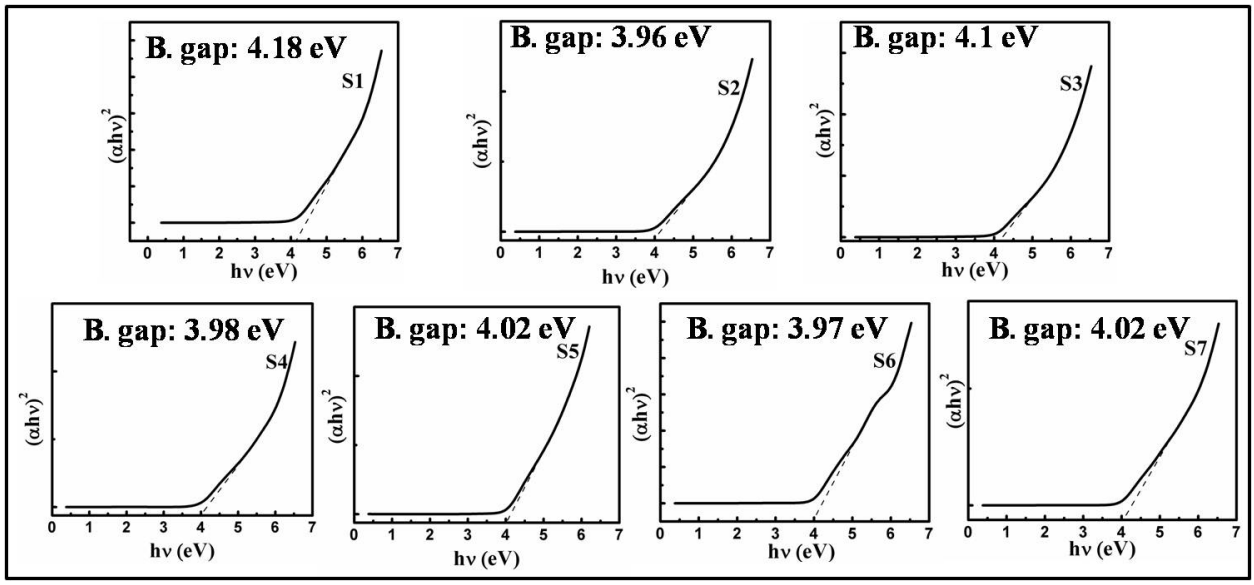

Figure 4.9: Tauc plot for S1 to S7.

Using the transmittance data at different wavelengths, band gap of the ITO film can be calculated from Tauc plot [56, 86]. Band gap for each film, calculated following the work done by H. R. Fallah et al., is in good agreement with the reported result [56]. The maximum difference in band gap is observed to be 0.22 eV, between S1 (3.96 eV) and S2 (4.18 eV). So, results indicate that there is no significant difference in band gap for different process conditions. Therefore, it can be concluded that, the change in resistivity is mainly caused by the change in grain size.

4.3.3 Comparison of results with reported literature

In this study, ITO has been deposited and optimized using RF sputtering technique. In this work transmittance for ITO films have been measured for 190-3300 nm range. No reported work is there for such wide spectral range. A comparative discussion of our results with best reported transmittance and resistivity values for ITO films has been presented here. In most of the literature reporting higher transmittance beyond 1400 nm, ITO films have been deposited using evaporation technique. So, the concern about film quality and uniformity associated with evaporation technique is always there.

Guillen and Herrero deposited ITO film at room temperature on a glass substrate by RF sputtering technique and best result was obtained for O_2 to Ar partial pressure of $P(O_2)/P(Ar)=0.004$ [60]. Annealing was not performed after deposition. Transmittance was measured in 400 to 1500 nm range. Result shows, 9 Ω/sq sheet resistance and an average transmittance of 85% for 400-800 nm range and 64% for 800-1500 nm range. Transmittance was observed to fall rapidly after 1400 nm and I(222)/I(400) was 0.71.

In the study performed by B. Zhang et al., the substrate temperature was varied from 0 to 400 °C and O_2 flow was varied from 0 to 1.5 sccm [61]. They observed that substrate temperature decreases the resistivity of the deposited film. Best transmittance was obtained for the film deposited at substrate temperature of 300 °C and 1.5 sccm flow rate of O_2. At 2500 nm transmittance reaches to 60%. Sheet resistance of 53 Ω/sq was obtained for the film . With a deviation from our result, their result shows (400) peak is being more significant with an increase in substrate temperature. They performed XRD measurements for the films deposited with O_2 flow rate 0.3 sccm.

M. D. Benoy et al. deposited ITO film by reactive evaporation technique [63]. Transmittance was measured for various film thicknesses varying from 80 to 350 nm and measurements were performed up to 2500 nm. The Best transmittance was observed for 80 nm thick film. 3.3×10^{-2} Ω-cm resistivity was obtained for the film.

M. M. Raheem et al. also deposited ITO using e-beam evaporation technique [64]. They used Glass/SiO_2/ITO structure for their study. SiO_2 films were deposited with substrate temperature varying from 200 to 400 °C. 200 nm thick ITO films were deposited in presence of O_2 and with different substrate temperatures (200 – 400 °C). No significant change in intensity of (400) peak for different substrate temperature was observed in XRD analysis. They obtained the best result for ITO films deposited at 325 °C substrate temperature on 80 nm thick SiO_2 buffer layer. 92% transmittance in the visible region and 83% in NIR region (up to 2500 nm) were observed for that film.

H. M. Ali et al., studied ITO film deposited by e-beam evaporation system [65]. After deposition at room temperature, ITO films were annealed at different temperature (200-400 °C) for different time (up to 120 min). Depositions were performed in an oxygen-free ambient. After annealing 150 nm thick film at 400 °C for 120 min, transmittance value of 82% in the visible region and 85.5% in NIR region (up to 2500 nm) and resistivity of 2.8×10^{-4} Ω-cm were obtained. To the best of our knowledge, this reported work displays best combination of optical and electrical properties of ITO film.

Table 4.2: Resistivity and average transmittance of ITO films.

Ref	Process parameters	Avg. %T (range)	Resistivity
[65]	E-beam evaporation; Sub. temp: 27 °C; Ann. temp: 400 °C Ann. time: 120 min	82% (vis. region); 85.5% (upto 2500 nm)	2.8×10^{-4} Ω-cm
Our work	RF sputtering; Sub. Temp: 400 °C Ann. temp: 600 °C Ann. time: 20 min	84.4% (350-800 nm); 91.7% (800-2500 nm) 85.5% (800-3300 nm)	10.7×10^{-4} Ω-cm

The best reported result and result of our study have been listed in Table. 4.2. Better optical property has been obtained in our experiment. Resistivity is little more than the reported work.

4.4 Conclusion

ITO films with different process conditions have been deposited by RF sputtered method in pure Ar environment. After deposition samples have been annealed in Ar environment. Substrate temperature during deposition results in (222) oriented film even in the absence of O_2. XRD result, for the film deposited at room temperature, shows prominent presence of (400) peak even after post deposition annealing. So, substrate temperature cannot be substituted by PDA.

Best electrical and optical property has been obtained for S3 with resistivity 10^{-3} Ω-cm and with average transmittance of 84.4%, 90.2% and 85.3% up to wavelength 800, 2500 and 3300 nm respectively. The result shows that annealing improves conductivity of the film significantly. Transmittance of the film has not been affected significantly by annealing. Transmittance of the ITO film, deposited at higher RF power shows better optical property.

Chapter 5

Establishment of Modified Trap Spectroscopy Technique and Characterization of Silicon Nitride Thin Films

Among different high-k materials studied for modern electronics, Silicon Nitride (Si_3N_4) is a prominent one due to its applications in different electronic devices like CMOS devices [87], flash memory [88], solar cells [89] etc. Silicon Nitride films are generally amorphous but, unlike other dielectric like SiO_2, contains many more chemical impurities such as bonded Hydrogen and Oxygen and sometimes have a slight Si-rich stoichiometry. Different models proposed to describe origin of trap levels in Si_3N_4 film has been discussed chapter 2. It has already been mentioned that, relatively less experimental works have been reported on energy position of trap levels in nitride film, specially for trap levels lying below mid-gap. In this work, we explore the trap levels lying near the valence band edge.

5.1 Study of the Silicon Nitride thin films deposited in various process conditions

In this study Silicon Nitride films have been deposited by LPCVD technique. Ultech furnace has been used to deposit Silicon Nitride films. Properties of the film depend on the process conditions. Silane and Ammonia were used as reacting gas gas, whereas, N_2 was used as diluent gas. Depositions were performed at temperature 780 °C. Films were deposited with different NH_3 flow rate and all other process parameters were kept constant. Thickness and refractive index (RI) of the film films were measured using ellipsometer. My group member, Mr. Satya Suresh has significantly contributed to the development of the nitride deposition process. The result is listed in Table 5.1.

Table 5.1: Deposition parameters and measured thickness and RI of the Nitride films.

Sample	SiH_4 (sccm)	NH_3 (sccm)	N_2 (sccm)	Deposition time (s)	Thickness (nm)	RI
1	45	40	1000	1500	18	1.98
2	45	60	1000	4200	42	1.89
3	45	200	1000	4200	32	1.8

The Deposition rate as a function of NH_3 flow rate is shown in Fig. 5.1.

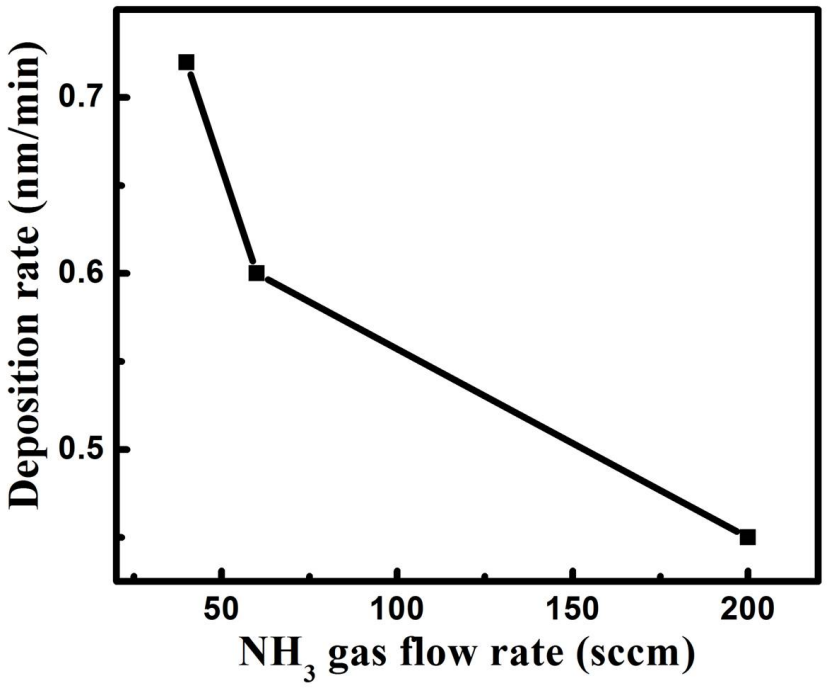

Figure 5.1: Influence of NH_3 flow rate on deposition rate.

Increase in partial pressure of NH_3 results in decrease in deposition rate. As NH_3 flow rate is increased, relative density of Si radicals is decreased. So, deposition rate is decreased. RI of the deposited film is also affected by the flow rate. RI versus Ammonia flow rate is shown in Fig. 5.2.

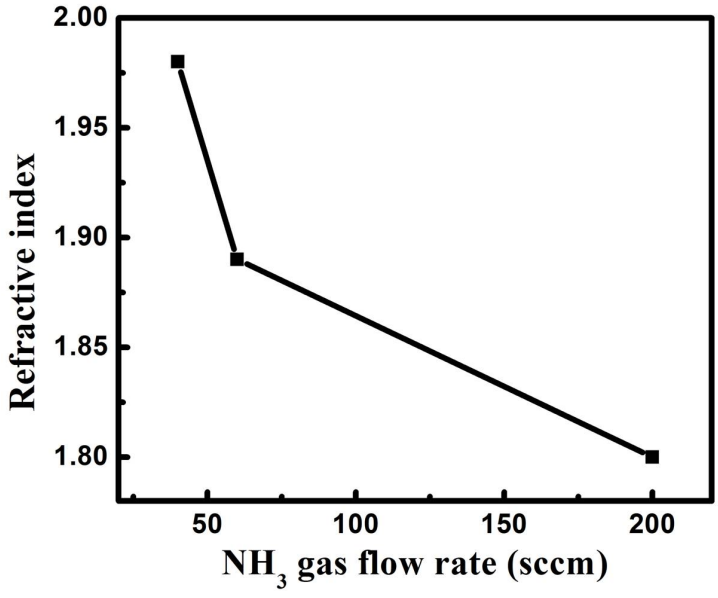

Figure 5.2: Influence of NH_3 flow rate on refractive index.

The result indicates, RI of the deposited films decreases with the increase in Ammonia flow rate. Film with less RI refers to Nitrogen rich nitride film. In this process Silane is the source of Si atoms. So, decrease in partial pressure of Silane results in Nitrogen rich Si_3N_4 film.

5.2 Trap characterization of Silicon Nitride film by modified trap spectroscopy technique

As discussed in Chapter 2, there is prominent existence of both electron and hole traps in Silicon Nitride. As mentioned earlier, aim of our work is to characterize bulk trap levels lying in Nitride layer. In chapter 2, a comparative study of different trap characterization techniques has been discussed. Several methods, such as TSEE [2], charge pumping [11], discharge current transient spectroscopy [90] etc., have been employed to determine the energy position and density of traps in Si_3N_4 thin films embedded in different structures. However, these techniques have certain limitations. TSEE needs complex experimental setup and analysis. Furthermore, this technique is not a very efficient trap detection method for wide band gap materials (like SiO_2, Si_3N_4 etc.). In order to detect the deep trap states in these materials TSEE relies on Auger recombination processes, which is less probable when the trap concentration is not sufficiently high. Charge pumping method is a costly technique, as it requires sophisticated transistor level fabrication. Discharging current transient spectroscopy technique is applicable only for shallow (up to ~ 1 eV) traps [90]. Compared to the above techniques, flat band voltage monitored trap-depopulation technique [3, 4] is a more direct method and require only a simple device structure. Bibyk and Kapoor [4] embedded 110 nm thick Si_3N_4 layer in a Metal-Nitride-Oxide-Semiconductor (MNOS) structure for their experiment. Traps in the dielectric were first filled by internal photo-emission [4] and then the device was

illuminated by photons of different energy to detrap the electrons.

But in these reports, the photon energy was scanned even above the mid-gap to obtain information about the trap levels lying below the mid-gap. However, for excitation with photon energy larger than $E_G/2$, where E_G is the band gap of the material, there is a probability of transfer of an electron from valence band to that trap level or some other empty state, leading to erroneous result for the calculated trap density. Modification has been introduced in the methodology, as discussed in section 5.2.1.

Furthermore, for photo-CV and photo-IV measurements, gate electrode needs to be transparent to enable photons to enter in the dielectric or semiconductor layer. In most of the reported literature thin semi-transparent Al or Au layer (~ 10-15 nm) has been used as gate electrode [3–5, 91]. However, the transmittance of metal layers of this thickness decreases substantially in the near infrared region [30, 31]. Therefore, metal gate is not a very good option for characterizing shallow traps. Moreover, it has to be noted that for such a thin metal layer, annealing cannot be performed after metalization, as the metal film might breakup into nanocrystals [92]. Furthermore, low transmission coefficient of metal layer demands the illumination to be carried out for extended duration (60 min or more) [3, 4]. Instead, if a transparent conducting layer like Indium Tin Oxide (ITO) is used as gate electrode, the transmittance will be much higher for a wider range of wavelength (including NIR region), as shown in chapter 4, enabling the characterization of even shallow traps with higher detrapping efficiency resulting in shorter measurement time. Here, we have used an 80 nm thick layer of ITO with transmittance of more than 80% instead of a thin metal layer as gate electrode, in our ITO/Si_3N_4/Si MOSCap structure.

5.2.1 Proposed theory

For opto-electrical measurement gate electrode needs to be transparent to allow light to the dielectric. In this work ITO has been used as gate electrode. With a departure from previous work, here two different methodologies are followed for trap levels lying from conduction band edge to mid-gap and from mid-gap to valence band edge of the dielectric.

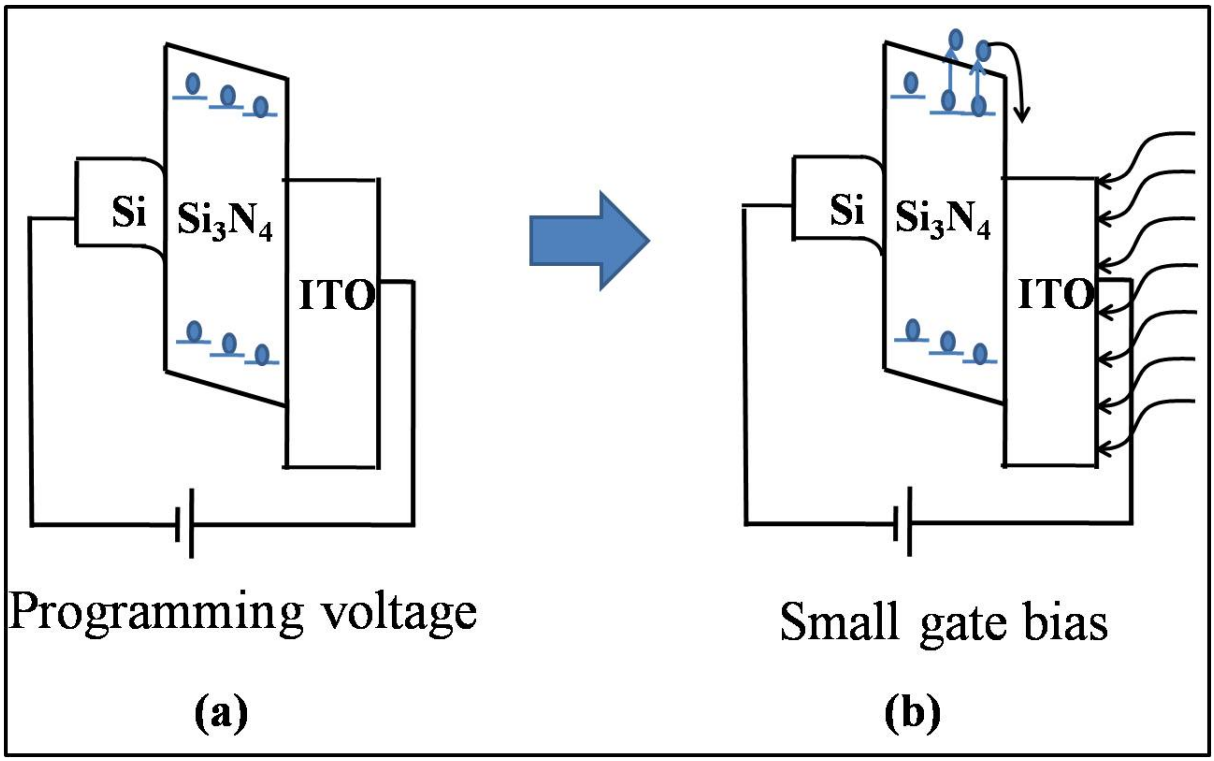

Figure 5.3: Pictorial description of the methodology for characterization of trap levels lying above mid-gap: (a) after programming of the device by +ve voltage all trap levels are filled by electrons, (b) detrapping of electrons from the trap levels, as a result of illumination of the device by appropriate photon energy.

First consider the characterization of the trap levels lying in upper half of the band gap. The device is initially programmed by a high positive gate bias. Bias should be sufficiently low so that it would not contribute to leakage current through dielectric. CV measurement is taken before and after programming to calculate the programming window. Here, we can consider after programming all trap levels in the dielectric are filled by electrons, as shown in Fig. 5.3 (a). Now the device is excited by a specific lower photon energy under small positive gate bias. Then the excitation energy is increased step by step. After each excitation CV measurement is taken. Now, when excitation energy matches with the energy depth of the trap level from conduction band edge, trapped electrons would be excited to the conduction band and flow towards conduction band of ITO, as shown in Fig. 5.3 (b). So, released electron would result in leftward shift in CV. To obtain accuracy the device should be illuminated for sufficient time so that all trapped electrons at that level are detrapped. Otherwise partially filled level can respond to higher excitation energy and lead to erroneous trap density calculation. Note that, as traps below mid-gap are already filled with electrons, during excitation no electron can be excited from valence band to be captured by a trap level. So, trap levels lying below mid-gap would not participate in the detrapping process. The excitation energy should be increased with small step (say, 0.1 eV) up to $E_G/2$.

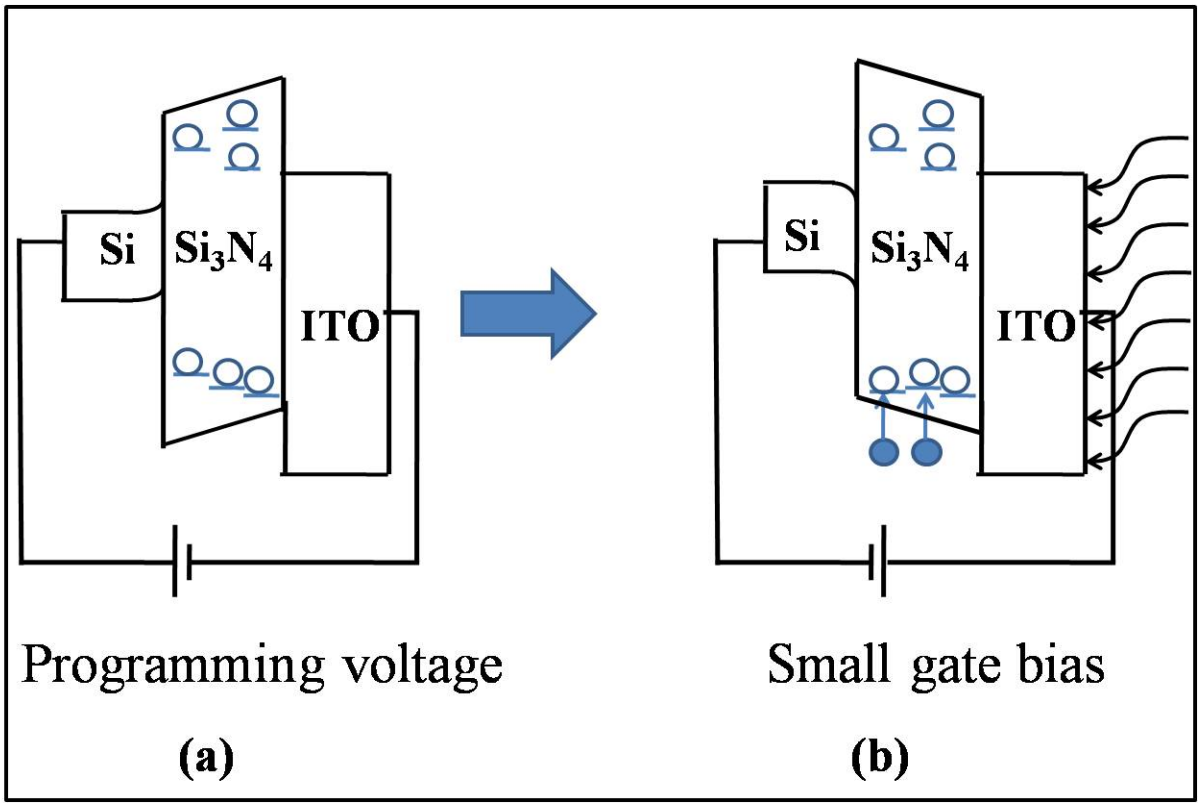

Figure 5.4: Pictorial description of the methodology for characterization of trap levels lying below mid-gap: (a) after programming of the device by -ve gate voltage all trap levels are filled by holes, (b) detrapping of holes from the trap levels, as a result of illumination of the device by appropriate photon energy.

Consider the case of characterization of trap levels lying below mid-gap. For this purpose device is first electrically programmed by negative programming voltage. So, in this case all the trap levels lying in dielectric would be filled by holes, as described in Fig. 5.4 (a). After that, device is again excited by specific photon energy under small positive gate bias. In this case when excitation energy would be equal to trap depth with respect to valence band edge, the electron from valence band will be excited and recombine with the trapped hole, or in other words trapped holes would be excited and released to the dielectric valence band (Fig. 5.4 (b)). Due to applied bias, released hole would flow towards the valence band of Si.

5.3 Experiments

5.3.1 Sample preparation

P-type Si wafer of (100) orientation and resistivity of 4-7 Ω-cm was cleaned using RCA cleaning procedure and was used as the substrate for device fabrication. 22 nm thick Silicon Nitride layer was deposited on this substrate by LPCVD process at 780 °C using SiH_4 and NH_3 as precursors. SE 800 ellipsometer, manufactured by Sentech Instruments, was used for measurement of deposited

film thickness and refractive index (RI). RI of 2.02 was measured for the Nitride film using a spectroscopic ellipsometer. 80 nm thick ITO dots of 1 mm diameter were deposited by RF sputtering through a hard mask. ITO was deposited at 40 W with a substrate temperature of 400 °C. The device was then annealed in Ar environment at 400 °C for 20 min. Backside Al metalization was done by thermal evaporation. ITO layers used in this work were found to show an average transmittance of 84% for the wavelength range of 360 nm to 3300 nm.

5.3.2 Measurement setup for trap spectroscopy

The schematic diagram of the measurement setup is shown in Fig. 5.5. The measurement setup consists of an aluminum stand to place the sample in front of a broadband light source. The sample was placed vertically, on the stand, by a Teflon pin. Since the backside is coated with Al, the pressure generated by the Teflon pin will be enough to provide a good electrical contact at back of the wafer. The front contact of the device was made by tungsten probe. The same voltage source was used for electrical stressing of the device, CV measurements and to provide positive bias to the sample during illumination. CV measurements reported below were carried out at a signal frequency of 10 kHz. The CV setup was interfaced with a computer for data collection. The light source in Perkin Elmer Lambda-750 spectrometer was used for illuminating the device. Excitation wavelength was scanned from 3100 nm to 756 nm corresponding to energy range of 0.4 eV to 1.65 eV.

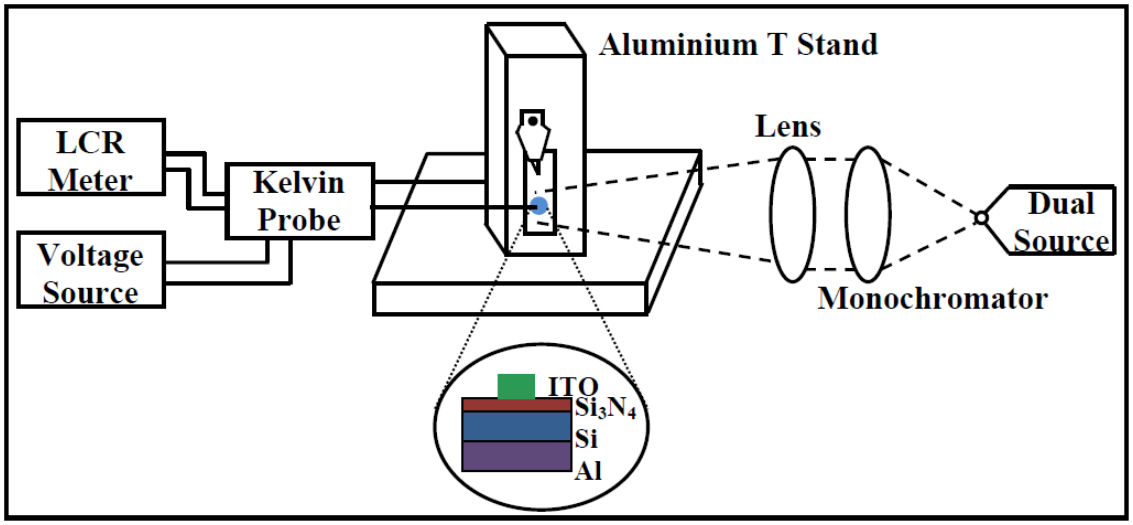

Figure 5.5: Pictorial depiction of the measurement set up. The inset shows the cross sectional schematic of the MOS device used.

5.4 Results and discussion

5.4.1 Comparison of performance of ITO with other standard gate electrode

In this study ITO has been used to retrieve different properties of bulk traps, lying in Si_3N_4 layer. It is noteworthy that, ITO has not been widely used as gate electrode in reported literature. So, prior to the actual trap characterization experiments, it is important to examine whether the electrical characteristics of the Nitride layer is influenced by ITO deposition or not. This examination process involves comparison of performance of ITO with Al and ITO/TiN gate electrode, as Al gate is very widely used as a gate dielectric in MOS devices for fundamental studies and also Titanium Nitride (TiN) is commonly utilized as a diffusion barrier [93].

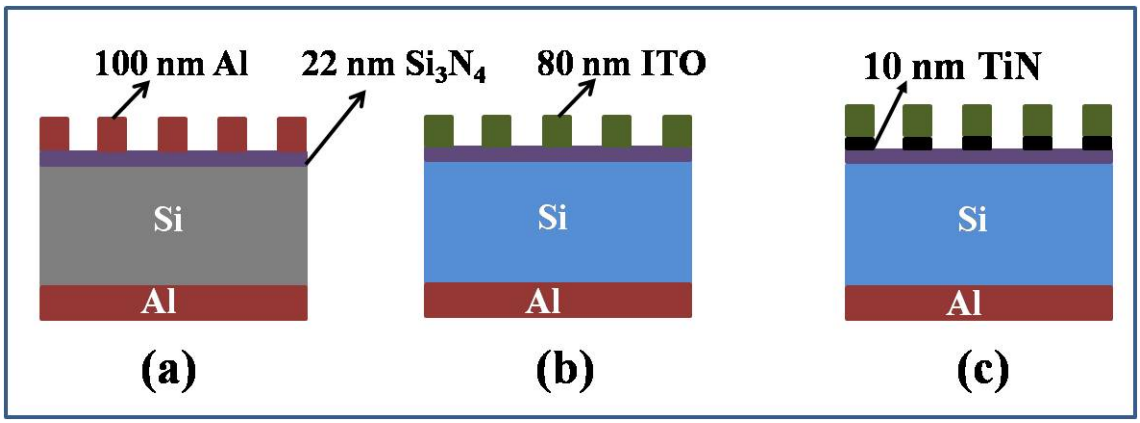

Figure 5.6: Schematic diagram of the devices with (a) Al (b) ITO and (c) ITO/TiN gate electrode.

First Metal-Nitride-Semiconductor (MNS) capacitors were fabricated with Al (100 nm), ITO (100 nm), ITO(80 nm)/TiN(10 nm) gate electrodes. 100 nm Al layer was deposited on the Nitride layer by thermal evaporation system. In the later case TiN was deposited by DC sputtering technique on top of the Nitride layer prior to the ITO deposition. TiN was deposited by reactive sputtering at 350 W with Ar:N_2=20 sccm:20sccm. ITO was deposited with same process conditions as decribed in section 5.3.1. The schematic diagrams of three device structures are shown in Fig. 5.6.

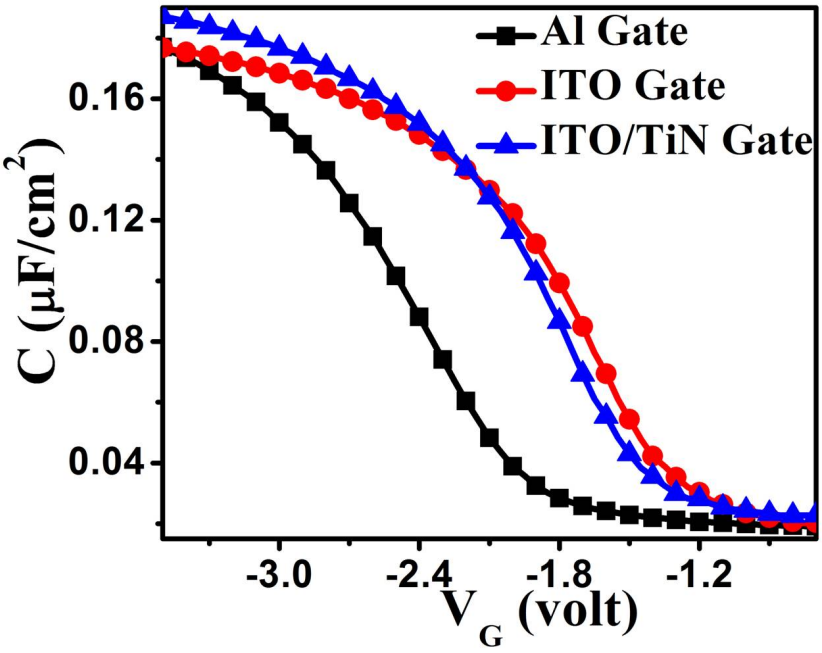

Figure 5.7: CV characteristics for devices with Al, ITO and ITO/TiN gate electrode.

Comparisons of CV characteristics for three different gates are shown in Fig. 5.7. A slight fluctuation of the C_{max} ($\triangle C_{max}$~0.01 μF/cm^2) value is well within the error bar associated with the estimation of the device area. Work function of Al, TiN and ITO have been considered as 4.1 eV, 4.6 eV [94] and 4.5 eV [95] respectively. The difference in V_{FB} for CVs (~ 0.57 V) with Al and ITO/TiN gate is almost equal to the work function difference between Al and TiN (~0.5 eV). D_{it} and Q_{ox} were calculated by HFCV technique i.e., using the shift in V_{FB} and V_{MG}. Calculated D_{it} and Q_{ox} are listed in Table 5.2.

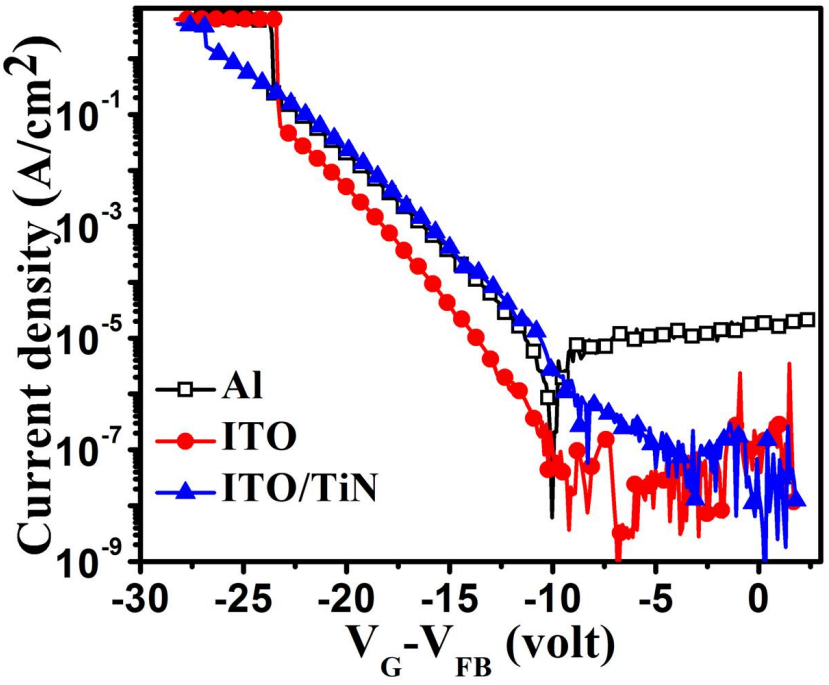

Figure 5.8: IV characteristics for Silicon Nitride thin film with Al, ITO/TiN, ITO as gate electrode.

Fig. 5.8 shows IV characteristics of the devices with three gate electrodes. Leakage current has been improved significantly for ITO gate with respect to Al gate, whereas no difference is seen between the ITO/TiN and ITO gates. The breakdown voltages, calculated from IV characteristics, are listed in Table 5.2.

Table 5.2: Parameters representing the electrical properties of Si_3N_4 for different gate dielectrics.

Gate Material	Al	ITO	TiN/ITO
Breakdown field (MV/cm)	7.8	7.7	8.9
D_{it} ($cm^{-2}eV^{-1}$)	2×10^{11}	3.9×10^{11}	1.1×10^{11}
Q_{ox} (cm^{-2})	1.5×10^{12}	1.2×10^{12}	1.4×10^{12}

The result shows, interface state densities and fixed oxide charge densities, as obtained from CV measurements, were found to be quite comparable between ITO, ITO/TiN and Al gates. Breakdown fields of the Nitride were measured to be 7.7 MV/cm, 8.9 MV/cm and 7.8 MV/cm with ITO, ITO/TiN and Al as gate electrodes, respectively. So, breakdown voltages are comparable for all cases.

From these results it can be concluded that the ITO, ITO/TiN and Al gates are comparable in terms of their influence on the Nitride.

5.4.2 Trap spectroscopy results

Fig. 5.9 shows the CV characteristic obtained for the ITO/Si_3N_4/Si MOSCap device structure under different conditions. The device was first programmed electrically by applying a gate bias of -15

V for 1 s, which resulted in a negative shift of the CV characteristic, evidencing hole trapping in the dielectric layer. It was observed that after programming, the CV characteristics moved slowly towards its pre-stress state even at room temperature, which might be due to detrapping from shallow states. Eventually, the CV stabilized with a significant left shift with respect to the initial state. In order to achieve the true stabilized state, the device was kept in floating condition in dark for 12 hours. Afterward, three consecutive CV measurements were taken in 30 min intervals, which did not result in any further shift in the characteristics, ensuring that a stabilized state has been obtained. After stabilization, the device was illuminated under a small positive gate bias of 2 V. The bias was needed to set up a field in the dielectric that would drive the detrapped holes towards the substrate. Note that the bias was too small to stress the dielectric. It is clear from Fig. 5.9 that the CV shifts to the right as the photon energy is scanned from the lower to the higher value of the spectrum, indicating hole detrapping mechanism.

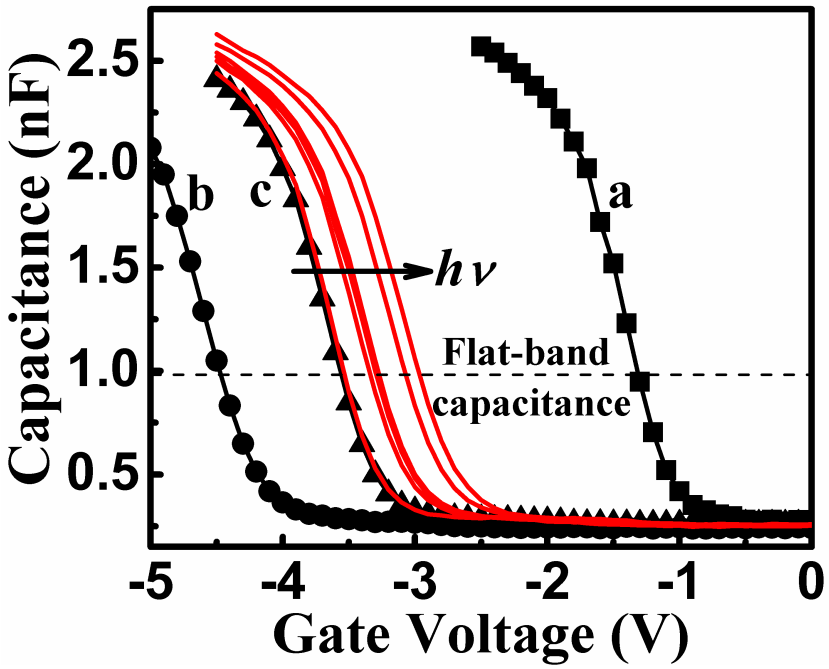

Figure 5.9: CV characteristics obtained at different conditions; (a) before programming (solid squares), (b) after programming (solid circles) and (c) 12 h after programming (solid triangle). CV, after 20 min of illumination with different excitation energies (red solid lines) are also shown.

Fig. 5.10 shows the flat band voltage ($\triangle V_{FB}$) as a function of the illumination energy. It may be noted that the energy is varied from 0.4 eV (3102.5 nm) to 1 eV (1241 nm) in steps of 0.05 eV and then up to 1.6 eV (775.6 nm) in steps of 0.1 eV. At every step, the sample is illuminated for 5min before CV measurements. It is evident from the Fig. 5.10 that V_{FB} does not monotonically vary with the photon energy; rather it changes in steps at certain specific energy values, indicating detrapping of holes from different trap states at those photon energies. The energy position of these traps with respect to the valence band maximum can thus be obtained (marked by arrows in the figure). The mechanism of detrapping can be understood from the schematic band diagram of our

device shown in the inset of Fig. 5.10. Band diagram is drawn based on the reported literature. Valence band offset between Si and Si_3N_4 is approximately 1.9 eV [3]. Considering band gap of Si 1.1 eV and band gap of Si_3N_4 is 4.7 eV [96], conduction band offset is deduced to 1.7 eV. Electron affinity of Si_3N_4 is 2.1 eV [97] and work function of ITO is 4.4—4.5 eV [95]. So, conduction band offset between Si3N4 and ITO is nearly equal to 2.3 eV.

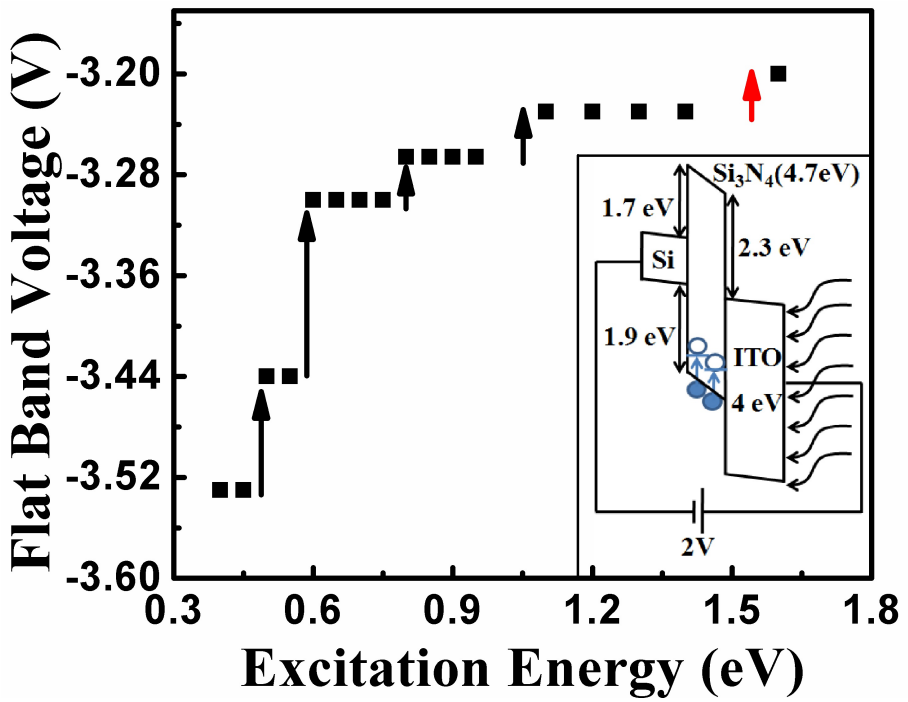

Figure 5.10: Flat band voltage as a function of excitation energy after 5 min of illumination. Inset: Pictorial description of detrapping mechanism. Band gap of Si_3N_4 has been considered as 4.7 eV [96].

Under illumination, holes can be detrapped from a certain trap level if the photon energy matches with the energy difference between the valence band and the trap level. This would result in a rightward shift of the CV. Note that, the step occurring at 1.6 eV (red arrow) might be associated with the photo-excitation of electrons from Si to Si_3N_4 because this energy is close to the conduction band offset between the two materials. In order to understand the timescale involved in these detrapping processes, CV measurements are carried out for different illumination time-spans at photon energy of 0.5 eV. It has been found that CV characteristic initially shifts with time but saturates after 12 min of illumination. It is noteworthy that, saturation time is around 1 h for both thin Al [4] and thin Au [5] gate electrode. Actually, $\triangle V_{FB}$ versus photon energy for 5 min illuminations is shown in Fig. 5.10. 5 min illumination is not sufficient time to obtain saturation in ΔV_{FB}, which means result of 5 min illumination is transitional, not steady state. The saturation value of the shift in flat band voltage ($\triangle V_{FB}^{s}$) is measured after 20 min of illumination only at those photon energies, where shifts in V_{FB} were observed for 5 min illumination. Calculated trap density from $\triangle V_{FB}^{s}$ is listed in Table 5.3.

It is well documented that traps in the Silicon Nitride film is not positioned only at Si/dielectric interface, but distributed in the bulk of the film [3, 24]. Moreover to estimate distribution of trapped charge in our Nitride film photo-IV measurement was carried out following the work done by R. F. DeKeersmaecker and D. J. DiMaria [25]. In this work they studied trapping and detrapping characteristics of As+ doped SiO_2 layer, embedded in Al (semitransparent)- SiO_2-Si structure, by CV and photo-IV measurements. To measure photo-current in their MOSCap structure (Si-SiO_2-Al) photon energy of 5 (4.5) eV was used for +ve (-ve) gate bias. For our study, Si/Si_3N_4/ITO structure has been used to estimate physical distribution of traps in the Nitride layer. $CB_{Si_3N_4}$-VB_{Si}=2.9 eV and $CB_{Si_3N_4}$-CB_{ITO}=2.3 eV. CB stands for conduction band and VB stands for valence band. Initially photocurrent was measured as a function of positive (negative) gate bias under illumination by 405 nm/3.1 eV (532 nm/2.3 eV) laser. After that, device was programmed by -15 V gate bias for 1 s. After programming, photocurrent was again measured in same condition as described above. The result is shown in Fig. 5.11.

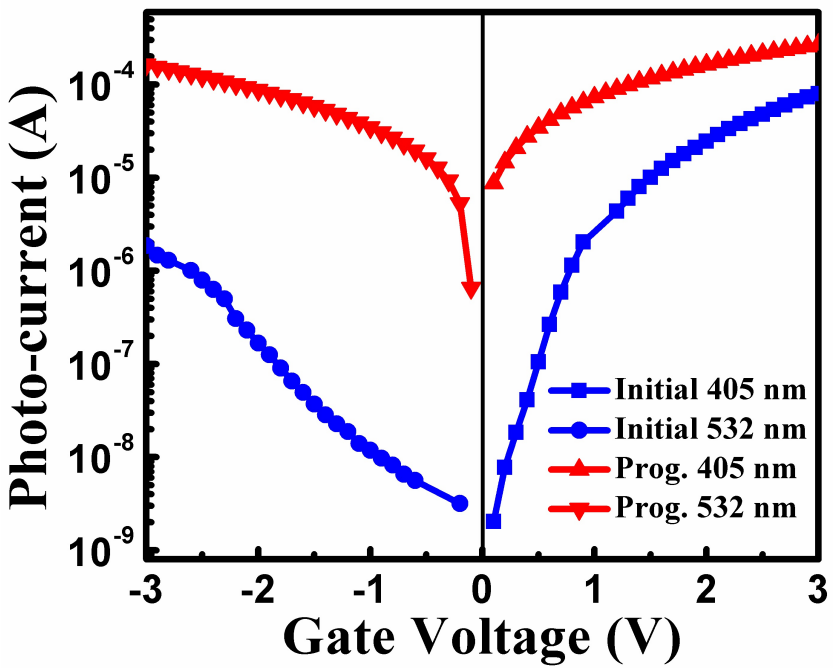

Figure 5.11: Photocurrent as a function of gate voltage before and after charging of the Nitride layer. Programming of the device was done by $-15\ V$ gate bias for 1 s.

For a fixed photocurrent the shift in gate voltage before and after programming can be expressed as

$$\triangle V_G^- = V_{GB}^- - V_{GA}^- = 1/\varepsilon\,(L - \bar{x})\,Q \tag{5.1}$$

$$\triangle V_G^+ = V_{GB}^+ - V_{GA}^+ = -Q\bar{x}/\varepsilon \tag{5.2}$$

where, (+ or -) refers to polarity of the gate voltage, a and b refers to the state before and after

charging, Q is the integral of trapped space charge density in the insulator over thickness L and $\overline{x}$ is the position of the trapped charge centroid measured from metal/dielectric interface.

From the above expression it is clear that $\triangle V_G$ strongly depends on the position of the charge centroid in the dielectric. $\triangle V_G^+$ is not sensitive to traps lying at Si_3N_4/ITO interface and $\triangle V_G^-$ is not sensitive to the trap levels lying at Si/Si_3N_4 interface. So, the significant shift in photocurrent after programming for both positive and negative gate bias clearly indicates that traps in Nitride layer are distributed in bulk of the dielectric.

For calculation of trap density, uniform spatial distribution of traps in Nitride layer [98, 99] has been assumed. Trap density can be calculated using saturation value shin in V_{FB} (i.e., $\triangle V_{FB}^s$), for different trap levels, following the equation [100],

$$\triangle V_{FB}^S = \rho X_T^2 / \left(2\varepsilon_N\right) \tag{5.3}$$

where, ρ is the trapped charge density (C/cm^3) and is equal to qN_T

$$N_T = 2\varepsilon_N \triangle V_{FB}^S / \left(qX_T^2\right) \tag{5.4}$$

where, X_T is the thickness of the region where the trapped charges are distributed, which is considered to be the entire thickness of the Si_3N_4 layer in this case. ε_N is the dielectric permittivity of Si_3N_4 layer and N_T is the volume trap density.

Table 5.3: $\triangle V_{FB}^S$ and N_T for different trap levels observed for Si_3N_4 layer.

Excitation wavelength (nm)/ energy (eV)	$\triangle V_{FB}^S$ V	N_T cm^{-3}
2482/ 0.5	0.18	1.2×10^{18}
1654.6 / 0.75	0.04	2.7×10^{17}
1151.2 / 0.8	0.02	1.3×10^{17}
1128.1 / 1.1	0.21	1.4×10^{18}
775.6 / 1.6	0.1	6.8×10^{17}

In Table 5.3, the trap density calculated (using $\triangle V_{FB}^s$) for different trap levels are listed. Note that the highest trap density is observed for the trap levels located at 0.5 eV and 1.1 eV above the valence band edge. It is noteworthy that Gritsenko et al. had also demonstrated the presence of hole traps at similar energy locations in Si_3N_4 using thermally stimulated depolarization (TSD) technique [101].

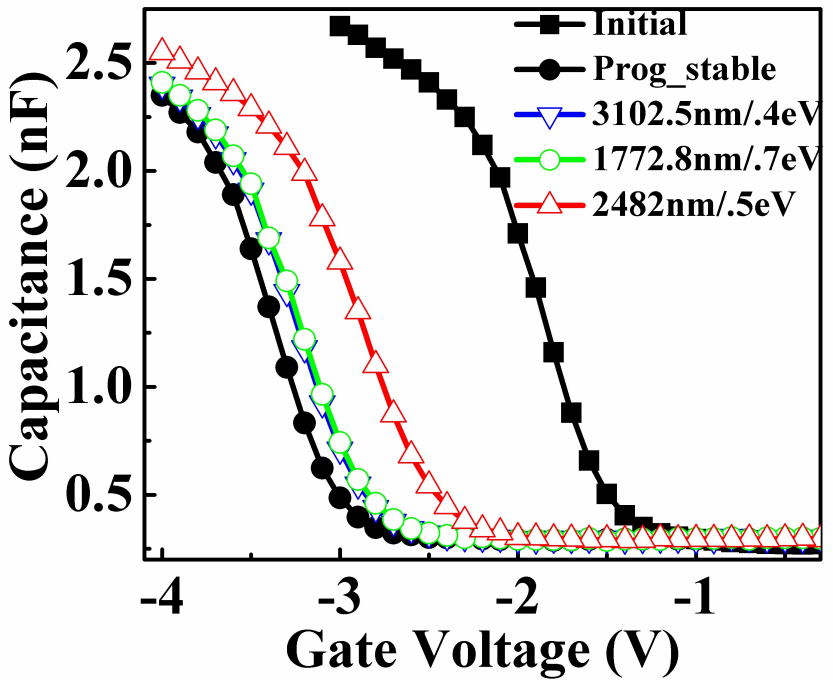

Figure 5.12: Results of Photo CV measurements after illumination, of programmed device. Illumination was carried out with photons of energy 0.4 eV, 0.7 eV and 0.5 eV respectively in that order for 20 min each.

Fig. 5.12 shows the CV characteristics for the device after exposing it to light of different photon energies for 20 min each in the following sequence: first with photon energy 0.4 eV then with 0.7 eV and finally 0.5 eV. After the first step of exposure, the CV slightly shifts towards the positive direction, which might be due to the detrapping of holes from shallow traps. Interestingly, after the second step of exposure with 0.7 eV of photon energy, no shift is found in the CV. However, after the third step of exposure with smaller photon energy (0.5 eV) as compared to previous step, the CV shows a significant shift.

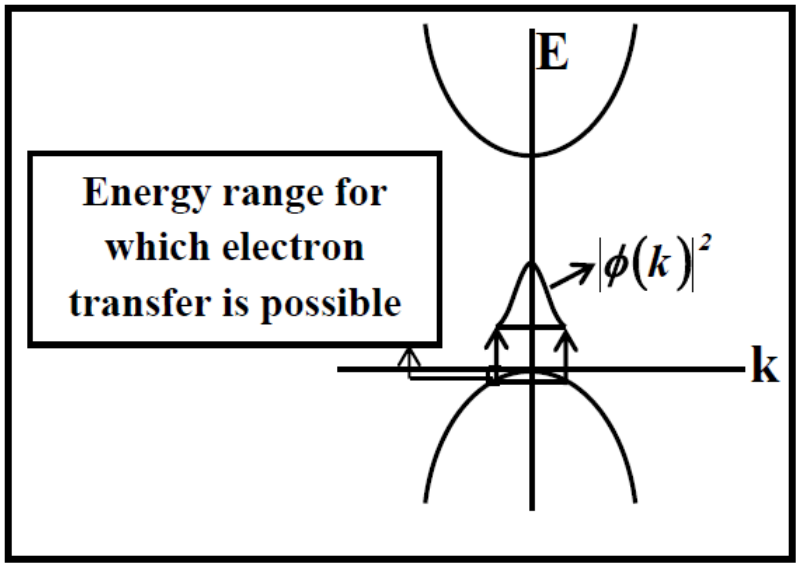

Figure 5.13: Schematic diagram of the detrapping process in k-space. $\mid \phi(k) \mid^2$ represents the probability distribution of electron in the trap level.

These findings suggest that the hole trap level at ~ 0.5 eV is associated with a very narrow probability distribution in the k-space such that, the valence band electrons with k-vector lying within a small range can effectively be transferred to the hole trap state (shown schematically in Fig. 5.13) [102]. Furthermore, this finding also implies that the k-nonconserving transitions via phonon mediated processes are not very significant in this case.

We have performed these experiments with ITO/TiN gate structure as well. The presence of a prominent trap level at energy 0.5 eV has already been observed in Nitride layer. To compare the detrapping efficiency for ITO and ITO/TiN gate, $\triangle V_{FB}$ of the programmed device was monitored as a function of time for excitation energy 0.5 eV. Comparison of saturation time for ITO and TiN/ITO gate electrode is shown in Fig. 5.14. The result shows, shift in V_{FB} almost saturates after 12 min for ITO gate. But, for ITO/TiN gate saturation occurs after around 60 min.

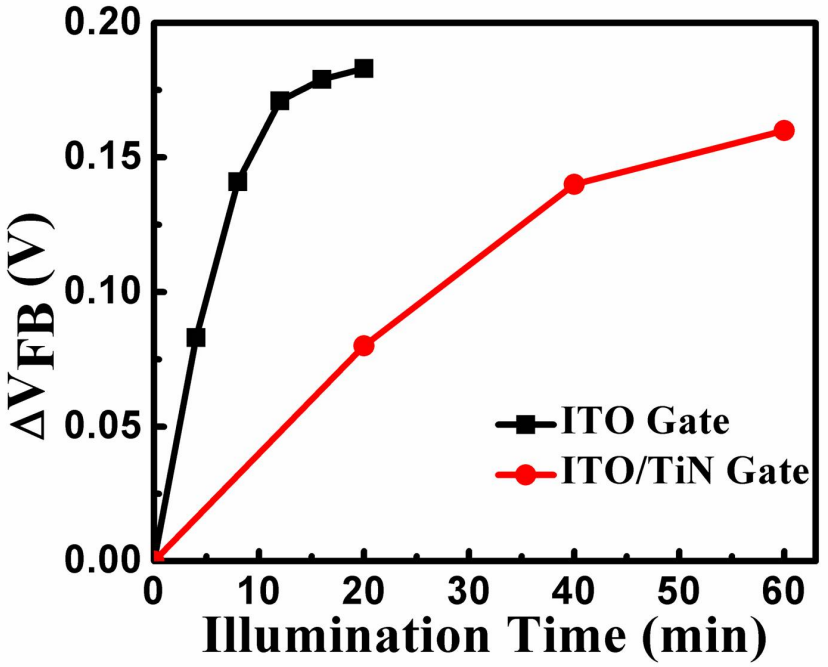

Figure 5.14: Detrapping transient for ITO and ITO/TiN gate at excitation energy 0.5 eV.

Additionally, trap spectroscopy experiment was performed with ITO/TiN gate stack to find out whether the gate structure has any influence on the trap characteristics of Silicon Nitride. The detrapping transient shows, saturation time for $\triangle V_{FB}$ is increased significantly for ITO/TiN gate stack compared to ITO alone (Fig. 5.14). For the trap spectroscopy experiment with ITO/TiN gate, we have scanned excitation energy from 0.4 eV to 1.6 eV with 0.1 eV increments. Device was excited for 30 min at each photon energy. The result is shown in Fig. 5.15.

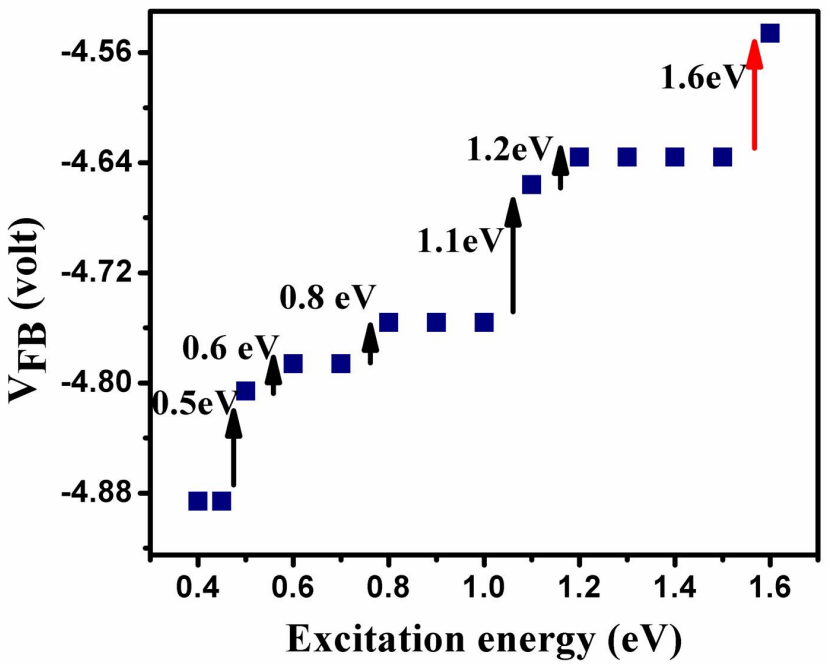

Figure 5.15: Flat band voltage as a function of excitation energy after 30 min of illumination with 10 nm TiN/80 nm ITO gate stack.

Result shows all the trap levels, which were obtained with ITO gate, could also be found in this case. The only difference was the illumination time; much longer illumination time was required in case of ITO/TiN gate as compared to ITO as the former is found to be less transparent. The result strongly suggests that the trap energy levels extracted above are intrinsic to the Nitride film and not related to the ITO deposition.

5.4.3 Comparison of results with reported literature

Our work was focused on characterization of trap levels lying below mid-gap in the Silicon Nitride thin film. Comparatively less reported literature is available on energy position of trap levels in Si_3N_4 film.

G. Rosenman et al. characterized Si_3N_4 film by TSEE technique. They used $Si/SiO_2/Si_3N_4$ structure for their experiment [1]. The temperature of the sample was increased from 300 K to 550 K. Considering Auger recombination, they calculated energy position of trap levels from TSEE glow curve. They found three trap levels lying at energy level (0.65-0.82) eV , (0.74-0.93) eV and (0.87-1.1) eV from conduction band edge. The result was also consistent with other reported results, (0.5-0.85) eV [103], (0.8-0.9) eV [104], (0.95-1) eV [105, 106] and 1.3 eV [107].

In another work, performed by the same group, the experiment was carried out up to higher temperature (850 K) [2]. Scanning up to higher temperature has shown another deeper trap level at 1.73 eV. But no information about trap levels lying below mid-gap was reported in their work.

J. U. Lee et al. performed optical capacitance voltage characterization of the Si_3N_4 film, em-

bedded in MNOS structure [108]. They reported deep trap level is lying over the energy 1.36-1.64 eV from conduction band edge. Again, information about trap levels lying under mid-gap was not extracted.

V. I. Belyi and A. Rastorguyev performed their experiment on Si_3N_4 films. The nitride film was deposited by PECVD method [109]. They measured luminescence spectra of nitride film deposited on different substrates (GaAs and quartz substrate). They compared their results with the theoretical model proposed by J. Robertson and proposed the existence of trap levels at energy (0.1 eV, 0.6 eV, 0.8 eV, 1.8 eV) from valence band edge and 0.8 eV, 1.6 eV, 2 eV) from conduction band edge. In our work also we found a significant change in V_{FB} at 1.6 eV. But, as this energy is almost matching with conduction band offset between Si and Si_3N_4, the shift was not considered.

V. A. Gritsenko et al. studied Si_3N_4 film, deposited by LPCVD technique. In their work, hole trap characterization of the Si_3N_4 film was done using thermally stimulated depolarization (TSD) spectroscopy method [101]. The aim of their work matches most with our work. Also, Si_3N_4 films were deposited using the same technique (LPCVD). In their work also, V_{FB} was measured at each step to track the amount of depolarization. They have reported the existence of two trap levels at 0.75 eV and 1.07 eV from valence band edge. In our study, two trap levels have been obtained at 0.5 eV and 1.1 eV (from valence band edge). So, one trap level is almost matching with their result (1.07 eV and 1.1 eV). Second trap level was found to be 0.25 eV deeper compared to our result. In their work, deposition ambient and RI of the deposited film have not been mentioned. Different film composition might be a reason for the discrepancy.

Table 5.4: Energy position of electron and hole trap levels in Si_3N_4 thin films.

Ref.	Film deposition method	Measur-ement method used	Energy positions above mid-gap (from conduction band edge)	Energy positions below mid-gap (from valence band edge)
[1]	Not mentioned	TSEE	0.65–0.82 eV 0.74–0.93 eV 0.87–1.10 eV	
[2]	CVD	TSEE	1.73 eV	
[108]	Not mentioned	Optical CV Method	1.36-1.64 eV	
[109]	PECVD	Luminescence Measurement	0.8 eV, 1.6 eV, 2 eV	0.1 eV, 0.6 eV, 0.8 eV, 1.8 eV
[101]	LPCVD	TSD Method		0.75 eV and 1.07 eV
This work	LPCVD	Modified Trap Spectroscopy Method		0.5 eV and 1.1 eV

5.5 Conclusion

The density and energetic position of hole trap centers in Si_3N_4 deposited by chemical vapor deposition was investigated using a modified photo-detrapping method. Two prominent hole trap levels at 0.5 eV and 1.1 eV above the valence band edge have been detected. It is also found that phonon assisted detrapping of holes is not a dominant mechanism at least for the 0.5 eV trap level in Si_3N_4. The technique can also be applied to characterize the electron trap levels. To characterize the trap levels above mid-gap, the device would be first programmed by positive gate bias to fill all states by electrons. The consecutive experiments could be followed in the same way, as discussed above.

Chapter 6

Study on UV Stability of Al_2O_3 Thin Films

Recent studies show, Al_2O_3 film is a promising candidate as passivation layer for p-type Si surfaces in solar cells. Positive response of Al_2O_3 film to UV illumination makes it more acceptable compared to Si_3N_4 and SiO_2 films.

Negative charge density is increased in Al_2O_3 film after UV illumination. B. Liao et al. proposed a model to demonstrate the increase in negative charges in Al_2O_3 layer due to injection of electron from Si to Al_2O_3 during the illumination. According to their model electrons can either tunnel through thin interfacial oxide layer or can be photo-injected from Si valence band into conduction band of Al_2O_3 by multiple photon induced electron injection dynamics. After that, from conduction band of Al_2O_3, electrons are diffused to trap sites in Al_2O_3.

Al_2O_3 layers, deposited by various methods, were proposed for its use as passivation layer. Literature shows ALD-Al_2O_3 is a promising candidate as passivation layer. T. T. Li and A. Cuevas reported that, sputtered Al_2O_3 also shows good passivation but not as good as ALD-Al_2O_3 [110].

Behavior of Al_2O_3 film against UV illumination has been studied by different researchers. But comparatively less work is reported about stability of UV induced charge in Al_2O_3 layer. In our wok performance of Al_2O_3 deposited by both sputtering and ALD method has been studied. Also, hardness of UV induced negative charge against optical and electrical stress has been examined.

Hoex et al. have shown that passivation effect increases with thickness of Al_2O_3 layer and almost saturates after 15 nm [111]. In this study thickness of Al_2O_3 layer is taken around 20 nm.

6.1 Experiments

The schematic structure of the device, used for this study, is shown in Fig 6.1.

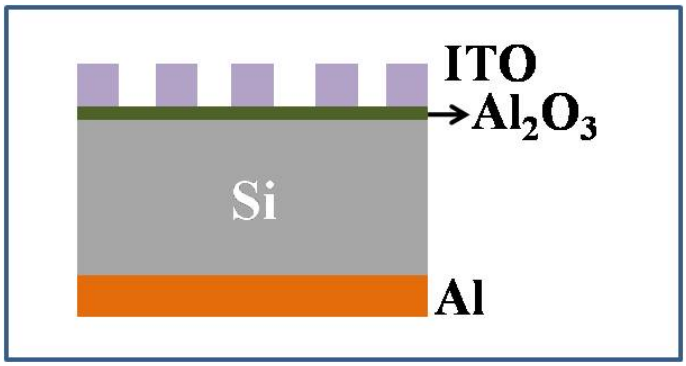

Figure 6.1: Schematic structure of the device.

Thickness was measured for all cases by ellipsometer. After that device was mounted in the same T-stand as shown in Fig. 5.5. The sample was illuminated by a high power (30 mW) laser source of wavelength 325 nm for different time duration. Helium-Cadmium (Hd-Cd) laser was used as source. A glass slide was placed between sample and laser source (as intensity was very high). CV measurements were performed before and after each step of illumination. Flat band voltage (V_{FB}) was tracked to follow effect of UV illumination on the film or more specifically to observe the change in amount of space charge in the film.

6.2 Sample preparation

6.2.1 Sputtering method

Sputtered Al_2O_3 film was deposited by reactive sputter system on RCA cleaned p-Si wafer with resistivity 1-5 Ω-cm. Al_2O_3 film was deposited at 1000 W in Ar:O_2=10:55 sccm for 240 s. Post deposition annealing was done at 520 °C for 20 min in N_2+O_2 ambient.

Work done by M. Bhaisare et al. shows, comparative study of sputtered films annealed at different temperatures (420-520 °C) and in different ambients (forming gas, N_2 and N_2+O_2) [112]. The study shows that film annealed at 520 °C in N_2+O_2 ambient shows minimum D_{it} and low surface passivation velocity. Also, this shows possibility of low cost process, as N_2+O_2 mixture can be replaced by dry air. Following the work, in this study also PDA has been performed at 520 °C in N_2+O_2 ambient.

6.2.2 ALD method

The film is deposited by thermal ALD process at 200 °C, with H_2O and Trimethyl Aluminum (TMA) precursor. The film is deposited by 200 cycles with 0.1 nm per cycle deposition rate. For ALD films also PDA was performed in N_2+O_2 ambient for 20 min at 520 °C.

After Al_2O_3 deposition by both methods, ITO film was deposited using Si hard mask, on samples with and without PDA by RF sputter system. ITO deposition was followed by 20 min annealing

in Ar ambient at 400 °C. The ITO layer, used in this work, has an average transmittance of 84% for wavelength range 360 nm to 3300 nm. At 325 nm ITO layer has 65% transmittance. Back side Al metalization was done by thermal evaporation.

6.3 Results and discussions

6.3.1 Thickness and RI measurements

Thickness of the films, prepared by sputter and ALD systems, have been measured using ellipsometer. The measured thickness and RI are given in Table 6.1.

Table 6.1: Thickness and RI of the films deposited by sputter and ALD systems.

Al_2O_3	Thickness (nm)	RI
Sputtered, Unannealed	23.6	1.682
Sputtered, Annealed	21	1.604
ALD, Unannealed	20.6	1.666
ALD, Annealed	20.9	1.64

The result shows after annealing noticeable change in thickness is observed for sputtered film, which means annealing results in denser film compared to as-deposited film. Such effect is not observed for ALD film. ALD process produces denser film compared to sputter method.

6.3.2 Band gap measurements

Al_2O_3 films deposited on quartz wafer were used for the measurement of the band gap. The band gap of the deposited films were determined from UV-Vis data using Tauc plot. Transmittance of the films were measured using Perkin Elmer Lambda-750 spectrometer. Band gap is measured using Tauc plot [56, 86]. Band gap of sputtered Al_2O_3 films were measured by my co-worker M. Bhaisare and it is found to be 3.46 eV and 4.25 eV for unannealed and annealed sample respectively [113]. Higher band gap is obtained for ALD-Al_2O_3, as shown in Fig. 6.2.

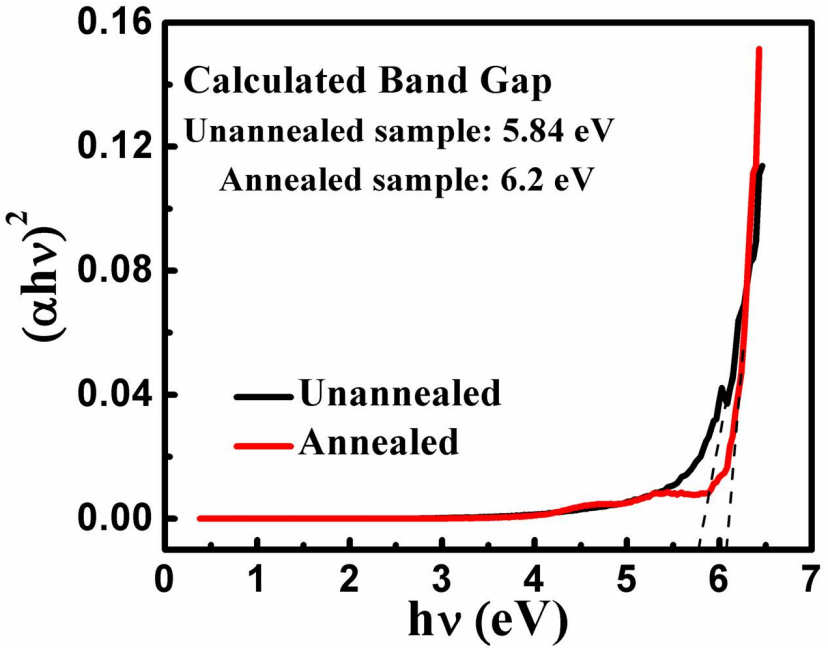

Figure 6.2: Tauc plot for ALD-Al_2O_3 with and without PDA.

5.84 eV band gap is obtained for the unannealed ALD-Al_2O_3 sample. For this case also band gap increases after annealing. After PDA band gap is found to be 6.2 eV.

6.4 UV stability measurements

To measure UV stability of sputtered film, device was illuminated by 325 nm laser without any gate bias (open circuit condition). After certain intervals of illumination time, CV measurements were performed to track change in fixed oxide charge density. Fig. 6.3 shows the shift in V_{MG} as a function of illumination time for sample 2 (sputtered and annealed) and 4 (ALD and annealed).

Fig. 6.3 shows that Q_{OX} saturates within 30 minutes of illumination for both the sputtered and ALD deposited films. Interface charge density (D_{it}) for both the samples were calculated using Termann method [84]. The values of D_{it} were found to be 2.8×10^{12} $cm^{-2}eV^{-1}$ and 2.5×10^{12} $cm^{-2}eV^{-1}$ for initial sputtered and ALD films respectively. For both the samples, no detectable changes in D_{it} were found after illumination.

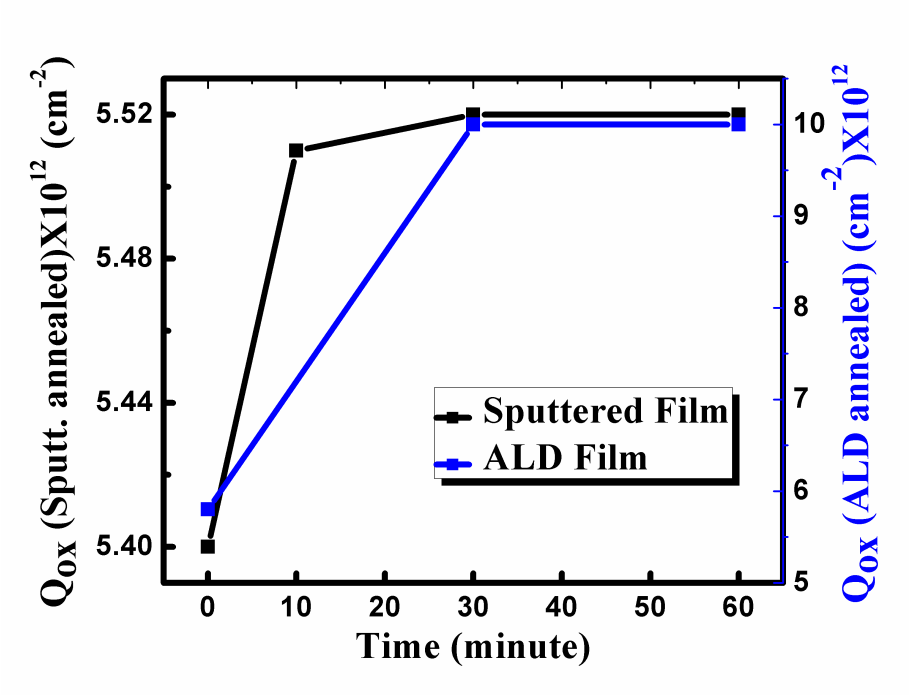

Figure 6.3: Fixed oxide charge (Q_{OX}) as a function of illumination time for (a) sputtered and (b) ALD-Al_2O_3 films.

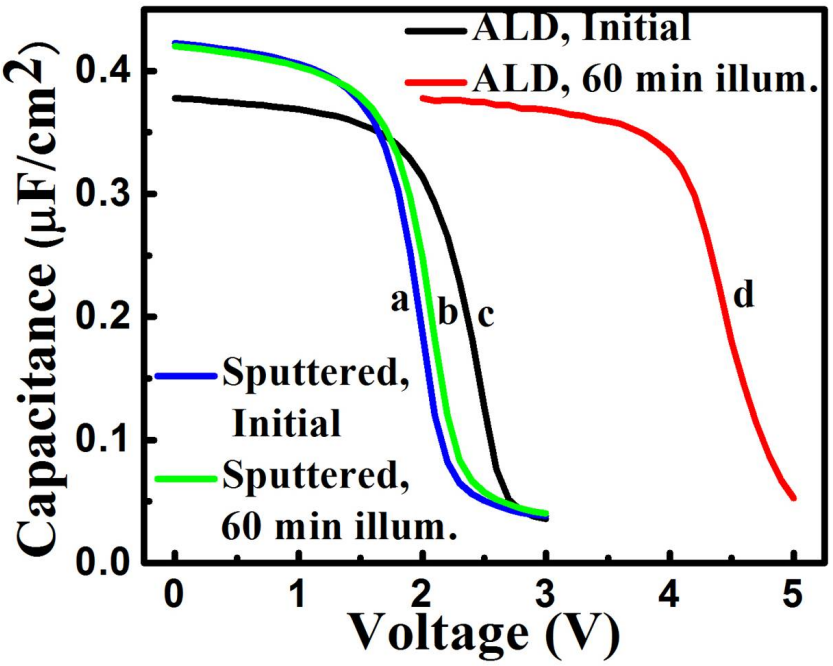

Figure 6.4: CV characteristics obtained for (a) sample 2 (b) sample 2 after 60 min of illumination (c) sample 4 and (d) sample 4 after 60 min of illumination.

Fig. 6.4 shows CV characteristics at initial state and after 60 min of UV illumination for annealed Al_2O_3 deposited by sputter and ALD technique. Initial CV characteristics for samples 2 and 4 clearly show that, fixed negative charge densities are nearly identical for both the films (5.4×10^{12}

cm^{-2} for sputtered film and 5.8×10^{12} cm^{-2} ALD film). As discussed earlier, values of D_{it} are also nearly equal. So, initially both the films are equally qualified to be used as a passivation layer. But, result also shows increase of negative charge occurs due to UV illumination and the difference in oxide charge density is more prominent between the films after illumination. For sputtered film fixed charge increases to 5.5×10^{12} cm^{-2} where, for ALD film fixed negative charge density is increased 10^{13} cm^{-2}. For both cases no significant change in interface trap density is observed after illumination.

It is reported that the increase in negative charge density is due to photo-injection of electrons from Si to dielectric [10]. Lower band gap of sputtered film may lead to easy tunneling of the electrons across the dielectric, leading to lower charge retention. It should be mentioned here that, work done by Hussain et al. shows work function of ITO is increased from 4.31 to 4.81 eV as O_2 flow rate increases in sputtering ambient from 0 to 0.1 sccm [114]. In our work ITO has also been deposited by RF magnetron sputtering system in absence of O_2. So, all calculations have been performed considering work function of ITO is 4.31 eV. Hazel and Jaeger reported an increase in negative charge due to photo-injection of electron from Si valence band to Al_2O_3 over interfacial SiO_2 layer, the threshold energy for this effect is 4.1 eV (i.e., λ=302 nm) [10]. But the result shows electron injection is possible even at lower energy (325 nm i.e., E = 3.8 eV). B. Liao et al. proposed that during UV illumination electron from Si can reach interfacial-SiO_2/Al_2O_3 in two ways: (i) electrons, from Si valence band, can overcome the barrier at Si/SiO_2 interface (ii) electrons can tunnel through the interfacial SiO_2 layer. The result actually supports the model proposed by B. Liao et al., as the interfacial SiO_2 layer is very thin (~ 1 nm) electrons can easily tunnel through this layer and get trapped in Al_2O_3 film [9].

Also, it is reported that for sputtered film interfacial oxide layer is quite thicker (~ 8 nm) compared to ALD film [112]. So, tunneling probability is less for sputtered film. This also explains comparatively smaller UV induced shift in V_{MG} for sputtered film. It is noteworthy that, spectral power distribution of sunlight at sea level shows insignificant contribution from wavelength range below 325 nm [115]. So, tunneling model is more relevant than photo-injection over the barrier.

So, it can be decided that sputtered film is more robust to UV illumination (or UV component of sunlight) compared to ALD film due to presence of thicker interfacial layer.

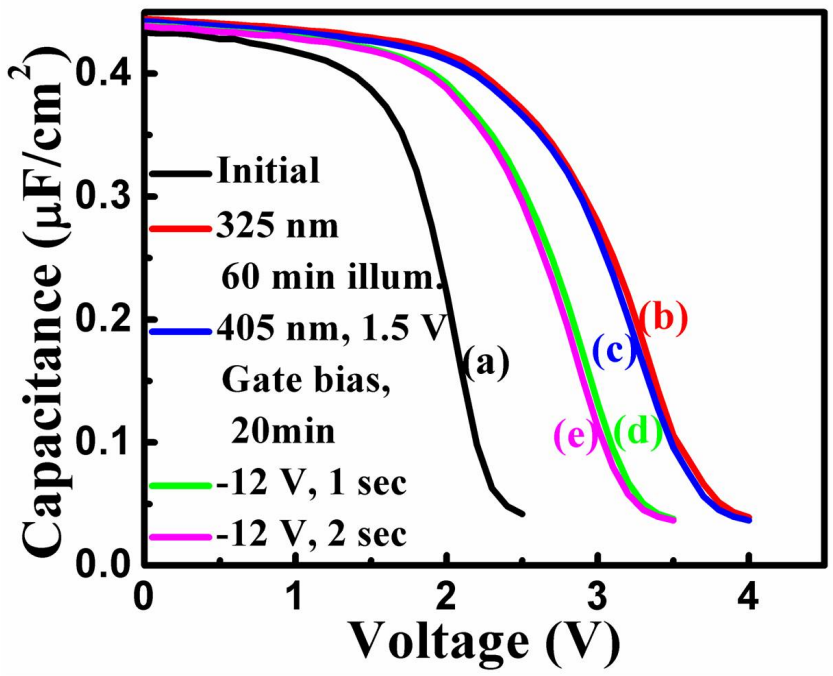

Figure 6.5: CV characteristics after different sequential steps: (a) initial state (b) after illumination of the device by 325 nm laser for 60 min (no gate bias) (c) after illumination of device under 405 nm laser with +1.5 V gate bias for 20 min (d) voltage stress by -12 V for 1 s and (e) voltage stress by -12 V for another 1 s.

Fig. 6.5 shows CV characteristics of as-deposited ALD film after different sequential steps. First, the unannealed sample was illuminated by 325 nm laser (in open circuit condition) for 60 min to ensure that ΔV_{FB} is saturated (Fig. 6.5 (b)). After that device was illuminated by 405 nm laser under small positive gate bias (+1.5 V) to release the trapped electrons. The CV characteristic is shown in Fig. 6.5 (c). Then, a voltage stress of -12 V was applied to the device for 1 s and a sequential measurement was performed (Fig. 6.5 (d)). Finally, the voltage stress part was repeated and the characteristic is shown in Fig. 6.5 (e). Values of Q_{OX} and D_{it}, calculated from CV characteristics, are listed in Table 6.2.

Table 6.2: Values of Q_{OX} and D_{it} calculated from CV characteristics.

	Initial	***60 minutes* illumination , *325 nm* laser, open circuit condition**	***20 minutes* illumination, *405 nm* laser, +1.5 V gate bias**	***-12 V* stress for 1 second**	***-12 V* stress for 1 second**
Q_{OX} (cm^{-2})	**5.2×10^{12}**	**9.1×10^{12}**	**8.9×10^{12}**	**7.5×10^{12}**	**7.3×10^{12}**
D_{it} ($cm^{-2}eV^{-1}$)	**2.6×10^{12}**	**2.8×10^{12}**	**2.7×10^{12}**	**3.2×10^{12}**	**2.9×10^{12}**

A careful observation in initial CV of annealed (Fig. 6.4 (c)) and as-deposited sample (Fig. 6.5 (a)) gives an idea how annealing affects the passivation quality of the film. It is already mentioned

that fixed negative charge density for annealed sample is 5.8×10^{12} cm^{-2} where, for as deposited sample fixed charge density is 5.2×10^{12} cm^{-2}. The difference is not significant. Also, there is always probability of degradation of interface when device goes through temperature treatment. Already it is observed that UV illumination introduces negative charge density. Calculation shows, after 60 min illumination of the as-deposited sample charge density is increased to 9.1×10^{12} cm^{-2}.

Now it should be noted here that, annealing introduces negative charges mostly by structural modification and therefore introduced charges are stable. But UV illumination increases charge density by electron injection. So the question arises whether the charge introduced optically are stable or not. To ensure that additional experiments have been performed. After UV illumination of as deposited sample we have performed trap spectroscopy experiment on that device. In this experiment device was excited by different excitation energy under a small positive gate bias (+1.5 V). The excitation energy was varied from 0.4 eV to 4 eV. Here, dual source of Perkin Elmer Lambda-750 spectrometer was used as source of illuminating energy. It was expected that depending on energy position of trap levels in Al_2O_3 film, at some specific illuminating energies trapped electrons would be released. But no significant shift was obtained (result is not shown here). So, trapped electrons are either at very deep levels or trap levels are with very high emission cross section. To confirm the optical stability of the charge, device was then illuminated with high intensity laser of wavelength 405 nm under 1.5 eV positive gate bias. As shown in figure, in this case also no significant shift is observed (Fig. 6.5 (c)). Also, no significant change in D_{it} is observed due to illumination. In solar cell device dielectric faces negligible electric field. Therefore, electrical detrapping of UV induced charges is not also possible. So, results indicate annealing can be replaced by UV illumination.

Additional experiment was performed to examine electrical hardness of the optically induced negative charges. In this case device was stressed by -12 V (i.e., 6 MV/cm) for 1 s (Fig. 6.5 (d)). The device was stressed again for another 1 s and no further shift in CV was obtained, as shown in Fig. 6.5 (e). As voltage stress was applied for very small time duration, it can be assumed that no additional charge state was generated during the voltage stress. It is observed that significant $-\triangle V_{MG}$ is obtained after first electrical stress. Negative voltage stress produces -0.49 V shift in flat band voltage which is equivalent to decrease in negative oxide charge by an amount of ~ 1.5×10^{12} cm^{-2}. Now negative shift can be achieved due to both electron detrapping or hole trapping. To get estimation of these two effects a fresh device was also stressed by same amount of negative field and that produces $\triangle V_{MG}$=$-$0.13 V ($\triangle Q_{OX}$~0.5×10^{12} cm^{-2}) (Fig. 6.6). For the fresh device it can be expected that, $\triangle V_{MG}$ comes from hole trapping.

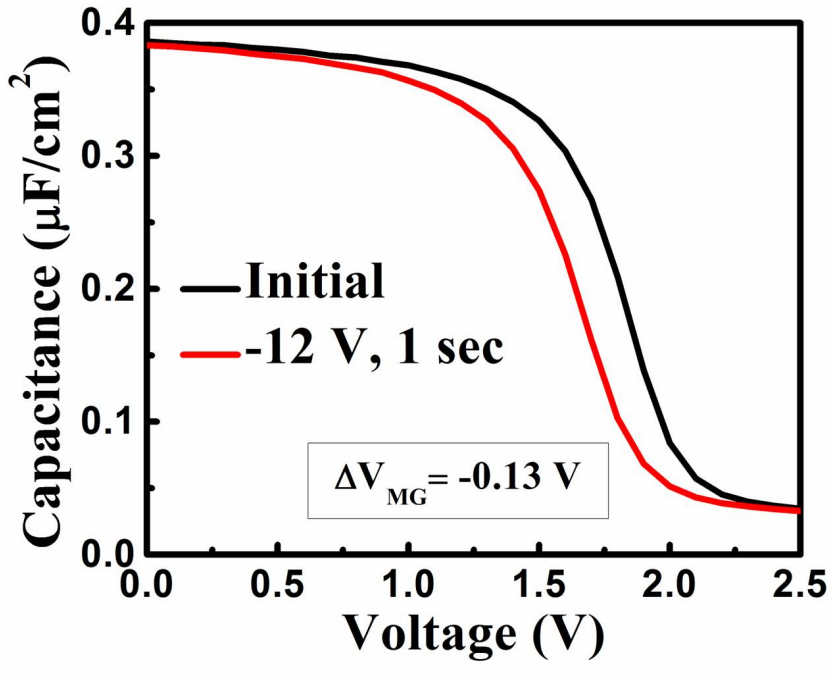

Figure 6.6: (a) Initial CV characteristic of a fresh device and (b) CV profile after voltage stress by -12 V for 1 s.

Results show, for unannealed ALD sample, approximately -0.36 V (-0.49+0.13 V) shift in V_{MG} is obtained by electron detrapping, whereas illumination produced +1.43 V (3.8-2.37) change in V_{MG}. In other words, 60 min of illumination increased Q_{OX} by an amount ~ 4×10^{12} cm^{-2}. Afterward, as device was stressed by -12 V, Q_{OX} was decreased by ~ 1.5×10^{12} cm^{-2} which is a combined effect of detrapping of photo-injected electrons (~ 1×10^{12} cm^{-2}) and trapping of holes (~ 0.5×10^{12} cm^{-2}).

So, results clearly indicate photo induced negative charge in Al_2O_3 film is stable against optical stress and partly stable against electrical stress.

6.4.1 Comparison of results with reported literature

It is well reported that performance of Si_3N_4 and SiO_2 degrades after UV illumination. But some contradictory statements are reported regarding performance of the Al_2O_3 film after UV illumination. J. Schmidt et al., reported that, after UV illumination no significant improvement in an effective lifetime for an Al_2O_3 passivated wafer was observed [116]. Contrary to this, many other groups have reported improvement in performance after UV illumination [9, 80]. The improvement is attributed to photo-injection of electrons from Si substrate. There is no clear evidence whether UV illumination introduces any structural modification or not. If improvement occurs only due to photo-injection of charges then the stability of those injected charges are also important. Comparatively limited works have been reported on the stability of injected charges. B. Liao et al. illuminated Si wafer with double side passivated by Al_2O_3. They found after illumination, effec-

tive lifetime was increased. After illumination, the device was kept in dark condition for a long duration. It was observed that in dark condition effective lifetime was decreased to the initial state after around 600 h (~ 25 days). This result indicates photo-injected charges are quite stable. Our result also shows the stability of injected charges even against optical stress.

Vandana et al. studied annealing effect on ALD-Al_2O_3 film. They used Al-Al_2O_3-Si structure for their study [117]. Post deposition annealing was performed by rapid thermal processing (RTP) at 400 °C. Q_{ox} and D_{it} were calculated from CV characteristics. Q_{ox} and D_{it} were found to be 1.22×10^{12} cm^{-2} and 1.4×10^{12} $cm^{-2}eV^{-1}$ respectively for annealed film. In our study corresponding values are found to be Q_{ox}=5.8×10^{12} cm^{-2} and D_{it} =2.5×10^{12} $cm^{-2}eV^{-1}$. Probably higher annealing temperature (520 °C), in our study, results in the difference.

J. M. Rafi performed quite a similar experiment with our study [118]. In their study Mercury probe setup was used to measure CV characteristics of the ALD-Al_2O_3/Si structure. Q_{ox} was found to be increased from 3.6×10^{12} to 5.6×10^{12} cm^{-2} after annealing at 450 °C. In contrast with our result and also many reported literature, Q_{ox} was decreased after UV illumination of as-deposited sample.

6.5 Conclusion

The passivation quality of annealed Al_2O_3 films deposited by ALD and sputter method has been compared. Sputtered Al_2O_3 film is more robust to UV illumination due to its thicker interfacial layer. Result also shows after UV illumination negative charge density in ALD-Al_2O_3 film is significantly higher compared to the annealed sputtered film. This suggests that, sputtered Al_2O_3 film may not be a good passivation layer compared to ALD-Al_2O_3. Also, for ALD film the increase in negative charge due to both annealing and UV illumination has been tested. UV illumination introduces significantly higher negative charge density compared to annealing step. It has also been found that optically introduced charges are stable against optical stress and partly stable against electrical stress.

Chapter 7

Conclusions and Future Scope

7.1 Conclusions

Process has been optimized successfully to obtain ITO layer with higher transmittance in visible and NIR range by RF sputtering method. It is reported that film with (400) crystal orientation has higher carrier concentration, which results in fall in transmittance in the NIR region due to free carrier absorption. The literature also indicates only presence of O_2 in sputtering ambient causes change in preferential orientation from (400) to (222). In a significant departure from most of the reported work on sputter deposited ITO, we have heated the samples during deposition. In this case even in 99.999% Ar ambient, (222) orientation has been obtained. It has been observed that, effect of substrate temperature cannot be replaced by PDA. For the film deposited at room temperature, presence of (400) peak was observed even after PDA. Best electrical and optical property has been obtained with resistivity 10^{-3} Ω-cm and with average transmittance of 84.4%, 90.2% and 85.3% up to wavelength 800, 2500 and 3300 nm respectively. The result shows that annealing improves conductivity of the film significantly. Transmittance of the film has not been affected much by annealing. Transmittance of the ITO film, deposited at higher RF power shows better optical property.

Modified trap spectroscopy technique has been established successfully using the optimized ITO layer. Si_3N_4 film, deposited by chemical vapor deposition was investigated using modified trap spectroscopy method. Two prominent hole trap levels at 0.5 eV and 1.1 eV above the valence band edge have been detected. It is also found that phonon assisted detrapping of holes is not a dominant mechanism in Si_3N_4 film.

UV effect of Al_2O_3 layer deposited by PVD and ALD method has been studied to find its suitability as passivation layer in solar cell. Result shows ALD-Al_2O_3 is better candidate for that application compared to sputtered film. UV illumination improves performance of ALD film by photo-injection of negative charge in Al_2O_3 layer. UV induced charges are found to be stable against optical stress and partially stable against electrical stress.

7.2 Future scope

Characterization of electron trap levels has not been attempted in this study. The same study can be done using trap spectroscopy method. Also, by this technique probability distribution function for each trap level can be found by minute observation of detrapping transient from corresponding level. Bulk trap level characterization of other wide band gap materials can also be investigated by this technique.

Trap spectroscopy can be applied to Silicon Nitride deposited by PECVD, which is widely used in Silicon solar cells.

Trap spectroscopy technique can be used to find the energy levels of the trap sites in Al_2O_3 film where UV induced charges are stored. Charge trapping and detrapping dynamics in Al_2O_3 film can be understood more minutely by performing such experiments.

In previous literature, it is only postulated that increase in negative charge due to electron injection. There is no clear experimental evidence that UV introduces charges by only electron injection or also by structural modification. To investigate that, first we need to find the temperature below which no annealing effect is observed (say,T_X). Then an UV illuminated (as-deposited) device can be annealed at temperature below T_X. If UV induced shift is due to electron injection only then the shift can be recovered.

A recent study has shown deep UV light (low pressure mercury lamp) results in densification of different sol-gel films (Indium Gallium Zinc Oxide (IGZO), Indium Zinc Oxide (IZO), In_2O_3 [119]. Sol-gel Al_2O_3 is also used as passivation layer [120]. But required high temperature treatment restricts its application for polymer substrate. So, it would be interesting to investigate whether UV illumination can avoid the high temperature treatment for sol-gel film. F. Tzompantzi et al. have shown XRD pattern of sol-gel Al_2O_3, annealed at different temperatures [121]. XRD measurement after UV illuminated as-deposited sample can correlate with the annealing temperature.

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List of Publications from this Thesis

- K. Midya, M. Bhaisare, A. Kottantharayil and S. Dhar, “Investigation of nature of UV induced negative charge in Al_2O_3 film”, presented in the International Conference on Emerging Electronics 2016 conference and under the publication process.
- K. Midya, S. Dhar and A. Kottantharayil, “Trap characterization of silicon nitride thin films by a modified trap spectroscopy technique”, J. of Appl. Phys., Vol. 114, pp. 154101, 1-4 (2013).
- K. Midya, A. Sharma, A. Kottantharayil and S. Dhar, "RF sputtered ITO thin film with improved optical property", MRS Proceedings, Vol. 1447, pp. mrss12-1447 (2012).