Study of Advanced MOS Devices: Fabrication and Characterization

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Technology

by

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This thesis is dedicated to my loving parents

Declaration of Academic Ethics

I declare that this written submission represents my ideas in my own words and where others‘ ideas or words have been included, I have adequately cited and referenced the original sources. I declare that I have properly and accurately acknowledged all sources used in the production of this thesis.

I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

Date: June 27, 2012 VENKATA NAVEEN KUMAR N (09307917)

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Abstract

With the advances in scaling trends, the classical MOSFETs suffer from the technology limitations. As the channel lengths go below 20nm, ultra-sharp doping concentration gradients are required at the source-channel and drain-channel junctions to sustain transistor behaviour. Such steep doping profiles are too hard to realize given the statistical nature of distribution of dopants and the laws of diffusion. Inorder to overcome this technology bottleneck, a novel device structure known as Junction-Less Transistor (JLT), with uniform doping concentration along source-channel-drain, was proposed and patented.

JLT has been a topic of research interest for the semiconductor community, heading into ultra-short channel regime. JLT on Silcon-On-Insulator(SOI) has been studied extensively in the past few years. Our group at IIT Bombay has proposed a Bulk Planar Junction-Less Transistor(BPJLT) which is a highly scalable and a more attractive device than the SOIJLT. We discuss the BPJLT fabrication process and the challenges faced during the course of this process.

We propose fabrication of BPJLT using shallow implant as device layer. Device isolation is created using standard LOCOS process. A gate stack of TiN/Al_2O_3 is optimized for the integration into BPLJLT process flow. As the implant conditions chosen were not able to achieve a ultra shallow junction for the BPJLT process, we have explored the possibility for poly-silicon as an alternative channel material. We present back-gated JLT as the test structure to study the suitability of poly-silicon as a device layer i.e. resistor action in the absence of gate field and the effects of depeletion in the presence of gate field. Fabrication process and the resulting I-V characteristics of back-gated JLT have demonstrated poly-silicon's effectiveness as an active device layer. Another BPJLT fabrication process with poly-silicon as device layer has been proposed with the change in gate stack $-$ Al/SiO_2. Roughness of poly-silicon plays the spoilsport in this process and more experiments are needed to finetune the poly-silicon deposition process. An alternative process flow with epitaxially grown p-type silicon as device layer is explored as another potential candidate.

We also study the fabrication of a long-channel NMOS transistor using standard CMOS

process. I-V characteristics of NMOS transistors with gate lengths 8.9μm, 2.5μm and 1.5μm are presented. The additional unit processes required for the short-channel NMOS fabrication are also covered.

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Chapter 1

Introduction

Scaling MOS technologies was necessitated by the significant gains seen in the three vital device metrics - performance, area and power dissipation. To reap the benefits of scaling, MOS transistor had stepped into the nanometer regime with the support of advances made in fabrication technology. Ion implantation and advanced lithography played a crucial role in realizing ultra-scaled MOSFETs.

Future projections on MOS devices with channel lengths less than 20nm do not seem to become a reality. Source-drain junctions pose a tough challenge in this regard. Very steep concentration gradients are desired at source-channel and drain-channel junctions, to realize channel lengths less than 10nm. Because of the statistical nature of distribution of dopant atoms and the laws of diffusion, which govern the implant and anneal behaviour, such doping gradients are too difficult to achieve. This limitation signals the end of road for CMOS scaling. As a solution to this technology bottleneck, a novel device structure, with no lateral concentration gradient along source-channel-drain, was proposed and patented[1]. This advanced MOS device, which is seen as a potential candidate to replace conventional MOSFET in the forth-coming ultra short channel era, is called the Junction-Less Metal Oxide Semiconductor Transistor or simply Junction-Less Transistor (JLT).

1.1 Junction-Less Transistor: A Glance at History

Fig.1.1 presents a schematic view of junction-less architecture: (a) an n-channel junction-less structure and (b) a tri-gated junction-less topology. The history of this structure dates back to 1928 when an Austrian- Hungarian scientist J.E. Lilienfeld filed patent for a device with the title “Device for Controlling Electric Current"[2]. Lilienfeld‘s device looked identical to the conventional MOS field-effect structure with a semiconducting layer deposited on a dielectric-metal stack. The metal film acts as the gate terminal and thereby modulates the carriers in the semiconductor film depending on the voltage applied. In a nutshell, the device is a resistor

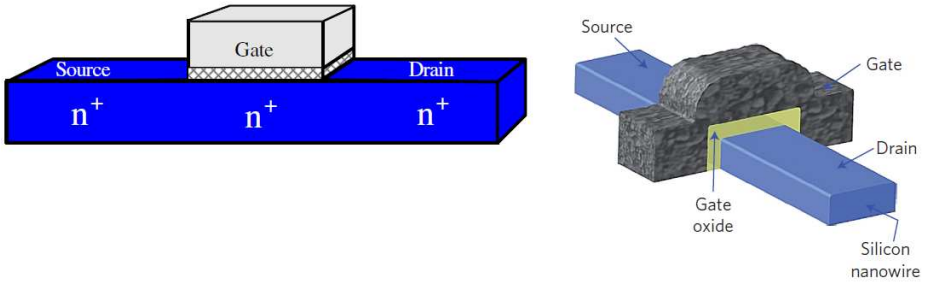


Figure 1.1: a) cross-section of an n-channel JLT[3] b) schematic of tri-gate JLT[4]

whose carrier density is controlled by the gate action. Technological challenges in fabricating ultra-short channel MOSFETs have aroused interest in this architecture in the recent years.

This junction-less module has become a subject of research interest at various institutes such as Tyndall National Institute, IMEC, Korean Advanced Institute of Science and Technology, IME Singapore and Indian Institute of Technology Bombay. A number of device architectures such as Vertical Slit Field Effect Transistor[5], Nanowire SOI Transistor[4], and Bulk Planar Junction-Less Transistor[6] have been proposed across the world and all these devices are based on same principle of operation as the junction-less architecture.

Having understood that realizing a classical MOSFET with sub-20nm channel length is a distant reality, our group at Centre of Excellence in Nanoelectronics(CEN), IIT Bombay started exploring the suitability of JLT in the short-channel era. By device simulations, we have identified that Bulk Planar Junction-Less Transistor(BPJLT), a bulk version of JLT, is highly scalable and an attractive candidate for short-channel applications[6]. This huge potential of JLT aroused interest and motivated us to fabricate the BPJLT and demonstrate its transistor action.

1.2 Organization of the Report

Chapter 2 deals with the literature of JLT: device physics, principle of operation and its comparison with conventional MOSFETs. A novel device architecture proposed at IIT Bombay – BPJLT is covered in this section. Chapter 3 focuses on process flow and experimental results in the fabrication of BPJLT with shallow implant serving as active device layer. Back-gated JLT process with polysilicon as device layer is discussed in Chapter 4. Chapter 5 talks about experiments on BPJLT with poly silicon as device layer and JLT based on epitaxially grown device layer. Chapter 6 deals with NMOS transistor fabricated using standard CMOS process flow. The SEM images of the final NMOS device and its corresponding I-V characteristics are

also covered in Chapter 6. Chapter 7 concludes the report with a brief summary and a glimpse of future work in this research module.

Chapter 2

Junctionless Transistor

2.1 Principle and Physics of JLT

The JLT operation is broadly summarized in two states: OFF and ON state. The OFF state is marked by the semiconductor layer (deep blue region in Fig.1.1(a)) fully depleted under the gate due to the field effect. The depletion region is fully devoid of carriers and hence provides a very high resistance to the current flow between the source and drain terminals. The ON state is characterized by the semiconductor layer that has come out of depletion. The device operates in or around flat band state in the ON state. The carrier presence under the gate channel forms a continuous channel with the carriers in the source and drain regions to facilitate current flow.

The trigate JLT structure on buried oxide (BOX) is shown in Fig.2.1(a). The width W and thickness T_{Si} of the uniformly doped layer are depicted in Fig.2.1(b). For the ease of understanding the underlying physics, the JLT can be viewed as a stack comprising three major portions:

- The bottom portion of the stack is the uniformly doped semiconductor device layer – yellow turf in Fig.2.1(a). This region is most critical for the device to demonstrate transistor behaviour. The thickness of this region T_{Si} needs to be accurately controlled such that it is thin and narrow enough to be fully depleted off the carriers in the OFF state. The device layer should be highly doped to ensure (a) high ON currents (b) reduced contact resistance at the source-drain terminals. But high dopings carry an inherent risk. For fixed gate dimensions, the higher the doping of the device layer the depletion region along T_{Si} becomes thinner. Then the semiconductor is not fully depleted in OFF state. This results in high currents even when the device is OFF and the switching action of transistor is lost. Therefore, the thickness T_{Si} and doping should be optimized in tandem with each other to achieve high ON currents and minimal OFF currents.

- The central portion of the stack is the gate oxide – white patch in Fig.2.1(a). The gate ox-

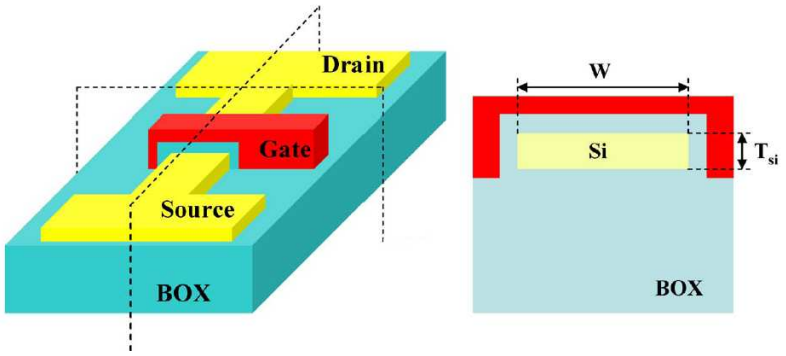


Figure 2.1: a) Schematic view of tri-gate SOI-JLT b) Width W and thickness T_{Si} of tri-gate SOI-JLT[7]

ide should not be more than a few nanometres so that the gate-field remains high enough to deplete the semiconductor material below. If the gate-field is reduced, the thickness of the depleted semiconductor region decreases which ultimately lead to high OFF currents and drastically reduces the ON/OFF ratio.

- The top portion of the stack is the gate shown in red in Fig.2.1(a). The gate engineering revolves around choosing the appropriate material for different devices. To ensure positive threshold voltages for the n-channel JLT, a p+ polysilicon or a metal with p+ work function is employed as gate. This p+ gate material, with its high work function difference with the n+ device layer, should be able to fully deplete the device layer when zero gate voltage is applied. Similarly, an n+ polysilicon or a metal with n+ work function has to be used in a p-channel JLT.

The electron concentration (in n-channel JLT) under the gate gets modulated in accordance with the gate voltage applied. In brief, JLT can be visualized as a resistor whose conductivity is influenced by the gate sitting above it. Fig.2.2 presents the electron concentration contour plots in an n-channel JLT for a range of gate voltages: $V_{GS} < V_T$ (less than threshold voltage) to $V_{GS} = V_{FB} \gg V_T$ (much greater than threshold voltage and equal to flat band voltage).

2.2 A Comparison with MOSFET

A cross-sectional view in Fig.2.3 shows how the JLTs differ from the classical inversion and accumulation mode MOSFETs. A p-channel SOI-JLT looks exactly like a p-channel accumulation mode SOI-MOSFET except for the non-uniform doping along the source-channel-drain in the case of latter. In JLT a uniformly doped p+ device layer is present along the source-channel-drain. In both these devices, the channel has the same polarity as that of the semiconductor region in which it is formed. However, there are two major differences that are explained below:

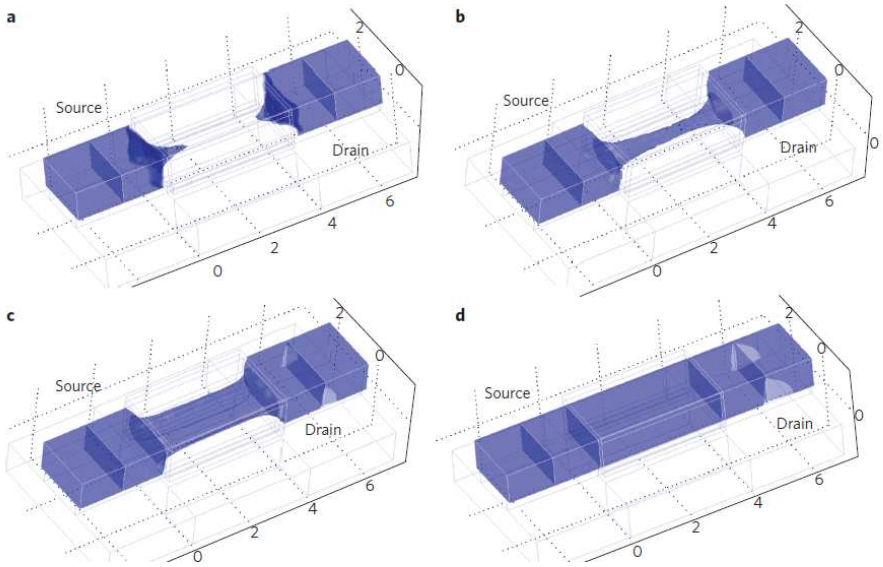


Figure 2.2: Electron concentration contour plots in n-channel JLT for a) $V_{GS} < V_T$ b) $V_{GS} = V_T$ c) $V_T < V_{GS} < V_{FB}$ d) $V_T \ll V_{GS} = V_{FB}$[4]

- The channel region is lightly doped in accumulation mode devices and therefore has higher resistance compared to their JLT counterparts. The accumulation mode devices have to be operated at sufficiently high gate voltages in order to drive a significant current through the device.

- Accumulation mode MOSFET, much like an inversion mode, exhibit surface conduction whereas JLT is a classical example of bulk conduction device. The $V_{GS} = V_{FB} \gg V_T$ state in Fig. 2.2 justifies the fact that conduction takes place throughout the thickness of silicon in JLT. In the MOSFET, the surface roughness at the oxide-silicon interface, due to abrupt termination of crystalline Si, and presence of interface traps scatter the carriers and impact their mobility. Since JLT supports bulk conduction, the carriers moving from source to drain are much influenced by surface defects.

Besides being structurally different with the inversion mode devices, there is one key aspect that stands out. In the inversion mode(enhancement) devices, the gate voltage needs to be sufficiently positive to create an inverted channel under the gate. So in the MOSFET during its ON state, the gate field penetrating into the semiconductor surface is high. The JLT is in its ON state when the device is biased around flatband(where the normal field is negligible). Therefore the JLT does not suffer from field dependant mobility degradation in its ON state[8]. This results in a higher ON current in JLT when compared to that of a classical MOSFET.

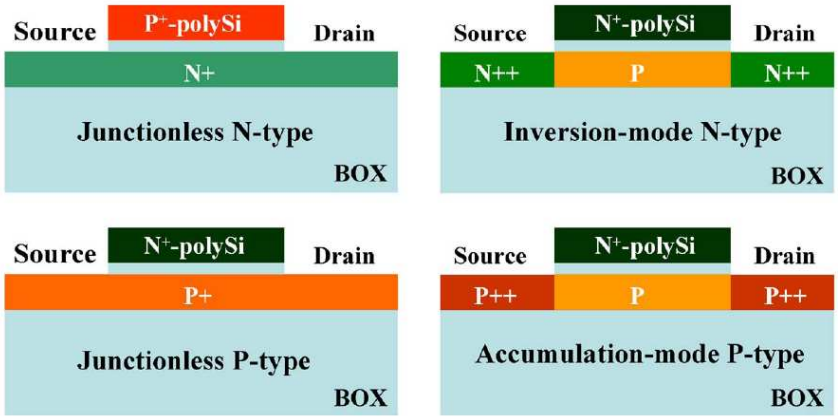


Figure 2.3: Cross-section of n-type JLT, p-type JLT, n-type inversion and p-type accumulation MOSFETs[7]

2.3 An Introduction to BPJLT

Most of the existing literature in JLT corresponds to devices fabricated on SOI structures. Experimental results of tri-gate SOI-JLT with 10nm thick semiconductor device layer (SOI), 10nm thick gate oxide, 1um gate length has been reported by Tyndall group in 2010[4]. Simulation results projected that an ultra thin Si body would be necessary for fabricating such devices with sub-20nm channel lengths[6, 9]. As getting a uniform 5nm SOI is technologically challenging and very costly to produce, our group at IIT Bombay proposed a novel device “BPJLT" which is a more attractive and less expensive alternative device for nanometre regimes[6]. Fig.2.4 shows the cross-sectional view of n-channel BPJLT and n-channel SOI JLT.

SOI-JLT is based on buried oxide(BOX) isolation whereas BPJLT is based on junction isolation. BPJLT is junction-less in the sense that there is no junction in the lateral direction at source-channel-drain interface. There is a junction with the substrate in the vertical direction to provide source-drain isolation with the bulk.

In the case of SOI-JLT, the semiconductor device layer is depleted from the top in the OFF state because of the work function difference with the gate. But in BPJLT, the semiconductor layer is depleted in both the directions, from the top and the bottom, in the OFF state. The additional bottom depletion in the device layer is caused by the p-n junction formed with the substrate. Fig.2.5 explains the notion in terms of band diagram.

To have an effective device layer (in BPJLT) thickness equal to the physical device layer thickness of SOI-JLT, the BPJLT can have a thicker physical device layer. Therefore the fabri-

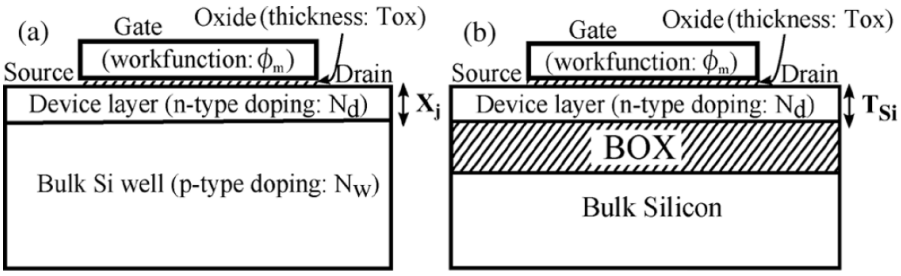


Figure 2.4: Schematic of a) n-channel bulk planar and the b) n-channel SOI junction-less transistors[6]

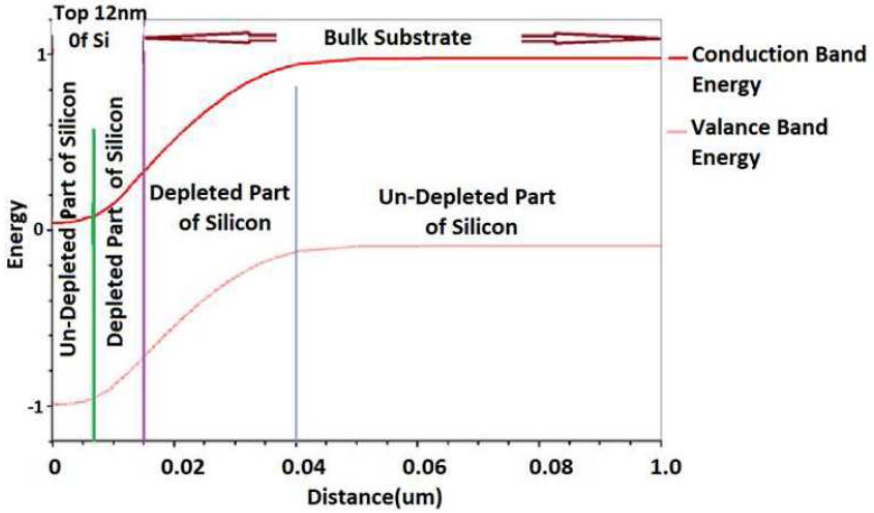


Figure 2.5: Band diagram in vertical direction at the mid of the channel of a BPJLT in the ON state[10]

cation constraints are less stringent in case of BPJLT when compared to SOI-JLT. This requirement on device layer thickness can be relaxed by 50 percent using parameters like substrate doping and substrate bias[6]. The additional knobs – substrate doping and substrate bias in BPJLT also serve the purpose of reducing the short channel effects (SCE). Thus, BPJLT stands out as a better option against its SOI counterpart for ultra-scaled gate lengths. The substrate doping is increased in order to improve the I_{ON} to I_{OFF} ratio which justifies the projection of BPJLT as a low standby power (LSTP) device. But increasing the substrate doping beyond a certain relative level (w.r.t. device layer doping) results in thinning of the depletion width and hence contribute to high tunnelling currents. These tunnelling currents contribute to the OFF current of the device and therefore the transistor action is disturbed.

Chapter 3

BPJLT – Shallow Implant as Device Layer

3.1 Introduction

The theory and physics behind Bulk Planar Junction-Less Transistor(BPJLT) is explained in Chapter 2. From the fabrication perspective, thin device layer (X_j shown in Fig.2.4(a)) with uniform thickness and doping turns out to be a major bottleneck. Several experiments have been planned using different materials as device layers. This chapter concentrates on BPJLT fabrication which uses shallow implant as the device layer.

Acknowledging the potential of BPJLT in the coming short channel era, our group has decided to take up the challenge of fabricating n-channel BPJLT in the CEN facility at IITB. A gate-last process is employed in the flow and the difficulty of gate alignment with source-drain region (which commonly occur in the gate last process of a classical MOSFET) does not factor in the case of JLT. With the absence of alignment issues, hallow and anti-punch-through implants, JLT wins over MOSFET in the ease of fabrication. Besides realizing the BPJLT device shown in Fig.2.4(a), the fabrication process incorporates an additional complexity. The target device layer thickness of 12-15nm is so shallow that when the device is probed, there is a high likelihood of punching through the source-drain regions and touching the substrate. So in order to account for the reliable characterization of the device, deep source-drain (also known as probe area) implants are included in the process flow. A separate mask called probe area mask has been designed to open windows for the probe area implants. Inclusion of this probe area mask makes this fabrication a 3-level mask process. A top view of the three masks with the required alignment is shown in Fig.3.1.

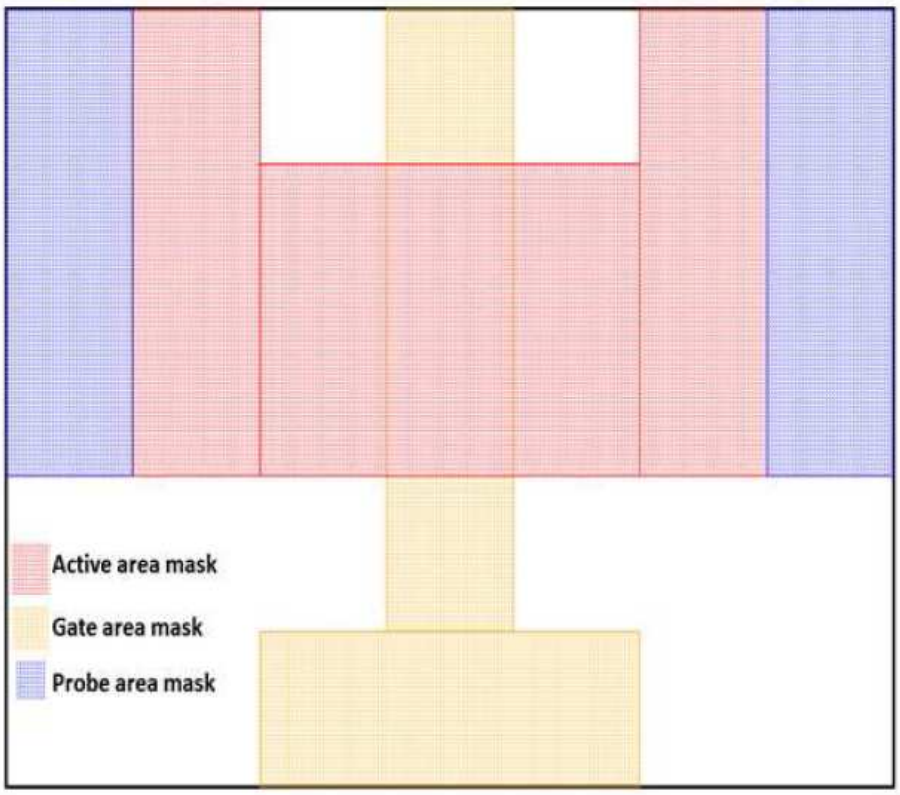


Figure 3.1: Top view of the three masks used in BPJLT fabrication. Dimensions are not to scale[10]

3.2 Experimental Work

The fabrication process starts with creating device isolations using standard Local Oxidation of Silicon(LOCOS) process. Then probe areas are defined within the active area pads, where deep source-substrate and drain-substrate junctions are formed. Subsequently a shallow junction, which serves as device layer, is formed in the active area of the device. Finally a gate stack is deposited and patterned to form a transistor. The entire fabrication process comprising 46 unit steps in total is broadly categorized into four modules: Active area definition, Probe area definition, Shallow junction definition and Gate stack definition. The 21 unit steps which form the crux of the processing are listed in Table 3.1 under their respective headings. Annexures, mentioned next to the corresponding headings, contain the process recipes and the equipment used in the fabrication process. Module-wise experiment details and results are provided below for the ease of trouble shooting and comprehension.The mask details and critical steps in each module are also explained. The schematic view of the device at different stages in the process flow is presented below in Fig.3.2.

Table 3.1: Major unit processes in the fabrication of BPJLT

Module Defintion	Unit Processes	Process Details
Active Area		Annexure I
1	RCA Clean	
2	Pad Oxide (SiO_2) Growth and Si_3N_4 Deposition	
3	Active Area Lithography	
4	Dry Etch of Si_3N_4	
5	Field Oxide (SiO_2) Growth	
6	Wet Etch of Si_3N_4	
Probe Area		Annexure II
7	Probe Area Lithography	
8	Probe Area Implant (Phosphorus)	
9	Piranha Clean	
10	Rapid Thermal Annealing	
11	Low Temperature Oxide(SiO_2) Deposition	
Shallow Junction		Annexure III
12	Shallow Implant (Arsenic)	
13	Solid Phase Epitaxial Regrowth at 650C	
14	Piranha Clean	
Gate Stack		Annexure IV
15	Al_2O_3 by Physical Vapour Deposition	
16	TiN by Physical Vapour Deposition	
17	Chemical Vapour Deposited(CVD) SiO_2 as hard mask	
18	Gate Area Lithography	
19	Wet Etch of TiN	
20	Wet Etch of CVD SiO_2	
21	Backside metallization (Al)	

3.2.1 Active Area Definition

The active area definition comprises a sequence of unit steps, numbered 1 to 6 in Table 3.1. A 4 inch p-type silicon wafer with 0.02-0.04 ohm-cm resistivity and <100> orientation is the starting substrate material. This resistivity is chosen to stay consistent with the required substrate concentration of 1 x 10^{18} $-$ 2 x 10^{18} cm^{-3}. The processing is done in two separate runs: Run I with four wafers and Run II with six wafers. All the ten wafers have been taken through the six unit steps in the required sequence 1 to 6. The process details, ellipsometry measurements and microscopic inspection points are listed in Annexure I.

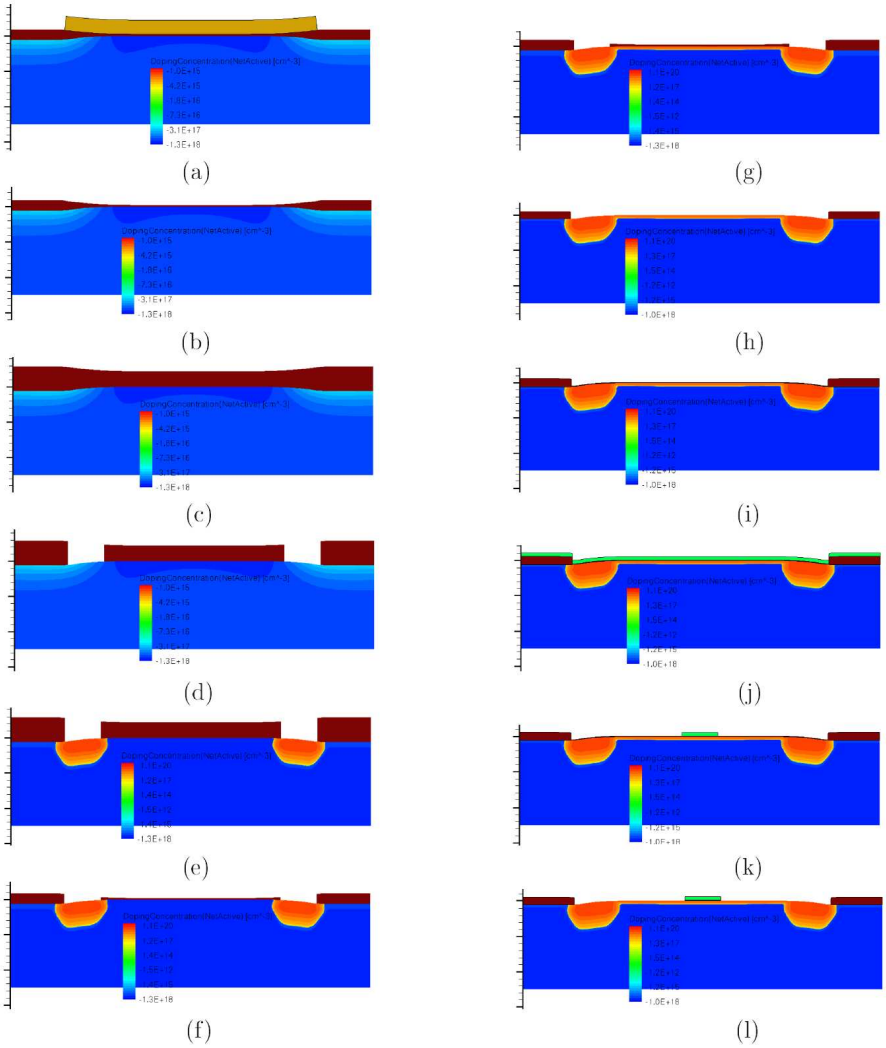


Figure 3.2: Process flow images after a) Field oxide growth b) Nitride wet etch c) Resist coating before probe area lithography d) Probe area lithography e) Probe Implant f) Resist removal + probe implant anneal g) LTO deposition + shallow implant h) LTO stripped + SPER i) Gate dielectric deposition j) Gate deposition k) Gate patterning l) Gate oxide removal from unwanted regions[10]

Thickness and refractive index(a check for stoichiometry) of pad oxide and nitride are measured immediatly after their respective growth and deposition. Duration of the etch process in the subsequent steps is tuned in accordance with the measured thickness. Stoichiometry of silicon nitride is more critical that it can act as a potential show stopper. Non-stoichiometric nitride cannot be etched in hot phosphoric acid (typical wet etchant for Si_3N_4) and without etching this nitride there is no way forward. Efforts have been put to optimize a stoichiometric silicon nitride (refractive index ~ 1.985). Table 3.2 contains the mean thickness and the mean refractive index values of pad oxide (SiO_2) and Si_3N_4 for all the ten wafers.

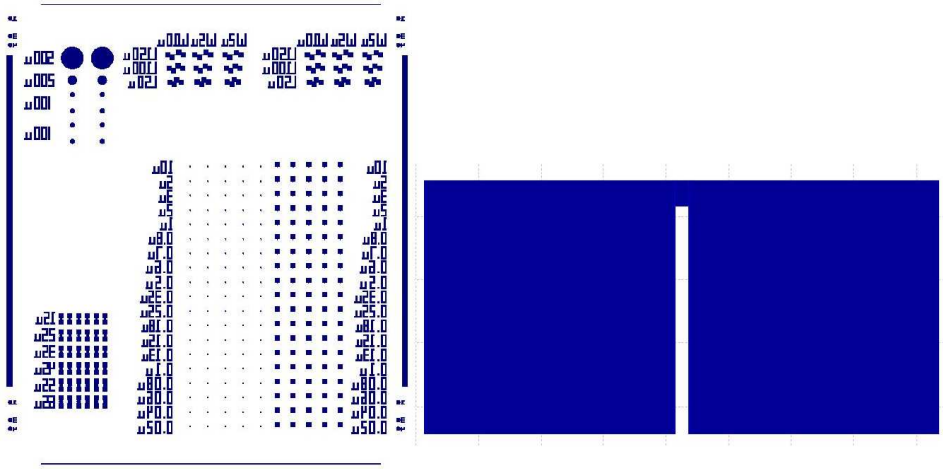


Figure 3.3: a) Active area mask for a die b) Active area pads of a device in a particular die

Active area lithography uses the CMOS active area mask with pad dimensions of 100μm x 100μm. The mask contains 10μm wide SEM lines spaced by 10μm and these lines are used for the cross-section SEM imaging and step-height measurement in profilometer. The gds image of a die on the active area mask is shown in Fig.3.3(a). The gds image of an active area pad on a die is shown in Fig.3.3(b). After the nitride dry etch, the wafers are dipped in Piranha solution (96% conc. H_2SO_4: 30% H_2O_2 in 7:3 volumetric ratio) for an hour. Piranha mixture is highly corrosive and is meant to clean the organic residues off the substrates. This treatment is especially important prior to the furnace processes. Subsequently the wafers have been transferred to pyrogenic(wet oxidation) furnace for the field oxide (FOX) growth. The mean thickness and the mean refractive index values of FOX (SiO_2) are also included in Table 3.2. With the wet etch of silicon nitride using hot phosphoric acid, the standard LOCOS process comes to an end. Fig.3.4 gives the top view of the wafer at different stages in the LOCOS process. Also shown in the figure is the SEM cross-section of FOX, famously known as “Bird‘s Beak".

3.2.2 Probe Area Definition

The probe area lithography comprises the series of unit processes, numbered 7 to 11 in Table 3.1. As discussed earlier, a probe area mask was designed to open windows for the probe implants. The mask is so designed such that the probe pads sit within the active area pads and the active area pad is 3μm wider than the probe area pad on one side, to allow room of misalignment during the lithography. The process details and microscopic inspection points are listed in Annexure II.

The probe area gds images are depicted in Fig.3.5. As seen in the figure, the mask contains local alignment marks around the probe pads to facilitate alignment of gate fingers of shorter

Table 3.2: Ellipsometry data for Pad Oxide(PO), Silicon Nitride(SN) and Field Oxide(FO). W No. - Wafer Number, M.T.- Mean Thickness(in nm), M.R. - Mean Refractive Index

W No.	M.T. – PO	M.R. – PO	M.T. – SN	M.R. – SN	M.T. – FO	M.R. – FO
1	7.70	1.457	65.31	1.971	280	1.464
2	7.92	1.459	66.15	2.001	288	1.471
3	7.66	1.461	65.40	1.982	257	1.459
4	7.81	1.449	62.45	1.981	270	1.441
5	8.01	1.447	59.33	1.979	312	1.461
6	8.35	1.453	62.12	1.982	296	1.473
7	8.04	1.464	63.90	1.987	317	1.457
8	8.41	1.460	62.81	2.010	312	1.462
9	8.02	1.452	61.27	2.001	309	1.455
10	8.10	1.459	60.01	1.992	316	1.460

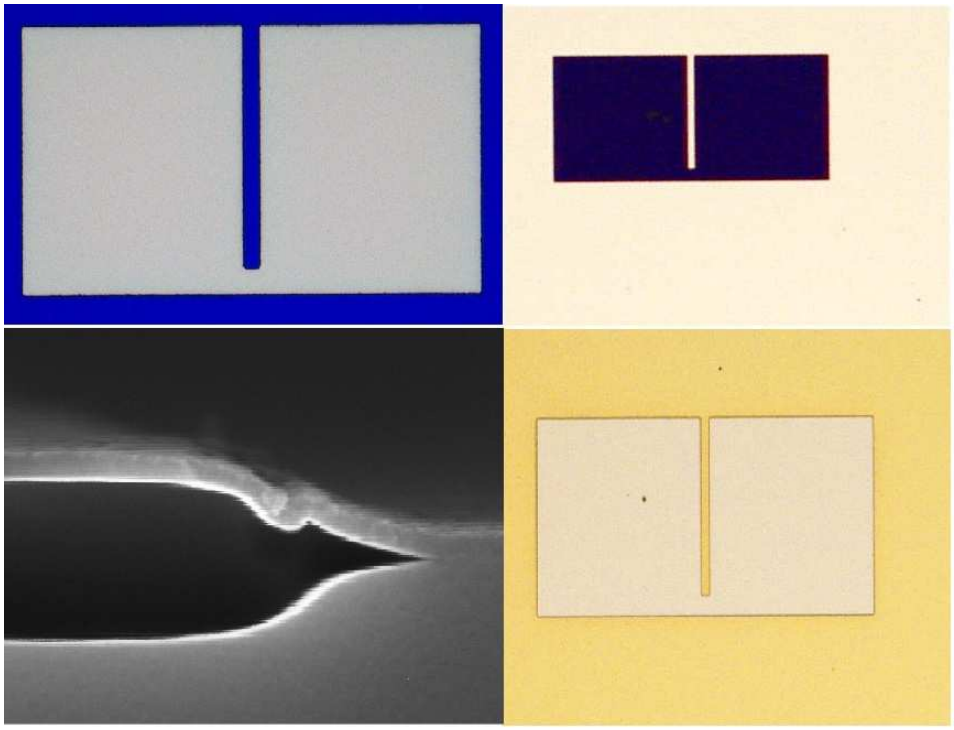


Figure 3.4: Microscopic images in LOCOS process – in the clock wise direction after a) Active area lithography b) Dry etch of silicon nitride c) Wet etch of silicon nitride d) SEM of Bird‘s Beak structure

channel lengths, if patterned using mix-and match lithography. With the knowledge of targeted junction depth and targeted concentration, the implant recipe is figured out using SRIM simulations. The simulated implant profile for achieving the required specifications is shown in Fig.3.6. The implantation has been done at Bharat Electronics Limited, Bangalore using the recipes optimized from simulations.

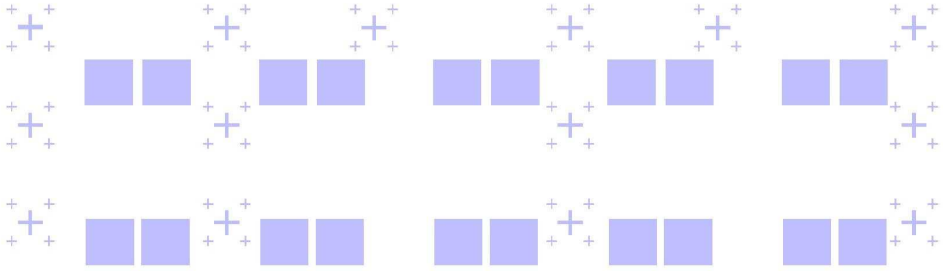


Figure 3.5: Probe area pads with local alignment marks

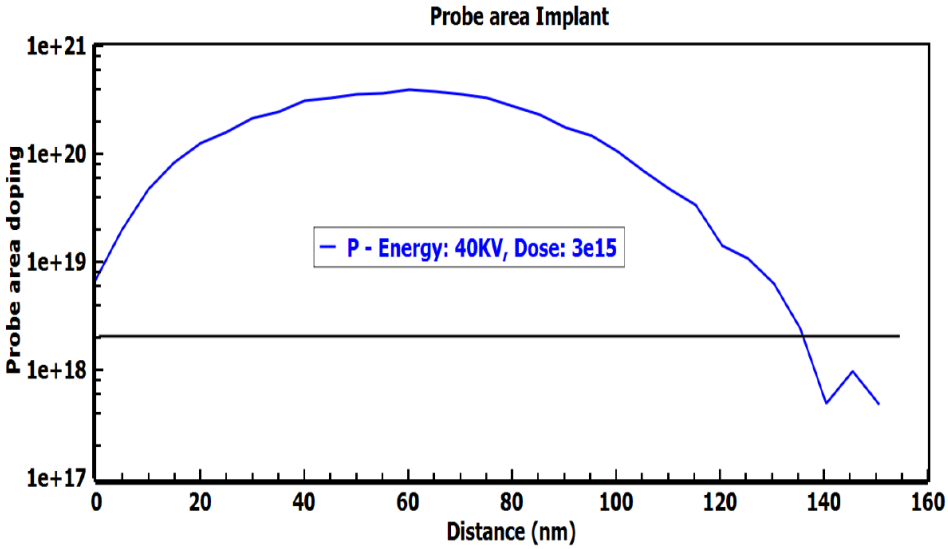


Figure 3.6: Simulated probe implant (Phosphorus) profile

The temperature for rapid thermal anneal has been chosen to be around 1000C for efficient dopant activation and effective damage anneal[11]. But to zero down on a particular temperature, time and ambient, experiments have been performed on diodes fabricated on dummy wafers where junctions are created using the probe implant recipe. The first experiment had anneal temperatures 1000C, 1050C and 1100C, each done in two time stamps – 5sec and 10sec respectively. The ambient for all six anneal recipes was 1000 sccm of N_2. The anneal recipe which gives the best forward current (at a forward bias 2V) and least reverse saturation current (at a reverse bias -1V) is picked up. The diode experimental data related to the above description is shown in Fig.3.7. It is clearly evident from the figure that recipe R1 is the best choice of all the recipes used in the first experiment.

The second experiment uses recipe R1 and introduces traces of oxygen in 50sccm, 75sccm and 100sccm respectively. Recipe OR2 – 1000C, 5sec, 1000 sccm N_2 and 50 sccm O_2 turned out to be champion, as depicted in Fig.3.8. It has been observed that higher traces of oxygen have reduced the forward current drastically and increased the leakage current marginally.

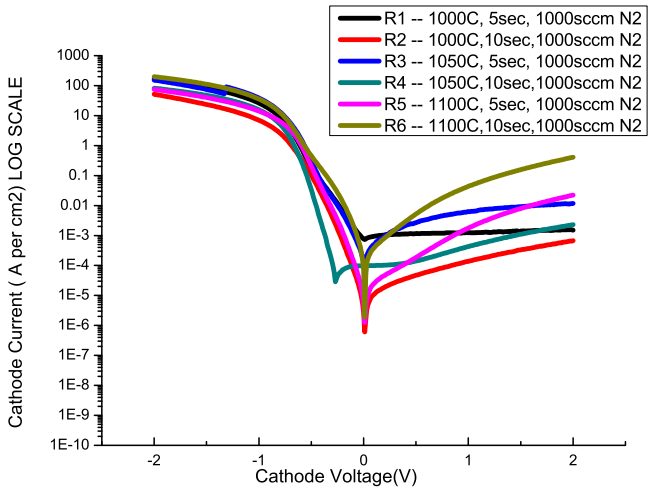


Figure 3.7: Forward and reverse bias diode currents (in A/cm^2) for six different recipes. R1 stands out

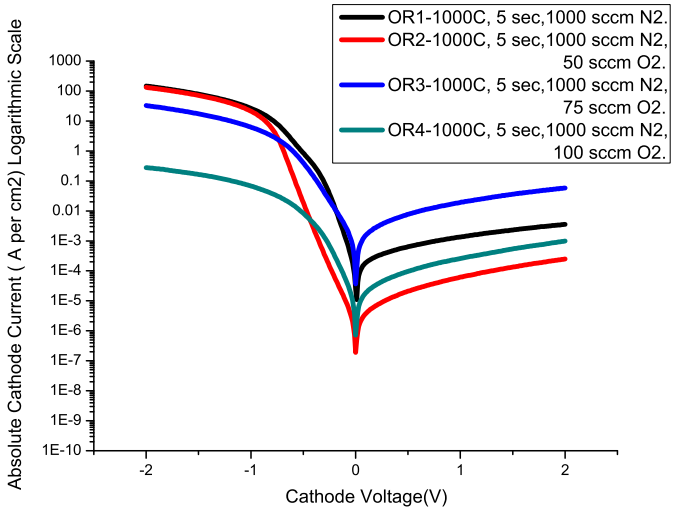


Figure 3.8: Forward and reverse bias diode currents (in A/cm^2) for four different recipes. OR2 stands out

Therefore recipe OR2 has been chosen to activate the probe implants.The surface SEM images of the probe area definition are presented in Fig.3.9. The inner side of the probe area pad within the active area is seen clearly due to the colour contrast.

3.2.3 Shallow Junction Definition

The shallow junction definition is a small section of three unit steps, numbered 12 to 14 in Table 3.1. Though the number of steps is less, this section is the most defining module for the successful fabrication of n-channel BPJLT. The target junction depth falls in the range of 10

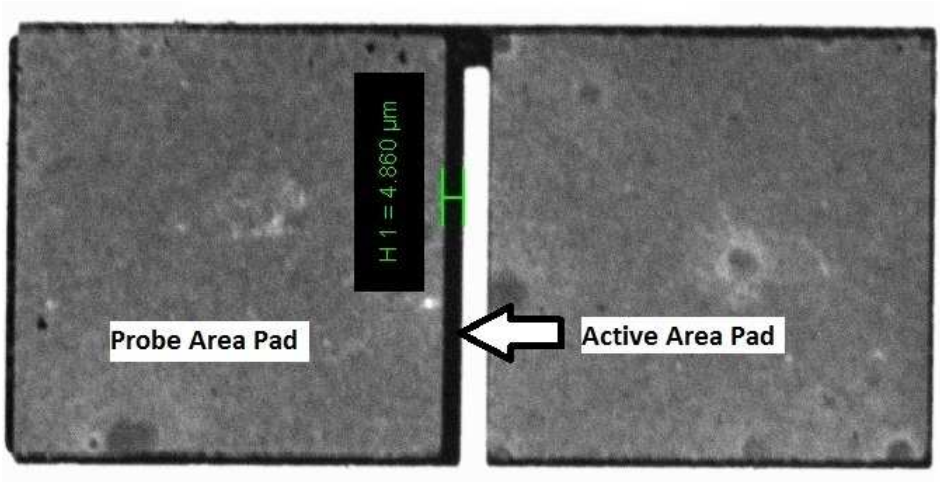


Figure 3.9: SEM image after Probe area definition. Grey colour square represents the probe area pad and the background black colour area represents the active area pad

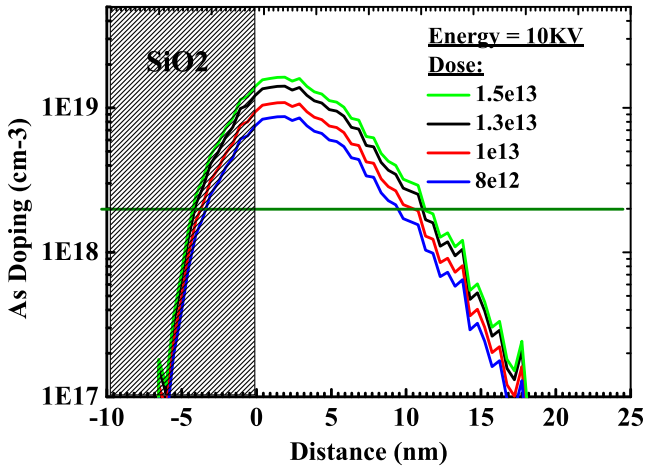


Figure 3.10: Simulated shallow implant (As) profile through 10nm thick screen oxide

– 15nm. Fabricating shallow junctions is very challenging from the technology perspective. Simulations to that effect have been done using SRIM to identify the implant energy and dose. Implant energies in the order of 10KeV are preferred when implanted through a 10nm screen oxide, as indicated in Fig.3.10. In the first place, the implanter should be sophisticated enough to accelerate dopant atoms with such small energies. Due to lack of such technologically advanced implanters in India, the processed wafers have been sent to USA for the shallow implant purpose. The primary reason for choosing Arsenic species is explained in the next paragraph. Only two doses – 1.5 x 10^{13} cm^{-2} and 1 x 10^{13} cm^{-2}, out of the four shown in Fig.3.10 have been used for the fabrication purpose. The process details for this section are jotted down in Annexure III.

An advanced technique called Solid Phase Epitaxial Regrowth (SPER) is utilized here as a replacement for the conventional rapid thermal or furnace annealing. SPER is a low temperature process that ensures highly activated ultra shallow junctions. The choice of 650C as the temperature for carrying out SPER and deep insight into physics behind SPER is available in the research domain[12]. If SPER was able to achieve what a conventional anneal can do, there is always a question that why SPER can‘t be integrated into CMOS technology process in place of high-temperature anneal. Actually in the SPER process flow, the wafers should go through special conditions before they actually get a dopant implant. The most important of all such conditions is the pre-amorphization implant (PAI). The pre-amorphization implant separates the dopants from the defects thereby streamlining SPER‘s duty to dopant activation only[12]. But PAI is not necessary when Arsenic in the dopant implant material as Arsenic is a self-amorphizing species. This is one major reason for choosing Arsenic as shallow implant dopant. Other reasons include higher solubility in silicon, lesser diffusion when compared to phosphorus due to its higher molecular weight.

The shallow junction definition section became a show stopper in the fabrication of BPJLT. Resistance measurements across the SPER activated device layers presented with currents in the order of few nanoamperes. These device layers are subjected to high-temperature anneal(around 1000C) to check if the problem is related to the low temperature SPER process. The currents continued to show up in the nanoampere range. This led to the conclusion that the implant could not manifest itself in the device layer. Lack of implanted region made this process flow redundant.

3.2.4 Gate Stack Definition

The gate stack definition comprises the sequence of unit process steps, numbered 15 to 21 in Table 3.1. This is the last section in the fabrication process and is responsible for the gate action. MOS capacitors have been made initially with TiN/Al_2O_3 gate stack to demonstrate gate action. Wet etching is utilised to define the gate regions. The use of TiN as gate material necessitated the inclusion of SiO_2 as hard mask as the wet etchant for TiN (NH_4OH:H_2O_2:H_2O in the ratio 1:2:7) also removes the protecting resist. The process conditions and inspection node points find mention in Annexure IV. The CMOS gate area mask is used to pattern the gate. The gds image of a gate pad with gate finger is shown in Fig.3.11(a). Fig.3.11(b) shows gds images of MOS capacitors(of diameters $-$ 500μm, 200μm and 100μm) on gate area mask. These MOS capacitors are meant for testing the gate action.

While fabricating MOS capacitors with TiN gate it has been observed that pinholes are

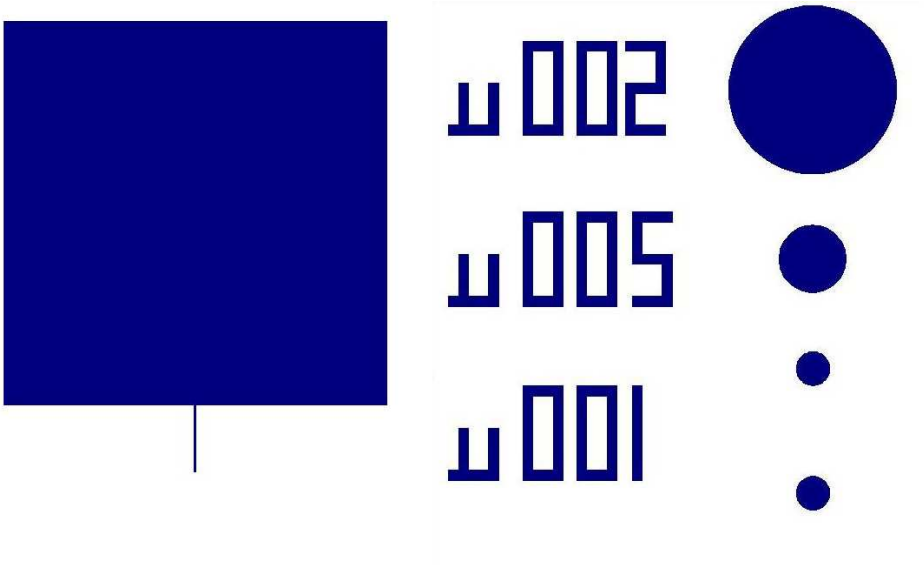


Figure 3.11: a) Gds image of gate pad with gate finger b) Gds image of MOS capacitors in CMOS gate area mask

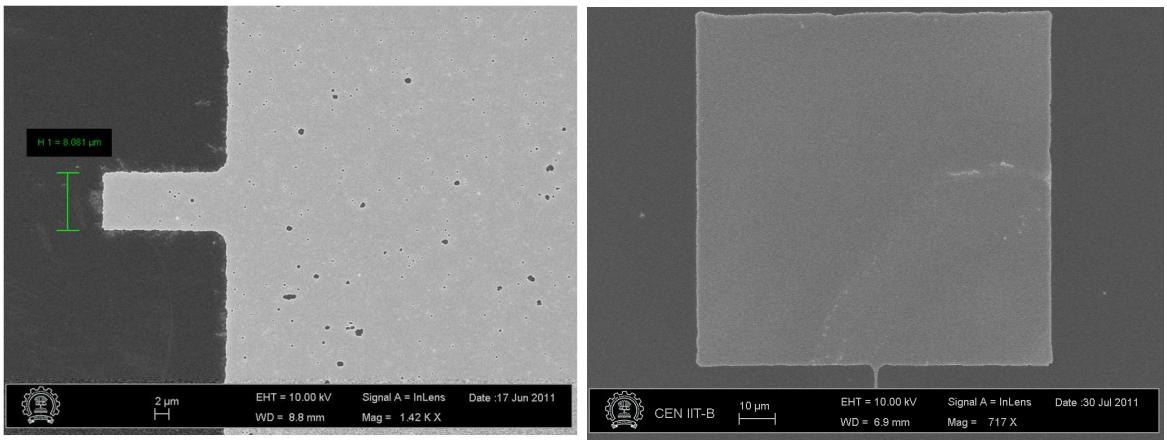


Figure 3.12: a) SEM image of TiN gate with pinholes b) SEM image of TiN gate with no pinholes

formed, as seen in Fig.3.12(a). After surface SEM inspections at different stages in the process, it became clear that the wet etchant of TiN attacks ICPCVD SiO_2 and thus reaches to the TiN underneath it. The C-V and I-V characteristics of such MOS capacitors are quite leaky. This leaky behaviour can be attributed to the presence of pinholes in TiN. To address this problem, a change in the process sequence is made. The resist which protects the hard mask SiO_2 is removed only after the wet etch of TiN. This helped in doing away with the pinholes, shown in Fig.3.12(b).

Experiments were carried out with process splits on deposition time of Al_2O_3 (30sec, 60sec, 90sec and 120sec) so as to identify the working recipe with the least Equivalent Oxide Thickness(EOT). But in all the experiments Al_2O_3 dielectric with 60sec deposition time gave reliable

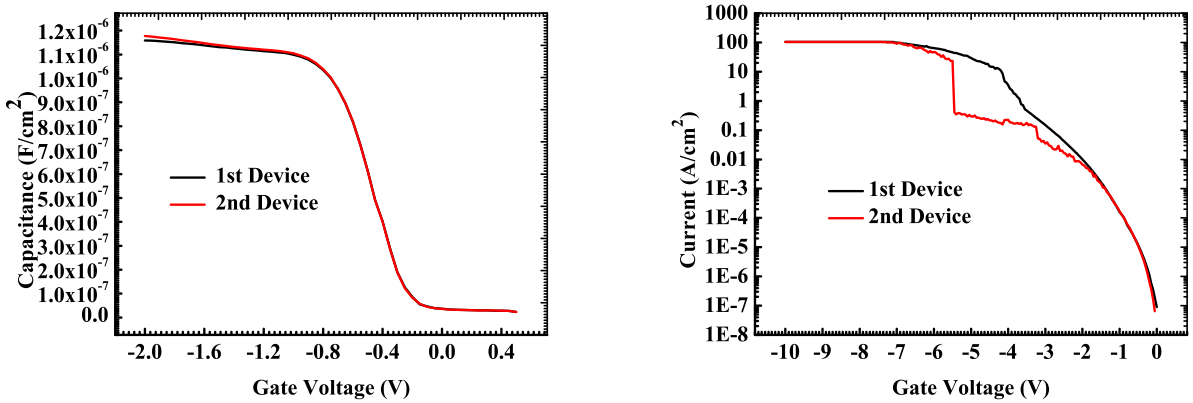


Figure 3.13: C-V , I-V (in accumulation only) of a TiN/Al_2O_3/Si MOSCAP with EOT = 2.95nm and substrate doping = 1 x 10^{15} – 1 x 10^{16} cm^{-3}

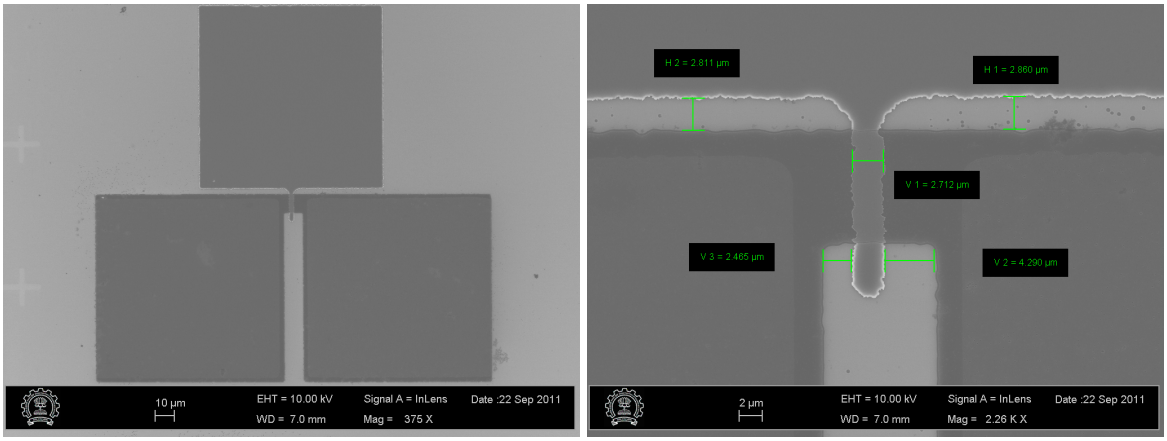


Figure 3.14: a) A surface SEM view of 2.7μm channel length n-channel BPJLT b) A magnified image of the same device

C-V characteristics. This 60sec recipe was freezed for the JLT fabrication then. The C-V and I-V data of two capacitor devices with 60sec Al_2O_3 deposition time is seen in Fig.3.13. The physical thickness of Al_2O_3 and its EOT are 4.15nm and 2.95nm respectively in this experiment. The breakdown field of the dielectric is $\sim$ 10 MV/cm.

3.3 Summary

The final device structure of BPJLT with shallow implant as device layer is depicted in Fig.3.14. The smallest gate length with a perfectly intact gate is 2.7μm. We also got devices with channel lengths less than 2μm but the gate fingers are disturbed at the points of non-planar topography. This usually happens with the wet etch and it should be more stringently timed. As pointed out in Section 3.2.3, the process conditions chosen for the shallow implant were not able to realize the device layer, there is no transistor behaviour seen in the structure shown in

Fig.3.14.

As an alternative to the shallow implant, poly-silicon, as a device layer, is proposed in the next two chapters. The process flow for the BPJLT fabrication remains more or less the same except for the replacement of shallow implant with a thin layer of n-type polysilicon.

Chapter 4

Back-Gated JLT – Poly-Silicon as Device Layer

4.1 Introduction

As the implant conditions we chose were not able to achieve a ultra shallow junction for the BPJLT process, we have explored the possibility for poly-silicon as an alternative channel material. Junction-less transistors with heavily doped poly-Si as nanowire have been recently investigated[13]. These transistors are seen as major drivers of innovation and growth in the flat panel electronics and other 3D IC applications.

When doping concentrations are identical, nanowires with smaller dimensions(width/thickness $\sim$ 25nm/10nm) demonstrate superior switching action(better I_{ON}/I_{OFF} ratio) than those with larger dimensions(width/thickness $\sim$ 75nm/35nm)[13]. Hence, as expected, the thickness of the poly-Si nanowire plays a crucial role in deciding the ON/OFF behaviour of a junction-less transistor. It has been reported in the literature that this idea can be demonstrated on planar thin film transistors(TFT), if the poly-silicon is sufficiently thin($\sim$ 10nm) and heavily doped($> 10^{19}$ cm^{-3})[14]. This chapter focuses on experiments leading to optimization of poly-Si device layer that can be later employed in the fabrication of BPJLT. Using this optimized poly-Si device layer, a simplified process flow for back-gated JLT has been developed and presented in the next section.The cross-section schematic of back-gated JLT is show in Fig.4.1.

Patterning the poly-Si device layer forms the crux of back-gated JLT fabrication. The CMOS active area mask, which was explained in Section 3.3.1 of Chapter 3, is employed in patterning the poly-Si device layer. The substrate, on which the device layer is built, behaves as the gate terminal and hence the name “back-gated" device. This process flow and experimental work is taken up to explore the possibility of BPJLT fabrication with poly-Si as device layer. We study the effectiveness of poly-Si as a device layer i.e. resistor action in the absence of gate field and

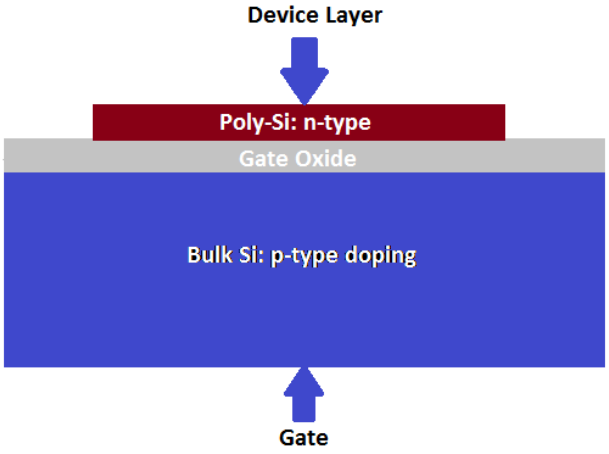


Figure 4.1: Cross-section schematic of back-gated JLT showing the substrate(blue), gate oxide(grey) and poly-Si device layer(dark red). Dimensions are not to scale

the effects of depletion in the presence of gate field.

There exist an uncertainty in the effective channel length of the back gated JLT. The substrate being the gate terminal, it overlaps with the entire poly-Si device layer. Technically, the gate sits over the source, channel region and drain in this transistor configuration. The gate-length is governed by the placement of probes on the source-drain pads. The distance between the two probe points(points where the probe tips touch the source and drain pads) defines the effective gate length.

4.2 Experimental Work

The fabrication process starts with the growth of gate dielectric on RCA cleaned wafers. Then a poly-Si layer is deposited and annealed at a high temperature for the activation purpose. Subsequently, the poly-Si device layer is patterned using CMOS active area mask. Finally back oxide etch and back side Aluminum metallization is done to complete the back-gated transistor flow.The 9 unit processes for the fabrication of back-gated JLT are listed in Table 4.1. Annexures, mentioned next to the corresponding headings, contain the process recipes and the equipment used in the fabrication process. The optimization experiments and the device characteristics are also explained in this section.

A 4 inch p-type silicon wafer with 0.02-0.04 ohm-cm resistivity and <100> orientation is the starting substrate material. Since the substrate is being used as the gate terminal, such low resistive(equivalent doping of 1 x 10^{18} – 2 x 10^{18} cm^{-3}) wafers are required. High dopings

Table 4.1: Major unit processes in the fabrication of Back-gated JLT

Module Defintion	Unit Processes	Process Details
1	RCA Clean	Annexure V
2	Gate Oxide (SiO_2) Growth	
Poly-Si Device Layer		Annexure V
3	N-Type Poly-Si deposition	
4	Rapid Thermal Annealing	
5	Active Area Lithography	
6	Dry Etch of Poly-Si	
7	Piranha Clean	
8	Backside Oxide Etch	Annexure V
9	Backside metallization (Al)	

ensure reduced gate resistance. After the RCA Clean, a gate oxide of 10nm is grown on these highly doped wafers in dry oxide furnace tube.

4.2.1 Poly-Si Device Layer Definition

The poly-Si device layer definition is the most important module of back-gated JLT process flow. The two stringent requirements for a poly-Si device layer – ultra-thin($\sim$ 10nm) and heavily doped($> 10^{19}cm^{-3}$). The experiment plan is to deposit an in-situ doped n-poly and anneal to check whether the doping meets the required specification and then scale the deposition time accordingly to suit the thickness requirement.

In-situ doped n-type poly-Si is deposited in AMAT polygen chamber at 700C using the gases SiH_4(85 sccm) and PH_4(120 sccm) for different deposition times. A control sample with a depostion time of 60 sec for the above-mentioned process conditions resulted in a thickness of $\sim$ 135nm(from SEM measurements). This control sample is annealed at 950C for 5 sec in N_2 ambient(1000 sccm). The sheet resistance map from the four-probe tool is shown in Fig.4.2.

From the mean sheet resistance of 151.17 Ω/square and the mean thickness of 135nm, the resistivity ρ of the film is calculated to be 2.04 mΩ-cm. Given the equation $1/\rho = q\mu N_D$, the product of mobility and poly-Si doping N_D can be extracted from the known values of ρ and q(1.6 x 10^{-19} C). The product μN_D turned out to be 3.06 x 10^{21} $V^{-1}cm^{-1}sec^{-1}$. The electron mobility in n-type bulk silicon at 300 K is reported to be $\sim$ 100 cm^2/Vs for a doping concentration of $10^{19}cm^{-3}$[15]. Given the fact that poly-Si films have lesser mobilities compared to that

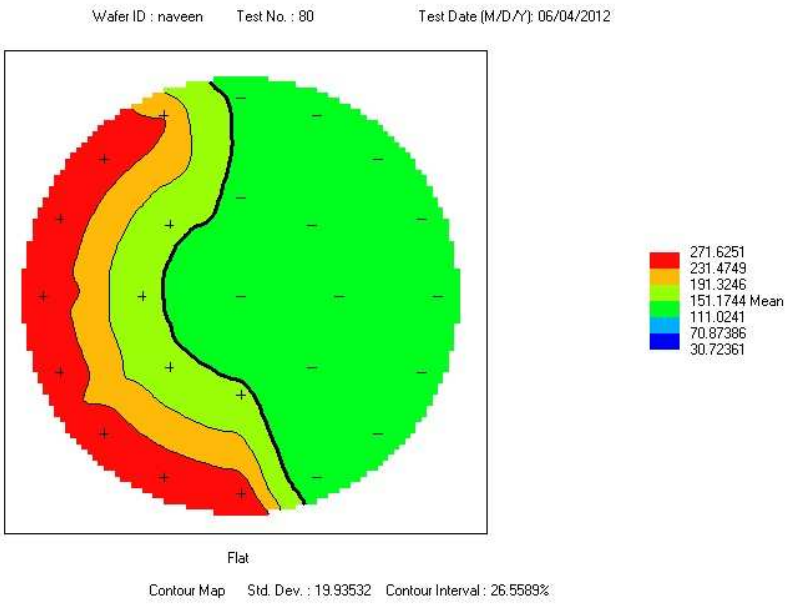


Figure 4.2: Sheet resistance map of 135nm thick n-type poly-Si annealed at 950C for 5 sec

of crystalline-Si and surface mobilities are lower than the bulk mobilities, due to surface scattering effects, it can be easily understood that the doping concentration of the deposited poly-Si film is greater than $10^{19}cm^{-3}$. This concentration meets the doping requirement of ultra-thin poly-Si channel based JLT.

Keeping the other process conditions fixed, experiments are performed with the splits in deposition times of n-type poly-Si − 5 sec, 7 sec, 10 sec and 15 sec on control samples. All these samples are subjected to anneal at 950C for 5 sec in N_2 ambient(1000 sccm). The poly-Si deposition times and their corresponding thicknesses are mentioned in Table 4.2. These thickness measurements are done after the rapid thermal anneal process.

From the data in Table 4.2, it is clearly evident that deposition times of 5 sec and 7 sec are the most suitable candidates for poly-Si thin film transistor. The cross-section SEM images of poly-Si(deposited for 5 sec and 7 sec) on grown SiO_2 are shown in Fig.4.3 and Fig.4.4 respectively. After optimizing the poly-Si deposition and anneal process conditions, lithography using CMOS active area mask is taken up. The mask gds and pad structure are discussed in Section 3.3.1 of Chapter 3. Dry etch of poly-Si is performed in STSRIE using CF_4 + O_2 chemistry. An over-etch is done to ensure that the poly-Si device layer is in clear contrast with the back-ground. The process conditions for all the above-discussed unit processes are included in Annexure V. Piranha clean, also mentioned in Section 3.3.1 of Chapter 3, is the final step in poly-Si device layer definition which is meant to remove the resist and remnant poly residues. The final SEM image after poly-Si device layer is patterned is depicted in Fig.4.5.

Table 4.2: Poly-silicon deposition times (in sec) and their thicknesses (in nm) as seen in SEM.

poly-Si deposition time	poly-Si thickness
5	10-14
7	15-18
10	23-27
15	38-44

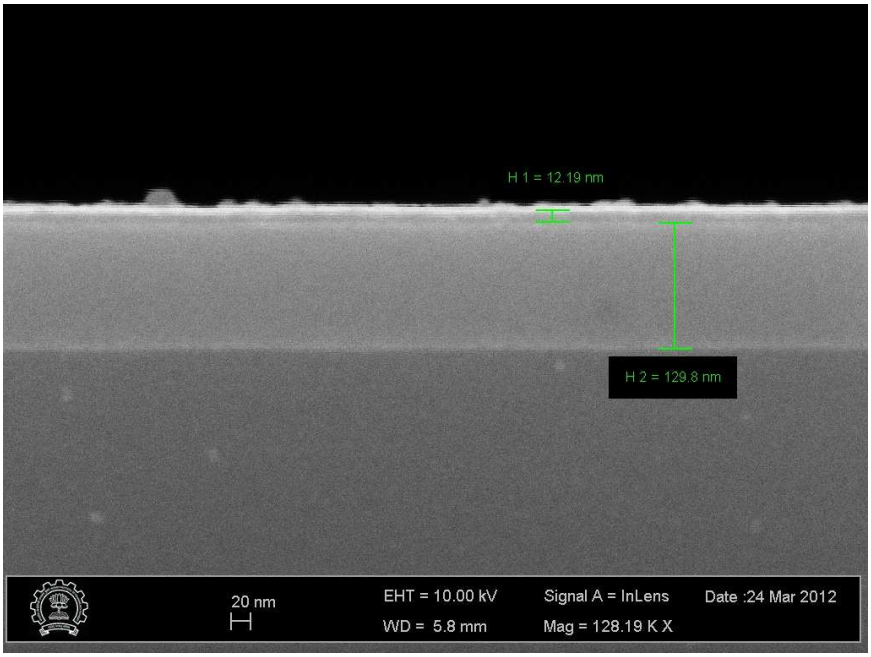


Figure 4.3: Cross-section SEM of poly-Si deposited for 5 sec on 130nm SiO_2

4.2.2 Poly-Si Device Layer: Other Experiments

Experiments are carried out to check the resistor action of the poly-Si device layer. Diode behaviour between the n-type poly-Si and the p-type Si substrate is also investigated. The test structure for all these experiments remains the same i.e. shown in Fig.4.5. The only difference is the absence of gate oxide. The in-situ doped poly-Si device layer directly sits on the p-type silicon wafer with 0.02-0.04 ohm-cm resistivity. The resistor behaviour of poly-Si device layer for different poly-Si deposition times $-$ 5 sec, 10 sec, 15 sec and 20 sec is shown in Fig.4.6(a) and Fig.4.6(b). Increase in poly-Si deposition time, which eventually leads to increase in device layer thickness, amounts to the decrease in resistance of the poly-Si wire. Though the 5 sec process recipe displays lesser drive current(a few μA), a thinner film is essential for a better I_{ON}/I_{OFF} ratio.

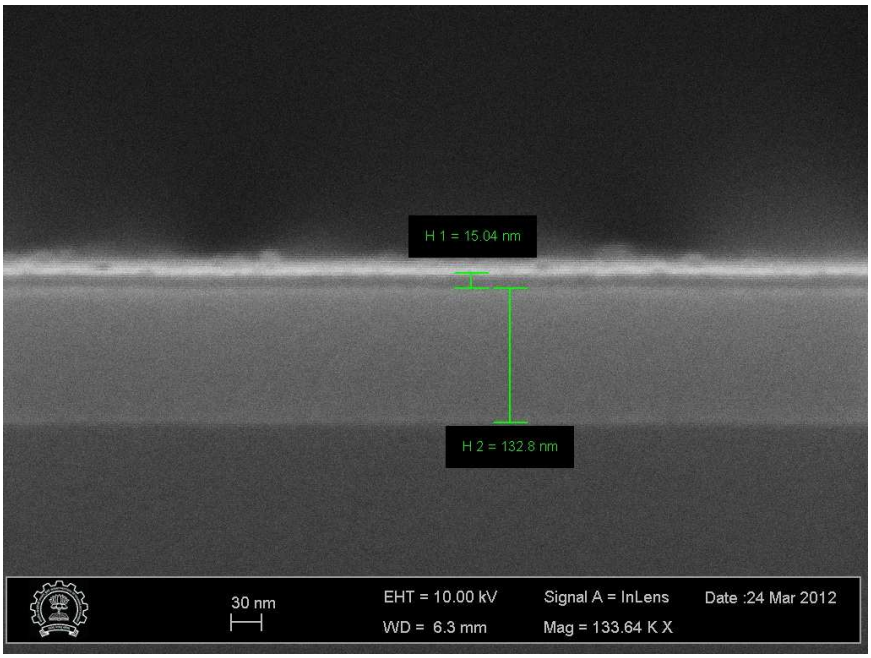


Figure 4.4: Cross-section SEM of poly-Si deposited for 7 sec on 130nm SiO_2

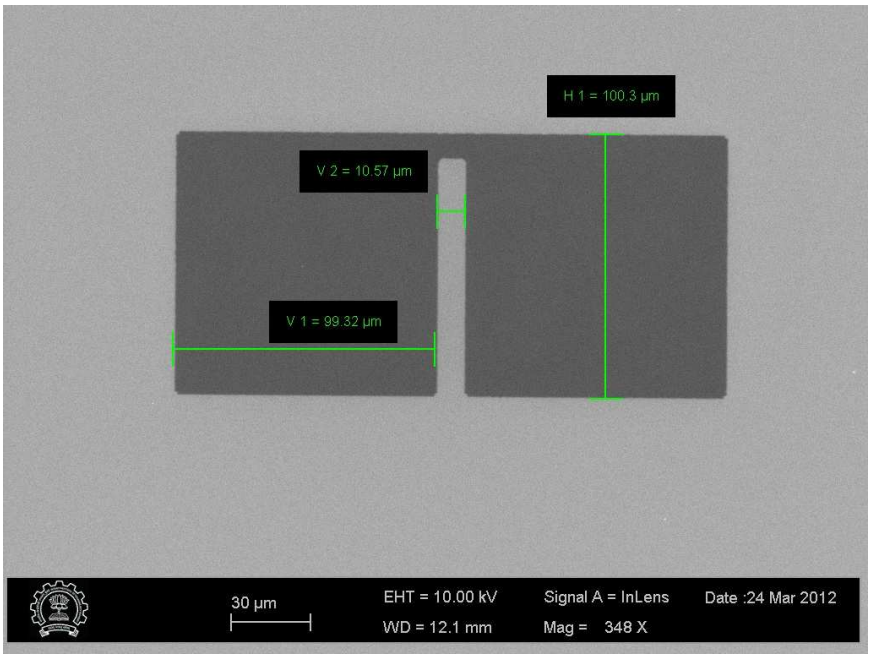


Figure 4.5: Surface SEM of poly-Si device layer patterned using CMOS active area mask

Fig.4.6(c) shows the log plots of the diode characteristics − n-type poly-Si with p-type Si. It is clearly apparent from Fig.4.6(c) that the reverse bias leakage current is significantly high. This can be attributed to the increased number of defects in poly-crystalline materials which act as generation and recombination centres and influnce basic device properties like mobility and minority carrier lifetimes. The fact that the poly-Si is ultra-thin ($\sim$ 10nm) and the uncertainity of the probe position in poly-Si have created further ambiguity in reasoning out. Using metal-contacts and low temperature anneal are perceived as two viable options to reduce the leakage

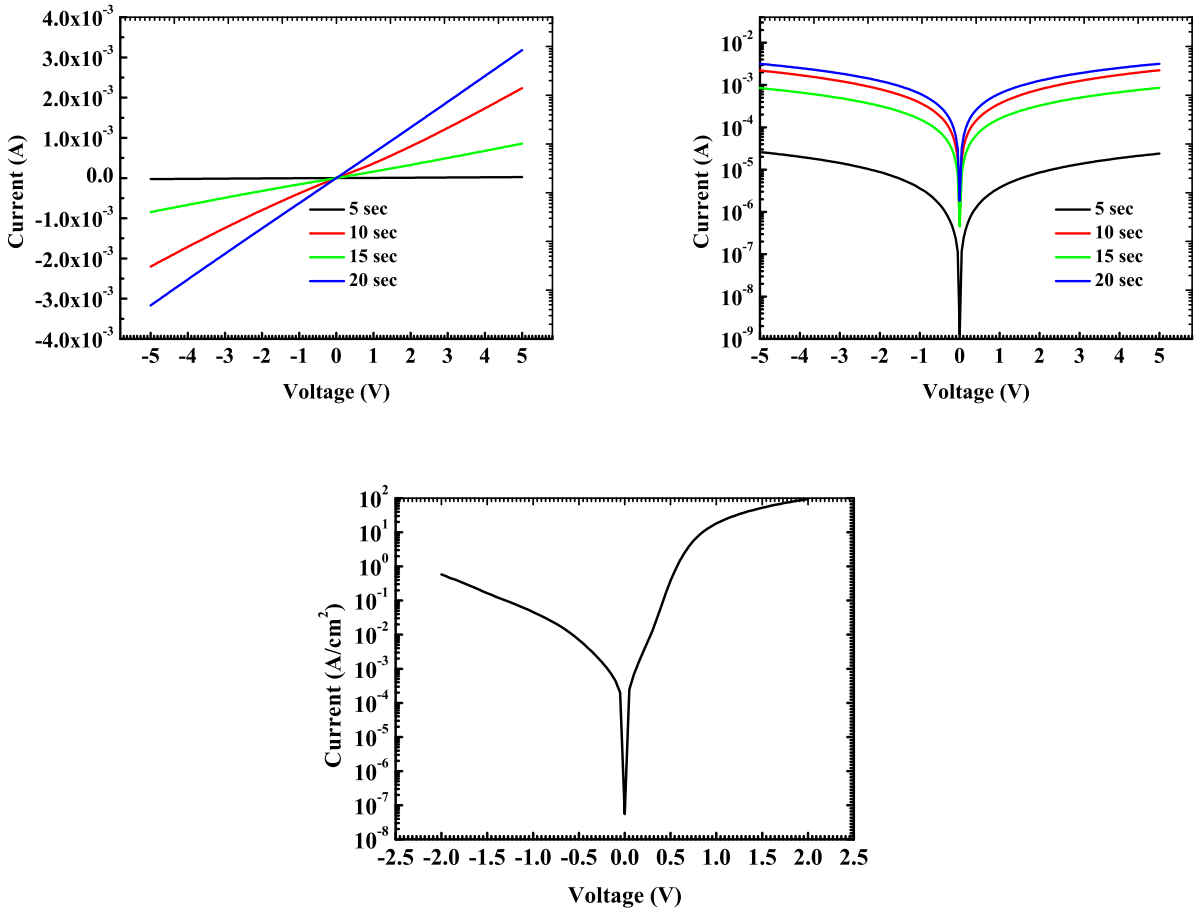


Figure 4.6: a) Resistor behaviour on a linear scale for poly-Si deposition times – 5 sec, 10 sec, 15 sec and 20 sec (top left) b) Resistor behaviour on a logarithmic scale for poly-Si deposition times – 5 sec, 10 sec, 15 sec and 20 sec (top right) c) Forward and reverse bias currents(log plots) for n-type poly-Si – p-type Si diode (bottom)

currents.

4.2.3 Back-gated JLT Characteristics

After the definition of poly-Si device layer, back-side oxide etch(using 2% HF) and back-side Aluminum metallization is done to wind up the fabrication process of back-gated JLT. As stated earlier, the transistor run is taken forward with splits on poly-Si deposition time - 5 sec and 7 sec. The back-gated poly-Si MOS capacitor C-V and I-V data is presented in Fig.4.7. The oxide thickness(T_{OX}) extracted from C-V plots is $\sim$ 11nm which is quite consistent with the SEM images and ellipsometry measurements(immediately after SiO_2 growth). From the I-V plot in Fig.4.7, it is evident that the devices breakdown beyond a gate bias of -7V.

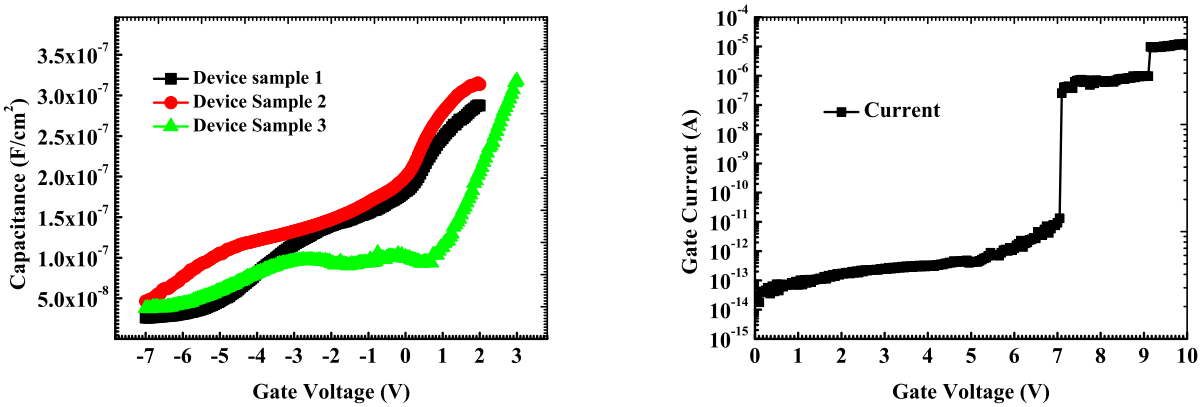


Figure 4.7: C-V and I-V measurements of back-gated poly-Si MOS capacitor

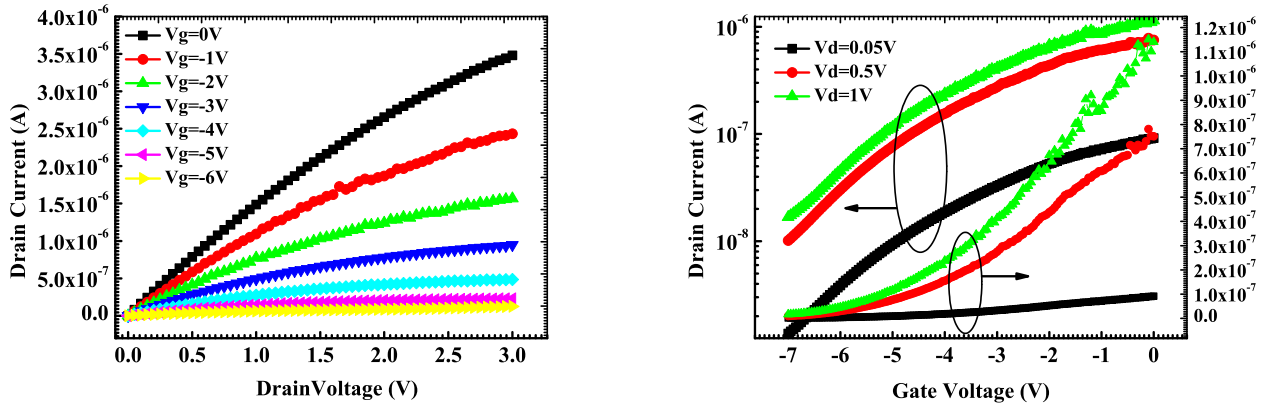


Figure 4.8: $I_D - V_{DS}$ and $I_D - V_{GS}$ of back-gated JLT with poly-Si deposition time as 5 sec

The $I_D - V_{GS}$ and $I_D - V_{DS}$ of back-gated poly-Si JLT are depicted in Fig.4.8 and Fig.4.9, for a poly-Si device layer with deposition time as 5 sec and 7 sec respectively. The chosen gate length, which is the distance between source and drain probes, is $\sim 30\mu$m in both the cases. The I_{ON}/I_{OFF} ratio is around 10^2 in the 5 sec deposition case and is more worse in the 7 sec deposition case. Comparison of I-V characteristics of both deposition times is presented in Fig.4.10. An interesting observation in this regard is that the 7 sec sample shows higher ON current but suffers from lower I_{ON}/I_{OFF} ratio when compared to 5 sec sample. This calls for careful tailoring of device layer thickness given the trade-off between the two important metrics.

Now that the decent I_{ON}/I_{OFF} ratio is achieved in 5 sec case, to provide a further boost an experiment is planned with poly-Si deposition time as 4 sec. To enhance the gate control, the gate dielectric thickness has been reduced to $3.5 - 4$nm. The rest of the process parameters and the sequence of the process flow is kept the same as previous run. The I-V characteristics of this experiment are shown in Fig.4.11. The effective gate length is kept same as that of previous experiment($\sim 30\mu$m). The most exciting aspect of the new run is the massive improvement in

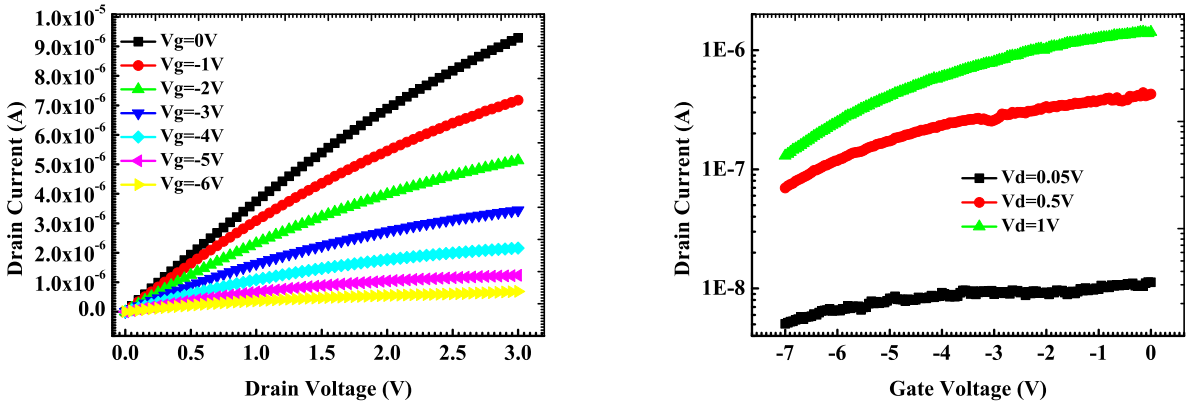


Figure 4.9: $I_D - V_{DS}$ and $I_D - V_{GS}$ of back-gated JLT with poly-Si deposition time as 7 sec

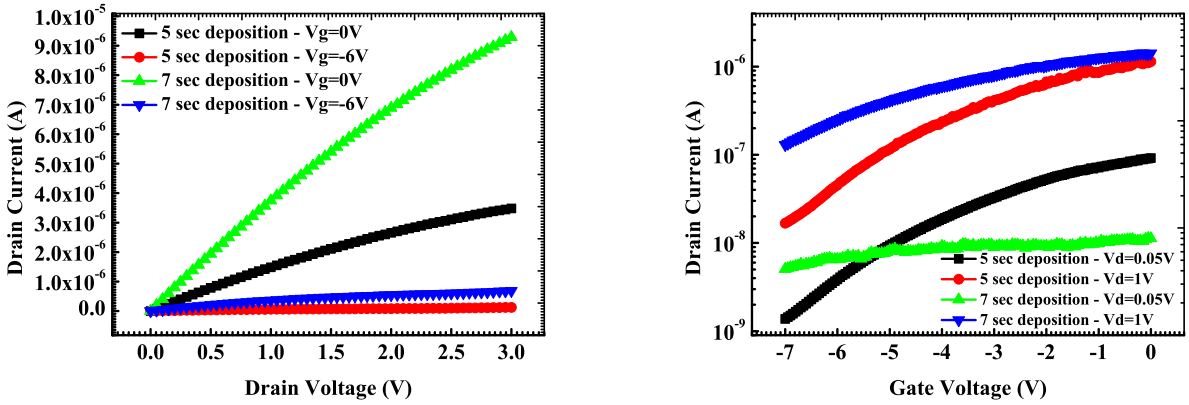


Figure 4.10: Comparison of I-V characteristics of back-gated JLTs with poly-Si deposition time as 5 sec and 7 sec

I_{ON}/I_{OFF} ratio to 10^5.

4.3 Summary and Future Scope

Besides optimising a process for thin poly-Si device layer, which is meant to be integrated into poly-Si BPJLT, a back-gated JLT device is also fabricated. Optimization procedure required a few runs to ensure the repeatability of poly-Si deposition process. Once the device layer is ready, another set of runs have been taken up changing different device parameters at different points in the process flow. The future scope in the back-gated JLT revolves around 3-level mask process. Two additional mask steps are introduced to ensure metal contacts on the poly-silicon pads. This will help in improving the I-V characteristics due to reduced contact resistance. The process of fine tuning the metal contact stack is currently in progress. Once the contacts are ready, better I_{ON}/I_{OFF} figures can be expected.

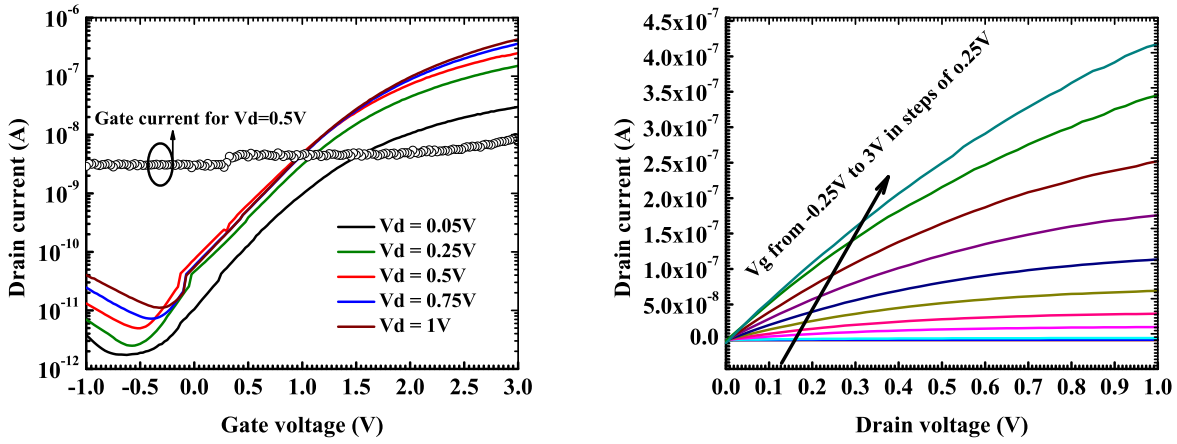


Figure 4.11: I-V characteristics of back-gated JLTs with poly-Si deposition time as 4 sec and and gate oxide as 4nm

Chapter 5

BPJLT – Poly-Silicon as Device Layer

5.1 Introduction

Poly-silicon device layer process flow and the corresponding characteristics are discussed in Chapter 4. The ultimate goal is to integrate that poly-Si device layer into the Bulk Planar Junction-Less Transistor fabrication. As stated earlier, this poly-Si device layer emerged as a suitable replacement for shallow implant which failed the BPJLT process(refer to Chapter 3). The unique aspect of this chapter is the BPJLT fabrication procedure utilises the process modules which are already defined in Chapter 3 and Chapter 4. Only the integration aspects and the problems that have come up are explained in this chapter.

One notable difference in poly-Si BPJLT process is the absence of probe area definition. The n-type poly-Si exhibited identifiable(not reasonably good) diode behaviour with p-type Si(as pointed out in Section 4.3.2 of Chapter 4) inspite of the fact that the poly-Si is very thin($\sim$ 10nm). This led to omission of probe area definition from the poly-Si BPJLT process flow. However, integration of metal contact stack deemed necessary to obtain reasonably good I-V characteristics. The experiment plan is to fabricate a basic version of poly-Si BPJLT and then improve the I-V behaviour by integrating metal contacts at a later point. The cross-section schematic of poly-Si BPJLT is shown in Fig.5.1. The process flow for realizing the schematic in Fig.5.1 is mentioned in Table 5.1. Annexures, mentioned next to the corresponding headings, contain the process recipes and the equipment used in the fabrication process.

In terms of process complexity, the fabrication continues to be a three mask process though the probe area definition opted out. The poly-Si device layer definition called for an additional mask wherein the patterned poly-Si has to exactly sit on the defined active area. The task of aligning poly-silicon device layer with active area is very challenging as the acceptable room for misalignment is very less. The gate area lithography in the subsequent stage, which is bound to

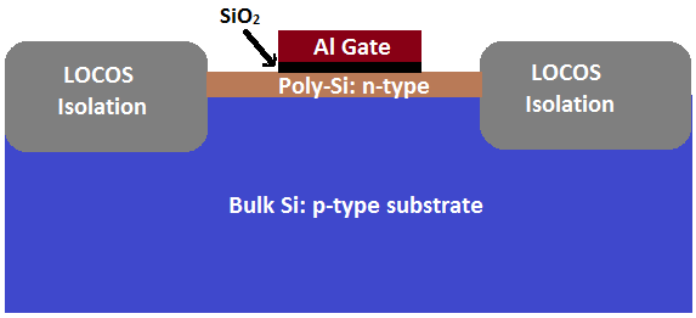


Figure 5.1: Cross-section schematic of poly-Si BPJLT showing the substrate(blue), LOCOS(grey), poly-Si device layer(brown), SiO_2(black) and Al gate(dark red). Dimensions are not to scale

introduce some misalignment, made the criteria more strigent. The plan is to limit the maximum misalignment at the poly-Si definition stage to less than 1μm. The other major observation in the process flow is to replace TiN-Al_2O_3 gate stack with Al-SiO_2. This change is necessitated by the etching concerns between the TiN-Al_2O_3 stack and n-type poly-silicon. A low temperature oxide(SiO_2) is used as a gate dielectric and Aluminum is used as a gate terminal.

5.2 Experimental Work

The fabrication process starts with creating device isolations using standard Local Oxidation of Silicon(LOCOS) process. Then poly-Si is deposited and annealed at a high temperature for the activation purpose. Subsequently, the poly-Si device layer is patterned using CMOS active area mask. Finally a gate stack is deposited and patterned to form a transistor. The entire fabrication process is broadly categorized into three modules: Active area definition, Poly-Si device layer definition, and Gate stack definition. The major unit processes in each of the three modules are listed in Table 5.1. This process flow looks similar to the shallow implant BPJLT(in Chapter 3) except for the poly-Si device layer in place of shallow junction definition.

The active area definition, which comprises a sequence of unit steps numbered 1 to 6, is already discussed in Section 3.3.1 of Chapter 4. The “Bird‘s Beak" structure and surface topology images are also covered in the same section. The poly-Si device layer definition, which include steps numbered 7 to 11, is explained in Section 4.3.1 of Chapter 4. The effectiveness of poly-Si to be qualified as semiconductor device layer is detailed in the same section. The integration of poly-Si device layer on the active area is shown in Fig.5.2. From the Fig.5.2 it is clear that the challenge of minimizing the misalignment has been successfully met.

The next step in the fabrication process is the integration of gate stack. On integrating the

Table 5.1: Major unit processes in the fabrication of Poly-silicon BPJLT

Module Defintion	Unit Processes	Process Details
Active Area		Annexure I
1	RCA Clean	
2	Pad Oxide (SiO_2) Growth and Si_3N_4 Deposition	
3	Active Area Lithography	
4	Dry Etch of Si_3N_4	
5	Field Oxide (SiO_2) Growth	
6	Wet Etch of Si_3N_4	
Poly-Si Device Layer		Annexure V
7	N-Type Poly-Si deposition	
8	Rapid Thermal Annealing	
9	Active Area Lithography	
10	Dry Etch of Poly-Si	
11	Piranha Clean	
Gate Stack		Annexure VI
12	SiO_2 by Chemical Vapour Deposition	
13	Aluminum by Thermal Evaporation	
14	Gate Area Lithography	
15	Wet Etch of Aluminum	
16	Backside Oxide Etch	
17	Backside metallization (Al)	

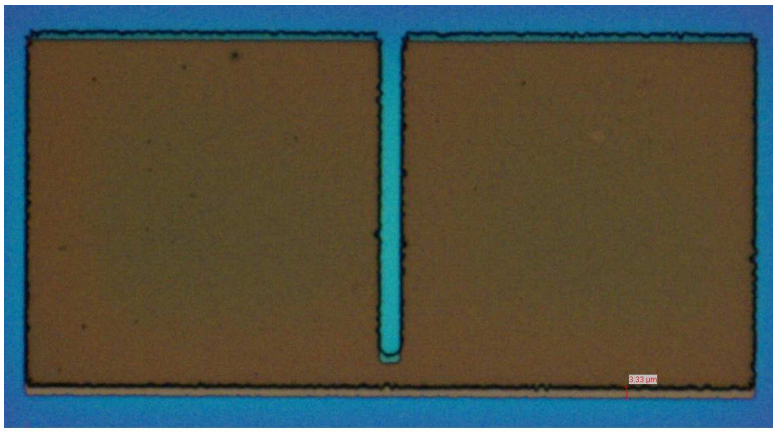


Figure 5.2: Microscopic image of poly-silicon device layer aligned with active area

TiN-Al_2O_3 gate stack, discussed earlier in Section 3.3.4 of Chapter 3, it was noticed that the wet etchant for TiN(NH_4OH:H_2O_2:H_2O in the ratio 1:2:7) ended up etching the Al_2O_3 and the underlying poly-silicon. The microscopic image after integration of TiN-Al_2O_3 stack is shown

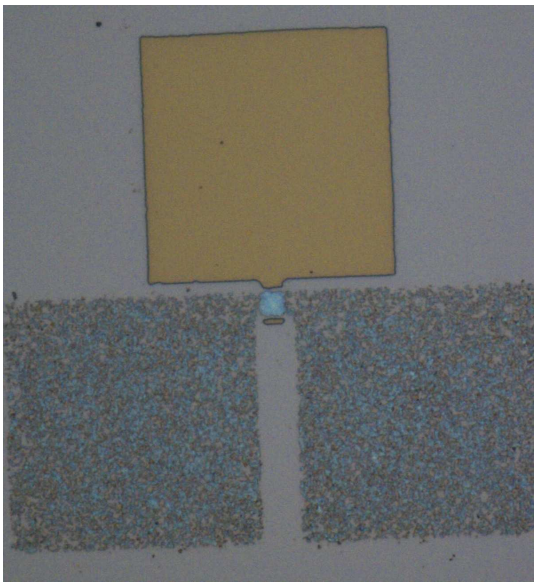


Figure 5.3: Microscopic Image of poly-Si BPJLT with TiN-Al_2O_3 gate stack. Poly-silicon pads are corroded by the wet etchant of TiN

in Fig.5.3. Having decided that TiN-Al_2O_3 stack is not a suitable candidate for poly-Si BPJLT, Al-SiO_2 gate stack is proposed. The wet etchant for Al(H_3PO_4:CH_3COOH:HNO_3:H_2O in the ratio 16:1:1:2), which is very selective to SiO_2, poly-Si and photo resist(S1813), turned the game in the favour of Aluminum gate.

Before integrating the Al-SiO_2 gate stack into poly-Si BPJLT process, MOS capacitors are fabricated using the same stack on p-type Silicon. The microscopic image of Al MOS capacitor is shown in Fig.5.4. The C-V and I-V data of four capacitor devices(with 100μm x 100μm dimensions) is seen in Fig.5.5. The oxide thickness T_{OX} extracted from C-V curves falls in the range 3.8-4.3nm. The extracted T_{OX} is consistent with the ellipsometry data taken after deposition of SiO_2(for 60 sec). The process conditions for Al-SiO_2 gate stack mentioned in Table 5.1 are presented in Annexure VI. The breakdown field of the SiO_2 turned out to be $\sim$ 13 MV/cm.

The Al-SiO_2 gate stack is then integrated into the poly-Si BPJLT process. The surface image of the 10μm gate length poly-Si BPJLT after the Aluminum etch is shown in Fig.5.5. The microscopic image in Fig.5.6 is inspected just before the resist removal and hence particle like structures are visible on the gate pad. Despite successful fabrication, there is no transistor action seen in the device. Troubleshooting started with MOS capacitor structures found on the die. Surprisingly unlike the Al/SiO_2/p-type Si, the Al/SiO_2/poly-Si MOS capacitor failed to give reliable C-V and I-V data. The C-V and I-V data of two capacitor devices(with 100μm x 100μm dimensions) is seen in Fig.5.7.

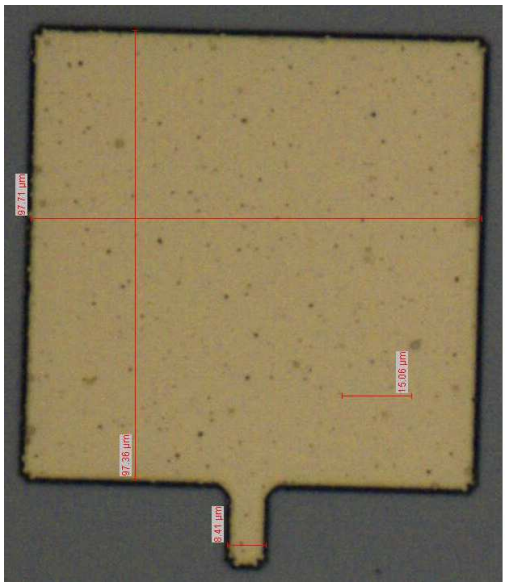


Figure 5.4: Microscopic image of Al gate MOS capacitor

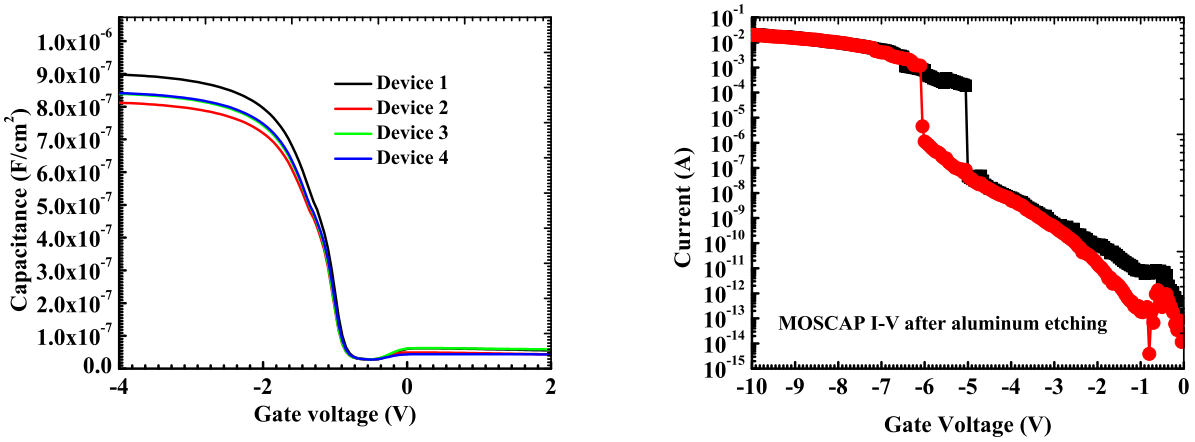


Figure 5.5: C-V and I-V (in accumulation only) of a Al/SiO_2/Si MOSCAP with EOT = 4nm and substrate doping = 1 x 10^{15} – 1 x 10^{16} cm^{-3}

After multiple experiments with Al/SiO_2 on thick poly-Si and thin poly-Si, it is suspected that the roughness of poly-Si played the spoilsport. The interface of the poly-Si with LTO is not the ideal expected one probably because of the roughness of poly-Si. The next course of action is to check the surface roughness in Atomic Force Microscope(AFM) for a thick poly-Si test structure. A 150nm thick n-type poly-Si is deposited at 700C and annealed at 950C for 5sec in 1000 sccm of N_2 ambient. This process recipe is the same one which is used for poly-Si device layer definition in Chapter 4, except for the increased deposition time. A 10μm x 10μm area in the centre of the poly-Si wafer is chosen for the AFM inspection. The 3D AFM image and the histogram shown in Fig.5.8 further confirmed the hypothesis. The x-axis of the histogram represents the peak roughness encountered at a sample point on the wafer. The y-axis of the histogram represent number of sample points at a particular peak roughness. The average

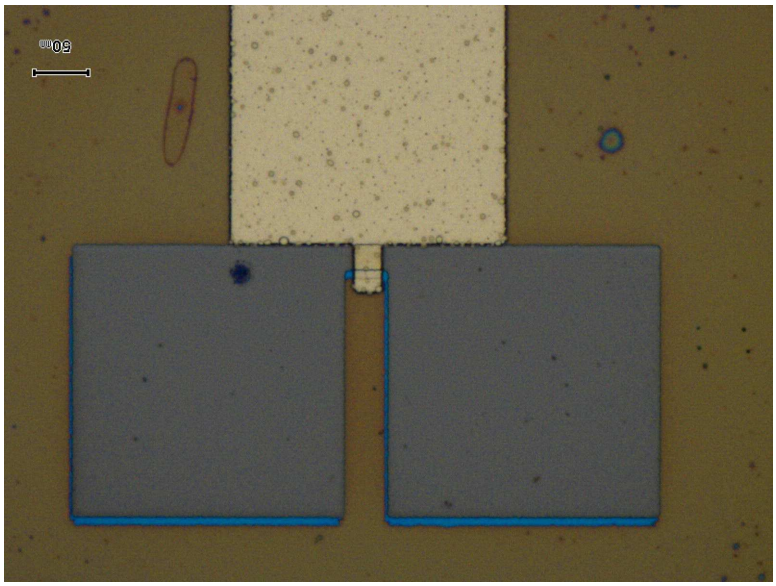


Figure 5.6: Microscopic image of 10μm gate length poly-Si BPJLT after the Al gate etch

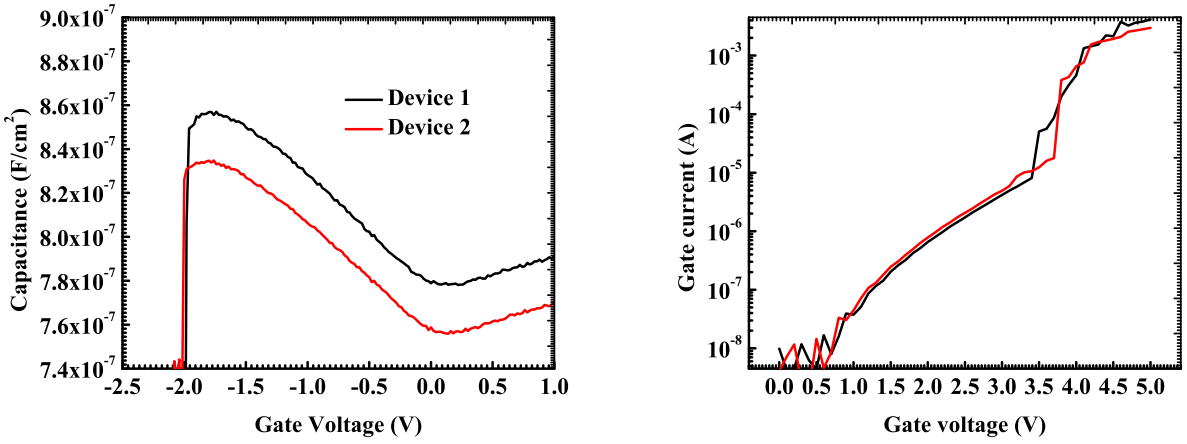


Figure 5.7: C-V and I-V (in accumulation only) of a Al/SiO_2/poly-Si MOS capacitor

roughness for this sample turned out to be $\sim$ 50nm. A smoother interface between poly-Si and gate oxide is required to ensure the appropriate capacitor and thereby transistor behaviour.

5.3 Summary and Future Scope

The finetuning of poly-Si deposition and activation anneal processes, inorder to achieve a smooth interface between poly-Si and gate oxide, is currently underway. A Al/SiO_2/poly-Si MOS capacitor with the C-V, I-V on expected lines would complete the job as the other process modules are already optimized.

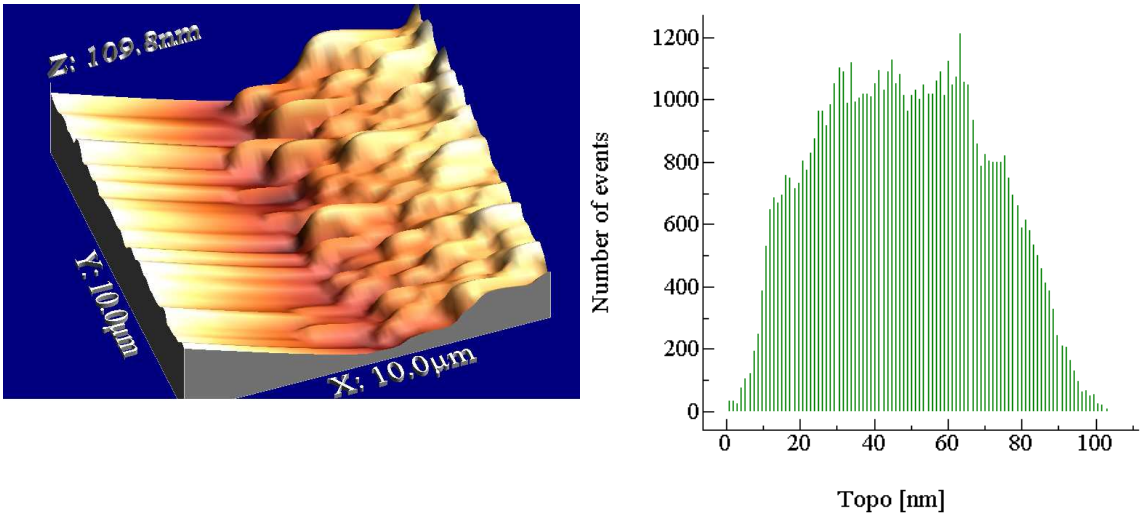


Figure 5.8: a) 3D AFM image of poly-Si in a 10μm x 10μm area b) Histogram of no. of sample points vs peak roughness in a 10μm x 10μm area

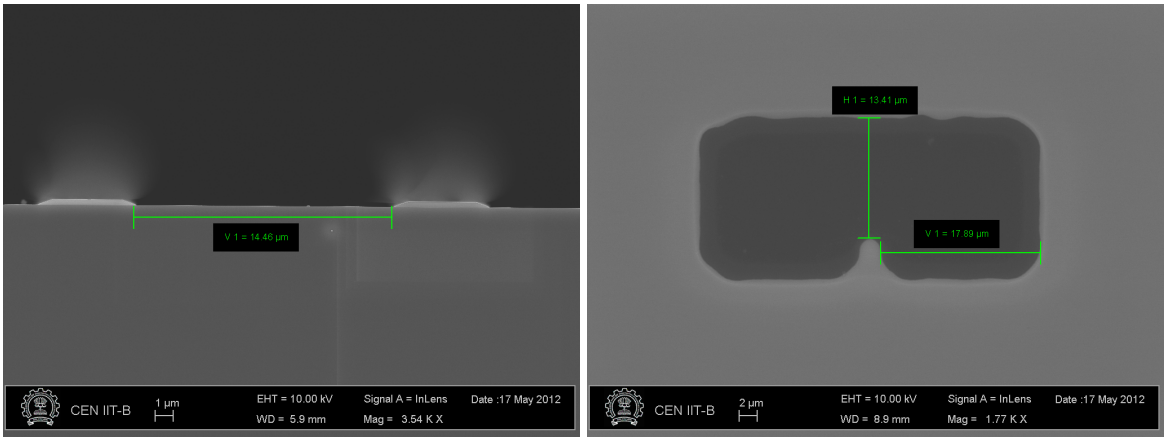


Figure 5.9: a) SEM cross-section of two isolations separated by active area b) surface SEM of 15μm x 15μm active area pads

Meanwhile, there is another process flow in the pipeline which relies on epitaxially grown Si as an active device layer. The schematic of the BPJLT device cross-section with p-type epitaxially grown layer looks exactly like Fig.2.4 except for the device layer being p-type and epitaxially grown. The requirements for the epitaxially grown layer remains the same as that of poly-Si device layer($\sim$ 10nm and doping > 10^{19} cm^{-3}). Like any BPJLT process, the device isolation is fabricated in the first step. This process uses a field oxide(FOX) isolation instead of a standard LOCOS process. FOX isolation is created by growing 300nm thick SiO_2 on RCA cleaned n-type Si wafers and patterning with CMOS active area mask. The SEM cross-section of two isolations separated by active area is shown in Fig.5.9(a).The surface SEM of 15μm x 15μm active area pads is presented in Fig.5.9(b).

These wafers, with oxide isolation, are sent to Stuttgart University, Germany for epitaxial growth. Once the wafers arrive from Germany, further processing can be taken up.

Chapter 6

NMOS Transistor – Fabrication and Characterization

6.1 Introduction

This chapter discusses the fabrication of an NMOS transistor using standard CMOS process flow. A team of few students are actively involved in this project specializing in photolithography, etching, depostion and anneal processes. The objective of this transistor fabrication is to provide recipes for baseline processes which are utilized as fundamental building blocks in many research activities, like junction-less transisitor, at CEN. My role in this project is to integrate all the unit processes and succefully fabricate the NMOS device. The NMOS fabrication is a two mask process, one for active area and the other for gate area definition. The device isolations are created using the standard LOCOS process. Grown silicon dioxide, which has the advantage of providing best interface with crystalling-Si substrate, is used as the gate dielectric. A gate first process is taken up to grab the advantage of self-aligned source and drain junctions.

6.2 Experimental Work for Long-Channel NMOS

The entire fabrication process is broadly summarised into three sections: Active area definition, Gate area definition and Source-Drain Engineering. The 18 major unit processes are listed in Table 3.1 under their respective headings. Annexures, mentioned next to the corresponding headings, contain the process recipes and the equipment used in the fabrication process. After the completion of the fabrication process, it was noticed that a particular 10μm feature on the mask manifested as 8.9μm on the die. Similarly a few 3μm and 2μm features turned up as 2.5μm and 1.2μm respectively.

Fig.6.1(a) shows the surface SEM of 8.9μm gate length NMOS transistor. The magnified view of the same device is shown in Fig.6.1(b). The $I_D - V_{GS}$ and $I_D - V_{DS}$ characteristics

Table 6.1: Major unit processes in the fabrication of long-channel NMOS transistor

Module Defintion	Unit Processes	Process Details
Active Area		Annexure I
1	RCA Clean	
2	Pad Oxide Growth and Si_3N_4 Deposition	
3	Active Area Lithography	
4	Dry Etch of Si_3N_4	
5	Field Oxide (SiO_2) Growth	
6	Wet Etch of Si_3N_4	
Gate Stack		Annexure VII
7	RCA Clean	
8	Gate Oxide (SiO_2) Growth	
9	In-situ Doped N+ Poly-Si Deposition	
10	Thermal Activation of N+ Poly-Si	
11	Backside N+ Poly-Si Etch	
12	Gate Area Lithography	
13	Dry Etch of N+ Poly-Si	
14	Piranha Clean	
Source-Drain Engineering		Annexure VIII
15	BEL Source-Drain Implant	
16	Rapid Thermal Anneal for Implant Activation	
17	Backside Oxide Etch	Annexure VIII
18	Backside metallization (Al)	
19	Forming Gas Anneal	

are shown in Fig.6.2. They former is scaled to the units uA/um and the latter to A/um. Also shown in the figure are the current components of source, drain, gate and bulk. It is clear from the figure that the source current follows the drain current in the entire voltage spectrum except for voltages less than V_T. For the sub-threshold region, the drain current traces the bulk current which is very much a standard manifestation of Gate Induced Drain Leakage(GIDL). Techniques like reducing source-drain overlap with the gate helps to contain this current.

The magnified view of the 2.5μm device is shown in Fig.6.3. The $I_D - V_{DS}$ and $I_D - V_{GS}$ characteristics are shown in Fig.6.4. Similar observations were made regarding the leakage currents i.e. drain currents less than threshold voltage.

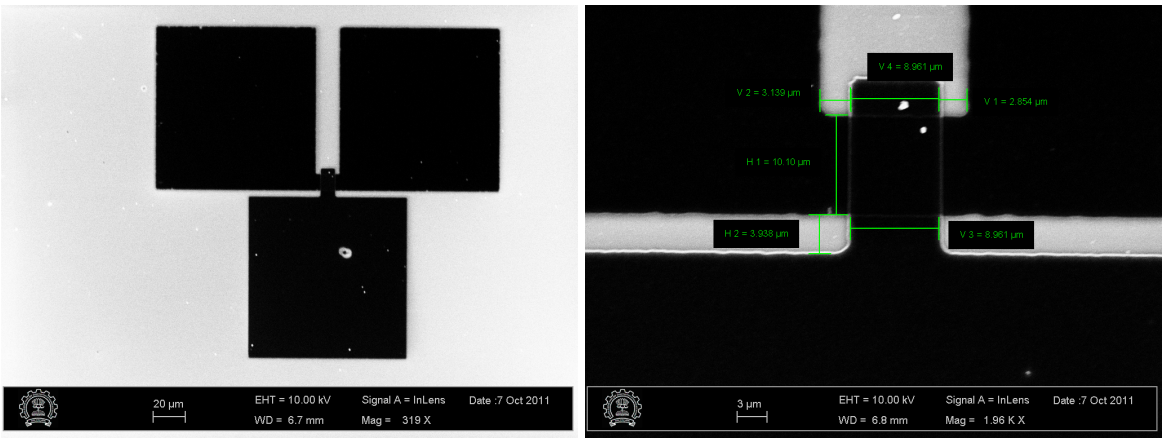


Figure 6.1: a) Surface SEM of 8.9μm gate length NMOS transistor b) Magnified view of the same device

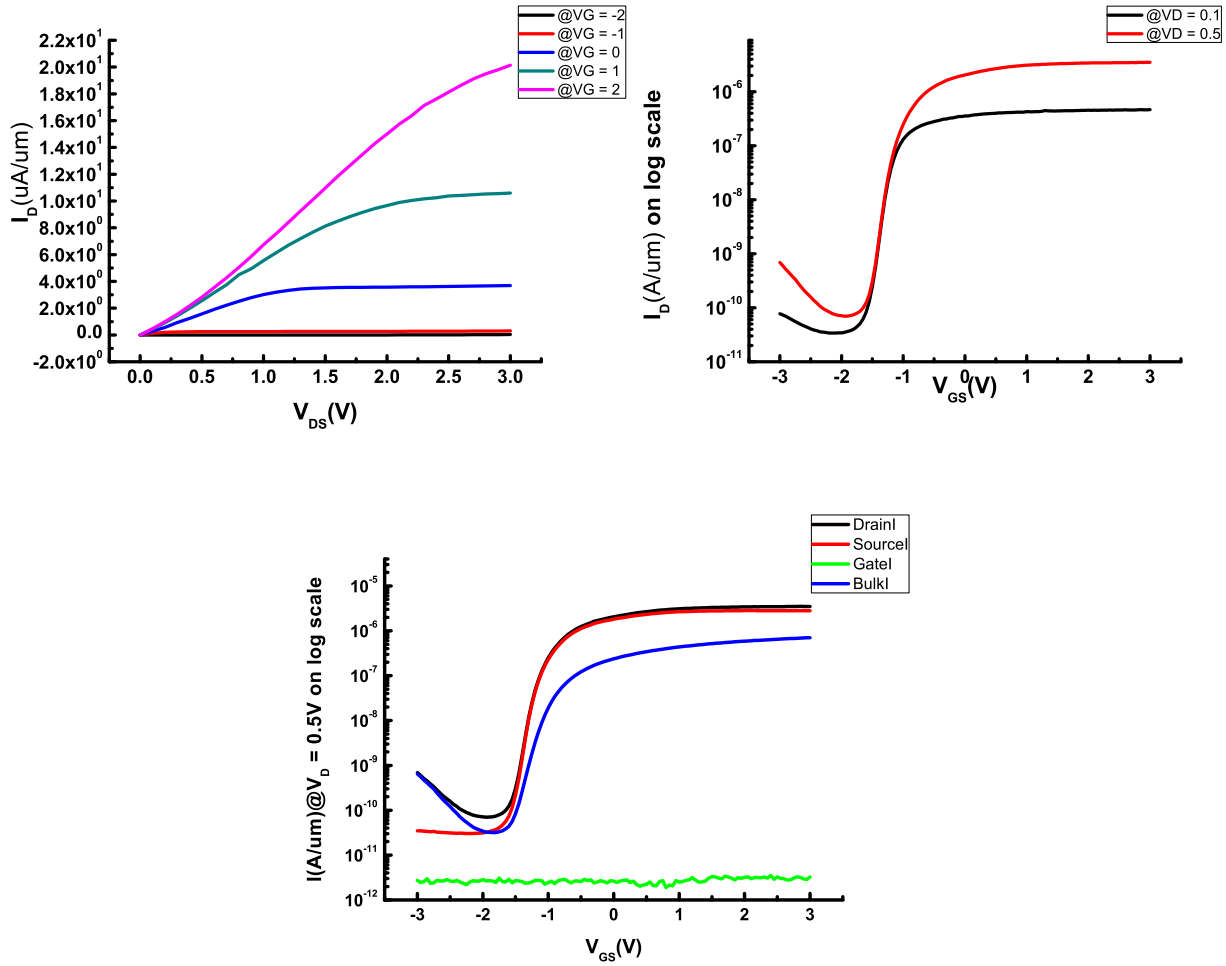


Figure 6.2: For a 8.9μm gate length NMOS a) $I_D - V_{DS}$ (top left) b) $I_D - V_{GS}$ on log scale (top right) c) I_D, I_S, I_B and I_G as a function of V_{GS} for V_D = 0.5V (bottom)

The magnified view of the 1.5μm device is shown in Fig.6.5. The$I_D - V_{DS}$ and $I_D - V_{GS}$ characteristics are shown in Fig.6.6. The GIDL component clearly dominates the gate-to-drain

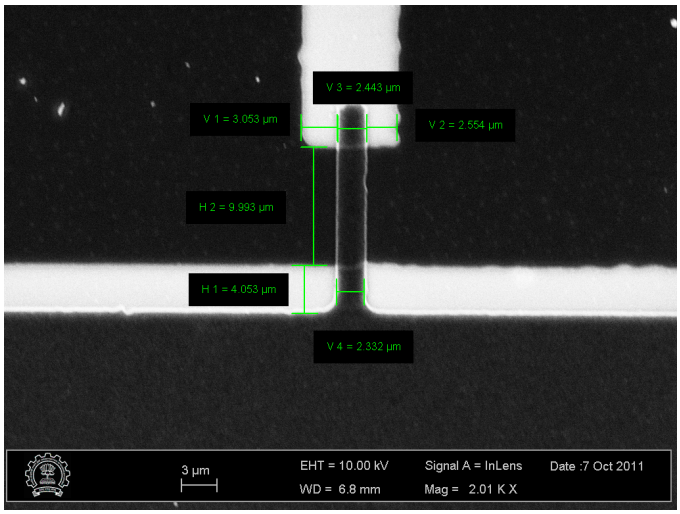


Figure 6.3: Surface SEM of 2.5μm gate length NMOS transistor

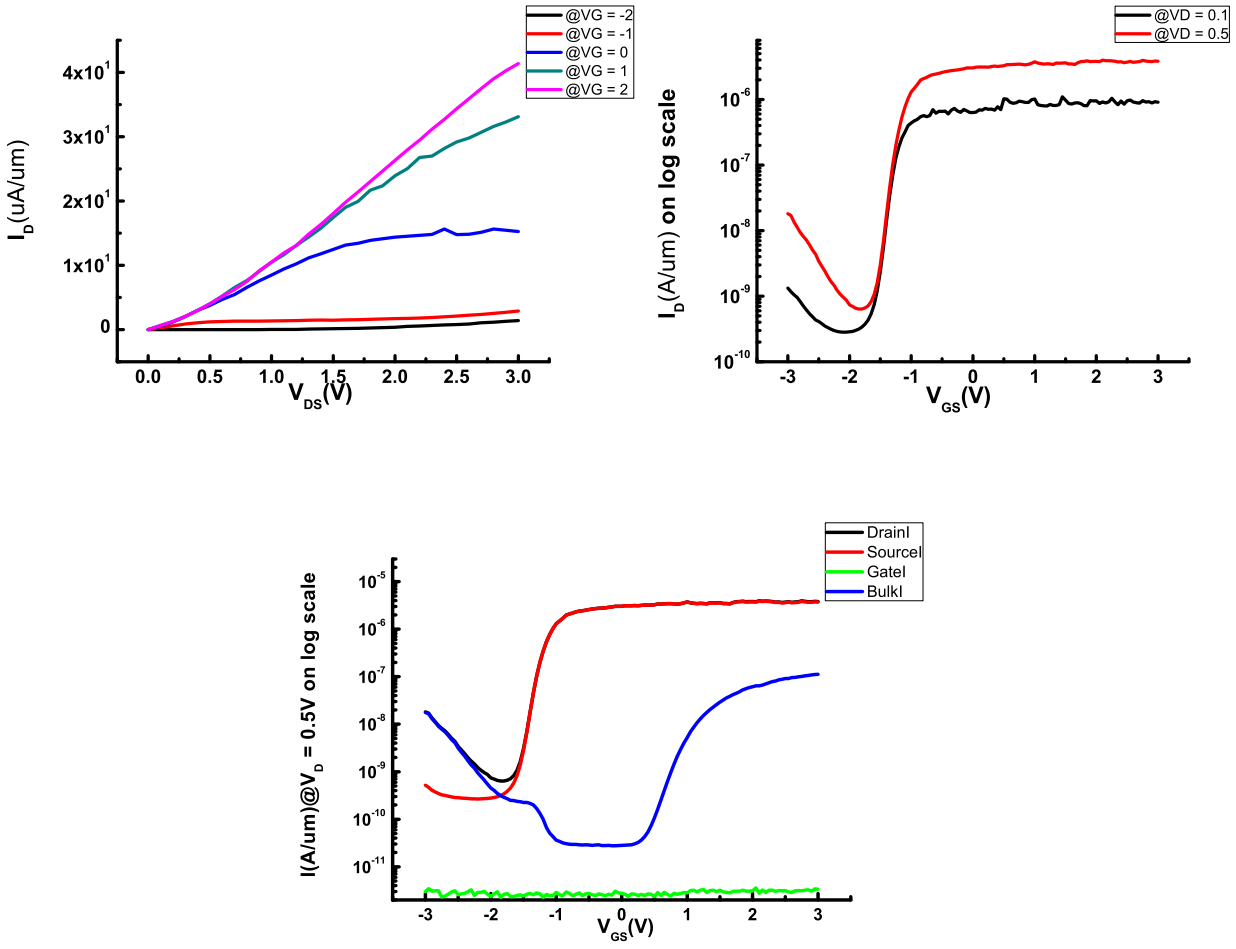


Figure 6.4: For a 2.5μm gate length NMOS a) $I_D - V_{DS}$ (top left) b) $I_D - V_{GS}$ on log scale (top right) c) I_D, I_S, I_B and I_G as a function of V_{GS} for V_D = 0.5V (bottom)

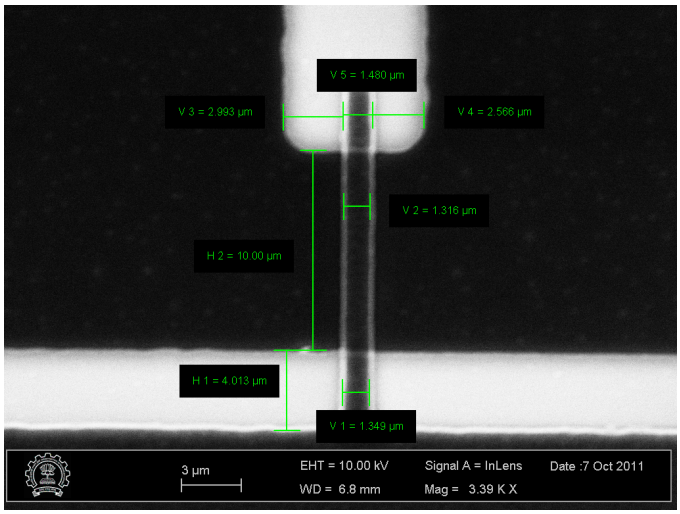


Figure 6.5: Surface SEM of 1.5μm gate length NMOS transistor

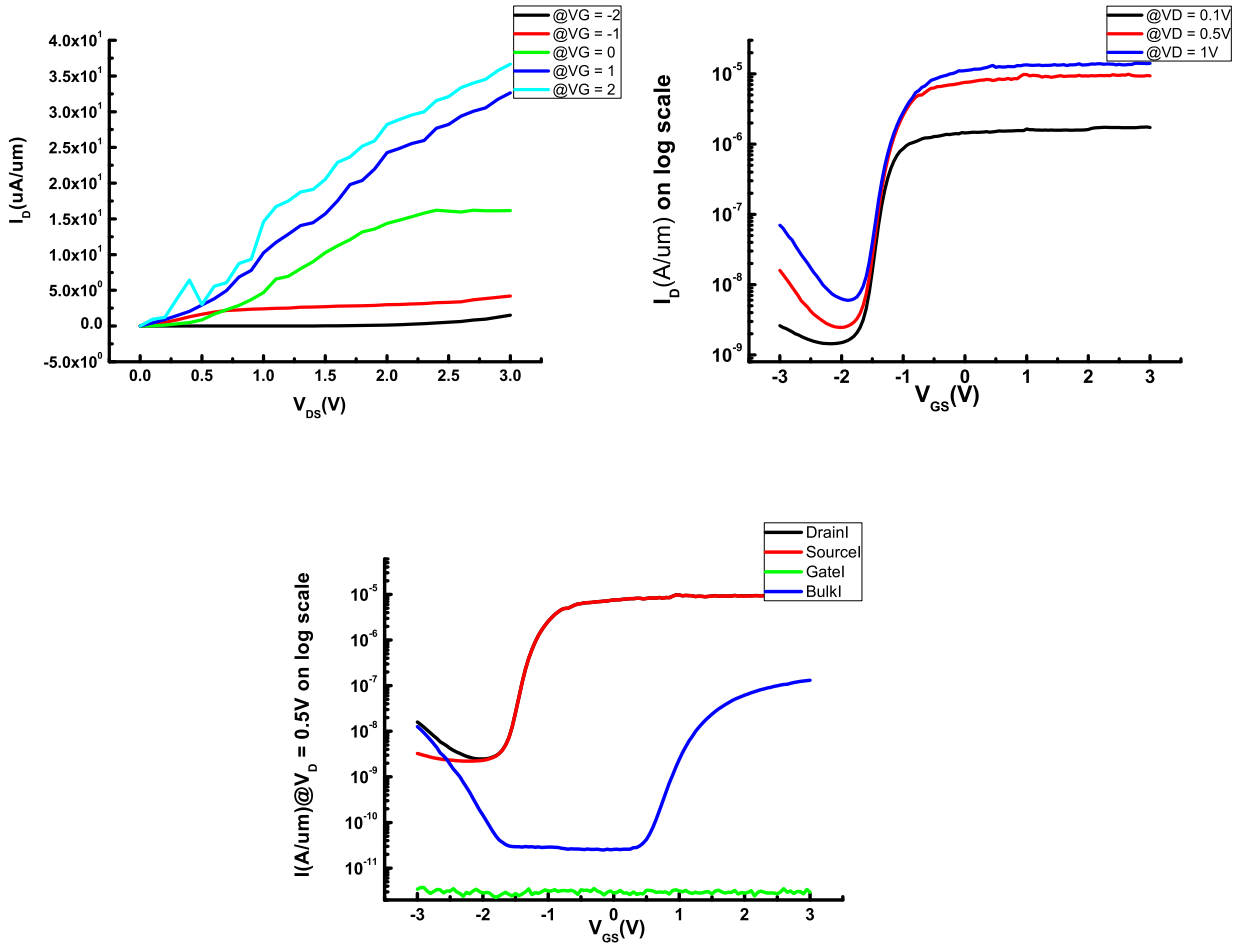
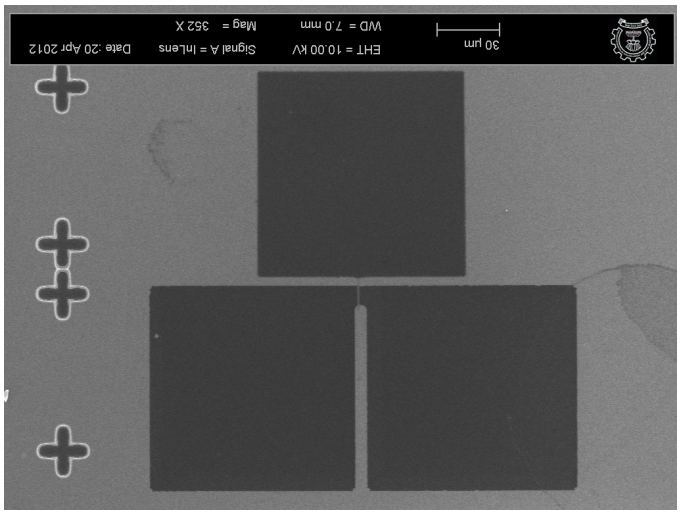
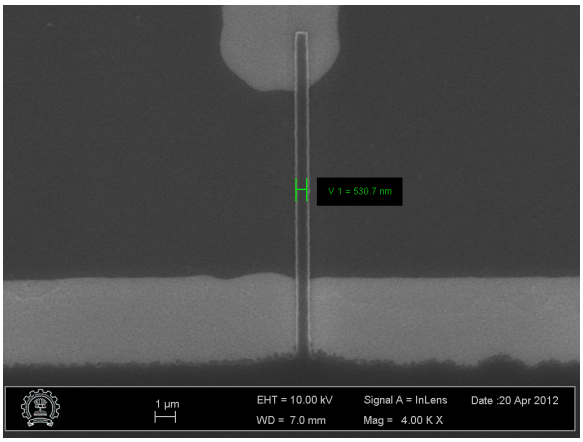


Figure 6.6: For a 1.5μm gate length NMOS a) $I_D - V_{DS}$ (top left) b) $I_D - V_{GS}$ on log scale (top right) c) I_D, I_S, I_B and I_G as a function of V_{GS} for V_D = 0.5V (bottom)

leakage component.





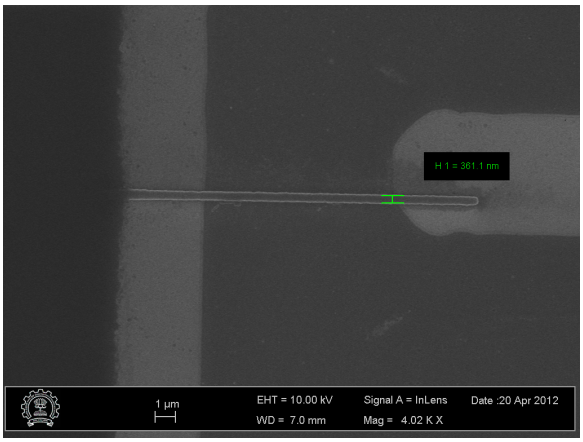


Figure 6.7: a) Surface SEM of a short-channel NMOS after gate etch b) NMOS with $\sim$ 500nm gate length c) NMOS with $\sim$ 500nm gate length

6.3 Experimental Work for Short-Channel NMOS

After the successful fabrication of the long-channel NMOS, we have taken up the task of realizing a short-channel NMOS with sub-500nm gate length. Mix and match lithography, an advanced technique which utilizes both optical and electron-beam lithography to pattern device structures, is included in the short-channel NMOS process flow. Process recipes for Sub-500nm gate features are developed and optimized using mix and match lithography. Probe area definition, which is explained in Section 3.2.2 of Chapter 3, is included in the short channel process flow to ensure reliable probing in the source and drain. The surface SEM of a short-channel NMOS transistor, just after the gate etch, is shown in Fig.6.7(a). Fig.6.7(b) and 6.7(c) represent devices with gate lengths of $\sim$ 500nm and $\sim$ 500nm respectively.

During the characterization, it has been noticed that the transistor action was missing in these short-channel devices. The $I_D - V_{GS}$ characteristics are shown in Fig.6.8. The gate field control is not observed in any of the devices. The C-V curves of MOS capacitors turned out

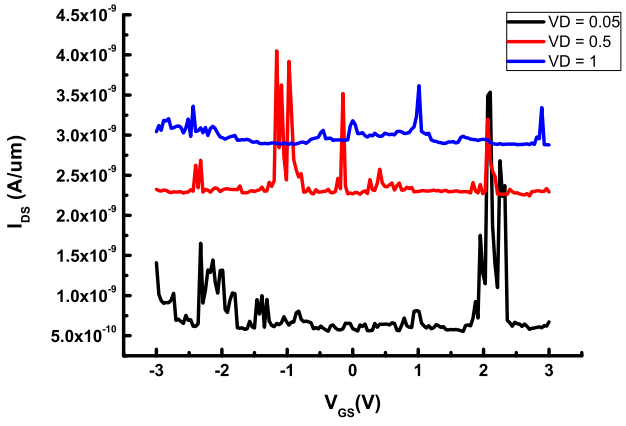


Figure 6.8: $I_D - V_{GS}$ of 500nm gate length NMOS transistor

as straight lines parallel to the voltage axis. The C-V curves of MOS capacitors, immediately after gate etch, displayed the sweep through accumulation, depletion and inversion. After the plasma immersion ion implant(PIII), these MOS capacitors lost their traditional behaviour. The thickness of the deposited poly-Si gate, which was $\sim$ 40nm as seen in cross-section SEM, was another major concern. It was clear that the plasma assisted implant disturbed the integrity of the gate. We were doubtful about the gate's ability to mask the implant from the channel region for two reasons: (a) thickness of the gate is $\sim$ 40nm (b) plasma assisted implant performs gate etch in parallel which further reduces the thickness. A process flow with thicker poly-Si and minimized plasma damage is ideal for the fabrication of short-channel NMOS.

Chapter 7

Summary and Future Work

Junction-Less Transistors(JLT) are seen as potential candidates to replace conventional MOSFETs in the forth coming short-channel era. As the scaling progresses to sub-20nm regime, requirement for steep doping concentration profiles at the source-channel and the drain-channel junctions, need for carefully tailored implants like anti-punch-through and halo(to minimize short channel effects) make the MOSFET processing tough and challenging. Though JLT appears to be an obvious choice in such a scenario, it has its own process complexities. Highly doped ultra-thin device layer is the most critical process and failure to realize the device layer(as per requirements) would make the JLT useless.

Fabrication of Bulk-Planar Junction-Less Transistors(BPJLT) is a major challenge for the present day research community. We have made attempts to fabricate BPJLT using shallow implant as a device layer. The shallow implant did not materialize as device layer and eventually we started exploring poly-silicon's suitability for the same. Experiments were done to fabricate a back-gated JLT with poly-silicon as device layer. High I_{ON}/I_{OFF} ratio($\sim 10^5$) of the back-gated JLT proved that poly-silicon can be used as device layer. Attempts to fabricate poly-silicon BPJLT hit a roadblock because of the surface roughness of poly-Si films.

Future work includes fabrication of BPJLT using epitaxially grown silicon as device layer. Back-gated JLT with two mask process (to reduce source-drain overlap with the back-gate) is another potential candidate waiting in the pipeline.

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Annexure I: Process Details of Active Area Definition

Process	Steps in Process	Specification	System	Recipe
LOCOS Isolation				
	RCA Clean		Micro-1 Wet Bench	2%HF dip - 1152ml DI water +48ml(49%HF) for 30sec; RCA1 - NH_4OH:H_2O_2:DI water in the ratio 125ml:250ml:875ml @75C; 2%HF dip for 30sec; RCA2 - HCl:H_2O_2:DI water in the ratio 125ml:250ml:875ml @75C; 2%HF dip for 30sec;
	Pad oxide growth	10nm	Ultech Furnace (Thin Dry Oxide)	Pre-growth step :
				Temperature : 850C
				O_2 gas flow: 50 sccm
				N_2 gas flow: ON
				Duration: 120 sec
				Growth step :
				Temperature: 850C
				O_2 gas flow: 5000 sccm
				N_2 gas flow: OFF
				Duration:1800sec
	Ellipsometry to determine the oxide thickness		Ellipsometer	Model :Air-Cau Thermal SiO_2-100 Si jellison; Cau Thermal SiO_2: R.I. 1.468;
	Nitride deposition	60nm, stoichiometric	Ultech Furnace (Silicon Nitride)	
				Ramp-up step: 300sec
				Temperature Stabilization step: 120sec
				Pressure Stabilization step : 300sec
				Deposition step :
				SiH_4 gas flow: 80sccm
				NH_3 gas flow: 100sccm
				N_2 gas flow: 1000sccm
				Temperature: 780C
				Pressure: 0.3torr
				Duration: 3900sec
	Ellipsometry to determine thickness of the nitride		Ellipsometer	Model :Air-Cau Si_3N_4- Cau Thermal SiO_2-100 Si jellison; Cau Thermal SiO_2: R.I. 1.468; Cau Si_3N_4 : R.I. 1.985;
	Active area photo-litho and development		Double Sided Aligner	Mask level : Level -1 (Active Area)
				Dehydration : 130C, >300sec on hot-plate
				HMDS spin : 7000 rpm,45sec
				Bake : 120C, 3600sec
				Photo-Resist : Shipley-1813
				Spinning : 6000rpm, 45 sec(Program E)
				Prebake: 90C,120sec

				Exposure : 64mJ/cm^2 (V+H)contact - 1um separation
				Development : MF-319(vertical), 25sec
				Post Development Bake : 90C, 60sec
	Microscopic Inspection	Four dies (B2,C3,D4,E5); Alignment marks	Olympus Microscope	Active area pads, Dimension of the region where gate falls in active area, Corner rounding in Active area, Global and Local alignment marks, any other strange feature.
	Nitride etch	Dry Etch	STSRIE	Time of etch : 200sec
				CF_4 gas flow : 40sccm
				O_2 gas flow : 4sccm
				RF Power for Selective Etch (SE) : 50W
				Chamber pressure(SE) : 110mTorr
				Etch rate of Si_3N_4 (SE) (nm/min) : 31
				Etch rate of SiO_2 (SE) (nm/min) : 9
				Selectivity obtained : 3.5
	Strip Resist	Acetone Strip	Sonicator	240sec in Acetone followed by 240sec in IPA
	Resist Ashing		AMAT Etch Centura	
				N_2 gas flow : 200sccm
				O_2 gas flow : 3500sccm
				H_2O flow : 300sccm
				Pressure : 2mTorr
				Source Power : 1400W
				Time : 120sec
	Piranha Clean		Micro-1 Wet Bench	H_2SO_4:H_2O_2 in the ratio 910ml:390ml for 3600sec
	Microscope inspections	Check for resist residues if any.	Olympus Microscope/Raith 150	
	HF dip		Micro-1 Wet Bench	2% HF, 30sec
	Field oxide growth	300nm pyrogenic oxide	Ultech Furnace (Pyrogenic Oxide)	Growth step:
				H_2 gas flow: 8000sccm
				O_2 gas flow: 6000sccm
				Temperature: 1000C
				Torch temperature: 835C
				Time: 2400sec
	Ellipsometry to determine the oxide thickness		Ellipsometer	Model : Air-Cau Thermal SiO_2-100 Si jellison; Cau Thermal SiO_2 : R.I. 1.468;
	Nitride etch	Wet Etch	TMAH Setup	BHF (5:1) dip : 10sec
				H_3PO_4 concentration : 0.87
				Etch temperature : 160C
				Si_3N_4 Etch rate : ~2nm/min
				SiO_2 Etch rate : 0.2nm/min
				Total etch time : 4500sec

Annexure II: Process Details of Probe Area Definition

Process	Steps in Process	Specification	System	Recipe
Probe Implant & Activation				
	Probe area photo-litho & development		Double Sided Aligner	Mask level: Level -2 (Probe Area)
				Dehydration: 130C, >300sec on hot-plate
				HMDS spin : 7000 rpm, 45sec
				Bake : 120C,360sec
				Photo-Resist : Shipley-1813
				Spinning : 6000rpm, 45 sec(Program E)
				Prebake : 90C,120sec
				Exposure : 64mJ/cm^2 (V+H)contact -1um separation
				Development : MF-319(vertical),25sec
				Post Development Bake : 90C,60sec
	Microscope Inspections		Olympus Microscope	
	Probe Area Implants	Junction Depth of 150nm	Ion Beam Implanter at BEL	Phosphorus Implant
				Energy : 40 KeV
				Dose : $3x10^{15}$ per cm^2
				Tilt angle : 7 degree
	Strip Resist	Acetone Strip	Sonicator	240sec in Acetone followed by 240sec in IPA
	Resist Ashing		AMAT Etch Centura	
				N_2 gas flow : 200sccm
				O_2 gas flow : 3500sccm
				H_2O flow : 300sccm
				Pressure : 2mtorr
				Source Power : 1400W
				Time : 120sec
	Piranha Clean		Micro-1 Wet Bench	H_2SO_4:H_2O_2 in the ratio 910ml:390ml for 3600sec
	Microscope Inspections	Check for resist residues if any.	Olympus Microscope	
	RTP	Anneal	AnnealSys RTP	Temperature : 1000C
				Time : 5 sec
				N_2 gas flow: 1000sccm
				O_2 gas flow: 50sccm
	HF dip		Micro-1 Wet Bench	2% HF, 90 sec
	Low Temperature Oxide deposition	10nm thickness	Ultech Furnace (LTO)	Temperature: 430C
				Time : 210 sec
				SiH_4 gas flow : 40sccm
				O_2 gas flow : 100sccm
				N_2 gas flow : 1000sccm
				Pressure : 0.2 Torr

Annexure III: Process Details of Shallow Junction Definition

Process	Steps in Process	Specification	System	Recipe
Shallow Implant & Activation				
	Shallow Implant	Junction of 12nm & Conc-1 : $1.6x10^{19}$ per cm^3 Conc-2 : 1 $x10^{19}$ per cm^3	Ion Beam Implanter at United States	Arsenic Implant
				Energy : 10 KeV
				Dose-1 : $1x10^{13}$ per cm^2 Dose-2 : $1.5x10^{13}$ per cm^2
				Tilt angle : 7 degree
				Rotation : 27 degree
	Activation (SPER)		AnnealSys RTP	Temperature: 650C
				Time : 80 seconds
				N_2 gas flow: 1000sccm
	HF dip		Micro-1 Wet Bench	BHF (5:1) dip : 15 sec
	Piranha Clean		Micro-1 Wet Bench	H_2SO_4:H_2O_2 in the ratio 910ml:390ml for 3600sec

Annexure IV: Process Details of TiN/Al_2O_3 Gate Stack

Process	Steps in Process	Specification	System	Recipe
Gate Stack Formation	Gate Oxide deposition(Al_2O_3)		AMAT Endura	
				Power : 200 W
				Argon gas flow : 10 sccm
				O_2 gas flow : 14sccm
				Time : 60sec
	Gate deposition (TiN)	~80nm thickness	AMAT Endura	
				Power: 300W
				Argon gas flow : 20sccm
				N_2 gas flow : 20sccm
				Time : 900sec
	Vacuum Anneal		AMAT Endura	
				Temp : 330C
				Time : 600sec
				Chamber pressure : $5x10^{-8}$ Torr
	SiO_2 as hard mask	~200nm thickness	ICPCVD	
	Gate Lithography			Mask level: Level -3 (Gate Area)
				Dehydration : 130C, >300sec on hot-plate
				HMDS spin : 7000 rpm,45sec
				Bake : 120 C, 360 sec
				Photo-Resist : Shipley-1813
				Spinning : 6000rpm , 45 sec (Program E)
				Prebake: 90C, 120sec
				Exposure : 50mJ/cm^2 (V+H) contact - 1um separation
				Development : MF-319 (vertical) ,25sec
				Post Development Bake : 90C, 60sec
	Wet Etch of SiO_2 using BHF			BHF(5:1) dip : 1 minute
	Wet Etch of TiN			$NH_4OH:H_2O_2:H_2O$ in the ratio 1:2:7@ 60C for 60sec
	Resist Strip	Acetone Strip	Sonicator	240sec in Acetone followed by 240sec in IPA
	Wet Etch of SiO_2 using BHF			BHF(5:1) dip : 60sec
	Back Side Al Metallization		Al Thermal Evaporator	Pressure : $2x10^{-6}$ mbar

Annexure V: Process Details of Back-gated JLT

Process	Steps in Process	Specification	System	Recipe
	RCA Clean		Micro-1 Wet Bench	2%HF dip - 1152ml DI water +48ml(49%HF) for 30sec; RCA1 - NH_4OH:H_2O_2:DI water in the ratio 125ml:250ml:875ml @75C; 2%HF dip for 30sec; RCA2 - HCl:H_2O_2:DI water in the ratio 125ml:250ml:875ml @75C; 2%HF dip for 30sec;
	Gate oxide growth	10nm	Ultech Furnace (Thin Dry Oxide)	Pre-growth step :
				Temperature : 850C
				O_2 gas flow: 50 sccm
				N_2 gas flow: ON
				Duration: 120 sec
				Growth step :
				Temperature: 850C
				O_2 gas flow: 5000 sccm
				N_2 gas flow: OFF
				Duration: 1800sec
	Ellipsometry to determine the oxide thickness		Ellipsometer	Model :Air-Cau Thermal SiO_2-100 Si jellison; Cau Thermal SiO_2: R.I. 1.468;
Poly-Si Device Layer Definition				
	N-type poly-Si deposition		AMAT Polygen	Temperature: 700C
				SiH_4 gas flow: 85 sccm
				PH_3 gas flow: 120 sccm
				Chamber Pressure: 275 Torr
				Time : 5sec, 7sec, 10sec and 15sec
	RTP	Anneal	AnnealSys RTP	Temperature : 950C
				Time : 5 sec
				N_2 gas flow: 1000sccm
	Active area photo-litho and development		Double Sided Aligner	Mask level : Level -1 (Active Area)
				Dehydration : 130C, >300sec on hot-plate
				HMDS spin : 7000 rpm,45sec
				Bake : 120C, 3600sec
				Photo-Resist : Shipley-1813
				Spinning : 6000rpm, 45 sec(Program E)
				Prebake: 90C,120sec
				Exposure : 64mJ/cm^2 (V+H)contact -1um separation
				Development : MF-319(vertical), 25sec
				Post Development Bake : 90C, 60sec
	Microscopic Inspection	Four dies (B2,C3,D4,E5);	Olympus Microscope	Active area pads, Dimension of the region where gate falls in active area, Corner

		Alignment marks		rounding in Active area, Global and Local alignment marks, any other strange feature.
	poly-Si etch	Dry Etch	STSRIE	CF_4 gas flow : 40sccm
				O_2 gas flow : 5sccm
				RF Power for Selective Etch (SE) : 350W
				Chamber pressure(SE) : 20mTorr
				Etch rate of poly-Si (SE) (nm/min) : 210
				Selectivity obtained with SiO_2 : 2.5
				Time of etch : 9sec
	Piranha Clean for Resist Strip		Micro-1 Wet Bench	H_2SO_4:H_2O_2 in the ratio 910ml:390ml for 3600sec
	Back Side Oxide Etch		Micro-1 Wet Bench	2% HF
Back Gate	Back Side Al Metallization		Al Thermal Evaporator	Pressure : $2x10^{-6}$ mbar

Annexure VI: Process Details of Al/SiO_2 Gate Stack

Process	Steps in Process	Specification	System	Recipe
Gate Stack Formation	Gate Oxide deposition(SiO_2)	10nm thickness	Ultech Furnace (LTO)	Temperature: 430C
				Time : 60 sec
				SiH_4 gas flow : 80sccm
				O_2 gas flow : 100sccm
				N_2 gas flow : 1000sccm
				Pressure : 0.2 Torr
	Gate deposition (Al)	~ 120nm thickness	Al Thermal Evaporator	Pressure : $2x10^{-6}$ mbar
	Gate Lithography		Double Sided Aligner	Mask level: Level -3 (Gate Area)
				Dehydration : 130C, >300sec on hot-plate
				HMDS spin : 7000 rpm,45sec
				Bake : 120 C, 360 sec
				Photo-Resist : Shipley-1813
				Spinning : 6000rpm , 45 sec (Program E)
				Prebake: 90C, 120sec
				Exposure : 50mJ/cm^2 (V+H) contact - 1um separation
				Development : MF-319 (vertical) ,25sec
				Post Development Bake : 90C, 60sec
	Wet Etch of Al			H_3PO_4:CH_3COOH:HNO_3:H_2O in the ratio 16:1:1:2@25C for 150sec
	Resist Strip	Acetone Strip	Sonicator	240sec in Acetone followed by 240sec in IPA
	Back Side Al Metallization		Al Thermal Evaporator	Pressure : $2x10^{-6}$ mbar

Annexure VII: Process Details of Poly-Si/SiO_2 Gate Stack

Process	Steps in Process	Specification	System	Recipe
	RCA Clean		Micro-1 Wet Bench	2%HF dip - 1152ml DI water +48ml(49%HF) for 30sec; RCA1 - NH_4OH:H_2O_2:DI water in the ratio 125ml:250ml:875ml @75C; 2%HF dip for 30sec; RCA2 - HCl:H_2O_2:DI water in the ratio 125ml:250ml:875ml @75C; 2%HF dip for 30sec;
	Gate oxide growth	~ 4nm thickness	Ultech Furnace (Thin Dry Oxide)	Pre-growth step :
				Temperature : 850C
				O_2 gas flow: 50 sccm
				N_2 gas flow: ON
				Duration: 120 sec
				Growth step :
				Temperature: 850C
				O_2 gas flow: 5000 sccm
				N_2 gas flow: OFF
				Duration:300sec
	In-situ doped N+ poly-Si deposition	~ 150nm thickness	Ultech Furnace (N-Poly)	Temperature: 650C
				SiH_4 gas flow: 80 sccm
				PH_3 gas flow: 8 sccm
				N_2 gas flow: 0 sccm
				Chamber Pressure: 100 mTorr
				Time : 6600 sec
	Thermal activation of N+ poly-Si	~ 16-20nm of SiO_2 to prevent outdiffusion of dopants	AnnealSys RTP	Temperature : 1000C
				Time : 30 sec
				O_2 gas flow: 900sccm
	Oxide Etch (Front and Backside)		Micro-1 Wet Bench	2% HF for 120 sec
Backside Poly-Si Etch				
	Resist spin		Spinner in Nano Lab	Photo-Resist : SPR 700
				Spinning : 3000rpm , 30 sec
				Prebake: 90C, 300sec
	HNA dip		Micro-1 Wet Bench	HNA sol: HF (2 ml) + HNO_3 (38 ml) + DI water (20 ml). HNA dip for 30 sec (N-Poly etch from back)
	Front side resist removal		Sonicator	240sec in Acetone followed by 240sec in IPA
Gate Lithography	Gate Lithography		Double Sided Aligner	Mask level: Level -3 (Gate Area)
				Dehydration : 130C, >300sec on hot-plate
				HMDS spin : 7000 rpm,45sec
				Bake : 120 C, 360 sec

				Photo-Resist : Shipley-1813
				Spinning : 6000rpm , 45 sec (Program E)
				Prebake: 90C, 120sec
				Exposure : 50mJ/cm^2 (V+H) contact -1um separation
				Development : MF-319 (vertical) ,25sec
				Post Development Bake : 90C, 60sec
Gate Etch	poly-Si etch	Dry Etch	STSRIE	CF_4 gas flow : 40sccm
				O_2 gas flow : 5sccm
				RF Power for Selective Etch (SE) : 350W
				Chamber pressure(SE) : 20mTorr
				Etch rate of poly-Si (SE) (nm/min) : 210
				Selectivity obtained with SiO_2 : 2.5
				Time of etch : 50sec
		Followed by		
				CF_4 gas flow : 40sccm
				O_2 gas flow : 5sccm
				RF Power for Selective Etch (SE) : 20W
				Chamber pressure(SE) : 500mTorr
				Etch rate of poly-Si (SE) (nm/min) : 25
				Selectivity obtained with SiO_2 : 12
				Time of etch : 30sec
	Piranha Clean for Resist Strip		Micro-1 Wet Bench	H_2SO_4:H_2O_2 in the ratio 910ml:390ml for 3600sec
	Microscopic /SEM Inspection	Four dies (B2,C3,D4,E5); Alignment marks	Raith 150/ Olympus Microscope	Gate fingers of 0.5um, 1um, 2um and 10um dimensions, Mis-alignment after second level litho (Both in x and y directions), Poly-Si etch profile on SEM lines on the wafer, Poly-Si remains , resist strains.

Annexure VIII: Process Details of Source-Drain Engineering in NMOS Transistor

Process	Steps in Process	Specification	System	Recipe
Source/Drain Implant & Activation				
	Source/Drain Implant		Ion Beam Implanter at BEL	Arsenic Implant
				Energy : 90 KeV
				Dose : $6x10^{14}$ per cm^2
				Tilt angle : 7 degree
	RTP		AnnealSys RTP	Temperature: 1050C, 1100C
				Time : 5 sec
				N_2 gas flow: 1000sccm
				O_2 gas flow: 50sccm
	HF dip		Micro-1 Wet Bench	2% HF for 60 sec
	Piranha Clean		Micro-1 Wet Bench	H_2SO_4:H_2O_2 in the ratio 910ml:390ml for 3600sec
	Back Side Al Metallization		Al Thermal Evaporator	Pressure : $2x10^{-6}$ mbar
	Forming Gas Anneal		Forming gas anneal furnace (CMOS) (Micro 1 lab)	H_2 (5%) + N_2 (95%), 400 C, 1200 sec