Charge-carrier Transport in VLS (Vapour-Liquid-Solid) Grown Silicon Nanowires

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Dedicated to

my Teachers

and Taxpayers

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Abstract

This work presents a study of electrical characteristics and charge carrier transport through vapour-liquid-solid (VLS) grown silicon nanowires using gold as catalyst. The silicon nanowires used for the study are grown using a simple cold-wall catalytic chemical vapour deposition (cat-CVD) tool. Silane (SiH_4) is used as the source of silicon in VLS growth process. The gas is flown into the spherical reaction chamber from top, the sample is kept just below the gas inlet, on top of a heated chuck. The exhaust is placed below the sample holder, which carried unreacted SiH_4 and reaction byproduct H_2, out of the chamber. Pressure inside the chamber is regulated by adjusting the gate valve fitted at the exhaust. Detailed overview of the growth process and details of optimisations are presented in this work. The simplicity of the process equipment and low thermal budget of the growth process described in this work should make VLS process accessible to a wider group of researchers and bring down the cost of production as well. It has been observed that, the current-voltage (IV) characteristics of the silicon nanowires exhibit a typical inverse-'S' like shape. The IV characteristics are almost linear at small voltages. However, at higher voltages, the conductivity of the nanowires vary linearly with square root of the applied voltage. Transition between these two regimes of conduction shifts to higher voltages as the temperature is reduced. This is a clear trait of Poole-Frenkel (PF) transport. PF is a well known form of hopping transport, where charge carriers are trapped inside a series of coulomb traps. At higher voltages (electric field), charge carriers are ripped from these traps and made available for conduction inside the solid. PF transport is always associated with disorderedness in the material. This is unlikely of a single crystal such as VLS grown silicon nanowires. Detailed physical characterisations are performed using transmission electron microscope (TEM) to investigate the structure of the nanowires. It has been found that the VLS grown silicon nanowires have several defects. Residue catalyst-silicon alloy are found trapped inside the native oxide shell and the surface of silicon nanowires. Two types of twin boundaries are found. One oriented along the axis of the silicon nanowires, the other spanning

as body diagonal of the nanowires. The biggest contributor to the origin of PF transport in these nanowires are hypothesised to be small ($<25\ nm^2$) regions of crystallographic misorientation found throughout the nanowires. These regions appear as dark patches in bright field TEM, but have no effect on the selected area electron diffraction (SAED) patterns, collected from the samples. This means that, the overall misorientation should be within 5° deviation from exact s-vector.

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List of abbreviations

CVD	Chemical vapour deposition
EBL	Electron Beam Lithography
EDX	Energy-dispersive X-ray spectroscopy
FECA	Foreign Element Catalytic Agent
FESEM	Field emission scanning electron microscope
HWCVD	Hot wire chemical vapour deposition
IV	Current-voltage
LPCVD	Low pressure chemical vapour deposition
PECVD	Plasma-enhanced chemical vapour deposition
PF	Poole-Frenkel
SEM	Scanning electron microscope
SAED	Selected area (electron) diffraction
TB	Twin boundary
TCAD	Technology computer aided design
TEM	Transmission electron microscope
VLS	Vapour-liquid-solid

Chapter 1

Introduction

Research on novel semiconductor devices is one of the important frontiers of modern science and technology. The improvement of semiconductor device technology, in terms of cost and performance, in last few decades, has impressed consumers and researchers alike. However, many experts believe that this rate of improvement will not be sustainable for the years to come, unless researchers keep on exploring new materials and technologies to improve the collective knowledge. This will increase the possibility for a paradigm shift. In this work, a material with potential application in making future electronic devices and interconnects is studied. Even though there are plenty of work in past which reported several aspects of the material, we have reasons to believe that the characteristics of the material is not completely understood.

Silicon nanowires are a type of nanostructure. They usually refer to rod shaped crystals of silicon, with diameter in the nanometer range. Publications throughout the last two decades exhibit its usefulness in making sensors and other electronic devices. Arrays of silicon nanowires can also be used as templates or as a light trapping layer to enhance the efficiency of solar cells. Even though all these applications of silicon nanowires have been explored relatively recently, the research on silicon nanowires started more than half a century ago. The first report on silicon nanowire (formerly termed as whiskers) is dated 1957 by Treuting and Arnold [1]. This unusual discontinuity between the discovery of the material and gaining recognition as a substance with application, can be attributed to the lack of demand of such a material in the decades in-between, in general. With the advancement of microelectronics and semiconductor fabrication technologies, and synthesis of silicon nanowires of nanoscale diameter by Morales and Lieber in 1998 [2], the scenario changed quite a lot. The development of “bottom-up” technology, in which nanostructures like silicon nanowires are assembled atom-by-atom from

their fundamental components, elevated research in silicon nanowires to a completely new level. Traditional “top-down” technology, in which materials in bulk form are shaped down to make nanostructures by removing excess material, fell short of high-yield production of nanoscale materials. One dimensional structures and alternative materials, such as carbon nanotubes, demanded a massive alteration of the existing technology.

This work provides an in-depth study of several steps of making silicon nanowire devices. A study of previous literature is presented in chapter 2, followed by an overview of the experimental techniques used for this work in chapter 3. In chapter 4, the most versatile and promising method of silicon nanowire growth, the vapour liquid solid (VLS) growth, is studied in detail. It has also been vividly documented, how, using a simple, low-cost reactor, good quality silicon nanowires can be produced. The grown silicon nanowires are used to fabricate test devices. After that, by specially designed study of electrical characteristics of the nanowires, the dominant mode of charge carrier transport through them is determined. The goal was to find out whether using VLS method for growth induces any characteristic peculiarity in these nanowires. It has been found, for the first time, that the current through the VLS grown silicon nanowires are dominated by Poole-Frenkel (PF) transport. The results are presented in chapter 5. Previous works missed this because of the nature of doping and contact formation of the nanowires. The onset of the phenomenon is experimentally demonstrated with electrical characteristics, and through rigorous physical characterisation and simulations. The physical origin of the transport (PF) is explained in chapter 6. We believe, this document would aid future researchers to develop functioning electronic devices, sensors or interconnects using silicon nanowires, as they can either intentionally make silicon nanowire devices within PF dominated regime, or out of it.

Chapter 2

Literature review

2.1 An overview of silicon nanowire synthesis techniques

Many techniques to synthesise silicon nanowires have been discovered and studied in the last five decades. The abundance of growth techniques actually stems from the diversity of applications, because a particular growth technique is useful for only a handful of applications. Different techniques of silicon nanowire growth can be roughly divided into two categories. 'Top-down', in which bulk silicon is turned into nanowires by removing excess materials. 'Bottom-up', in which nanowires are made by self-assembly of individual atoms or clusters of atoms. The top-down approach to growth is usually preferred for photovoltaic applications to make arrays of silicon nanowires for light trapping. Bottom-up technique is more useful for microelectronic applications such as nanowire transistors. Keeping the plethora of available growth techniques in mind, only the most commonly used growth techniques are discussed here. The physical and chemical etching based techniques are discussed under the name- top-down techniques. Followed by short discussions on bottom-up techniques such as, solution based techniques, silicon monoxide evaporation, laser ablation, and VLS method.

2.1.1 Top-down techniques

Top-down techniques for silicon nanowire synthesis mostly rely on lithography and etching processes. One of the most commonly used top-down techniques is Langmuir-Blodgett assembly and etching [3]. In this, nanosphere lithography is used to make array of vertical nanopillars of silicon. This is then oxidised to make silicon nanowires. A typical process flow is de-

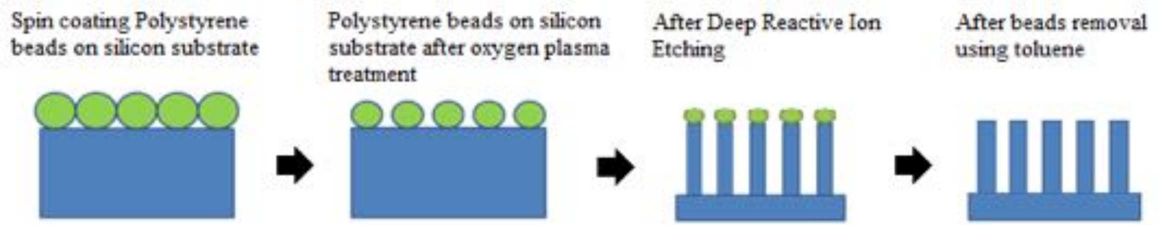

Figure 2.1: Schematic diagram of simplified process flow of a typical nanosphere lithography process.

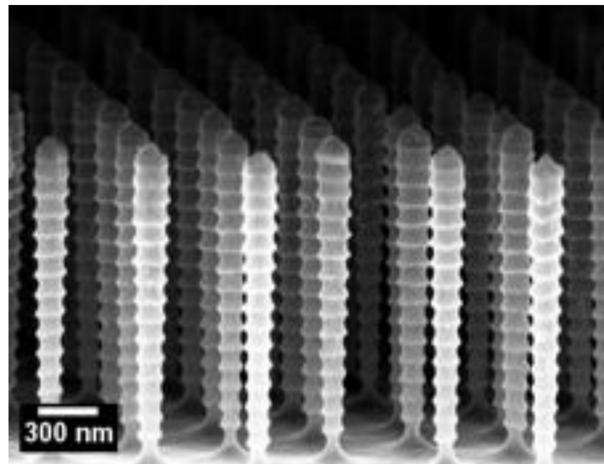

Figure 2.2: 45° tilted Scanning Electron Microscope (SEM) images of an array of silicon nanowires synthesised by a top-down method similar to what is described in figure 2.1. The image is taken from the work of Raja Sekhar Baddula, CRNTS, IIT Bombay with permission from the author.

scribed with the help of schematic diagrams in figure 2.1. Figure 2.2 exhibits an array of silicon nanowires on silicon substrate, fabricated using a process similar to what is described in figure 2.1. However, to obtain horizontal nanowires, an approach other than nanosphere lithography has to be used. One such method is performing electron-beam lithography (EBL) with silicon-on-insulator (SOI) wafers [4]. This produces silicon nanowires parallel to the buried silicon surface. A major disadvantage of using top-down method is creation of surface defects. Since, in this process, the desired geometry is obtained by aggressive processing and removal of materials. Often times, this leads to a high number of defects on the surface. To counter this effect, nanowires synthesised using this method are advised to be passivated before use.

2.1.2 Solution based techniques

Solution based techniques are also referred to as supercritical fluid based techniques. In this method, a liquid silicon precursor is used along with a highly pressurised supercritical organic fluid. This fluid contains the catalyst. To synthesise silicon nanowires, silicon diffuses through the surface of the catalyst to initiate one-dimensional growth [5]. In this method, silicon nanowires are grown suspended in a solution rather than attached to a growth substrate. This has several advantages, such as physical characterisation. There are disadvantages as well, such as growth without a substrate limits these nanowires' usability in several applications like photovoltaics.

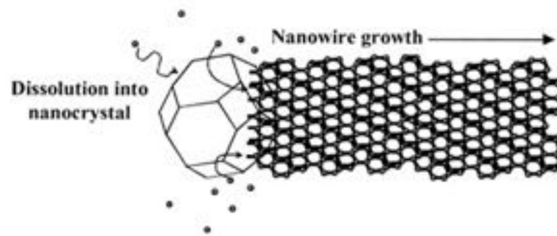

Figure 2.3: Schematic diagram explaining silicon nanowire growth in solution phase. The figure is taken from reference [5].

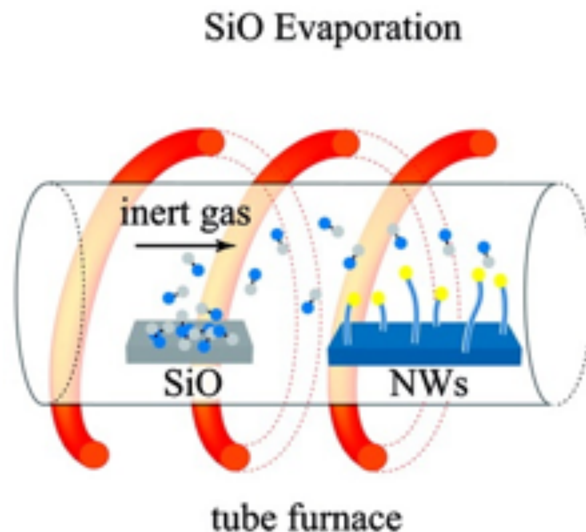

Figure 2.4: Schematic diagram of silicon nanowire growth by silicon monoxide evaporation in a tube furnace. The figure is taken from reference [6].

2.1.3 Silicon monoxide evaporation

This method requires a rather complex setup. A tube furnace is heated with multi-zone external heating elements. In which silicon monoxide (SiO) is kept on the hottest zone of the furnace. A steady flow of inert gas needs to be monitored from the hotter parts to the colder parts of the furnace. This allows the SiO to evaporate and get carried by the inert gas flow towards the colder zones. In the colder zones of the tube furnace, the evaporated SiO undergoes a disproportionation reaction to form Si and SiO_2. This reaction results in silicon nanowires with an oxide shell [7]. Nanowires grown by this method have less surface defects as the surface is passivated by the oxide shell. However, for many applications, this brings extra complexity. In order to establish electrical contact with the nanowires, one has to remove the shell either locally or completely.

2.1.4 Laser ablation

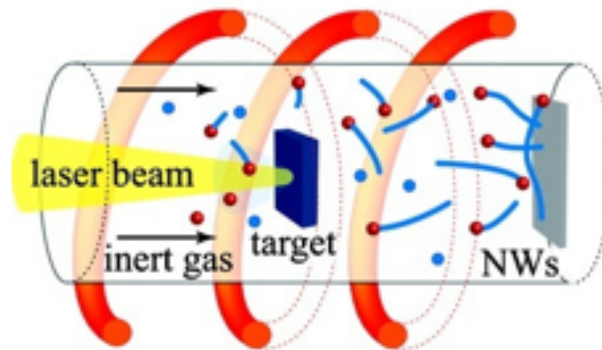

Figure 2.5: Schematic digram of silicon nanowire growth process by laser ablation in a tube furnace. The figure is taken from reference [6].

A striking characteristic of growth of silicon nanowires by laser ablation technique is that the actual growth of silicon nanowires happens in the gas phase. A target is prepared by fusing silicon and a catalyst material together in proper ratio. This is then kept inside a tube furnace. The furnace is heated before the pulsed laser hits the prepared target and elevated temperature is maintained throughout the process. At this point, the laser ablates silicon-catalyst alloy particles from the target in the heated tube. These particles are carried by a flow of inert gas to the other

end of the tube where a substrate is placed. As the inert gas carries the ablated alloy particles far from the target, the particles condense to form liquid droplets. These droplets then initiate growth of silicon nanowires. The nanowires collected on a substrate usually have a crystalline core and amorphous shell [2]. When invented, this method revolutionised research in silicon nanowires. The first truly 1-D nanowires (diameter less than 10 nm) were grown using this method.

2.1.5 Vapour-Liquid-Solid (VLS) method

Since its invention in 1964 by Wagner and Ellis [8], the VLS (Vapour-Liquid-Solid) method of nanowire synthesis has been heavily studied. The interest is mainly because of the fact that this method can be used for a wide range of process conditions. As a result, nanowires with different physical properties and dimensions can be produced with repeatability [6]. Considering the diversity of applications of silicon nanowires [9], it is not surprising that such a method would become widely used. The name, VLS growth, came from the trail of the element silicon during the growth process. In this process, the silicon from the gaseous precursor (vapour) diffuses through an eutectic alloy droplet (liquid) until gets crystallised and finally forms nanowire (solid) [8]. Usually the process takes place inside a Chemical Vapour Deposition (CVD) system. A silicon rich, oxygen free, gas supplies silicon to the CVD chamber. Typical choices of the precursor gas are silane (SiH_4), disilane (Si_2H_6), dichlorosilane (SiH_2Cl_2), and tetrachlorosilane ($SiCl_4$). The growth conditions depend on the selection of the precursor gas. For example, VLS growth using tetrachlorosilane ($SiCl_4$) as a precursor gas necessitates a process temperature from about 800 °C [10] to well beyond 1000 °C [11]. On the other hand, VLS growth using silane as a precursor gas requires only $400-600$ °C [12]. This is because of the difference in the activation energy required to dissociate each precursor. There are other effects to be considered as well. Using chlorinated precursor results in etching of the substrate as well as the wall of the reaction chamber. Depending on the aim of the experiment, this could be desired or unacceptable.

The VLS method requires a Foreign Element Catalytic Agent (FECA) for nanowire growth. An FECA is a metal, capable of forming eutectic alloy with silicon, below the VLS growth temperature. The most frequently used FECA in published literature is gold [12]. A close look at the binary phase diagram [6] of gold and silicon reveals the fact that the binary phase of silicon and gold is of simple eutectic type. It is characterised by a single eutectic point at 363 °C. When

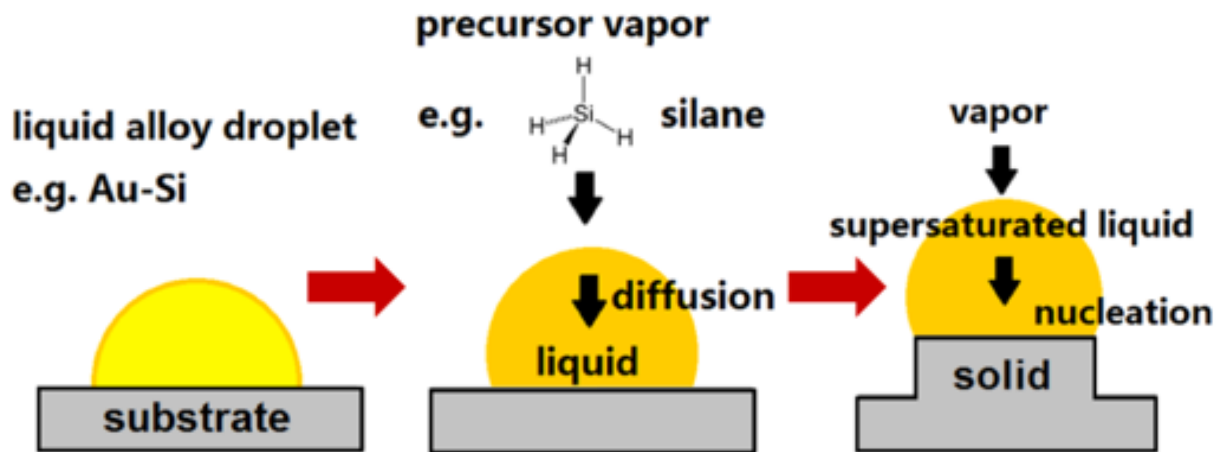

Figure 2.6: Schematic representation of silicon nanowire growth by VLS method. Image taken from Prof. Wei Cai's (Stanford university) blog (URL: http://imechanica.org/node/17430).

a silicon wafer, containing gold thin film or gold nanoparticles on top, is heated over 363 °C, liquid Au-Si eutectic droplets form in a silicon-abundant environment. These liquid droplets act as FECA during VLS growth of silicon nanowires. But the process needs even higher temperature for dissociation of the precursor gas. This precursor gas dissociates on the surface of the FECA into solid silicon and a gaseous byproduct. This results in supersaturation of silicon inside the eutectic droplet, followed by crystallisation of silicon at the FECA-substrate interface. The silicon nanowire grows with the FECA droplet on the top if steady supply of precursor gas is maintained. The diameter of the growing nanowire becomes equal to that of the liquid droplet. This process is exhibited schematically in figure 2.6. In this study, gold is used as FECA for simplicity of optimisation and abundance of available literatures to compare the results with.

As mentioned earlier, this process is heavily optimised and studied ever since its discovery for quite a few precursor gases and FECA [6]. These experiments have resulted in silicon nanowires which are diverse in geometry and physical properties. This, to a large extend, can be attributed to the choice of the equipment used for the process as well. The equipments range from Low-Pressure Chemical Vapour Deposition (LPCVD) [13], Plasma-Enhanced Chemical Vapour Deposition (PECVD) [14] to tube furnaces [15]. Sometimes more complicated systems like Transmission Electron Microscope with integrated CVD process [16], Molecular-Beam Epitaxy (MBE) [17] or Metal-Organic Chemical Vapour Deposition reactor (MOCVD) [18] are also being used to carry out VLS growth of silicon nanowires. In this work, a rather simple, and indigenous, instrument has been used to grow silicon nanowires by VLS method. The results

are presented in chapter 4. The instrument is a Cold Wall cat-CVD with spherical reaction chambers. We believe this to be quite significant for mass production. This instrument clearly brings down the complexity of the equipment needed for VLS growth process. The thermal budget is significantly lower than traditional VLS process, where the entire process chamber is heated up to the growth temperature. As a result, the cost to produce VLS grown silicon nanowires should go down significantly, if this method is implemented.

2.2 Growth models

In last five decades of silicon nanowire research, attempts of modelling the VLS growth has been quite scarce compared to the bountiful reports of experiments. It can be said that the quantitative understanding of the growth process is still evolving. Over the years, the concepts have been rethought many times with the insights created by experimental results. Bootsma et al. [19] attempted to model VLS growth in 1971. According to their understanding, VLS growth was controlled by a single activation step. The conclusion was that, the decomposition of the gaseous precursor at the vapour-liquid interface is the controlling step for growth rate. The concepts reached a dialectical phase in 1975, when Givargizov et al. [11] claimed that the nucleation at the solid-liquid interface to be the defining step for growth rate. This disagreement continued untill recent times as well [20]. A new epoch of understanding started when Schmidt et al. [21] and Dubrovskii et al. [22] applied the steady state hypothesis to nanowire growth. They proposed that, for a growth mechanism involving a series of steps, it is feasible to not have a single rate defining step. In our work, we chose to explicate the VLS growth of silicon nanowires using the model of Lu et al. [23]. The choice is made based on correctness and simplicity of the model. Conventionally, the VLS growth process is divided roughly into the following four steps: (i) supply of precursor material to the vapour phase, (ii) reaction at the vapour-liquid droplet interface, (iii) diffusion of the species through the liquid FECA and (iv) crystallisation at the liquid droplet - solid substrate interface. But Lu et al. [23] have divided the transport of the material, contributing to the nanowire growth, into three kinetic parts: (i) 'Direct effective impingement of deposit atoms on the catalyst liquid droplet', (ii) 'Diffusion of the atoms that hit the sidewall area of the NW at an incident angle θ' and (iii) 'Diffusion flux of adatoms from the substrate surface toward the droplet along the nanowire sidewalls'. The model is based on two steady-state diffusion equations. One describing the diffusion of the

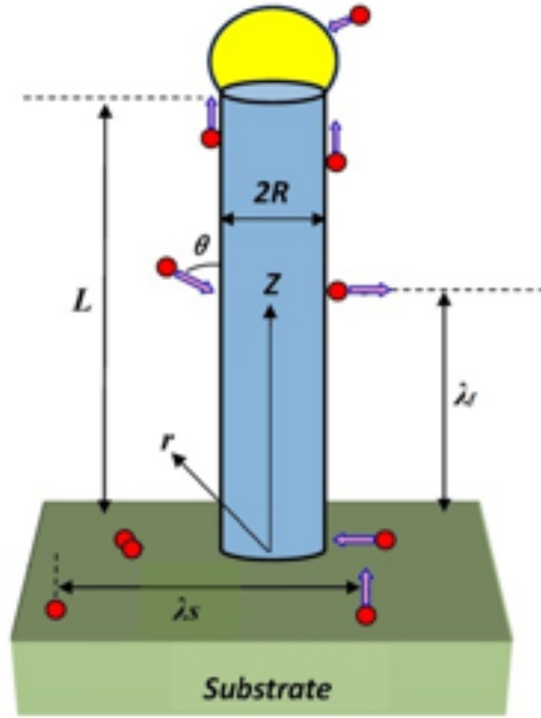

Figure 2.7: Schematic diagram for the understanding of the model proposed by Lu et al. Figure taken from reference [23].

adatoms on the substrate surface and the other describing the diffusion of the adatoms on the nanowire sidewall. These equations describing the adatom flux are continuous at the base of the growing silicon nanowires. The adatoms concentration on the substrate surface, n_s should satisfy the following equation:

$$\frac{\partial n_s}{\partial t} = D_s \nabla^2 n_s - \frac{n_s}{\tau_s} + J cos\theta \tag{2.1}$$

Where D_s is the diffusion coefficient of adatoms on the substrate surface. τ_s is the average time, an adatom spends on the substrate surface, before deposition, J is the impinging flux of adatoms from the vapour phase and ∇^2 is the 2D Laplace vector. Similarly the adatoms concentration on the sidewall of nanowires, n_f should satisfy the following equation:

$$\frac{\partial n_f}{\partial t} = D_f \frac{\partial^2 n_f}{\partial^2 z} - \frac{n_f}{\tau_f} + J sin\theta \tag{2.2}$$

Where D_f is the diffusion coefficient of adatoms on the nanowire sidewall and τ_f is the average time, an adatom spends on the nanowire sidewall, before deposition. In order to achieve steady

state ($\frac{\partial n_s}{\partial t}$ = 0) solution for equation (2.1), we may assume the boundary condition $n_s(R) = 0$, where R is the radius of the growing nanowires. Finally, the solution can be expressed in terms of the modified Bessel function of the second kind, $K_0(x)$.

$$n_s(r) = R_s \tau_s \left[1 - \frac{K_0(\frac{r}{\lambda_s})}{K_0(\frac{R}{\lambda_s})}\right] \tag{2.3}$$

Here, $\lambda_S = \sqrt{D_s \tau_s}$, is the diffusion length of the adatoms at the substrate surface. This solution is valid only if the separations of the adjoint nanowires are very large. Using an analogous approach the steady state solution for equation (2.2) can be achieved using the following boundary conditions. $\left[D_s \frac{\partial n_f}{\partial r}\right]_{r=R} = \left[-D_f \frac{\partial n_f}{\partial z}\right]_{z=0}$ at the bottom of the nanowires and $[n_f]_{z=L}$ at the top of the nanowires. Where, L is the length of the growing silicon nanowires. The solution can be expressed as,

$$n_f = J \tau_f \sin\theta \left[1 - \frac{\cosh(\frac{z}{\lambda_f})}{\cosh(\frac{L}{\lambda_f})}\right] + \frac{\lambda_f}{D_f} \frac{\sinh(\frac{L-z}{\lambda_f})}{\cosh(\frac{L}{\lambda_f})} \frac{J \cos\theta \lambda_s K_1 \frac{R}{\lambda_s}}{K_0 \frac{R}{\lambda_s}} \tag{2.4}$$

here, λ_f is the diffusion length of the adatoms on the nanowire sidewall. Therefore the total adatom diffusion flux to the FECA droplet can be written as,

$$J_{diff}(L) = \left[-D_f 2 \frac{\partial n_f}{\partial z}\right]_{z=L} \tag{2.5}$$

The net flux impinging on the FECA droplet from vapour phase can be written as,

$$J_{top} = \frac{P - P_\infty exp(\frac{2\sigma_{lv}\Omega_l}{RK_B T})}{\sqrt{2\pi m K_B T}} \tag{2.6}$$

Here, P is the partial pressure of the precursor inside the reactor chamber. $P_\infty$is the pressure of the reactant species in a droplet of infinite radius of curvature. σ_{lv} is the surface energy density at the vapour-liquid interface and Ω_l is volume per atom in the liquid phase. Now, using steady state hypothesis, the number of atoms transferred from vapour phase to the FECA droplet per unit time can be equated with the number of atoms crystallised at the FECA droplet - substrate interface per unit time.

$$\therefore 2\pi R^2 J_{top} \alpha + J_{diff}(L) \alpha' = \left(\frac{\pi R^2}{\Omega_s}\right) \frac{dL}{dt} \tag{2.7}$$

Where Ω_s is the volume per atom in crystal phase, α is the sticking coefficient of the atoms impinging on FECA droplet from the vapour phase and α' is the sticking coefficient of the substrate surface. Substituting equation (2.4), (2.5) and (2.6) into equation (2.7) we get the following.

$$\frac{dL}{dt} = \left[\frac{2\Omega_s J \sin\theta \lambda_f}{R}\tan(\frac{L}{\lambda_f}) + \frac{2\Omega_s}{R\cosh(\frac{L}{\lambda_f})}\frac{J\cos\theta\lambda_s K_1\frac{R}{\lambda_s}}{K_0(\frac{R}{\lambda_s})}\right]\alpha' + 2\Omega_s\frac{P - P_\infty exp(\frac{2\sigma_{lv}\Omega_l}{RK_BT})}{\sqrt{2\pi m K_B T}}\alpha \quad (2.8)$$

The first term of the above expression represents the diffusion of atoms impinging on nanowire sidewall. The second term represents diffusion from substrate surface along the nanowire. And the third term represents atoms impinging directly on the FECA from vapour phase. It has been experimentally observed that the sticking coefficient of the FECA droplet, α is two orders of magnitude higher than that of substrate surface, α' [19],[24]. This confirms the direct dependence of nanowire growth rate, $\frac{dL}{dt}$ on the effective impingement of the precursor material from the vapour phase, partial pressure of the precursor inside the reactor chamber, P and growth temperature, T.

2.3 Structure of VLS grown nanowires

Physical characteristics of a silicon nanowire is extremely important as electrical, mechanical and optical properties of the silicon nanowire depend on it. Growing nanowires with definite crystallographic orientation also helps maintaining a uniform separation between nanowires and assists in-place growth. Typically, VLS grown nanowires exhibit $\langle 110\rangle$, $\langle 112\rangle$ and $\langle 111\rangle$ growth directions. The growth direction is almost independent of the method used for growth. However, the growth direction and crystallography of the nanowires do depend on growth conditions such as temperature and pressure [6]. Another important phenomenon is the diameter dependence of silicon nanowire growth direction [26]. It has been observed that nanowires having diameter larger than 50 nm favour $\langle 111\rangle$ orientation. $\langle 110\rangle$ direction is preferred by nanowires having diameter less than 20 nm. There is always a probability that a fraction of nanowires would grow in the $\langle 112\rangle$ direction. This probability is significantly higher for wire diameters between 20 nm to 50 nm [27]. This diameter dependence can be associated with the scaling behaviour of different energetic contributions. The two most prominent of them are the contribution of the side faces and the contribution of the liquid FECA - solid interface. Both components are dependent

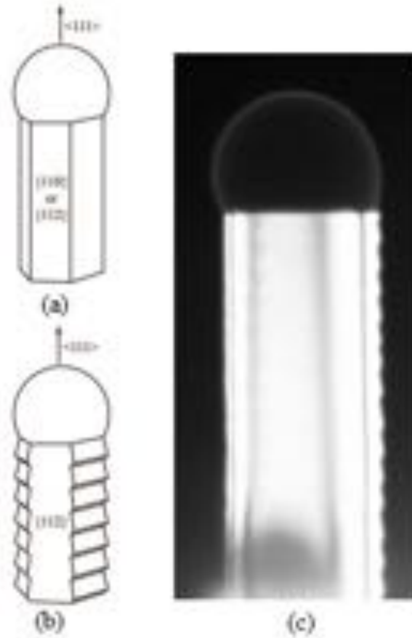

Figure 2.8: (a) Schematic diagram of a silicon nanowire with hexagonal cross section and crystallographically defined sidewall facets. (b) Schematic diagram of a nanowire with three sawtooth faces. (c) TEM image of such a nanowire. The image is taken from reference [25].

on the diameter of the growing nanowire. The thicker nanowires grow in such a direction which minimises the contribution of the FECA - solid interface and the thinner nanowires grow in a direction that minimises the contribution of the sidewalls. Like all other crystalline materials, silicon nanowires have a natural tendency to grow crystallographically defined surfaces. This behaviour becomes prominent at higher temperatures as surface diffusion becomes faster. It has been observed that $\langle 111 \rangle$ silicon nanowires exhibit hexagonal cross section with $\{110\}$ or $\{112\}$ surface facets [28]. This is schematically shown in figure 2.8(a). Similarly $\langle 110 \rangle$ oriented nanowires exhibit hexagonal cross section with four $\{111\}$ and two $\{100\}$ facets [29]. Silicon nanowires can also exhibit sawtooth faceting. For example, an [111] oriented silicon nanowire with hexagonal cross section and six $\{112\}$ faces can demonstrate a structure where three of the faces are flat planes and the other three are roughened in a regular sawtooth-like pattern [25]. A schematic diagram of such a nanowire is shown in figure 2.8(b). Figure 2.8(c) exhibits TEM image of one such nanowire. The crystal structure of silicon nanowires are typically assumed to be diamond like, identical to bulk silicon. Although Fontcuberta et al. [30] claimed to find evidence of silicon nanowires exhibiting wurtzite crystal structure. Properties of any material primarily depend on its fundamental structure. However the situation with nanomaterials are a bit different. Due to small size of nanoparticles and nanowires, the surface to volume ratio of

these materials is extremely high. Because of this, the properties of these materials are heavily influenced by their surface properties.

2.4 Applications of VLS grown nanowires

Silicon nanowires have found use in quite a large number of applications. Where some applications take advantage of the typical geometry, some rely on its size dependant or surface dominated properties. Extremely thin ($<$10 nm) silicon nanowires also exhibit quantum mechanical confinement effect. However, the focus of this report is on electrical characteristics of silicon nanowires, outside the realm of quantum mechanical effects. The following section presents a summary of the most common applications of silicon nanowires.

2.4.1 Templates

Silicon nanowires can be used as a template to make other nanostructures which are otherwise difficult to synthesise. For example, in a study, silicon nanowires coated with gold were subsequently furnace annealed at 880 °C and treated with HF. The SiOx formed by the earlier process were etched by HF in the later process, leaving only gold nanowires [31]. This process can also be used to synthesise magnetically hard materials. In another study, silicon nanowire templates were used to assemble Ni particles to form a quasi one-dimensional structure. This exhibits an enhanced coercivity of 315.2 Oe at room temperature [32]. Other than metal nanostructures, silicon nitride nanowires have also been grown using this method [33].

2.4.2 Solar cells

Solar cells are one of the most common applications of silicon nanowires. The main reason behind introducing silicon nanowires to photovoltaics is to reduce the cost of the effective material. Studies show a solar cell constructed using silicon nanowires can achieve efficient photon absorption by using just 1% of the active material required to construct a conventional silicon solar cell [35]. The solar cells constructed using silicon nanowires have few other advantages over conventional crystalline silicon solar cells fabricated using silicon wafers. For instance, unlike silicon wafers the substrate made of silicon nanowires can be of any shape and size. As a result, the short circuit current through the cell can be engineered. On the other hand, the shape

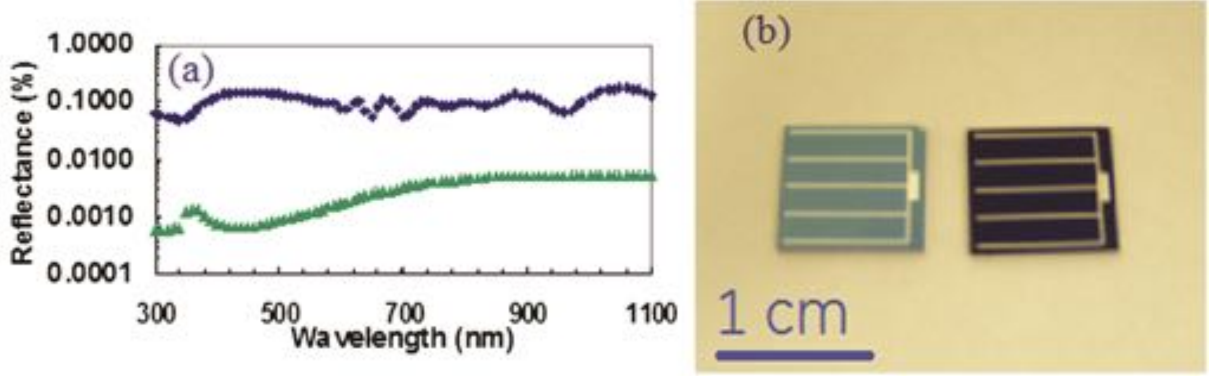

Figure 2.9: (a) Specular reflectance, in log scale, of conventional solar cell (blue curve) and silicon nanowire solar cell (green curve). (B) Photographs of conventional solar cell (faint green) and silicon nanowire solar cell (dark blue). Figures taken from reference [34].

and size of the silicon wafers is constricted by the wafer growth processes which has certain limitations. The short circuit current through a solar cell can be described using the following equation [36].

$$I_{sc} = qAG(L_n + W + L_p) \tag{2.9}$$

Here L_n and L_p are the minority carrier diffusion length of electron and hole. W is width of the depletion layer. G is the rate of carrier generation and A is the substrate area exposed to the incident illumination. This is why modulating A has such enormous effect on I_{sc}. Another advantage of using silicon nanowires as substrate is that thin layers of silicon nanowires are reasonably flexible. This property makes the silicon nanowires more interesting for solar cell application as it leads to the fabrication of flexible solar cell and roll-to-roll processing. Experiments also confirm that silicon nanowires demonstrate significant light trapping property. As a result, the energy conversion efficiency of silicon nanowire based solar cells may become as high as 12% [34] even after using so little material. After generation, separation of the charge carriers is of prime importance for the operation of a solar cell. A huge advantage of silicon nanowires is that they allow lateral diffusion of minority carriers, as in most cases the junction is located along the radial direction [34]. This phenomenon can dramatically increase I_{sc} and hence the efficiency of the solar cell as the efficiency is related to I_{sc} by the following equation [36].

$$\eta = \frac{I_{sc} V_{oc} FF}{P_{in}} \tag{2.10}$$

Here, P_{in} is the power of the input illumination, V_{oc} is the open circuit voltage and FF is the fill factor of the solar cell.

2.4.3 Lithium ion batteries

In conventional lithium ion batteries, to store one lithium ion in the anode, six carbon atoms are needed. On the other hand, one silicon atom can make alloy with more than four lithium ions. This was the motivation behind the research on silicon nanowires as an efficient anode material for lithium ion batteries. Other reasons behind the use of silicon nanowires as anode material for rechargeable lithium ion batteries are, its low-cost, good conductivity and scalability. It has been experimentally proven that silicon nanowire anode lithium ion batteries show larger charge capacity and longer cycling stability than conventional lithium ion batteries [37]. This is mostly because of the efficient charge transport and extraction-insertion of Li ions through the nanometer-scale rough surface of the anode.

2.4.4 Thermoelectricity

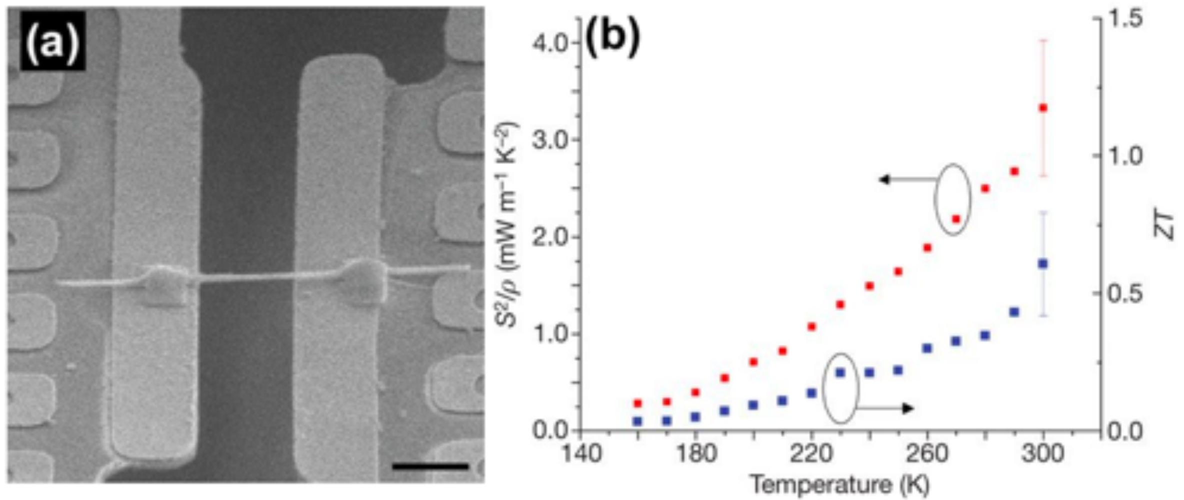

Figure 2.10: (a) A silicon nanowire device made to study the thermoelectric performance of the silicon nanowire. (b) Power factor, S^2/ρ (red squares) and thermoelectric figure of merit ZT (blue squares) of a silicon nanowire of diameter 52 nm. The figures are taken from reference [38].

The simplest measure of how good a thermoelectric material, is to look at a quantity known as thermoelectric figure of merit. Most commonly used thermoelectric material is bismuth telluride (Bi_2Te_3) and its alloys. Their thermoelectric figure of merit, ZT $\approx$1. The thermoelectric figure of merit can be defined using the following equation.

$$ZT = \frac{S^2 T}{\rho k} \tag{2.11}$$

Where, S is the Seebeck coefficient, ρ is the electrical resistivity and k is the thermal conductivity of the material. Despite being the material of choice, Bi_2Te_3 has a major problem. It is very difficult to scale bulk Bi_2Te_3 for large scale energy conversion. Fabricating nanostructured Bi_2Te_3 is even more difficult and expensive. On the other hand, bulk silicon has thermal conductivity of 150 W m^{-1} K^{-1} at room temperature [39]. This leads to a rather low ZT ($\approx$ 0.01) [40]. Silicon nanowires have Seebeck coefficient and electrical conductivity same as bulk silicon but the thermal conductivity of silicon nanowires are a function of its diameter. For example, a silicon nanowire of diameter about 50 nm can exhibit 100 fold reduction in the value of k and therefore exhibit ZT = 0.6 at room temperature [38]. Unlike Bi_2Te_3, silicon is an abundant material in earth's crust. Also the established infrastructure to support low cost, high yield processing of silicon makes silicon nanowire a promising material for waste heat recouping, solid-state refrigeration and alternative energy production.

2.4.5 Sensors

The operation of silicon nanowire sensors are mostly based on the following two principles. (i) Surface-enhanced Raman scattering (SERS) and (ii) field-effect transistors (FETs). It has been observed that silicon nanowires, coated with metals, are capable of enhancing Raman signals based on SERS effect. Using this phenomenon a detection limit as low as 600 molecules [41] can be achieved. Silicon nanowires, coated with gold, were used to detect dichlorvos (a pesticide) at a concentration of 8ng/L [42]. Nanowires coated with silver are being used for the detection of many biological molecules like rhodamine 6G [43] and calf thymes DNA [44]. These nanowires have also demonstrated excellent surface-enhanced fluorescence of lanthanide ions [45].

Silicon nanowire FETs, on the other hand, were used to sense the presence of heavy metal ions in a solution. An increase of current in the linear IV region of the FET has been reported with increasing concentration. In one reported experiment, a silicon nanowire FET demonstrated very high sensitivity to heavy metal ions. The device was able to detect Cd^{2+} ions upto 10^{-4} M and Hg^{2+} ions upto 10^{-7} M [46]. These solutions were streamed with a steady flow, over the gate region of the FET. Other than heavy metal ions, silicon nanowire FETs have also been used to successfully detect other molecules like deoxyribonucleic acid (DNA) with a detection limit in the sub-femtomolar level [47].

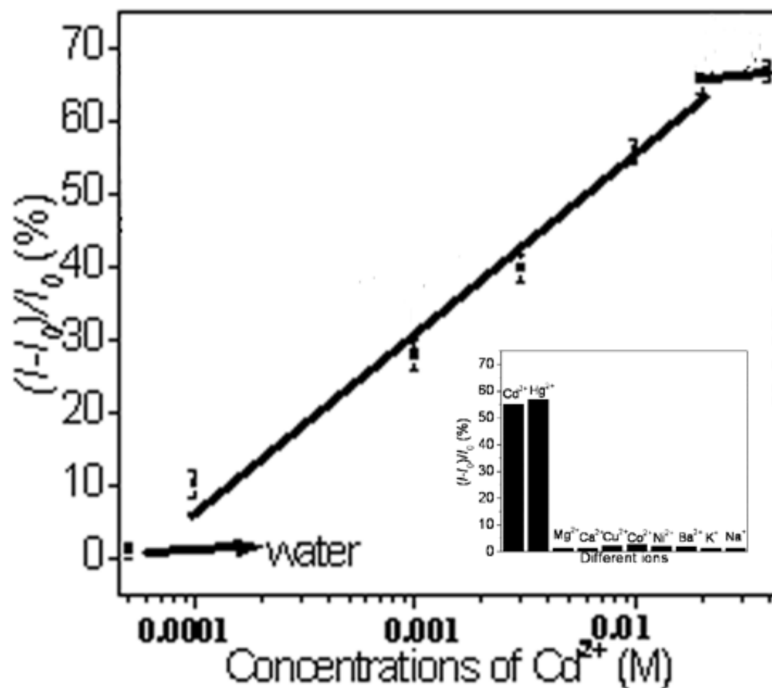

Figure 2.11: Percentage change in current vs Cd^{2+} concentration. Inset shows the selectivity of the sensor over different metal ions. The figure is taken from reference [46].

2.4.6 Targeted delivery into biological cells and tissues

One of the most important developments in research of biological applications of silicon nanowires took place when Nagesha et al. [49] successfully reported cell assays with silicon nanowires. The authors also reported 'in vitro' (in test tube) gene delivery using silicon nanowire arrays. In another reported experiment, mouse embryonic stem (mES) cells and human embryonic kidney (HEK 293T) cells have been cultured on a silicon nanowire array. The nanowires were previously functionalised with electrostatically deposited plasmid DNA. One day later, some of the cells returned positive result to green fluorescent protein (GFP) test [50]. This signifies successful delivery of exogenous gene to the mammalian cell and normal function of the cell after that.

The lack of proper control on maintaining therapeutic level of conventional drug delivery systems such as peroral or topical, motivated the researchers to focus more on the development of targeted drug delivery systems. Research on silicon nanowire arrays revealed that silicon nanowires are bioresorbable [51] and possess strong antibiofouling property. These findings along with the results of cell assays show that silicon nanowires are congruent with 'in vivo' (inside living organism) applications. The drug release profile of silicon nanowires have been observed experimentally, in which, an array of silicon nanowires released antibiotics (penicillin

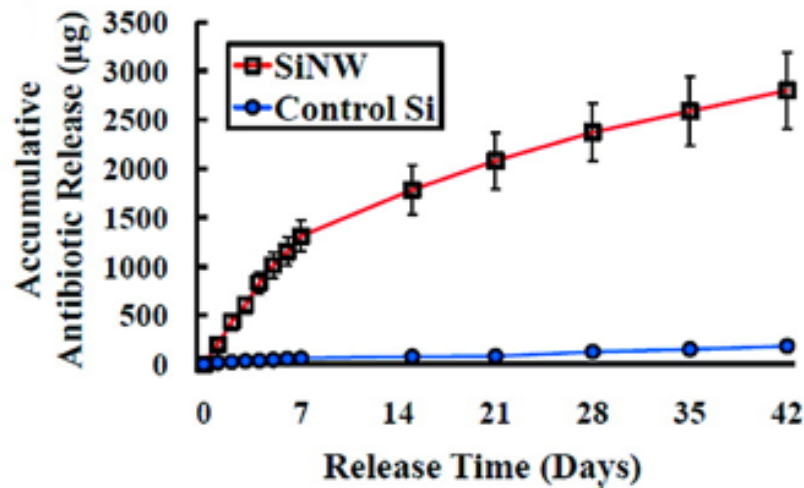

Figure 2.12: Absolute release of penicillin + streptomycin solution plotted as a function of sampling time. The average release amount is represented by the discrete points. The figure is taken from reference [48].

+ streptomycin) within therapeutic window for 42 days [48]. The drug release profile from silicon nanowire array showed near zero-order kinetics over time which means that the release of drug is independent of the remaining concentration of drug in the nanowire array. It makes silicon nanowires an exceptionally stable source for drug delivery.

2.5 Discussion on the electrical properties of 'non-quantum' silicon nanowires

The definition of what can be called as 'nanowire' is subjective. However, in our work, we have referred to single crystals of silicon with diameter in nanometer range as silicon nanowires. This includes wire-like structures of silicon with diameter roughly upto 300 nm. Using this definition includes very thin nanowires with diameter only a few nanometers (< 10nm) as well. The properties of those ultra-thin nanowires is not discussed or studied in this report. The main reason behind this is that, they exhibit some peculiar characteristic which is far from the silicon nanowires grown by us (diameter in the range about 350 nm to 50 nm). For instance, the first principle calculations of the electronic properties of silicon nanowires revealed the fact that the band-gap of very thin silicon nanowires are fundamentally different from that of crystalline bulk silicon or polysilicon. Basically the electronic band gap has a inverse relationship with the diameter of the silicon nanowires. Nevertheless, this is true only for silicon nanowires with diameter of 5 nm or less [52]. Later on, several experiments have been conducted to test this hy-

pothesis. In one of the experiments [29], ultrathin silicon nanowires with diameter ranging from 7nm to 1.3 nm were fabricated and their electronic band-gap was experimentally determined using Scanning Tunneling Spectroscopy (STS). The results of that experiment completely support the previous hypothesis which can be observed in figure 2.13.

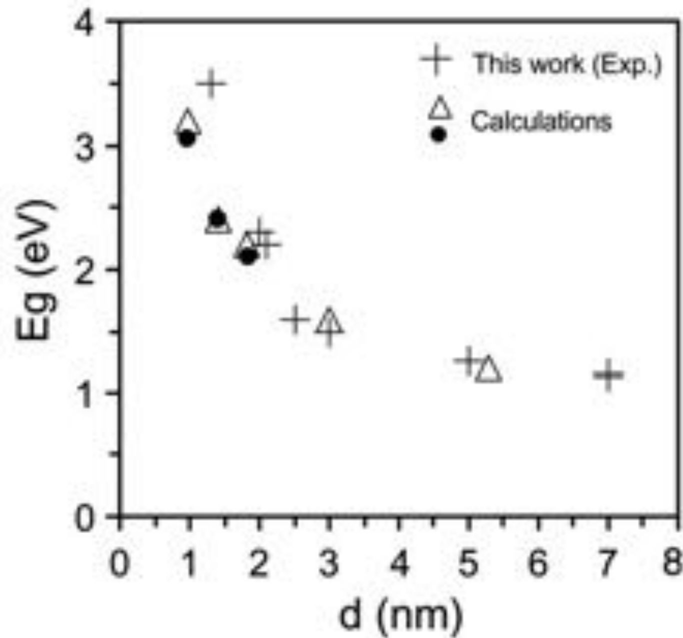

Figure 2.13: Experimentally determined band-gap of ultrathin silicon nanowires. The figure is taken from reference [29] in which the authors compared the results of their experiment with mathematical models such as reference [52].

Both theoretical and experimental studies support that it is acceptable to assume that size dependant and quantum mechanical effects such as widening of band-gap is irrelevant while discussing the electronic properties of silicon nanowires with diameter ranging from 350 nm to 50 nm [53]. This assumption will be used throughout this report unless mentioned otherwise. In spite of the absence of any confinement related phenomenon in electronic properties, it will be completely inaccurate to assume the properties of silicon nanowires described here to be similar to bulk silicon. Like other nanomaterials, silicon nanowires possess a large surface to volume ratio. This is true even for nanowires with relatively larger diameters (such as 350 nm). Which means, the properties of the surface of this material have huge impact on the overall properties of the material. This is a great departure from bulk materials. On top of that, the outer surface of any structure of silicon has a tendency to get oxidised to form native oxide. Silicon nanowires are no exception to this. It is almost impossible to find a silicon nanowire, in real world, without a thin layer of native oxide on its surface. Treatment with hydrofluoric acid can momentarily

remove this thin oxide and terminate the outer surface with hydrogen bonds. But other than that it is always a good idea to assume the existence of a few monolayer thick SiOx on the surface of a silicon nanowire for any practical purpose.

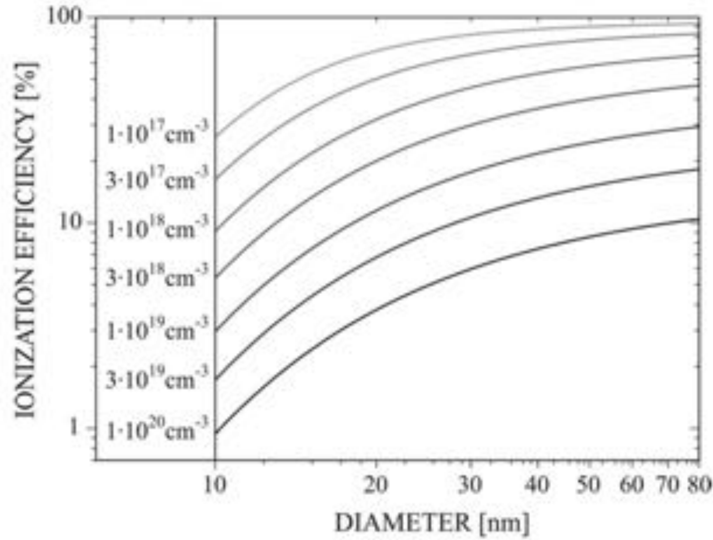

Figure 2.14: Variation of impurity ionization efficiency with diameter of silicon nanowires. Image taken from reference [54].

Whether hydrogen terminated or SiO_2 covered, any real life nanostructure of silicon must have a finite number of dangling bonds. In other words, it is highly unlikely that all unsatisfied bonds at the surface become terminated by oxygen, hydrogen, or any other species. This leads to the creation of surface charges and interface trapped charges on the nanowires and this is one of the most influential factors determining the electrical characteristics [6]. Quantum confinement is not observed in the nanowires of our interest. But there is another type of confinement called dielectric confinement, existence of which in silicon nanowires has been experimentally proven. It was first observed when an anomaly in relating the conductivity of a doped silicon nanowire to its experimentally determined doping concentration was found [55]. In a typical experiment, VLS grown silicon nanowires are doped in-situ (inside the growth chamber, during VLS growth) with phosphorus and boron. After growth, their conductivity is measured by using a four-probe method followed by measurement of dopant atom concentration by Secondary Ion Mass Spectroscopy (SIMS). It was reported that, the conductivity of silicon nanowires was one order of magnitude less than what was expected from the knowledge of equivalent bulk silicon doping. Because, in bulk silicon the coulomb potential of impurity nucleus is strongly screened. But, in silicon nanowires, because of the geometry of the material, impurity atoms are not surrounded by a semi infinite ensemble of silicon atoms. This leads to dielectric mismatch

between the surrounding and wire material. As a result, energy required for impurity ionisation increases. This phenomenon is commonly known as dielectric confinement. Effect of this can be observed in figure 2.14 taken from reference [54]. In this, ionisation efficiency (100 % means all impurities are ionised) is studied as a function of the diameter of a silicon nanowire. Decrease in wire diameter results in increase in surface to volume ratio. This, in turn, increases dielectric confinement and thereby decreasing ionisation efficiency.

2.6 Transport through silicon nanowires

The revival of research interest in silicon nanowires, at the begining of twenty first century, stems from the fact that it is the smallest dimension structure for efficient transport of charge carriers (electrons and holes) through silicon [2]. As the resurgence continued, it has been observed that this material can be further designed to act like electron devices such as diodes [56], transistors [57] or more complicated [58] devices. However, the abundance of publication on a variety of microelectronic devices made using silicon nanowires did not extend to the study of charge carrier transport. In this work, we have made the study of charge carrier transport through silicon nanowires, one of the central objectives. An effective way to get a reasonable understanding of the conceptual status quo of this subject, would be to look at several seminal articles which deals with transport through silicon nanowires, starting with the work of Heath et al. [59], who modelled transport through silicon nanowires when a silicon nanowire is connected to several metal contacts. According to them, when two or more metal contacts are connected to a single silicon nanowire, to extract its characteristics, the current always flows through a metal contact, into silicon, and to metal again. This is why the characteristics is always determined by reverse bias characteristics of Schottky diode. However, this metal-semiconductor contact resistance is quite low when compared to the resistance of the actual silicon nanowire which is technically connected in series (figure 2.15(a)).

But these metal-semiconductor contacts carry out most of the non-linearities of the current-voltage characteristics. The magnitude of this effect will hugely depend on the diameter of the silicon nanowire. This argument is rather admissible with experiment, where structures like these are subjected to a long anneal (figure 2.15(b)), have shown consistent improvement of conductivity [60]. The silicon nanowires in this experiment were grown by VLS method using gold as catalyst. It is experimentally proven that VLS grown silicon nanowires have catalyst

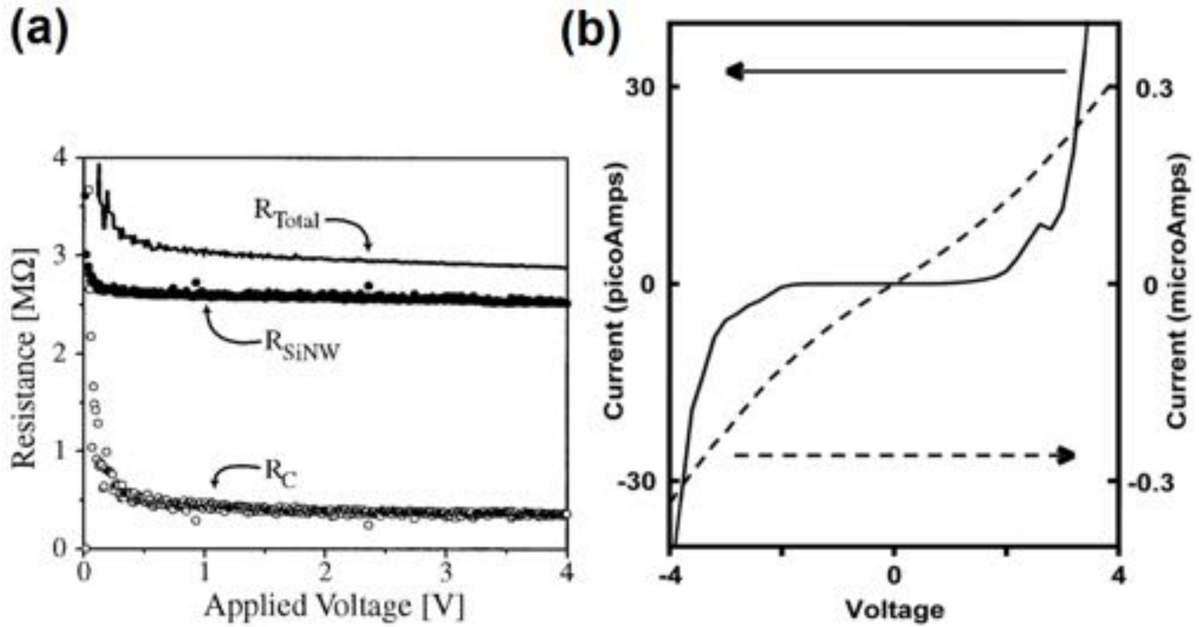

Figure 2.15: (a) Comparison of contact resistance with resistance of silicon nanowire (which is acting as channel). The graph is taken from reference [59]. (b) IV characteristics of silicon nanowires (diameter 20 nm) contacted with Ti/Au electrodes, before (solid) and after (dashed) annealing at 750 °C for 1 hour. The graph is taken from reference [60].

(used to grow the nanowire) all over its surface [13] and volume [61]. Not necessarily, all the gold catalysts accumulated in the silicon nanowire during VLS growth are at the substitutional sites (in other words, thermally activated). According to the authors of the study, a long anneal can thermally activate more gold atoms inside silicon nanowire. Gold is a p-type dopant in silicon alongside being a deep level impurity [62]. Therefore, a change in thermally activated gold concentration inside silicon nanowire can change the hole doping level, and in turn change the metal-semiconductor barrier (contact resistance). This could be the reason for conductivity improvement after annealing. Other publications also follow this conceptual framework of electrical transport through silicon nanowire devices. For example, in experiments, where characteristics of same silicon nanowire are extracted using both, two-terminal and four-terminal measurements, it has been observed that the four-terminal IV characteristics is much more linear and conductive than its two-terminal counterpart [57]. These observations led to the belief that the metal-semiconductor junctions at the contacts add both contact resistance and non-linearity to the characteristics. A four-probe measurement essentially nullifies the effect of contacts, thereby producing a more linear characteristics with higher current level. In silicon nanowire transistors, where the conductivity between source and drain contacts is varied by application of gate bias (figure 2.16), the gate response is primarily attributed to the variation

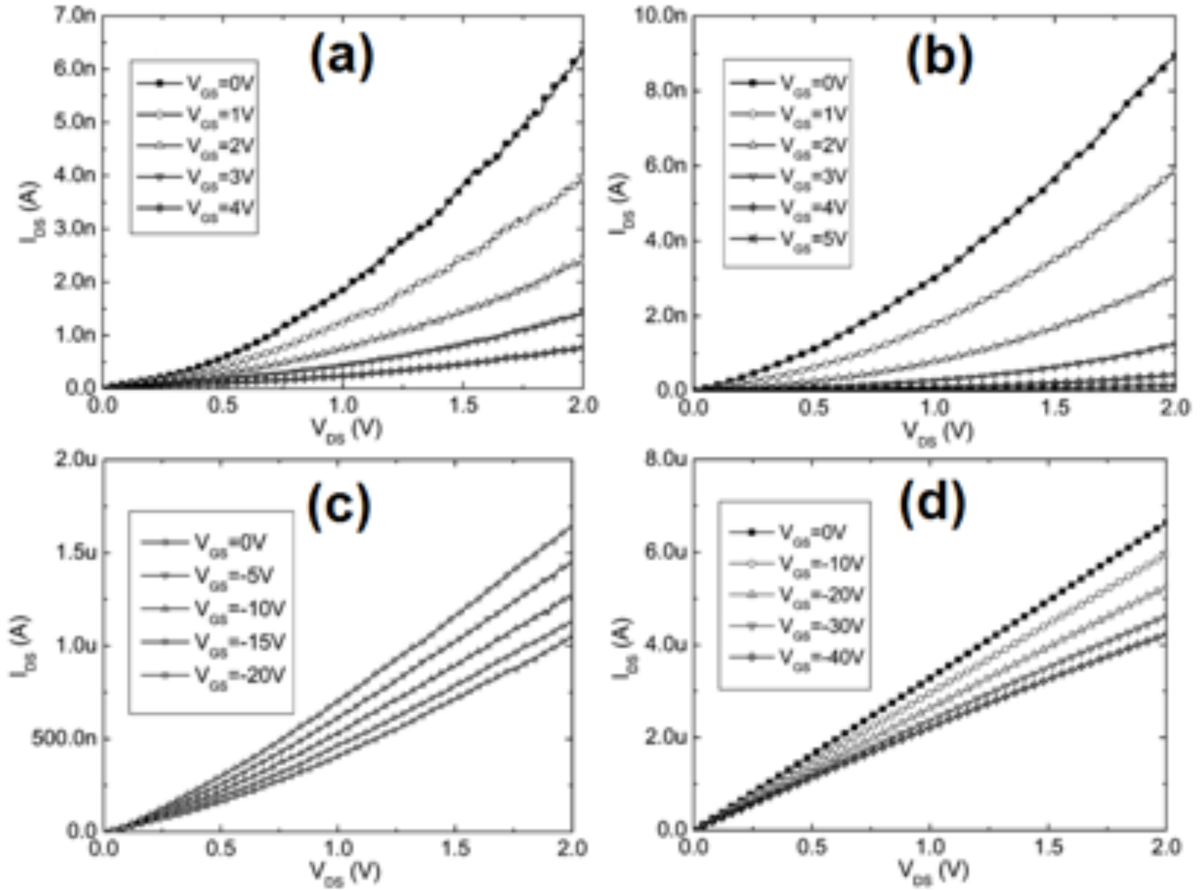

Figure 2.16: Output characteristics of back-gated SiNWs grown with the following volumetric ratios of dopant to precursor in the inlet gas to the process chamber. (a) [P:Si] = 0, (b) 2×10^{-5}, (c) 7×10^{-5}, and (d) 2×10^{-4}. The plots are taken from reference [55].

of contact barriers by applied gate bias rather than accumulation, inversion and depletion of the channel [55]. This is a rational claim as the nanowire devices used for this experiment didn't have n-p-n or p-n-p doping regions like traditional MOS transistors. In fact, the devices were just silicon nanowires lying on oxidised silicon wafers, connected to multiple metal contacts with metal contact on the back surface of the substrate acting as gate terminal.

Most of the reports of experimental characterisation and modelling electrical characteristics of silicon nanowires, so far, revolved around the injection of charge carriers into silicon nanowires through the modulation of metal-semiconductor contact barriers. This is due to the lack of experimental results that establishes the transport of charge carriers through silicon nanowires as an important factor in defining the overall electrical characteristics of silicon nanowires. In some cases, where the nanowires are very thin (less than 7 nm) [29], or the nanowire is made using a harsh process, which led to silicon nanowires with crystal defects throughout its surface [63], the effect of surface is brought into consideration and identified

as a crucial factor in determining the electrical characteristics. But, for most part, the silicon nanowires were considered as a resistor, whose value is determined by the intentional or unintentional doping during fabrication.

This work, however, focuses on extracting information about the transport characteristics of the silicon nanowires. Whether any characteristic peculiarity is inherent to the VLS grown nanowires. To make sure, the characteristics is not induced from surface or confinement related effects, silicon nanowires in the diameter range of 50 nm to 350 nm are studied. To avoid any impurity related effects and to make the silicon nanowires more resistive than the contacts, the nanowires are left intrinsic. In this way, the characteristics of the fabricated nanowire devices is dominated by the silicon nanowire channels, rather than the silicon-metal contacts. This electrical characteristics is then compared to simulation results with different transport models. It has been found that, transport in VLS grown silicon nanowires is dominated by Poole-Frenkel mechanism. Physical origin of this transport is then investigated using physical characterisations.

Chapter 3

Experimental techniques

3.1 Cold-wall catalytic chemical vapour deposition (cat-CVD)

Cold-wall catalytic chemical vapour deposition (cat-CVD) is a technique of material deposition which relies on the chemical reaction on the surface of the substrate. In this way it is similar to conventional CVD. However, the difference lies in the way energy is supplied to the system. In a typical CVD, a chemical precursor is passed through a tube furnace. The substrate is kept inside the furnace and the entire chamber is heated from outside. Since the external heating elements apply high temperature to almost the entire wall of the chamber, the conventional CVD chambers can be referred to as hot-wall CVD chambers. These are widely used because of relative ease of construction and operation. However, one disadvantage of using the conventional CVD in our case is due to the nature of reaction. We have used SiH_4 as the source of Si in our reaction. To get Si from SiH_4, the precursor has to undergo a dissociation reaction, in which Si atoms and gaseous H_2 are formed. But, this dissociation reaction has to take place on the substrate surface, not elsewhere. Otherwise the anisotropic growth required for the growth of silicon nanowires can't be achieved. Instead, an isotropic silicon deposition will cover the substrate. There are several ways of tackling this. One way is using a catalyst. Catalysts bring down the activation energy of the dissociation reaction. Now, if the temperature of the reaction chamber is set to a value such that it is sufficient for catalysed dissociation of SiH_4 but not un-catalysed dissociation, then the reaction will take place only on the sites where the catalyst is present. There is another way of restricting the reaction to the surface of the substrate. By placing a heating element under the substrate and removing heating elements from the wall of the reaction chamber, this can be achieved. This, along with the help of catalyst, is known as

catalytic chemical vapour deposition (cat-CVD).

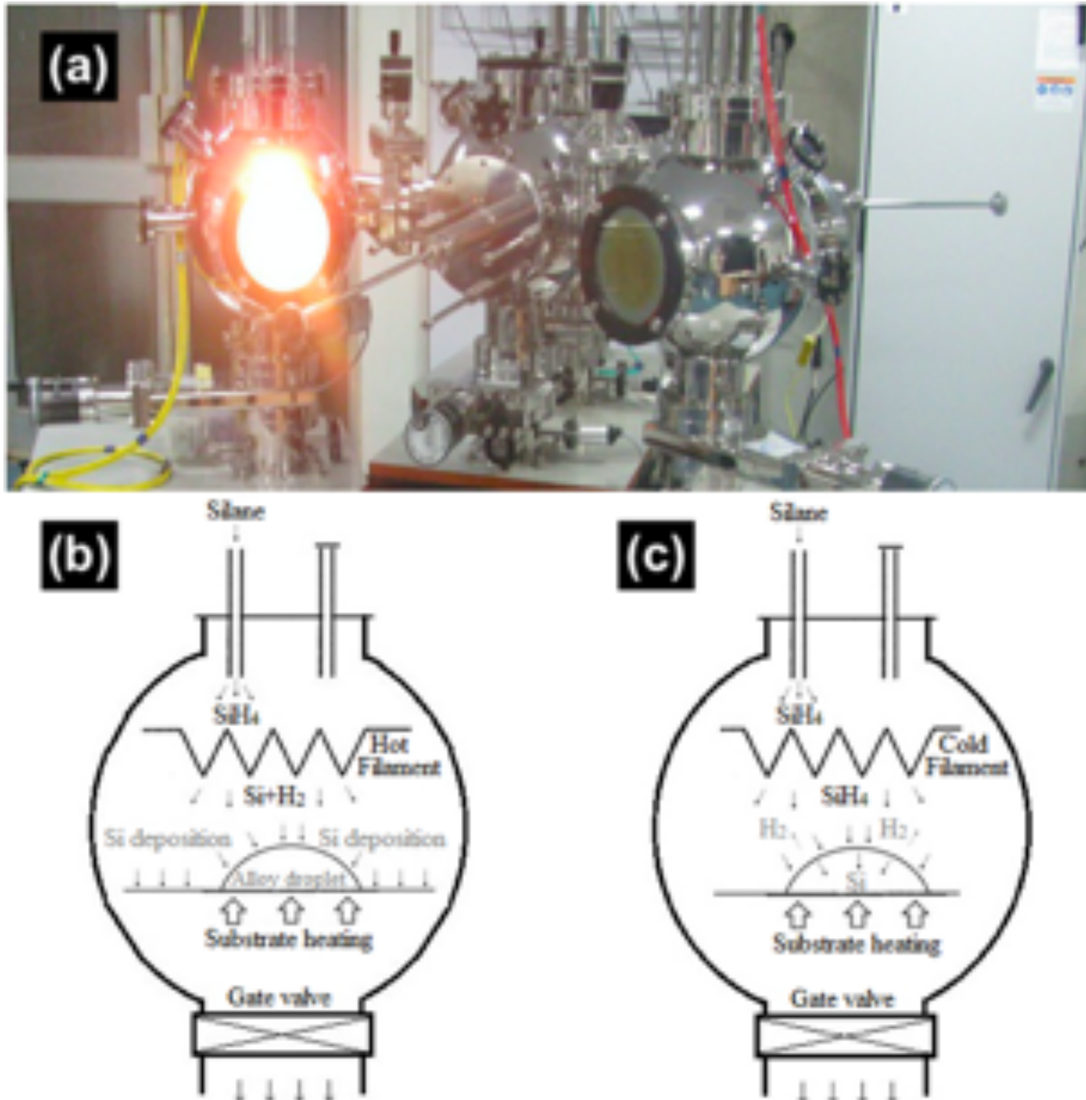

Figure 3.1: (a) Photograph of the cat-CVD instrument used for the silicon nanowire growth by VLS method. The image is taken from our laboratory website (URL: http://www.cen.iitb.ac.in/cen/index.php). (b) Schematic diagram explaining the tool's operation in HWCVD mode (glowing reaction chamber in the photograph). (c) Schematic diagram of the tool's operation in CVD mode (the right reaction chamber in the photograph).

Figure 3.1(a) exhibits a photograph of the instrument used for this study. The spherical chambers seen in this image act as reaction chambers. The chamber on the left can be seen to glow but not the chamber on the right. This is because of the different modes of operation. Schematic diagrams explaining the different modes are presented in figure 3.1(b) and (c). SiH_4 is used as a precursor for Si and flown inside the chamber through mass flow controllers (MFC). When the filament near the precursor gas inlet is turned 'on', and SiH_4 is passed, the precursor immediately dissociates into solid Si and H_2 gas. This is shown in figure 3.1(b). However, the

precursor reaches the substrate, unperturbed, when the filament is turned off. The difference in the silicon nanowires grown using these two methods are detailed in chapter 4. The gasses inside the chamber are taken out by an exhaust fitted at the bottom of the spherical reaction chamber. A gate valve is fitted near the exhaust to control this. The valve can also be used, along with the MFC in the inlet, to modulate the pressure inside the chamber.

3.2 Scanning Electron Microscope (SEM)

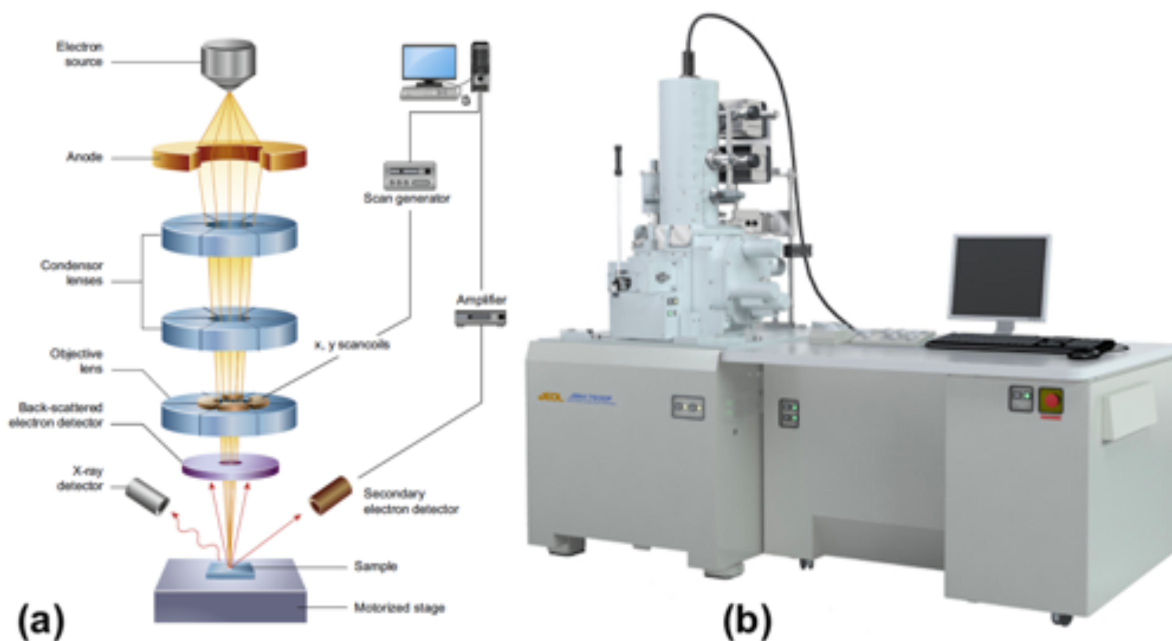

Figure 3.2: (a) Schematic diagram exhibiting the operating principe of an SEM instrument. The figure is taken from reference [64]. (b) Photograph of the instrument used in this work. The image is taken from the website of the manufacturer (URL: http://www.jeol.co.jp/en/products/detail/JSM-7600F.html).

Scanning electron microscopy (SEM) is used throughout this work as one of the primary physical characterisation techniques. Even though SEM analysis could result in destruction of the sample, specially in case of biological samples. In our work, we found SEM to hardly affect the quality of the samples. This is partly because of how electron beam interacts with our sample and partly due to the nature of our study. A schematic of fundamental processes responsible for operation of an SEM tool is exhibited in figure 3.2(a). Photograph of the tool used in this work is presented in figure 3.2(b). The vertical cylinder, connected to the black power line on top, is known as the electron column of the instrument. The top of the column acts as the source of electron schematically shown in figure 3.2(a). The sample is placed at the

bottom of the column. Electrons from the electron source are accelerated towards the sample by an anode placed inside the column close to the electron source. Electron sources are commonly known as electron guns due to their electron emitting nature. Based on the principle of electron emission from the electron gun, SEM systems are broadly divided into two categories. Thermal SEM and field-emission gun SEM (FESEM). Among these two variants, the latter offers higher resolution in exchange of higher cost. The instrument used for the analysis presented in this work is a FESEM. After emission from gun, and acceleration by the anode, the electrons pass through a number of magnetic lenses. These magnetic lenses condense and focus the electrons to create a beam using Lorentz force. For this reason, these lenses are commonly referred to as condenser lenses. In between these lenses, electron beam paths may collimate or converge to a point and then diverge again, depending on the design of the column. The last of these lenses, close to the sample, is known as the objective lens. This lens is fitted with capability of performing raster scan over sample. Depending on the desired magnification, the raster scan can cover a large or small area. Smaller area results in higher magnification. Finally, near the bottom of the column, the electron beam passes through a small aperture. Most SEM systems are fitted with a few switchable apertures. The user may chose an aperture size depending on the demand of the analysis. A smaller aperture size will result in lower noise in the image. But doing so will also result in an increase in depth of focus. Intensity of the image will decrease as well. The electrons in a SEM are typically accelerated by an anode potential of 0.1 kilovolt to 30 kilovolt. When an electron beam with such high energy strikes the sample, several phenomena take place. However, in the context of SEM, a few of them are actually of interest. After impact on the sample surface, most of the impinging electrons will penetrate the sample to a certain depth, propagating through numerous scattering events. During each scattering event, the electrons from the column, may change their path or exchange energy or both. These scattering events may actually be elastic or inelastic. A portion of the electrons, striking the sample, may come out of the sample after several scattering incidents. These electrons are known as backscattered electrons. They are high in energy and can be used to image samples. To form an image of the sample, using backscattered electrons, a backscattered electron detector has to be fitted at the bottom of the column. Typically, images using backscattered electrons are useful for compositional analysis of the sample because the number of protons (positive charge) at the centre of an atom and the number of electrons (negative charge) in the electron cloud around it, greatly impact the scattering of electrons inside the sample. During impact on

the surface as well as scattering inside the sample, the impinging electron also transfers energy to the electron cloud of numerous atoms of the sample. The transferred energy is usually so large that it results in electron emission from the sample atoms. These electrons are known as secondary electrons, because they are emitted from the secondary source, which is the sample itself. The secondary electrons are also useful for imaging the sample. To image with secondary electrons, a secondary electron detector has to be fitted, in vicinity of the sample, inside the vacuum chamber of the instrument. Since secondary electrons are low in energy, the secondary electron detector has to be covered with a Faraday cage to collect the electrons. An image taken with secondary electrons usually provide good information about the topography of the sample. The tool used for this study is JSM-7600F FEG-SEM by Jeol Ltd.

3.3 Transmission Electron Microscope (TEM)

In many ways transmission electron microscopes (TEM) are similar to SEM. However, the biggest difference lies in how image is captured in these systems. In TEM, electrons which transmit through the sample are analysed. This puts a much more stringent requirement on samples. Extremely thin and electron transparent samples are required for TEM analysis. Also, the energy of the electrons in the electron beam is much higher compared to SEM. In a typical TEM instrument, 80 kilovolt - 300 kilovolt is applied to the anode to accelerate electrons emitted from the electron source. Figure 3.3(a) exhibits a schematic of TEM operation. Photograph of the actual instrument used for this work is presented in figure 3.3(b). Like SEM, the vertical cylinder here is also known as the column of the instrument. However, the biggest visual difference from SEM is in the size of the column. One of the main reasons why columns of TEM instruments are longer because they have to accommodate a higher number of lenses. In a TEM instrument, the electron beam is converged before the sample to have a small area of interaction with the sample. The objective lens is placed under the sample to create image of the sample. The beam then traverses through multiple apertures and detectors. At the bottom of the column, the beam strikes a fluorescent screen to create the image. During analysis, the image can be observed from this screen. However, to digitise and capture images, modern TEM instruments are fitted with a charge-coupled device (CCD) camera, which is typically placed under the image viewing screen. The tool used for the study is a Tecnai G2 F30 TEM by FEI.

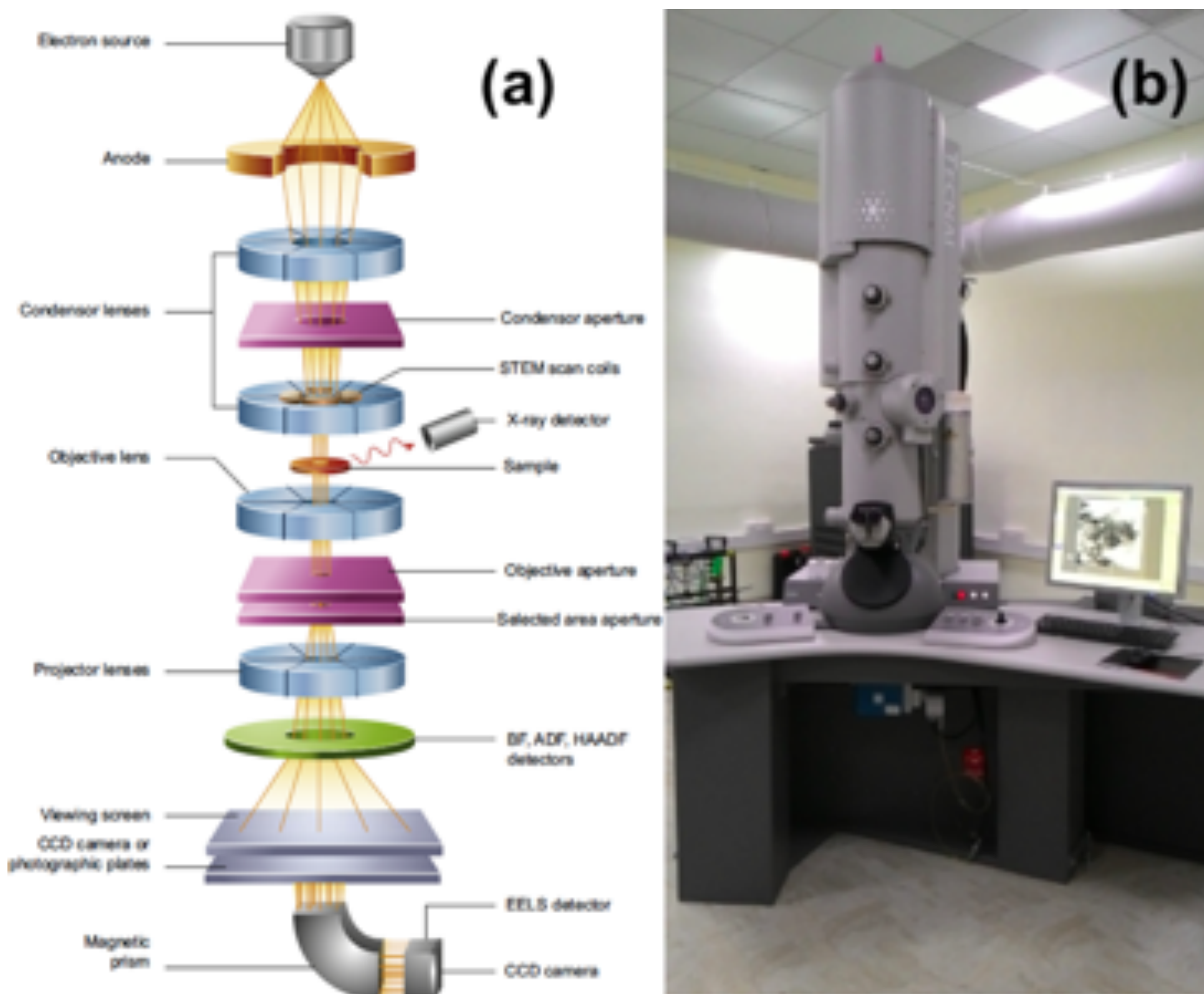

Figure 3.3: (a) Schematic diagram exhibiting the operating principle of an TEM instrument. Figure taken from reference [64]. (b) Photograph of the instrument used in this work. Image taken from IIT Bombay sophisticated analytical instrument facility website (URL: http://http://www.rsic.iitb.ac.in/hr-tem300kv.html).

3.4 Selected Area (Electron) Diffraction (SAED)

Even though a solid sample may look like a continuous, dense object, for a high energy electron travelling through the sample, the sample actually appears as periodic arrangement of positively charged nucleases surrounded by negatively charged electron cloud. This arrangement may or may not have long range order. Nevertheless, due to the wave property of electrons, this results in constructive and destructive interference of the passing electron waves. If a detector or fluorescent screen is placed below the sample in a TEM column, different patterns can be resolved corresponding to the probability of finding electrons in a plane parallel to the sample. This is useful information because the pattern created in this way, depends on the arrangement of atoms inside the solid sample. Figure 3.4 presents three distinct examples of SAED taken from ref-

erence [65]. Typical example of a SAED pattern generated by a crystalline sample is exhibited in figure 3.4(a). It can be seen from the image that, passing through the crystalline sample, electrons have created periodic arrangement of high and low electron density in the plane of the detector. This plane is parallel to the plane of the sample. Periodicity in this pattern is related to the sample lattice in k-space. Many of the vectors from the sample's k-space can be calculated by measuring the relative distance between the bright spots. This presents information about different lattice planes and d-spacing of the sample. Figure 3.4(b) and (c) exhibit SAED pattern of a polycrystalline and amorphous sample. SAED pattern of polycrystalline samples look like concentric hollow circles with a bright circular region in the middle. The radius of each circle corresponds to a family of lattice planes. The electron diffraction patterns reported in this work are taken using the same tool as the TEM images, Tecnai G2 F30 TEM by FEI.

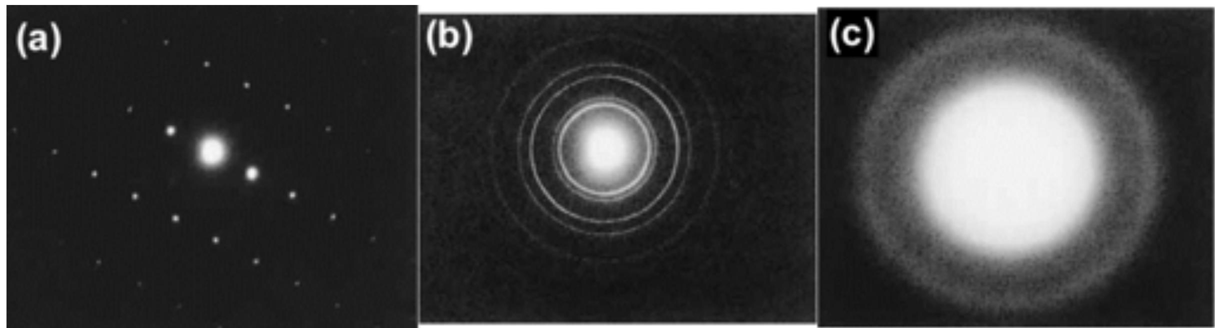

Figure 3.4: (a) Electron diffraction pattern of a typical single crystalline sample. (b) Electron diffraction pattern of a polycrystalline sample. (c) Electron diffraction pattern of a amorphous sample. Figures are taken from reference [65].

3.5 Energy-Dispersive X-ray spectroscopy (EDX)

At the heart of any SEM or TEM system is a high-energy electron beam, interacting with the sample. In most of the tools (both SEM and TEM), this is achieved by accelerating electrons emitted by an electron source using magnetic lenses inside the column. These accelerated electrons are also condensed into a beam before they strike the sample. When these electrons strike the sample, electrons come out of the sample in the form of Auger electrons, back-scattered electrons or secondary electrons. These electrons from the sample are analysed to form images. However, the sample-electron beam interaction not only ends by producing electrons in response to electrons only. Because of the high energy of the accelerated electrons, sometimes core electrons of the sample atoms can be knocked out of the shell as well. In that case, the

atom relaxes by rearranging its electrons. Sometimes one or more valance electrons can move to the core shells to maintain the stability of the atom. When this happens, the excess energy is radiated in the form of packets electromagnetic wave. If the transition is large, the dissipated energy has to be large. In that case, the sample may emit X-ray. For smaller energies, the sample may emit photons. In most practical situations, all these phenomena happen simultaneously. Therefore, a sample hit by a high-energy electron beam could emit photons and X-rays dispersed over a range of energies. Since these energies are correlated to the energy transitions of the sample atoms, analysing these energies quantitatively can result in identifying the atomic composition of the sample. One of the ways to do that, is by installing a X-ray detector in the vicinity of the sample. This characterisation technique is known as energy-dispersive X-ray spectroscopy or EDX. It has been widely used in this work to figure out the elements present in solid samples. The EDX results presented in this work are taken from either Jeol JSM-7600F FEG-SEM or Jeol JEM 2100F HR-TEM fitted with X-ray detector by Oxford Instruments plc.

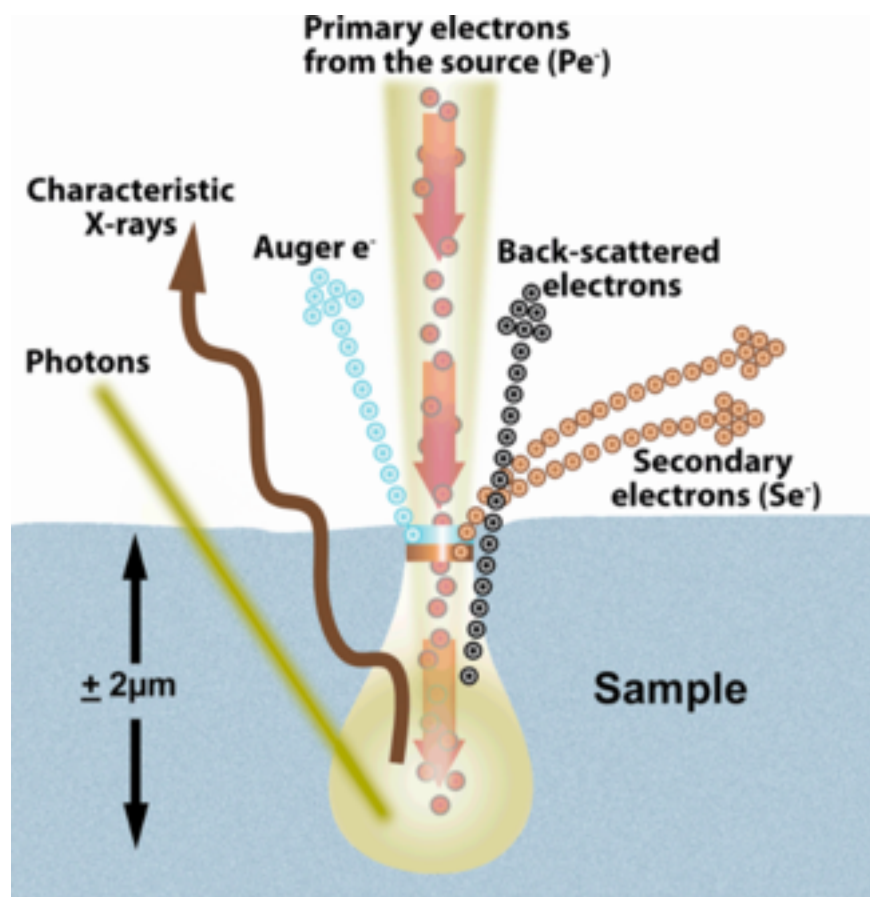

Figure 3.5: A schematic diagram explaining important features of interaction of a high-energy electron beam with a solid sample. The figure is taken from reference [66].

3.6 Electron Beam Lithography (EBL)

Lithography is one of the most ubiquitous and important processes of making and studying electronic devices since the beginning of VLSI era. As a matter of fact, throughout the history of VLSI devices, lithography was one of the defining steps for most of the developments. Lithography is mainly used to facilitate selective addition or removal of materials from a sample. During fabrication of devices for electrical characterisation experiments, several unit processes are required which consist of such selective addition or removal. However, for industrial applications, innumerable unit processes have to be performed in perfect synchronisation to achieve a cutting edge design specification. Another important factor in industrial processing is scaling. Most of the unit processes in industrial production is designed with batch processing in mind. It is as important as meeting the design specifications. For this reason optical lithography is preferred by most industrial applications. The resolution of the features obtained by optical lithography is inversely proportional to the numerical aperture of the optical lens and proportional to the wavelength of the light source. Since optical lenses can only be made with a finite numerical aperture, the wavelength of the light source becomes the deciding factor in determining the resolution. For most commercial fabrications, argon fluoride laser with wavelength of 193 nm is used as light source. The situation is different in small scale research laboratories. In this case, the devices are made in small numbers. Sometimes even a single device may also get fabricated. Therefore, most of the emphasis is given to achieve as high accuracy as possible. By replacing ultraviolet, visible or infrared light with a beam of electron, many of the problems can be avoided. This also leads to much higher resolution. Another important difference between commercial lithography and lithography for research is that, instead of using the same pattern repeatedly, research laboratories have to make consistent changes in the patterns to accommodate the findings. Conventional optical lithography needs a physical mask to write a pattern, where in EBL, the pattern is generated by executing a set of instructions from a computer. This is known as a pattern generator. To achieve this, the sample stage is fitted with motors and microcontrollers. The tool manufacturer calibrates the movement of the stage with respect to the beam in the form of a computer software. Therefore, a pattern can be easily edited using the graphical user interface, without making any physical changes. The process is, however, completely analogous to optical lithography. The resists used in EBL toggle between polar and non-polar states in response to electron beam instead of a beam of light. Just like optical lithog-

raphy, both negative and positive resits are available with different modulation transfer function (MTF). For most of our work we used Poly(methyl methacrylate) or PMMA and EL9 copolymer as resist. Multiple layers of resists are used wherever possible to obtain cleaner lift-off. The tool used for this work is a RAITH 150 Two electron beam lithography system.

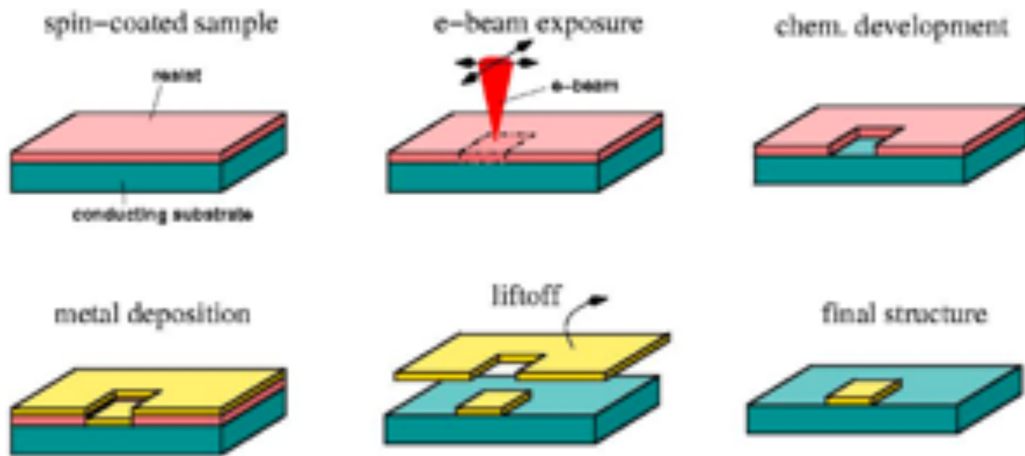

Figure 3.6: A schematic diagram explaining contact formation using EBL and liftoff. The figure is taken from Nano-Optics Group, Institute of Physics - Karl Franzens University Graz website (URL: http://nanooptics.uni-graz.at/ol/work/m_ebl.html).

3.7 Semiconductor device parameter analyser (Electrical characterisation)

One of the pivotal tasks in semiconductor device research is to analyse the performance of the device. Most of this can be achieved through two ubiquitous techniques. Current-voltage (IV) and capacitance-voltage (C-V) analysis. The main reason this is possible is because almost all semiconductor devices can be pedagogically divided into series and parallel combinations of junctions and capacitances. A junction allows a significant current to pass through it in response to the potential difference applied across. A capacitance, however, won't allow a significant current to pass in response to a potential difference across it. Therefore, to measure current, in response to an applied voltage, a small resistance is connected in series and the small voltage drop across it is measured. This indirect approach is used because, an ampere of current is defined as one coulomb of electrical charge or 6.24×10^{18} electrons passing through a point in the circuit in one second. This high number of elementary charge computation within such short time interval creates severe problem with the accuracy of the measurement. Figure 3.7(a) schemati-

cally explains the measurement process. However, this type of measurement introduces a small error because of the voltage dividing characteristics of the small internal resistance of the ammeter. In places with a requirement of higher accuracy, measurement technique which relies on the principle of Lorentz force can be applied. In case of measurement of alternating current, a transformer based measurement circuit can also be used. Figure 3.7(b) schematically explains capacitance measurement circuit. In that image, C_X represents parts of the circuit whose capacitance has to be determined. In the measurement circuit, C_X is inserted inside a half-bridge configuration connected to the function generator. By measuring the waveforms in channel 1 and channel 2 of the oscilloscope, the equivalent series resistance (ESR) and capacitance of C_X can be measured.

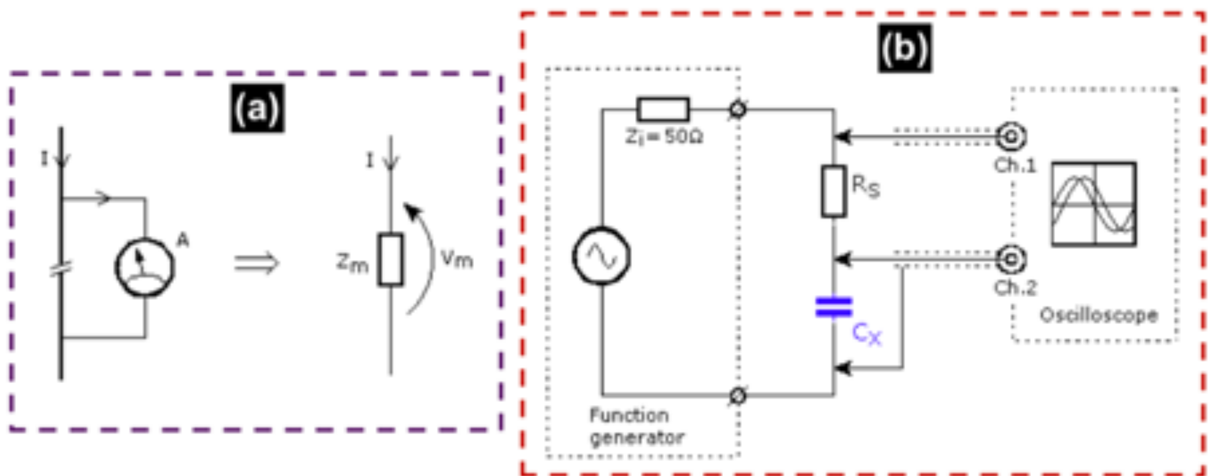

Figure 3.7: Schematic diagram of (a) current measurement and (b) capacitance measurement circuit. The figures are taken from Meettechniek website by Freddy Alferink (URL: https://meettechniek.info/main.html).

In most research labs, including ours, typical lifecycle of a device start with identifying a problem followed by design and planning of a device. Sometimes this second phase consists of simulation exercises. After that a set of devices are made. These devices are then tested by electrical characterisation. Sometimes these characterisations may get rigorous by introducing factors like temperature dependence or speed of measurement. If any peculiarity is observed during measurement, these devices are then subjected to physical characterisation (destructive or non-destructive). The purpose of this is to identify the physical reason behind the problem. Identifying the problem brings us again to the design and planning step. From this, another iteration of device lifecycle starts. It can be seen that, a typical research project comprises of several iterations of device fabrication and characterisation. Therefore, unlike industrial man-

ufacturing, fabricated devices in research labs are almost never packaged into a chip. In fact, individual devices inside a fabricated dice are characterised. Since the size of the devices are in micrometer or nanometer range, we have used purpose built probe stations. In these setups, the sample is placed on a conducting chuck. The chuck can also be used as a back-contact. Temperature of the chuck can be modulated to get characteristics much higher or lower than room temperature. The chuck also provides insulation from any vibration hindering the measurement. The probe stations are fitted with four probe manipulators and an optical microscope. The microscope can be used to guide the probes to the contacts of the device under test. The probe manipulators are equipped to connect to external circuits through source measure units (SMU) or pulse generators. In most cases, to get rid of noise during measurement, the signal obtained from SMUs are integrated over a period. We have used Keysight B1500A Semiconductor Device Analyzer for recording current-voltage characteristics. The samples are probed using a probe station by SS MicroTec for measurements at room temperature and above. For low temperature measurements, CRX-4K cryogen-free closed cycle refrigerant probe station by Lake Shore Cryotronics, Inc. is used. Photograph of the room temperature measurement setup is exhibited in figure 3.8.

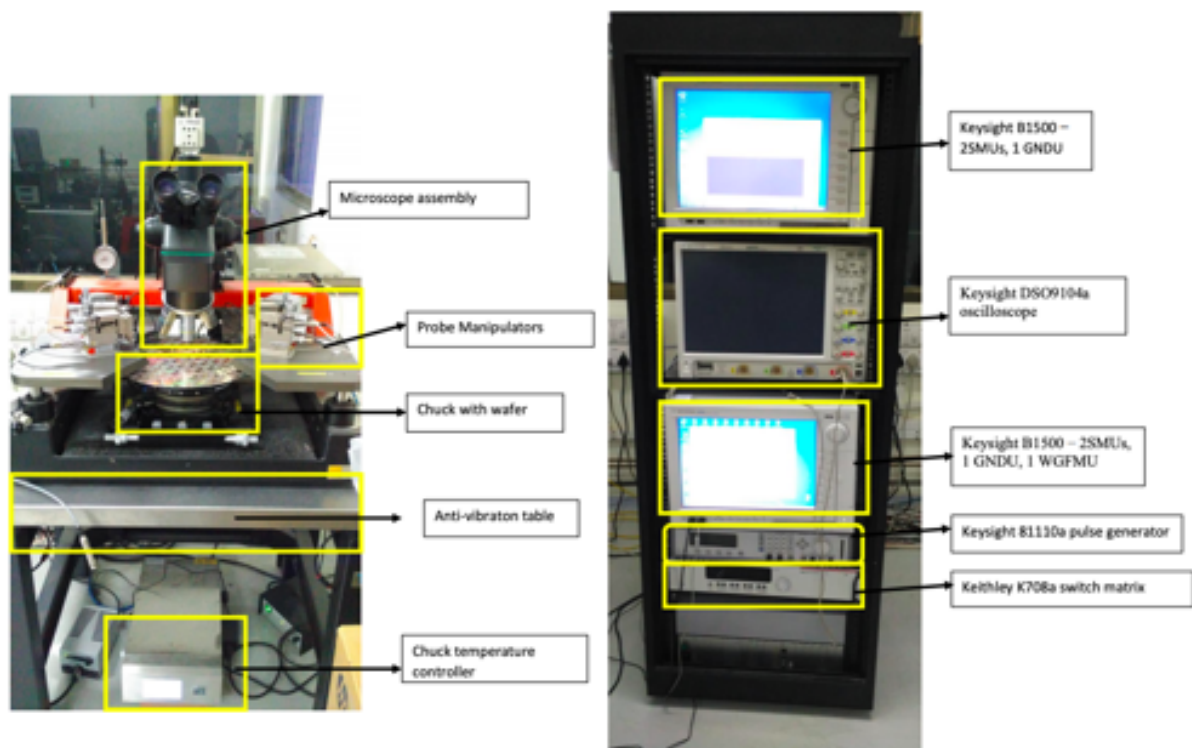

Figure 3.8: Picture of one of the semiconductor device parameter analysers used in this work. The figure is taken from our laboratory website (URL: http://www.cen.iitb.ac.in/slotbooking/GLIMPSE/125_GLIMPSE.pdf).

3.8 Technology computer aided design (TCAD)

The main tool used to perform the simulations reported in this work is Sentaurus TCAD, developed by Synopsys, Inc. This package comes with suites to simulate microelectronic device fabrication process and electrical characterisation of the device. A common use of this is to reduce the actual number of experiments to be performed to optimise the fabrication process of a particular device. But the software can also be used to understand previously performed experiments as well. In this work, we used the tool to gain understanding on the mechanism of charge carrier transport through the nanowires. To do that, similar devices, like the ones fabricated to record IV characteristics, are created in the software environment. In this case, the process simulation was skipped as the result of the processes are already known. Instead, knowledge from the fabrication process and that obtained through physical characterisations are directly plugged into the software. For example, it was already known during the fabrication of the devices, which metal is used to make the contacts. When creating the same device in simulation environment, the same metal is selected from a library of the materials available in the software. In cases where the exact material is not available, the software allows the user to edit the material parameters or create a completely new material. To create a new material, all parameters relevant to the analysis like electron affinity, thermal expansion coefficient, or Fermi velocity, have to be defined manually from credible sources (like a seminal work from a peer reviewed journal or a widely cited book). On the other hand, an example of using knowledge of physical characterisation to the simulation is the use of SEM characterisation results to define exact dimensions of the devices. Since several dimensions of the devices are in nanometer range, SEM has to be carried out post-fabrication to get information about the exact dimensions of the device.

Once the device is created in the simulation environment, its electrical characteristics can be obtained by executing the device structure in Sdevice (Synopsys, Inc.) software. The software divides the device structure into small solution regions called meshes, and self consistently solves equations related to the electrical characteristics of the device. The size and distribution of the solution regions (meshes) can be controlled by the user. A smaller and denser mesh distribution usually produces more accurate results. However, this also results in higher computation time. For any practical simulation exercise, a number of simulations has to be performed to achieve any realistic goal. This is why there has to be a trade-off between simulation time and

accuracy. The user must design the mesh size and distribution keeping this in mind.

Even though each simulation is different, most simulations involve the following two steps. In the first step, the electrostatics inside each mesh is solved by Poisson's equation in finite difference form. This is only the initial solution. After this, the solution of the electrostatics is used to solve for the transport in the mesh using continuity equations. The boundary conditions are checked in the boundaries of each mesh. After that, the process is repeated by plugging in the solution of the second step to first. This process is continued till the condition of the error is met or the maximum number of allowed iterations is over. The user can opt for the exact mathematical method for the solution, the number of iterations and the error. Using this foundation, the mechanism of charge carrier transport in silicon nanowires can be studied. Once the structure is made and divided into meshes, a number of simulations are carried out with slightly different conditions. The results are compared with experimental results to check for correlations. For example, when we wanted to observe the effect of different tunneling at the metal-silicon interface, we have performed several simulations with and without different form of tunneling. To do that, the generation part of the continuity equation is modified for the meshes in the silicon side of the interface, close to the meshes in metal. When tunneling was turned off, we calculated generation only through thermal (kT dependent) and Shockley-Read-Hall (SRH) generation-recombination process. To study the effect of tunneling, different tunneling models such as Fowler-Nordheim tunneling, band-to-band tunneling, or trap-assisted tunneling are used one-by-one and in combinations to calculate generation of charge carriers in the meshes close to the interface. Another example of studying different conditions is study of the effect of Poole-Frenkel (PF) transport. To enable the calculation of current through PF transport, the electric field dependent current equation is considered, along with drift and diffusion in the continuity equation for the meshes an mesh boundaries inside the silicon nanowire region of the device. Detailed discussion of these simulations can be found in chapter 5. An example of the codes used in the simulations is presented in appendix B.

Chapter 4

VLS growth of silicon nanowires in cold wall cat-CVD chamber

4.1 Introduction

The name VLS growth came from the trail of the element silicon during the growth process. In this process, the silicon from the gaseous precursor (vapour) diffuses through an eutectic alloy droplet (liquid) until finally gets crystallised and forms nanowire (solid) [8]. Usually the process takes place inside a Chemical Vapour Deposition (CVD) system. A silicon rich oxygen free gas supplies silicon to the CVD chamber. Typical choices of the precursor gas are silane (SiH_4), disilane (Si_2H_6), dichlorosilane (SiH_2Cl_2), or tetrachlorosilane ($SiCl_4$). The growth conditions immensely depend on the selection of the precursor gas. For example VLS growth using tetrachlorosilane ($SiCl_4$) as a precursor gas necessitates a process temperature from about 800 °C [10] to well beyond 1000 °C [11]. On the other hand, VLS growth using silane as a precursor gas requires only $400 - 600$ °C [12]. The VLS procedure requires a Foreign Element Catalytic Agent (FECA) for nanowire growth. An FECA is a metal capable of forming reasonable low temperature eutectic alloy with silicon. The most frequently used FECA in literatures is gold [12]. A close look at the binary phase diagram of gold and silicon in figure 4.1 reveals the fact that the binary phase of silicon and gold is simple eutectic type and characterised by a single eutectic point at 363 °C. When a silicon wafer containing gold thin film or gold nanoparticles on top is heated over 363 °C, liquid Au-Si eutectic droplets form in a silicon-abundant environment. These liquid droplets act as FECA during VLS growth of silicon nanowires. But the process needs higher temperature for the dissociation of the precursor gas which dissociates on

the surface of the FECA, which results in supersaturation of silicon on the eutectic droplet and an inevitable crystallisation of silicon at the FECA-substrate interface. The silicon nanowire grows with the FECA droplet on the top and with a diameter equal to that of the droplet.

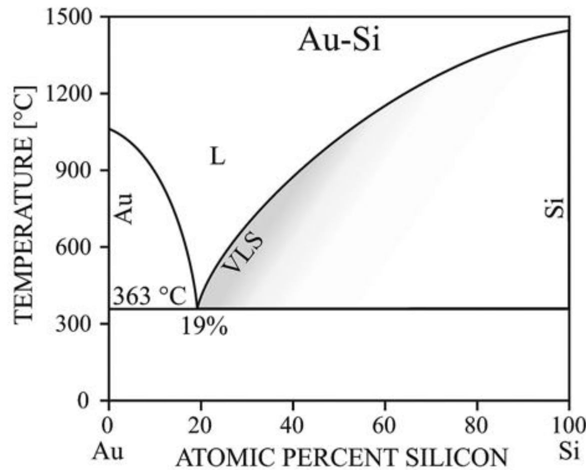

Figure 4.1: Binary phase diagram of gold and silicon. The figure is taken from reference [6].

The VLS growth process is optimised ever since its discovery for an expansive range of precursor gases and FECA [6]. This colossal experimentation have resulted in silicon nanowires which are diverse in geometry and properties. Which, to a large extend, can be attributed to the choice of the equipment used in the process. These equipments range from LPCVD [13], PECVD [14] to tube furnaces [15]. Sometimes more complicated systems like Hitachi UHV H-9000 Transmission Electron Microscope (UHVTEM) [16], RIBER SIVA 45 Molecular-Beam Epitaxy [17] or Thomas Swan atmospheric-pressure Metal-Organic Chemical Vapour Deposition (MOCVD) reactor [18] are being employed to perform VLS growth of silicon nanowires. In this work a rather simple instrument have been used to grow silicon nanowires by VLS method and the results are presented. The instrument is a Cold Wall cat-CVD chamber, which, if found useful will be of great interest for mass production. As it will bring down the complexity of the equipment and therefore, cost of production.

4.2 Details of experiment

VLS growth of silicon nanowires are done in a spherical cat-CVD chamber [67]. The construction of the instrument can be observed from figure 4.2. Precursor gases are introduced to the chamber from top, which then pass through a tungsten filament (‘Wire’) to reach the substrate

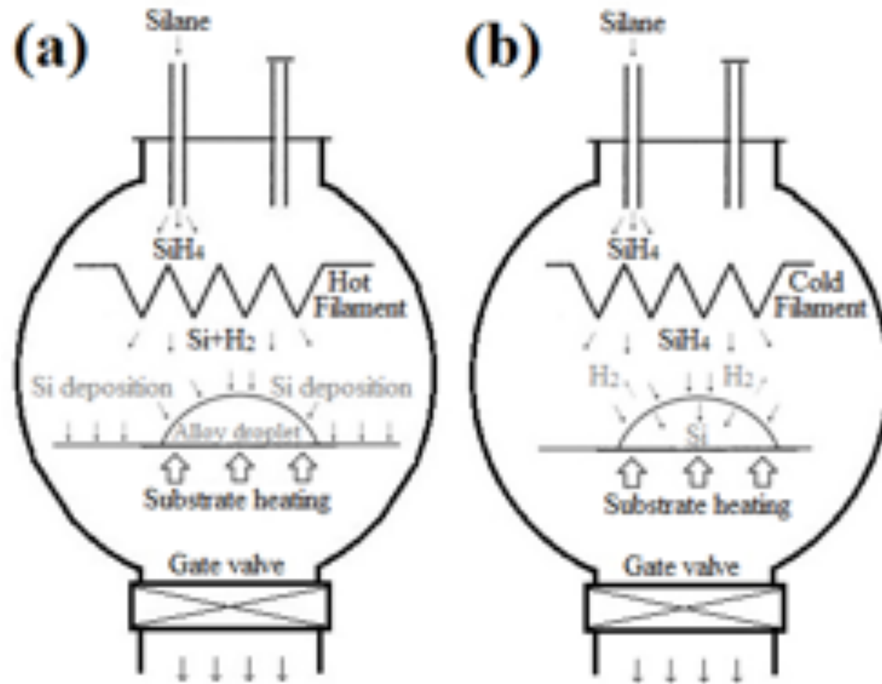

Figure 4.2: Schematic diagram of the indigenous cat-CVD instrument used to grow silicon nanowires by VLS method (a) Operation in HWCVD mode (b) Operation in CVD mode.

surface. There is provision for heating the substrate and the filament which gave the instrument its familiar name 'Hot Wire Chemical Vapour Deposition' (HWCVD). Flow of gasses into the chamber is controlled by Mass Flow Controllers (MFC) installed in the gas lines. The exhaust, situated at the bottom of the chamber, is connected to a rotary and turbo pump assembly through a gate valve which operates manually (Figure 4.2). When the tungsten filament is turned on, it can reach temperatures upto 2000 °C. At this moment if the precursor gas (SiH_4) is allowed to enter the chamber, it dissociates as soon as it passes through the heated filament ('Hot Wire'). This mode of operation is called HWCVD mode which is shown in figure 4.2(a). Likewise, when the filament is off, the precursor passes through the filament without being dissociated and reaches the substrate unperturbed. This mode is called CVD mode and is shown in figure 4.2(b). Experiments in this two modes have been conducted. Substrate for those experiments are prepared by two techniques.

Some of the samples are prepared by annealing silicon wafers with gold thin film on top, thickness of which have been carefully optimised along with the annealing temperature and duration of annealing to get near-circular gold-silicon eutectic alloy [6] nanoparicles (figure 4.3(a)). Also, an effort has been given to make sure that the FECA nanoparticles have a moderate separation between them. All the silicon wafers used to prepare substrate for VLS growth are cleaned

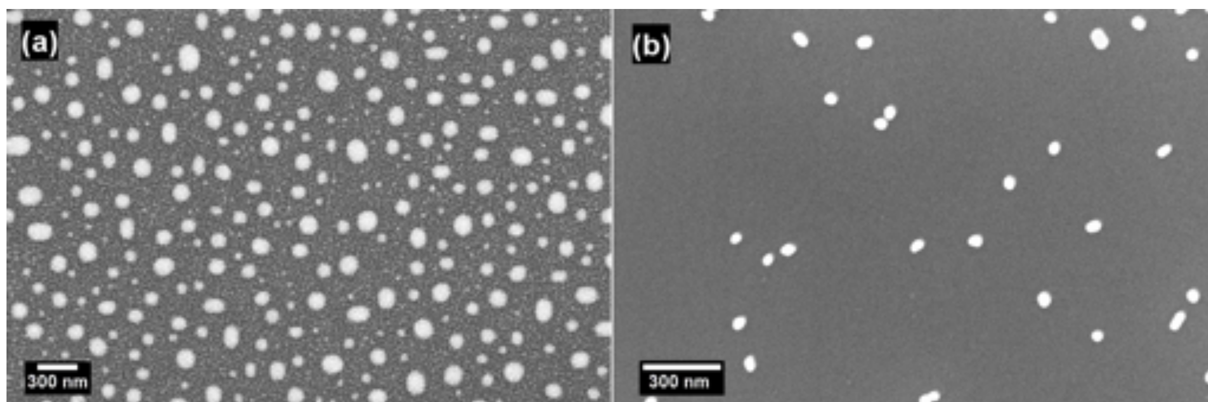

Figure 4.3: Scanning Electron Microscope images of the substrate prior to VLS growth of silicon nanowires (a) Silicon wafer with 5nm gold thin film on top, annealed for 2 min at 800 °C, post-deposition (b) Hydrophilic silicon wafer with chemically attached colloidal gold nanoparticles (diameter 70nm) on top.

by RCA cleaning procedure [68] ending with a 2% HF dip for chemical oxide removal. However, for substrates for deposition of colloidal gold nanoparticles on top, the final oxide removal step is discarded to make the silicon substrate hydrophilic. These hydrophilic silicon wafers are then immersed into a (3-aminopropyl)triethoxysilane solution (APTES) to silanize the surface. These silanized silicon wafers are then dipped into a solution of colloidal gold nanoparticles in citrate buffer to immobilise gold nanoparticles on the silicon substrate surface (figure 4.3(b)). To get well-separated gold nanoparticles on silicon surface the concentration of the colloidal gold solution and interaction time between the solution and the substrate have been optimised. All these substrates are subjected to VLS growth by both modes (HWCVD and CVD) to observe the growth of silicon nanowires on (100) silicon substrate. The primary tools used in the characterisation of the VLS grown nanowires are Scanning Electron Microscope (Zeiss Ultra 55 FE-SEM) and Transmission Electron Microscope (Jeol JSM 4600). Energy-dispersive X-ray spectroscopy of the nanowires have also been carried out (Oxford EDX system).

4.3 Results and discussions

Let us first consider the growths by the HWCVD mode. In this growth mode, the samples prepared by both the methods (thermal annealing and chemical attachment) have shown almost similar results. This is due to uncatalysed deposition of silicon on substrate surface. Since in HWCVD mode SiH_4 passes through the heated tungsten filament after its introduction to the chamber (figure 4.2(a)), it is already dissociated into Si and H_2 by the time it arrives at

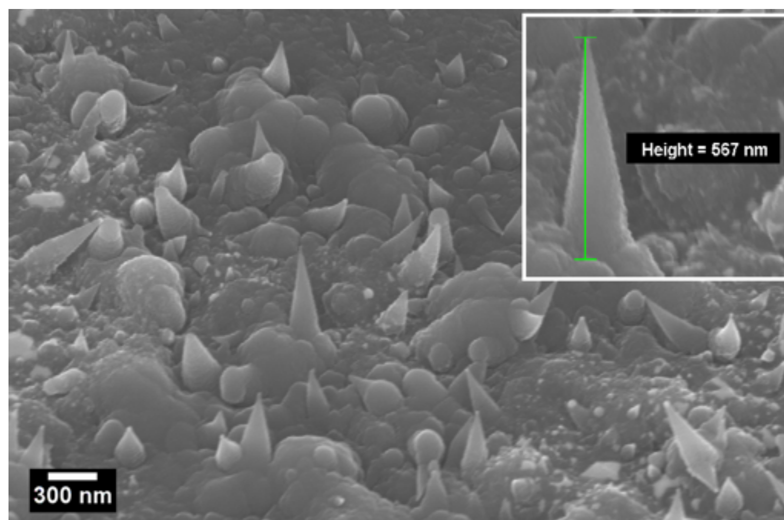

Figure 4.4: 45° tilted Scanning Electron Microscope images of the substrate after VLS growth of silicon nanowires in HWCVD mode (inset shows the image of a single nanowire after growth).

the substrate. Therefore no 'catalytic action' takes place on the FECA rich substrate surface. Anisotropic growth happens solely due to the fact that solubility and sticking coefficient of the oncoming Si adatoms are much higher in liquid FECA droplets than on the solid silicon substrate. After optimisation, the parameters that are found most suitable for this particular reactor and these samples are SiH_4 flow rate = 8 sccm, substrate temperature 400°C and filament temperature 1800°C for 4 minutes. Although this short duration of growth may appear surprising, a close look into figure 4.4 reveals the fact that the nanowires are grown to their limits. This conclusion is drawn from the fact that all the nanowires are conical in shape with a pointed tip. Principal reason for the growth of these kind of structures is the elevated temper-

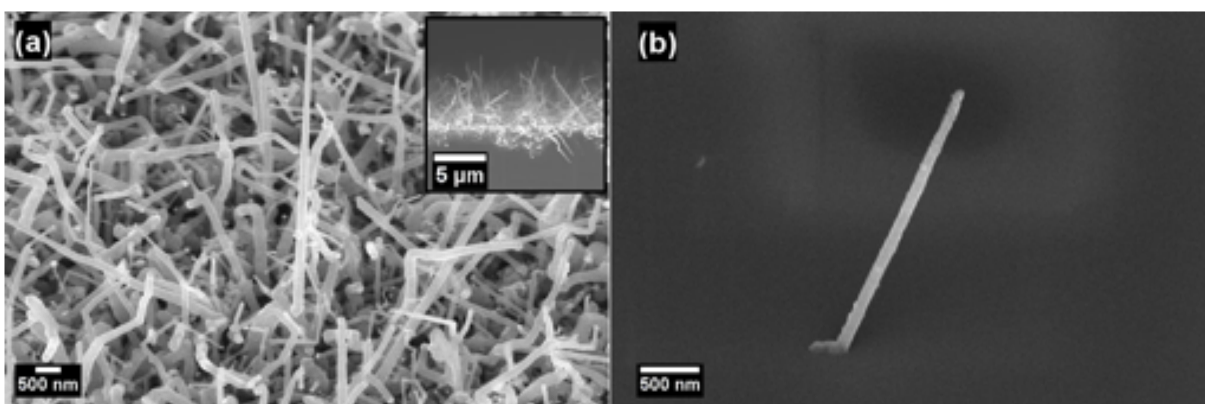

Figure 4.5: 45° tilted Scanning Electron Microscope images of the substrates after VLS growth of silicon nanowires in CVD mode (a) Thermally annealed samples (inset shows cross section SEM of the sample after growth) (b) Samples prepared by adhesion of colloidal nanoparticles to the substrate surface.

ature inside the reactor. In HWCVD mode, the filament is turned on along with the substrate heater. Both of them help the ambient inside the spherical chamber to go up much higher than the minimum temperature required for catalytic dissociation of SiH_4 which makes the growth rate of silicon nanowires extremely high. Another important factor responsible for the growth of conical nanowires is that the diffusion of the liquid alloy FECA along the sidewall of the growing nanowires is very high at such high temperature. This is the reason why the nanowires have gone out of catalyst soon after VLS growth started and ended up with a pointed tip with terminated VLS growth. Because of these reasons growth in HWCVD mode has produced very short nanowires figure 4.4 (inset).

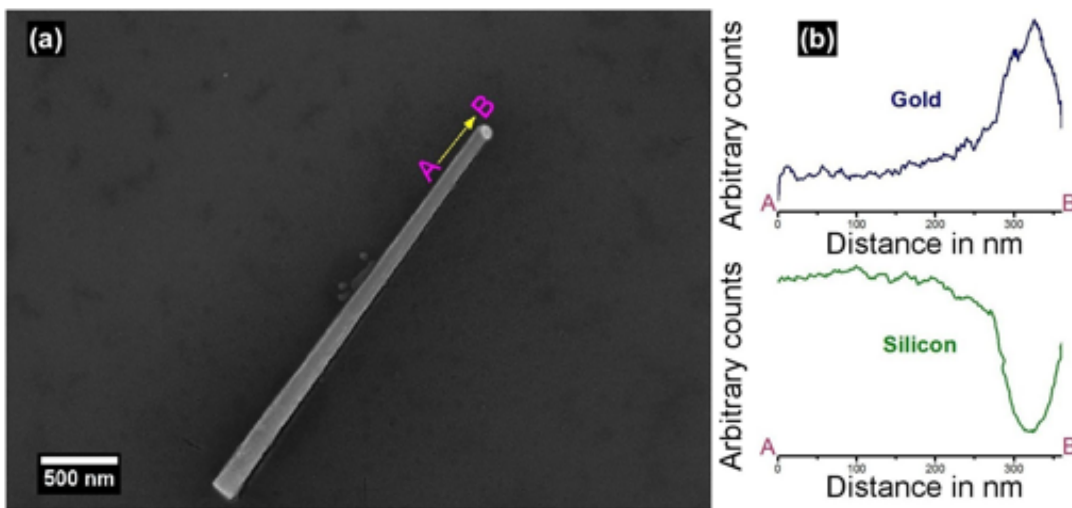

Figure 4.6: (a) SEM image of a silicon nanowire transferred to SiO_2 substrate for physical characterisation. (b) Energy-dispersive X-ray spectroscopy results obtained by scanning from point A to point B. The blue curve indicates variation of gold concentration and the green curve indicates silicon concentration along the line-scan from A to B.

On the other hand, the nanowires grown in CVD mode are considerably longer and their diameter is somewhat constant through their length. This can be seen in figure 4.5. This is due to the reason that during growth in CVD mode, the tungsten filament is kept off which brought down the temperature inside the spherical chamber drastically. Growth at such low temperature has reduced the diffusion of liquid catalyst along the sidewall of growing nanowires. This is the reason for the diameter of the nanowires grown in CVD mode being much more uniform through its length. The liquid FECA on the top of the nanowires are not lost during the VLS growth. Figure 4.6 and figure 4.7 confirms this hypothesis. The parameters that are found most suitable for this particular reactor and these samples after optimisation are SiH_4 flow rate = 10 sccm and substrate temperature of 650 °C for 4 hours. In fact lowering the temperature

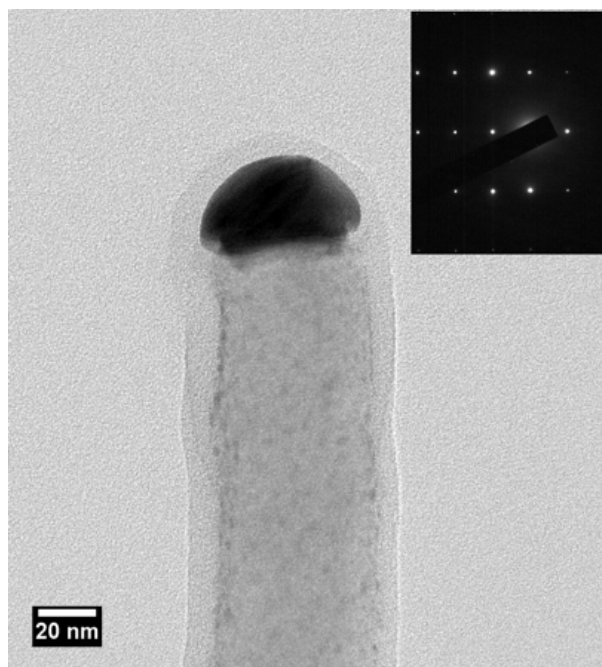

Figure 4.7: Transmission Electron Microscope image of a single silicon nanowire after VLS growth in CVD mode (inset shows the Electron Diffraction pattern of the same nanowire).

have made the reaction rate so low that no nanowire growth was observed untill the pressure inside the cat-CVD chamber during growth is increased from 10^{-3}mbar to 5×10^{-2}mbar. This increase in pressure is achieved by closing the gate valve (figure 4.2) between the chamber and the exhaust by almost 90 per cent.

Other than reduction of gold diffusion along nanowire sidewall, turning the filament off has another important effect on VLS growth. In this case, uncatalysed silicon deposition on the substrate is absent. When the filament is turned off, SiH_4 dissociates selectively on the surface of FECA nanoparticles but not on the bare silicon substrate because of the lack of activation energy (figure 4.2(b)). This is why thin film of silicon other than conical nanowires seen on the substrate surface of figure 4.4 is missing in figure 4.5. Because of the same reason a huge difference between the VLS growth in the samples prepared by thermal annealing (figure 4.5(a)) and chemical attachment (figure 4.5(b)) have been observed for silicon nanowires grown in CVD mode. The samples prepared by thermal annealing have resulted in dense array of muddled nanowires. The array is so dense that, the substrate underneath became practically invisible. The samples prepared by chemical attachment, on the other hand, resulted in individual nanowires in place of the attached nanoparticle on the substrate. The substrate underneath can be visible and appeared to be clean. A close look in figure 4.3 would clarify the cause of the difference. Even after turning significant attention to optimise the thin film deposition

and annealing process to get gold nanoparticles of good separation, it is found that the silicon surface in between the gold nanoparticles is not completely devoid of gold for thermally annealed substrates (figure 4.3(a)). As expected, this is not the case for substrates prepared by chemical attachment (figure 4.3(b)). Due to this fact, the growth of silicon nanowires, which are completely isolated from other nanowires or any other structures, was possible. This helped study the characteristics of individual VLS grown nanowires. Figure 4.6 presents the result of energy-dispersive X-ray spectroscopy of such a nanowire, captured using an FESEM tool. To do the measurement, substrates with VLS grown silicon nanowires on top are sonicated in deionised water and then the resultant suspension was drop-casted on SiO_2 substrate. The line scan shown in the figure, starts from an arbitrary point on the nanowire sidewall and ends at the tip of the nanowire. This proves that the bright spot observed at the tip of the nanowire in the adjoining SEM image is the gold-silicon alloy nanoparticle that acted as catalyst (FECA) during the growth. Because of growth in CVD mode it is still present even after the nanowires have grown to a few micrometers. The presence of the nanoparticle could again be observed from figure 4.7 which is a TEM image of a VLS grown nanowire in CVD mode. To get the image, suspension of silicon nanowires have been drop-casted in a copper grid. The crystalline nature of the grown nanowires can be seen from the inset of the figure, which shows electron diffraction pattern of the nanowire. The electron diffraction pattern resembles single crystal bulk silicon lattice. This shows the single crystal nature of the grown silicon nanowires.

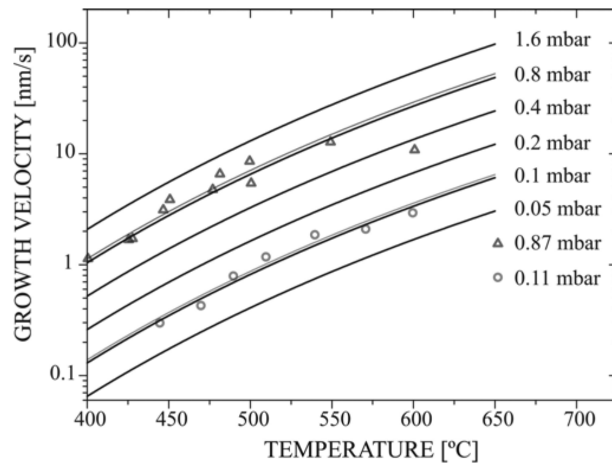

Figure 4.8: Dependence of gold catalysed silicon nanowire growth rate on temperature and pressure. The discrete data points indicate experimental results. The figure is taken from reference [6].

4.4 Effect of separation of the catalyst nanoparticles on the structure of the VLS grown silicon nanowires

In general, the parameters that influence supersaturation of the catalyst alloy or silicon crystallisation at the catalyst-substrate (or catalyst-nanowire) interface have considerable impact on the rate of VLS growth of silicon nanowires. Varying the pressure of the precursor inside the process chamber, or the temperature, change the condition for supersaturation and impact growth rate. The trend can be observed in figure 4.8. Similarly by choosing the crystal orientation of the substrate, the growth rate can be altered as it influences the crystallisation process [11]. These influences are widely studied repeatedly over the years. An interesting aspect of VLS growth got revealed when Boles et al. [18] have grown silicon nanowire by VLS method with solution of colloidal gold nanoparticles of different concentrations. This technique allowed the authors to roughly control the separation between the catalysts. They have designed experiments to study the proximity effect of catalysts on VLS growth. The results can be observed from figure 4.9. The silicon nanowires grown from a dense array of catalyst nanoparticles have become considerably longer than those grown from uncrowded arrays. In fact, the growth rate increases with decreasing separation between the catalyst particles. According to the authors, this is due to the "synergistic effect" between the neighbouring silicon nanowires.

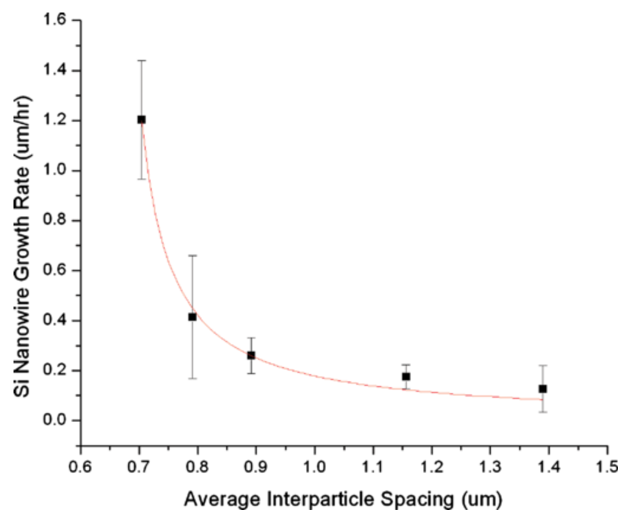

Figure 4.9: Plot comparing the Si nanowire growth rate vs the average inter-particle spacing. Error bars in the y-direction were determined from the standard deviation of wire lengths in each SEM image taken at the corresponding spacing. The figure is taken from reference [18].

A mathematical model in support of the analysis is given by Boles et al. in their article. However, the effect of catalyst proximity on the structure and crystallography of the VLS grown

silicon nanowires have not been studied. To investigate this, we have made arrays of gold 'nanopads' by electron beam lithography followed by thermal evaporation of gold and lift-off, with various separations. This technique allowed us to control the separation of the catalysts for VLS growth, with precision. The results of the experiment is presented in figure 4.10. The

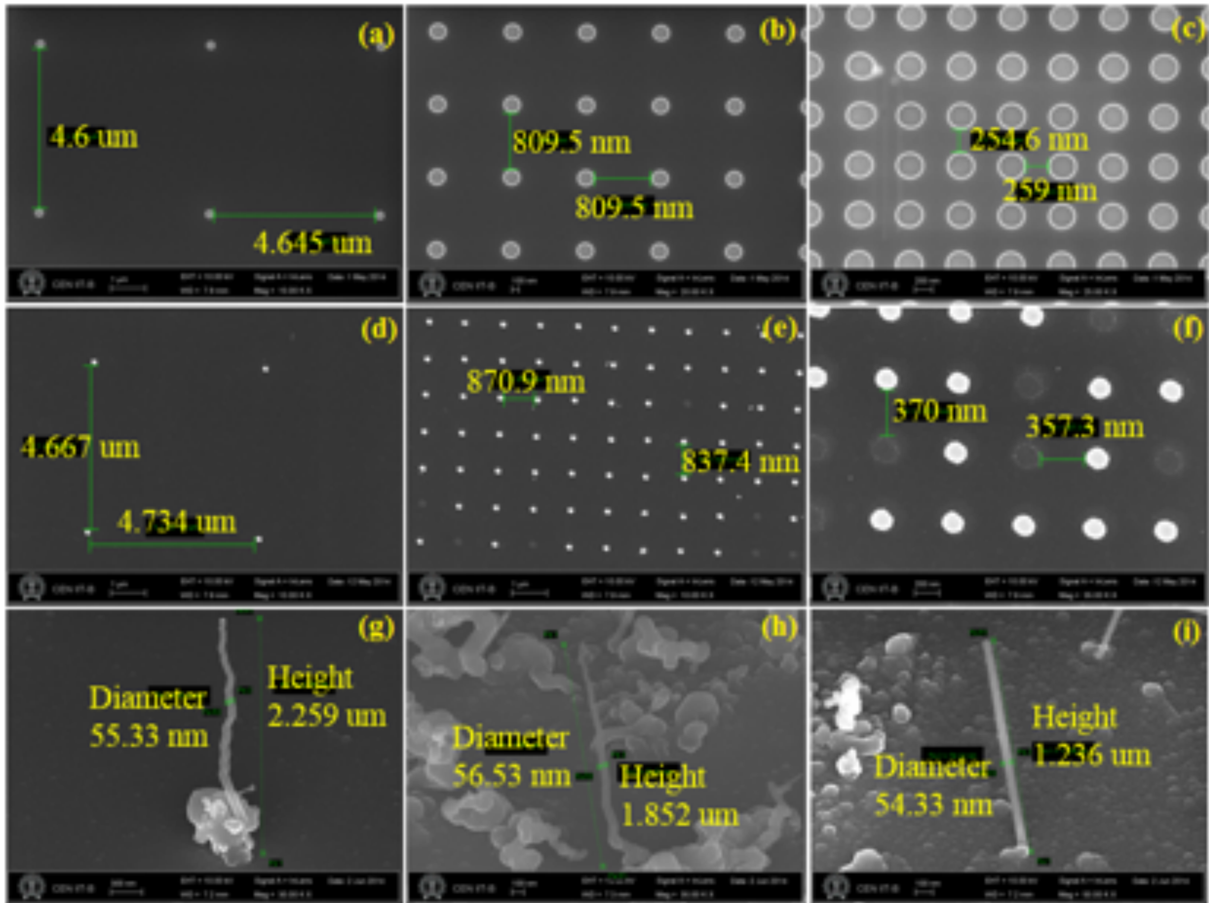

Figure 4.10: (a-c) SEM images of the substrates with patterned resist on top. The average distance between the features are, (a) 4.6 μm, (b) 800 nm and (c) 250 nm. (d-f) SEM images of the substrates after gold deposition and lift-off. The average distance between the gold pads are, (d) 4.6 μm, (e) 800 nm and (f) 250 nm. (g-i) 45° tilted Scanning Electron Microscope images of the substrates after VLS growth of silicon nanowires. The average distance between the silicon nanowires are, (g) 4.6 μm, (h) 800 nm and (i) 250 nm.

results show a completely reverse trend than what was reported by Boles et al. [18], which states that the growth rate of the silicon nanowires decreases with increasing separation between the catalysts. Kendrick et al. [69], on the other hand, have reported a trend similar to ours. They have pointed out the fact that, during VLS growth, the incoming flux of the silicon rich precursor is fixed. On its arrival at the substrate, the flux is distributed between the catalyst particles for absorption. An increase in the density of catalyst particles then can be correlated to a local drop in precursor partial pressure. Since the consumption by the competing growing nanowires is

much higher. This could be the reason for the growth of shorter nanowires in densely distributed areas. In our experiment, gold pads with separation of 4.6μm, 800nm and 250nm are created in the same substrate (figure 4.10(d),(e) and (f)). Hence, the duration of the VLS growth process is exactly same for all the three separations. 4.6μm separated nanowires have the highest average length (2.26μm), followed by 800nm separated nanowires (1.86μm) and 250 nm separated nanowires (1.2μm). Other than average height, the most prominent distinction between the silicon nanowires grown using catalysts with different separation is the overall structure of the grown nanowires. Almost all nanowires grown using catalysts placed 250 nm apart, are straight throughout their length, whereas the nanowires grown from higher separation exhibit multiple 'kinks' along their length (a 'kink' refers to a change in growth direction). Moreover, the number of 'kinks' along the nanowire's length are considerably higher in case of the nanowires grown from 4.6μm separated samples. This phenomenon can be observed from figure 4.10 (g),(h) and (i).

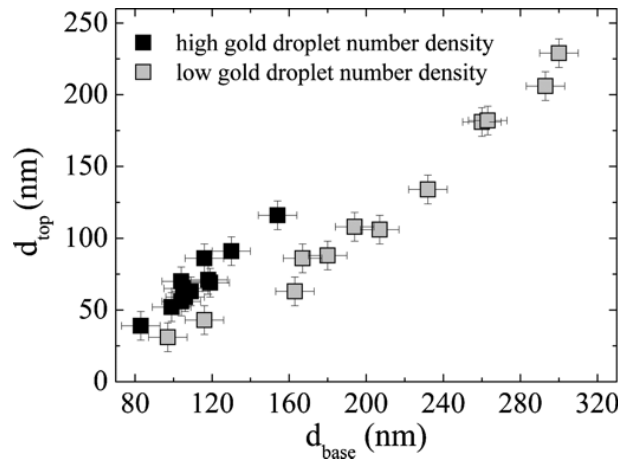

Figure 4.11: Measurement of the diameters of VLS grown silicon nanowires at the top d_{top} vs at the bottom d_{base}. The figure is taken from reference [70].

Another observation from the experiment is the following. From the base to a height of 1.2 μm, the longer nanowires (figure 4.10 (g) and (h)) are not straight. Based on this, it can be said that the 'kinking' incidents occured when the nanowires grew longer. The fact that the longer nanowires started 'kinking' from a position close to their bases, indicates that the nature of the VLS growth changes with the separation of the catalysts. Further investigations on this subject is required to formulate a solid hypothesis behind this behaviour. Results of this experiment also conform with the observations of Chen et al. [70], in the context of 'tapering effect' with separation of the catalysts. The trend, which they have observed, is presented in figure 4.11.

From figure 4.10 (g), (h) and (i) it can be clearly seen that the diameter of the VLS grown silicon nanowires is almost same at the base and at the top for the substrate, in which silicon nanowires are grown from 250nm separated catalysts. As the density of the catalyst became less, the reduction in nanowires diameter at the top from the bottom of the nanowires became more prominent. From these two observations (kinking and tapering), it can be said that the stability of the liquid catalyst droplet got affected with the increase of separation between the gold nanopads. It is, however, true for the energetic condition (growth temperature = 650 °C, growth pressure = 5×10^{-2}mbar) of this experiment. A detailed study is required to understand the complete picture of dependence of nanowire morphology with the separation of catalysts.

These studies on VLS growth of silicon nanowires have led to our strong first-hand understanding of the VLS growth process. This is important as far as the research in silicon nanowire devices is concerned. To meet any design requirement for the device, silicon nanowires with predefined geometry, morphology and physical characteristics have to be grown. The next step in silicon nanowire device research is electrical characterisation of the grown silicon nanowires, in order to gain understanding of the charge carrier transport through them. This is studied in chapter 5.

Chapter 5

Study of electrical transport through silicon nanowires

5.1 Introduction

Even though silicon nanowires have been synthesised and studied since 1950s [1] and 1960s [8], the actual surge in interest started from early 2000s. This interest stems from the scaling of silicon devices with dimensions in nanometers. Devices like diodes [56], transistors [57, 71], solar cells [58] and sensors [46] have been demonstrated in silicon nanowires. Silicon nanowires can be realized using processes like lithography and etch [72], VLS growth [8] and metal assisted electroless etching [73]. VLS growth is a widely used process due to its simplicity and reasonable control on the process, and the bottom up approach of fabrication resulting in good quality nanowires [74]. Initial exploratory experiments were primarily concerned about the conductivity of silicon nanowires. Chung et al. modelled metal - silicon nanowire - metal structures as back-to-back Schottky diodes connected through a resistor which is the nanowire [60]. Estimation of the resistance under diverse conditions hugely improved in the later years with inclusion of the effect of surface charge [75] and dielectric confinement [54]. In parallel, quantum mechanical confinement effects were also explored [29] in sub-10 nm diameter silicon nanowires.

Poole-Frenkel (PF) effect [76] is a well known form of hopping transport used to model pre-breakdown current enhancement in insulators and semiconductors. Occasionally, it is used to describe charge carrier transport through compound semiconductor nanowires [77], perovskite nanowires [78], field emission through nanowires [79] or transport through a random network of

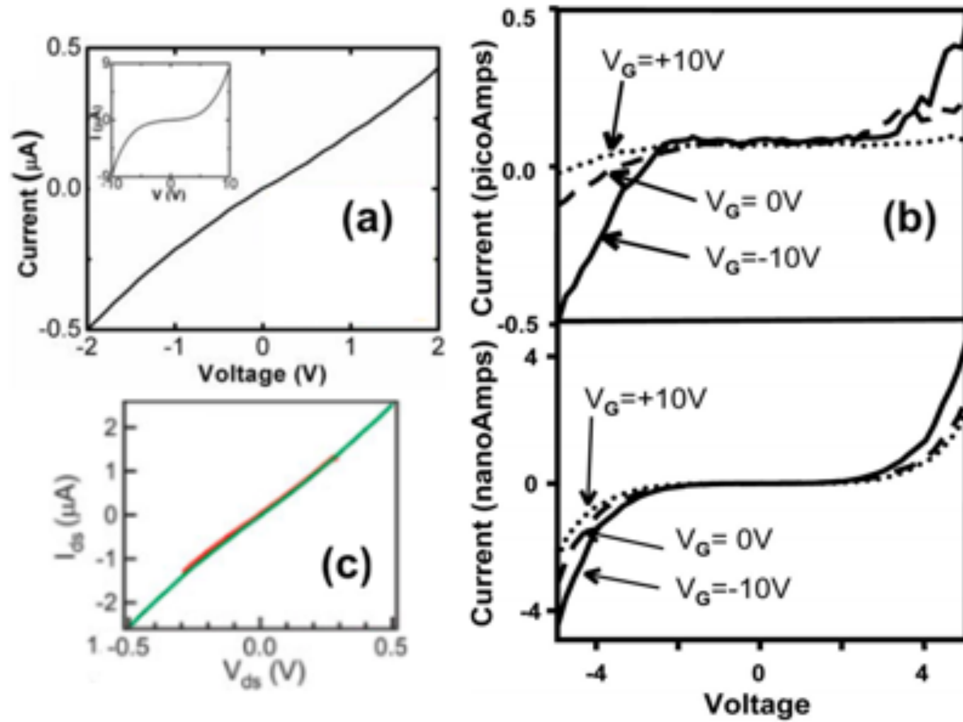

Figure 5.1: (a) IV characteristics of a silicon nanowire device. Inset: the IV characteristics for a larger voltage range. The figure is taken from reference [63]. (b) IV characteristics of a silicon nanowire device before (top) and after (bottom) annealing at $550\,^{\circ}C$. The figure is taken from reference [60]. (c) Current-voltage characteristics of a silicon nanowire device measured using two terminal (green curve) and four terminal (red curve) measurement. The figure is taken from reference [57].

nanowires [80]. Weisse et al. fabricated silicon nanowire arrays using Ag-assisted electroless etching [63]. They reported linear IV characteristics for devices fabricated using nonporous nanowires. However, in porous nanowires, the IV characteristics were reported to be non-linear and better described using PF transport. Figure 5.1(a) exhibits the result reported in that publication. The IV characteristics can be observed to exhibit inverse-'S' like characteristics at higher voltages (inset). Chung et al. reported electrical properties of 15 - 35 nm diameter silicon nanowires grown by VLS technique using Au and Zn as catalysts [60]. The IV characteristics were reported to be nonlinear. Though thermal annealing of the devices hugely improved the conductance of the devices, the nonlinearity was not eliminated. Figure 5.1(b) exhibits the results from that publication. The top IV was recorded before thermal annealing and the bottom IV was recorded after thermal annealing of the device. Both characteristics exhibit non-linear, inverse-'S' shaped characteristics. The authors had attributed this to back-to-back Schottky contacts. Zheng et al. reported silicon nanowire transistor with wire diameter of 20 nm [57]. The phosphorous doped nanowires were grown by VLS technique using Au as catalyst. Both

2 and 4 probe measurements were reported. 4 probe measurement is expected to eliminate the influence of contacts. Indeed the 2 and 4 probe IV of heavily doped nanowires were reported to be identical, indicating that the contacts do not limit the measurement. The IV result is exhibited in figure 5.1(c). The green curve represents data recorded using 2 probe measurement and the red curve represents data recorded using 4 probe measurement. However the IV characteristics reported are discernibly nonlinear, which is not explained to the best of our understanding. In this chapter, combining experiments and simulations, we demonstrate that PF mechanism is a major contributor to transport in Au catalysed VLS grown silicon nanowires.

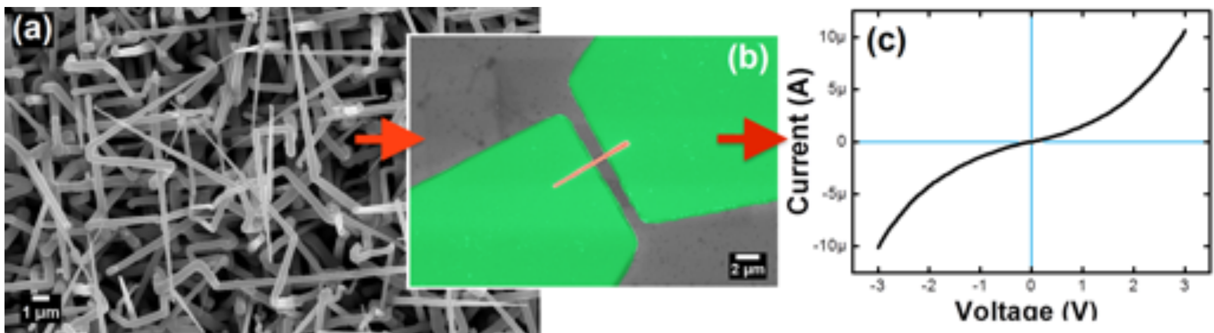

Figure 5.2: (a) 45° tilted SEM image of the substrate after VLS growth of silicon nanowires. (b) SEM image of a test structure made after transferring the VLS grown silicon nanowires to oxide substrate and metal contact formation using lithography. The nanowire is marked in transparent red and the Ti/Au contacts in transparent green. (c) Current-voltage characteristics of the silicon nanowire device shown in (b).

5.2 Experimental

The VLS growth process used for fabrication of nanowires is described in chapter 4. These results were also published in a conference article [81]. Figure 5.2(a) shows a 45° SEM image of one of the samples immediately after growth process. Since the silicon substrate used for the growth process had an orientation of (100), the silicon nanowires have grown in all equivalent {111} directions, which is always the case for nanowires with diameter in this range [27] because of the scaling behaviour of different energetic contributions for VLS growth. Silicon nanowires were separated from the growth-substrate by ultrasonication in ethanol and the resultant solution was dispersed on SiO_2 substrate. After gentle drying of the solution, silicon nanowires were located and marked by SEM imaging. RAITH 150 Two electron-beam lithography (EBL) tool was used to pattern contacts on silicon nanowires through PMMA (polymethyl

methacrylate). Substrates with PMMA were developed using a 1:3 MIBK/IPA developer solution. After development, metals were deposited using thermal evaporator and the samples were kept immersed in acetone for lift-off. The distance between the contacts is referred to as 'channel length' in this work. SEM image of one such device is presented in figure 5.2(b). To record the electrical characteristics at room temperature or higher, Agilent B1500 Semiconductor Device Analyzer was used. The sample was kept on a vibration resistant, temperature controlled metal chuck with in-built heating element. LakeShore XCRX-4K cryogenic probe station was used for low temperature measurements.

5.3 Transport models

IV characteristics obtained from the nanowire test structure shown in figure 5.2(b), is presented in figure 5.2(c). The device has a channel length of 1.1 μm and 268 nm is the diameter at the middle of the channel. Despite being this thick, the device exhibited inverse-'S' like IV characteristics which is typical of silicon nanowires (figure 5.1). Previous studies explained this behaviour using either quantum mechanical effects [29, 53] or the non-linearity of the metal-silicon contacts [82]. Figure 5.3 exhibit the results from those articles. Ponomareva et al. have theoretically studied the electronic properties of silicon nanowires. They have found that, unsaturated bonds at the silicon nanowire surface play a key role in determining the electrical characteristics of a silicon nanowire. Figure 5.3(a) exhibits the effect. The ab initio calculations using density functional theory (DFT) reveal that, these unsaturated bonds in the surface result in creation of additional states within the band-gap of silicon. The IV characteristics shown in figure 5.3(a) exhibits that these states can indeed result in more current than the nanowire without them. Moreover, the nature of the current induced by these states is of inverse-'S' shape. However, these calculations are done for silicon nanowires with diameter 6 nm or less. Similar results are reported by Ma et al. through experiments. The results are exhibited in figure 5.3(b). The IV characteristics presented here are taken by scanning tunneling spectroscopy (STS) of silicon nanowires with diameter of 7 nm to 1.3 nm. In these experimental IV curves, the inverse-'S' nature can be clearly visible. However, this shape of IV characteristics is also reported for silicon nanowire with diameter of 50 nm. The result is presented in figure 5.3(c) from the work of Samanta et al. Since the diameter of the nanowires used to fabricate devices for that work is far beyond the realm of quantum mechanical effects, the inverse-'S' nature of the

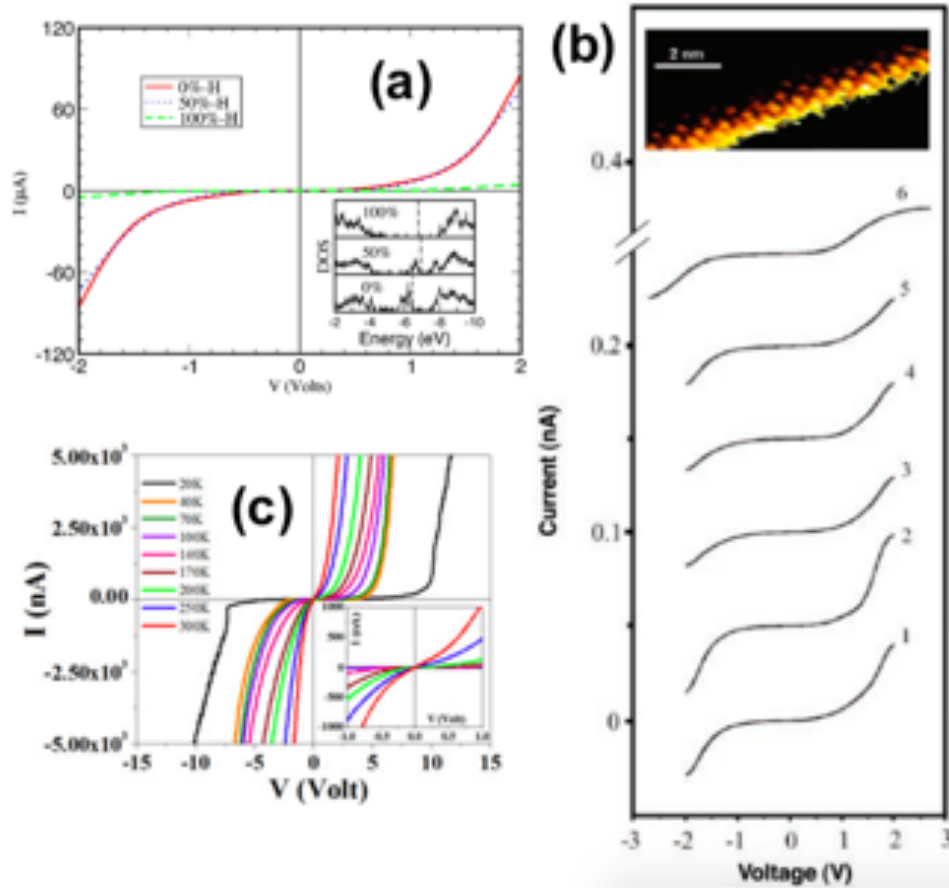

Figure 5.3: (a) Inverse-'S' like IV characteristics obtained by numerical calculations. The figure is taken from the work of Ponomareva et al. [53]. The inset shows the effect of unsaturated bonds on the surface of the nanowire on its density of states. (b) Inverse-'S' like IV characteristics obtained by STS measurements of very thin nanowires. Diameters of wires, marked with 1 to 6, are 7, 5, 3, 2.5, 2, and 1.3 nm, respectively. The figure is taken from the work of Ma et al. citeDDDMa. (c) Inverse-'S' like IV characteristics obtained from silicon nanowire metal-semiconductor-metal devices. The figure is taken from the work of Samanta et al. [82]. Inset exhibits the same characteristics for lower voltages.

characteristics in that work is explained using the non-linear nature of metal-silicon contacts. This is why, to investigate the actual nature of the current-voltage characteristics, Sentaurus (Synopsys, Inc.) simulations [83] calibrated to materials and physical dimensions of our experiment is used. The equivalence of the simulated structure and experimental device can be observed from figure 5.4(a) and (b). Here, the structure used for simulation is essentially a 2D cross section through the yellow dashed line drawn over the SEM image of the test structure presented in figure 5.4(c). Figure 5.5(a) summarises the solution regions used in simulation. The 'M-S contact' region is modelled after the Ti-Si contact. Different current models have been studied with aforementioned setup and the results of three relevant transport mechanisms are presented in figure 5.4(c). To simulate and study the effect of metal-semiconductor contact,

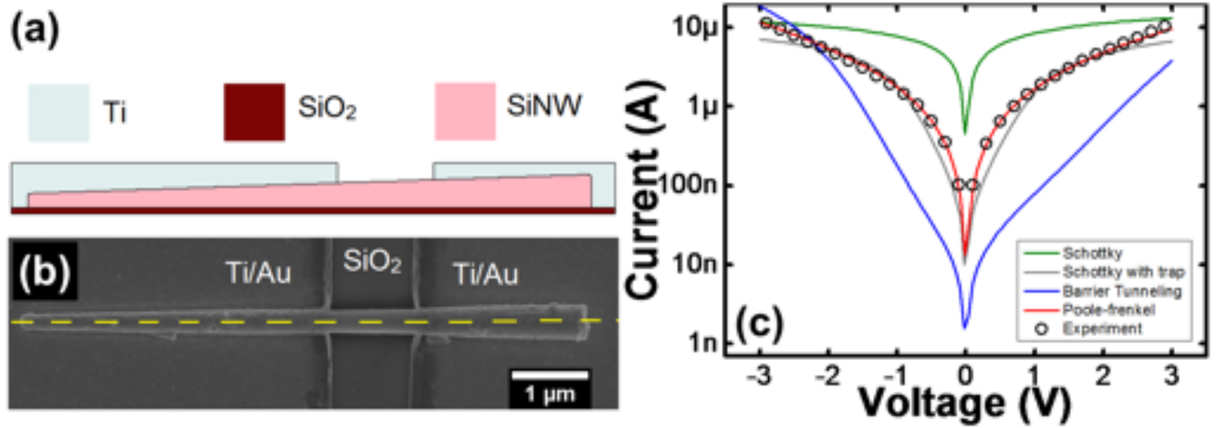

Figure 5.4: (a) The structure used in simulator. (b) SEM micrograph of the fabricated device. The structure for simulation is obtained by taking a 2D cut along the yellow dashed line to have smaller computation time. (c) Comparison of simulation and experimental results. Open circles represent experimental data. The green and grey lines are simulation result considering Schottky model without and with traps, red line is for Poole-Frenkel model, and blue line is for barrier tunneling at metal-semiconductor contact.

Schottky, Ohmic and barrier tunneling models [84] were used for Ti/Si material interface. In all cases, mobility in silicon was described by Philips unified mobility model (PhuMob) [84]. For studying the effect of PF transport, PFMob model [84] was activated for high electric field. Even though previous experiment and modelling work suggest that the non-linear part of the IV characteristics should be defined by the Schottky barrier modulation at source and drain metal contacts [82], we have found a significant mismatch with that hypothesis through our work. This assumption holds true when the resistivity of the channel is insignificant compared to the contact resistances, as the IV characteristics is modelled by two back-to-back Schottky barriers connected through the resistance of the channel. In our work, the long, intrinsic silicon nanowire channel exhibited very high resistivity, and therefore, the IV characteristics was dominated by the silicon nanowire channel. Nevertheless, the matching of experimental results with simulation using Schottky model improves, when the effect of traps are considered [85]. Grey curve in figure 5.4(c) shows the best match achieved by using Schottky model. The curve is obtained with acceptor trap distribution centred around the mid-gap with trap concentration of $7.5 \times 10^{14}\ cm^{-3}$. We also looked into the complete picture of tunneling at metal-semiconductor contact separately. The result is presented in figure 5.4(c), blue curve. Green, grey and blue, all three curves are obtained for 0.45 eV metal-semiconductor energy barrier for electrons. It has also been observed that the output current is insensitive to metal-semiconductor interface state density and the resulting image-force barrier lowering. This is due to the intrinsic nature

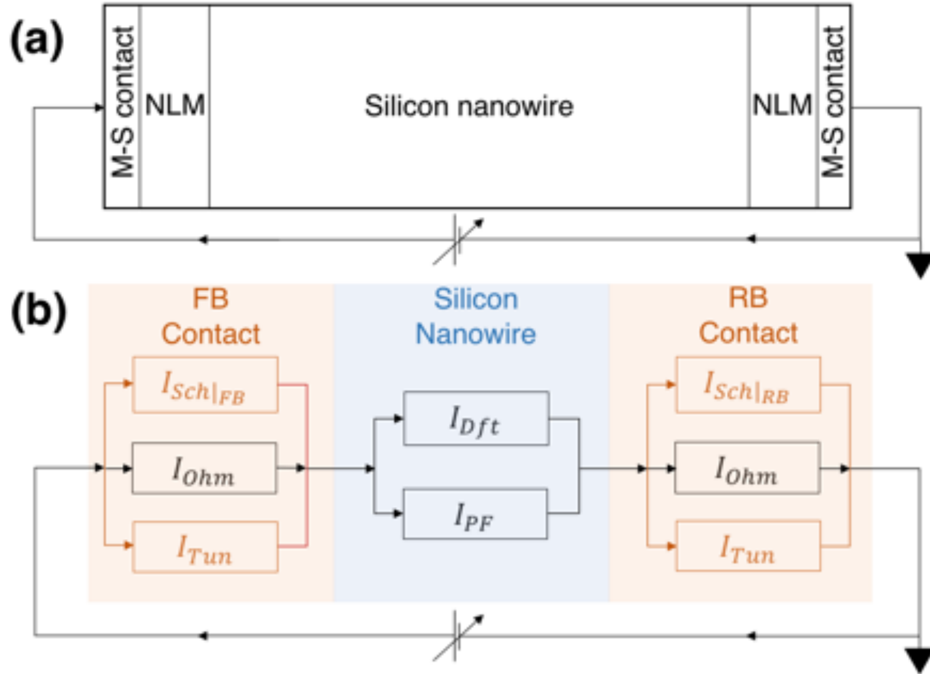

Figure 5.5: (a) Schematic of the simulation setup showing different solution regions. 'M-S contact' regions are referred to the interface region between Ti and Si. A virtual solution region named 'NLM' (Non-Local Mesh) is used to account for charge carriers undergoing tunneling phenomenon in the vicinity of the contacts. (b) Schematic of different current components considered during simulation. Best match between simulation and experiment have been found by using components with black outline only. 'FB' and 'RB' refer to Forward Bias and Reverse Bias. Meaning of the subscripts are as following; *Sch*: Schottky, *Ohm*: Ohmic, *Tun*: tunneling, *Dft*: Drift, *PF*: Poole-Frenkel.

of the silicon nanowire which led to negligible band-bending at the interface. We found the best match between simulation and experiment when PF effect [76] is considered during modelling. Figure 5.4(c) shows a near-perfect match between experiment and simulation adopting PF transport (red curve). Table 5.1 summarises the models used to obtain simulation results presented in figure 5.4(c).

Table 5.1: Models used in TCAD simulations. Colours refer to those used in figure 5.4(c).

Region $\rightarrow$	**Silicon nanowire**	**Silicon/Titanium interface**
Set 1 (green line)	PhuMob	Schottky
Set 2 (grey line)	PhuMob	Schottky
Set 3 (blue line)	PhuMob	BarrierTunneling
Set 4 (red line)	PhuMob + PFMob	Ohmic

5.4 Role of metal contact

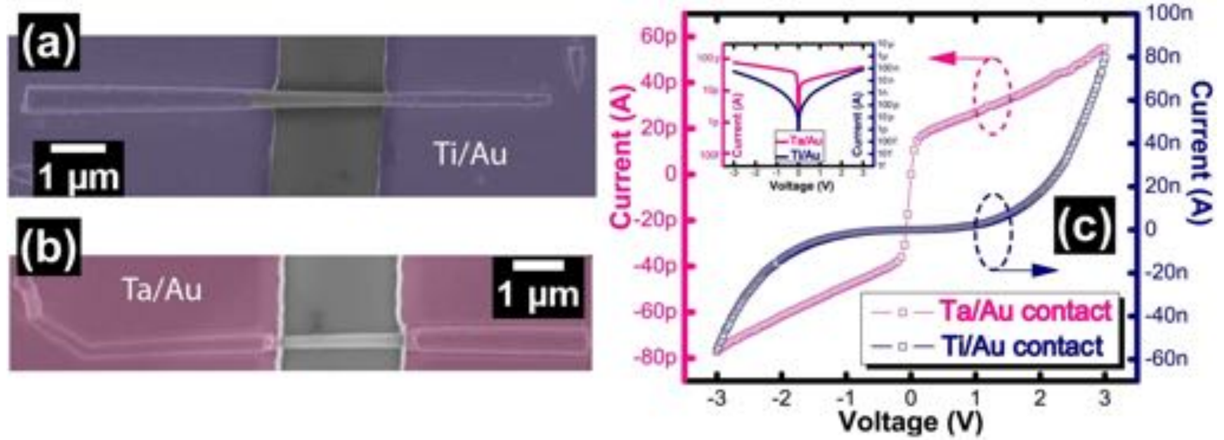

Figure 5.6: (a) SEM image of a silicon nanowire device with Ti/Au contacts. (b) SEM image of a silicon nanowire device with Ta/Au contact. The devices shown in (b) and (c) are almost identical in dimensions. Both nanowires are 9.5μm long. Both devices have a channel length of 2.2μm. Mean diameter of both nanowires in the channel region is around 250 nm. (c) IV characteristics obtained from the two devices. Magenta curve is obtained with Ta/Au contacts and blue curve is obtained with Ti/Au contacts. Inset exhibits these curves in log scale.

To check the correctness of the framework presented in figure 5.5 and to ensure PF dominated transport regime for the transport study, the following experiment is conducted. Few identical devices with two different types of contacts have been fabricated. Some devices are made using titanium (Ti) as contact, while the others are made using tantalum (Ta) as contact. Typically Ti has a work function of 4.33 eV and Ta 4-4.8 eV, depending on the orientation of the surface [86]. However, in practical cases metal contacts rarely follow the work function obtained by theoretical calculations, as effects of interface states and non-ideality induced by the deposition technique complicate the case. Figure 5.6(a) and (b) exhibit SEM images of two devices made on SiO_2 substrate. The nanowires used to fabricate these two devices are made simultaneously using the same process condition, on the same substrate, and are dimensionally almost identical. Distance between the metal contacts is kept as 2.2μm in both devices. However, the contacts in these two devices were made using different metals to observe the onset of PF transport. This exercise also makes sure ohmic contact formation. The IV characteristics of the devices are presented in figure 5.6(c). At any bias condition, one of the contacts will be in high-resistance state (reverse bias) while the other in low-resistance state (forward bias) (figure 5.5). If the resistance of the high-resistance contact exceeds the resistance of the nanowire channel, the output will be dominated by that contact. In most reports of electrical

characteristics of VLS grown silicon nanowires [60], the nanowire used to make the test device was doped. That made the reverse biased contact the current deciding factor. Since the de-

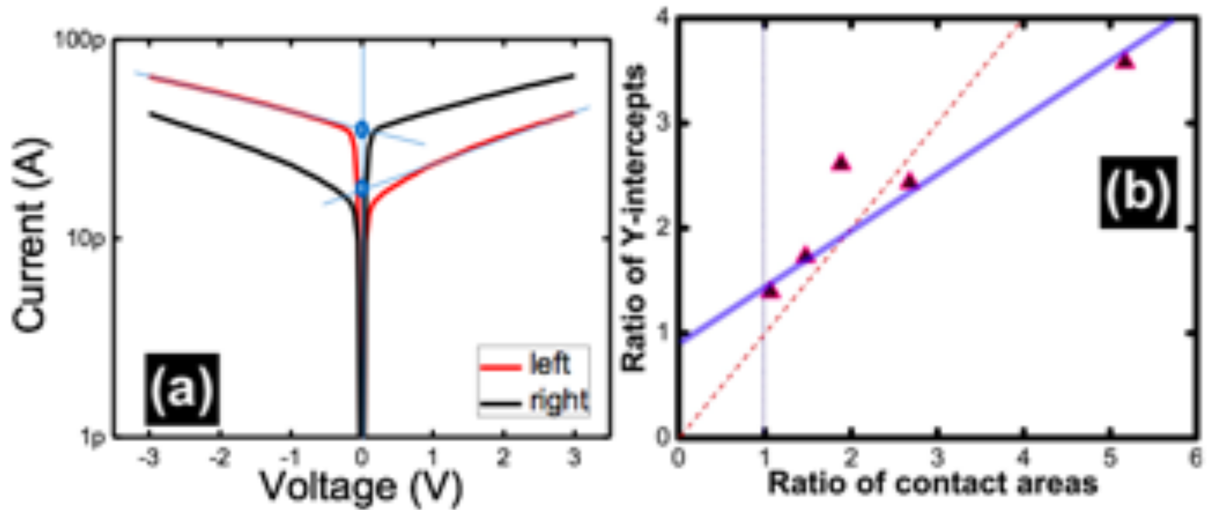

Figure 5.7: (a) Reversibility of the IV characteristics of the device shown in figure 5.6(b). The red curve is obtained by applying potential to the left metal contact and connecting ground to the right terminal. The black curve is obtained by applying potential to the right metal contact and connecting ground to the left terminal. (b) Ratio of the intercepts (blue circles in (a)) vs the ratio of the contact areas of several devices. Slope of the red dashed line is = 1 and slope of the blue line is = 0.5.

vices shown in figure 5.6(a) and (b) are made with intrinsic nanowires and long channel length (2.2μm), it was possible to lower contact resistance below the resistance of the nanowire and exhibit PF dominated IV characteristics. The change in the transport is more apparent when the characteristics are plotted in log scale (figure 5.6(c) inset). The contact dominated device (magenta curve) exhibited different current levels for different polarities of the applied voltage, due to the difference in contact areas of the device figure 5.6(c). To check this, the measurement setup is reversed. That resulted higher current level for opposite polarity of the applied voltage. Figure 5.7(a) exhibits the IV characteristics of the device shown in figure 5.6(b) with two different measurement setups. The red curve is obtained when the potential is applied to the left metal contact and the right metal contact is connected to ground. The black curve is obtained when the right terminal is connected to the applied potential and the left to the ground terminal. The high voltage regions in the graph are fitted with a straight line and their Y-intercept is obtained for comparison. When the ratio of these intercepts are plotted against several devices with different source and drain contact areas, a clear correlation emerges. The result is exhibited in figure 5.7(b). However, the same exercise on devices with Ti/Au contact, like the one shown in figure 5.6(a), have resulted in exact same curve when the measurement setup is reversed.

This behaviour indicates a clear difference between the two different modes of transport. Since the devices made with Ti/Au contacts are experimentally confirmed to be not of Schottky type, further discussions are carried out in the context of those devices.

5.5 Simulation

When 'Schottky' model is on, the current density through these regions can be calculated using the equation 5.1-5.3.

For the forward biased contact,

$$J_{Sch|_{FB}} = \frac{m^*}{m_0} A^* T^2 e^{-\frac{(\phi_B - qV_A)}{k_B T}} \tag{5.1}$$

For the reverse biased contact,

$$J_{Sch|_{RB}} = \frac{m^*}{m_0} A^* T^2 e^{-\frac{\phi_B}{k_B T}} \tag{5.2}$$

where,

$$A^* = \frac{4\pi m^* q k_B^2}{h^3} \tag{5.3}$$

Here m^* and m_0 are carrier effective mass and rest mass respectively. A^* is the Richardson's constant. T is the temperature in Kelvin. ϕ_B is the metal-semiconductor barrier in eV. q is the electronic charge in coulomb. V_A is the applied voltage in volt. k_B is the Boltzmann's constant in SI unit. h is the Planck's constant. Turning on 'Schottky' model also enables calculation of current density by Fowler-Nordheim (FN) tunneling at higher electric field using the equation 5.4.

$$J_{FN} = \frac{q^2 \varepsilon^2}{8\pi h \phi_B} e^{-\frac{4\sqrt{2m}\phi_B^{3/2}}{3\hbar q \varepsilon}} \tag{5.4}$$

Here ε is the electric field. $\hbar = \frac{h}{2\pi}$ and $m = m_0 m^*$. However, during simulation it is possible to model the 'M-S contact' region by an Ohmic contact with a distributed contact resistance r_d such that the current density through these regions may follow the simple equation 5.5.

$$J_{Ohm} = \frac{1}{r_d} V_A \tag{5.5}$$

Similarly, current through the 'M-S contact' region can be entirely calculated by Wentzel-Kramers-Brillouin (WKB) approximation based tunneling models [84] which takes into account any arbitrary shape of potential. Current calculated through this method is denoted as I_{Tun}. Due to the absence of any charge carrier concentration gradient, it is reasonable to assume that current density through the silicon nanowire channel is almost entirely due to drift of charge carriers in response to the applied voltage and therefore can be modelled by the equation 5.6.

$$J_{Dft} = q(\mu_n n + \mu_p p)\varepsilon \tag{5.6}$$

Here, μ_n and μ_p are the electron and hole mobilities in $cm^2/V.s.$ n and p are the electron and hole concentrations in cm^{-3}. In order to incorporate the effect of PF transport, equation 5.7 and 5.8 are considered.

$$J_{PF} = G_0 e^{-(E_A/k_B T)} e^{\sqrt{V_A/V^*}} V_A \tag{5.7}$$

where,

$$\sqrt{V^*} = \frac{k_B T}{q} \Big/ \sqrt{\frac{q}{\pi \varepsilon L}} \tag{5.8}$$

G_0 in equation 5.7 represents conductance pre-factor, E_A is the activation energy in eV required to de-trap charge carriers from the Coulomb potential of the trap site, V^* is defined by equation 5.8. Equation 5.8 only consists of material and geometrical parameters of the silicon nanowire. Here, ε is permittivity in F/cm and L is the channel length in cm. It can be observed from equation 5.7 that PF transport only becomes relevant beyond a certain applied voltage (V_A) which is determined by the activation energy, E_A.

In steady state, continuity equation in silicon nanowire channel takes the form of equation 5.9.

$$0 = \frac{1}{q}\nabla(J_{Dft} + J_{PF}) - R|_{N_T(E)} \tag{5.9}$$

Where, $R_{N_T(E)}$ is the recombination rate as a function of concentration of recombination-generation (R-G) centres per cm^3 which is a function of energy within the band gap. A simulation without any trap sets $R_{N_T(E)} = 0$ in equation 5.9. Solution of equation 5.9 may differ when the function of R-G trap centre distribution is changed (eg. Gaussian distribution with peak at mid-gap, delta-distribution at mid-gap, etc.) as doing that modifies $R_{N_T(E)}$. A simu-

lation without the effect of PF transport sets $J_{PF} = 0$ in equation 5.9. To study the effect of tunneling in the vicinity of contact regions virtual solution regions named Non-Local-Mesh (abbreviated 'NLM') were established. Steady state continuity equation in 'NLM' regions is given by equation 5.10.

$$0 = \frac{1}{q}\nabla(J_{Dft} + J_{PF}) + G|_{N_T(E),\varepsilon} - R|_{N_T(E)} \tag{5.10}$$

Here, $G|_{N_T(E),\varepsilon}$ is the carrier generation rate through various tunneling events as a function of trap distribution and electric field. A simulation without trap sets $R|_{N_T(E)} = 0$ and makes $G|_{N_T(E),\varepsilon}$ a function of electric field only in equation 5.10. Figure 5.5(b) summarises the relationship between these current components. In the form of equation 5.11 they act as boundary conditions to 'stitch' the solution of continuity equation between different solution regions.

$$J_{Sch} + J_{Tun} + J_{Ohm} = J_{Dft} + J_{PF} \tag{5.11}$$

Form of equation 5.11 will differ between different simulations depending on which models were selected. J_{FN} is calculated as part of both J_{Sch} and J_{Tun}. The simulation software (Sentaurus) is equipped to handle multiple models at once and will not result in double calculation of components such as J_{FN}. Please note that figure 5.5(b) summarises the current components in the entire circuit. But, in equation 5.11 current densities are used in place of current. The reason behind this is that the silicon nanowires used to make the test structures had uneven cross-section and uneven coverage of metal in source and drain contacts. As boundary conditions are applied across the same cross-section, current densities can be used in place of currents. However, when describing the 'full-picture' in the measurement circuit, current components should be used in place of current densities.

figure 5.8 exhibits some simulation results relevant to the preceding framework. As shown in figure 5.4(c) before, the best match between experiment and simulation was obtained through adopting a PF based transport for the silicon nanowire channel (equation 5.7). In figure 5.8(a), alongside PF transport based model (solid lines) results of similar simulation excluding PF models are also presented (dotted lines). As expected, simulation without PF (equation 5.6 only) agree with experiment only till certain voltage (determined by E_A of equation 5.7). The phenomenon is shown for two different channel length devices in figure 5.8(a). For this set of simulations, equation 5.11 will take the form of equation 5.12 and equation 5.13.

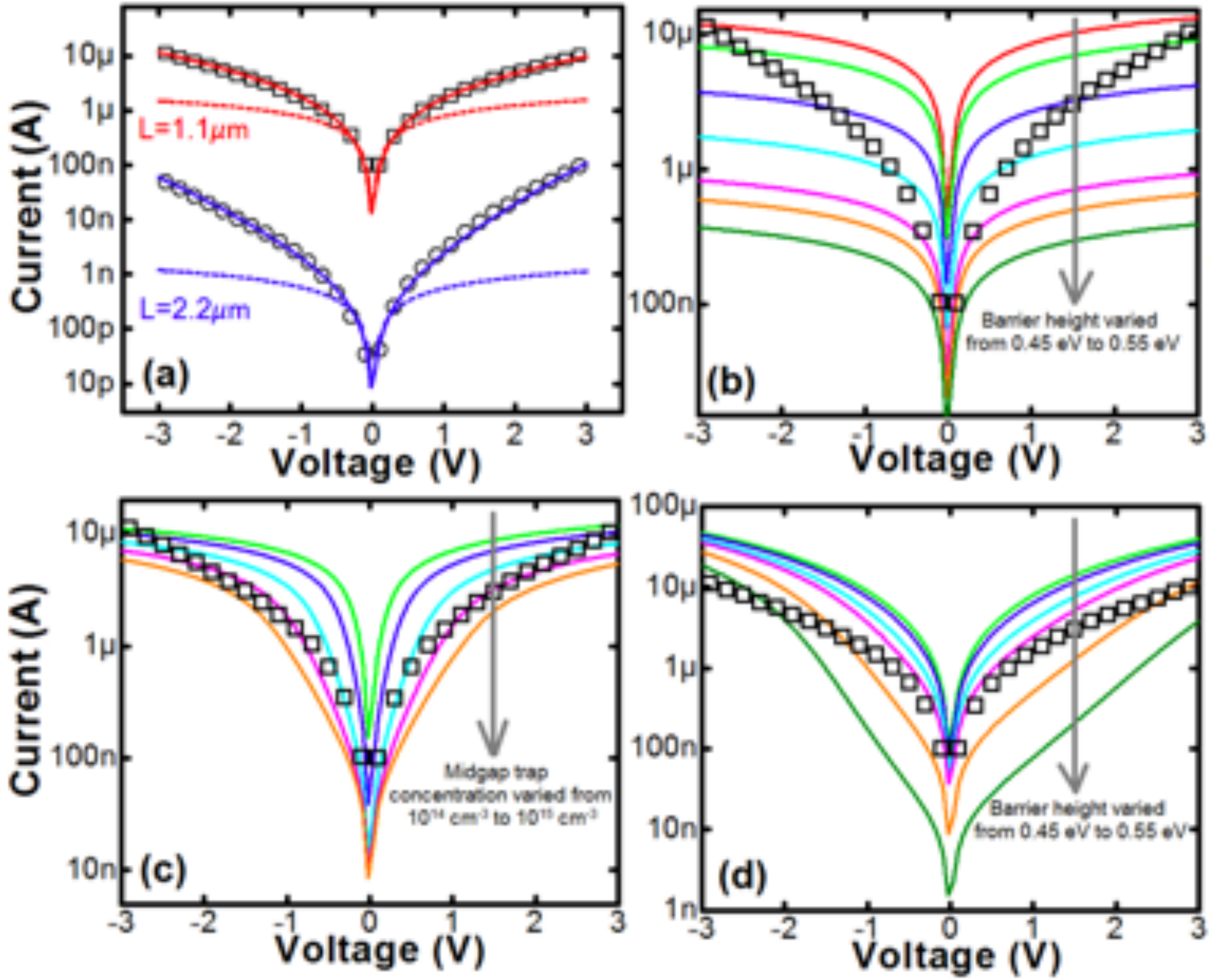

Figure 5.8: (a) IV characteristics in log scale. The red curves are for nanowire devices with channel length of 1.1 μm and blue curves for channel length of 2.2 μm. Solid lines represent simulation results obtained by adopting Poole-Frenkel transport model for the nanowire channel. Dotted lines present the results of exact same simulation except Poole-Frenkel model. Discrete points (hollow squares and circles) represent experimental results. (b) Comparison of simulation results for silicon nanowire device with channel length of 1.1 μm with experimental results (hollow squares) when Schottky contacts are assumed for Ti-Si contacts. (c) Same as (b) with addition of mid-gap traps. (d) Same as (b) except when WKB based barrier tunneling models are assumed for Ti-Si contacts.

$$J_{Sch} + J_{Tun} + J_{Ohm} = J_{Dft} + J_{PF} \text{ ; } \textit{solid line} \tag{5.12}$$

$$J_{Sch} + J_{Tun} + J_{Ohm} = J_{Dft} \text{ ; } \textit{dotted line} \tag{5.13}$$

However, skipping J_{Sch} and J_{Tun} from the LHS of equations 5.12 and 5.13 have produced the same result which can be understood by observing figure 5.5(b). As the three regions, 'FB Contact', 'Silicon nanowire' and 'RB Contact' are in series connection, they must account for

the same current through them. Physical dimension and doping concentration (no doping) of our devices are such that the middle region ('silicon nanowire') accounts for the least current and therefore determines the overall current. However, within the same region the two competing current components (J_{Dft} and J_{PF}) work in parallel, resulting in the higher among them determining the overall current. Therefore, equations 5.12 and 5.13 can be written in the form of equations 5.14 and 5.15 without distorting the results.

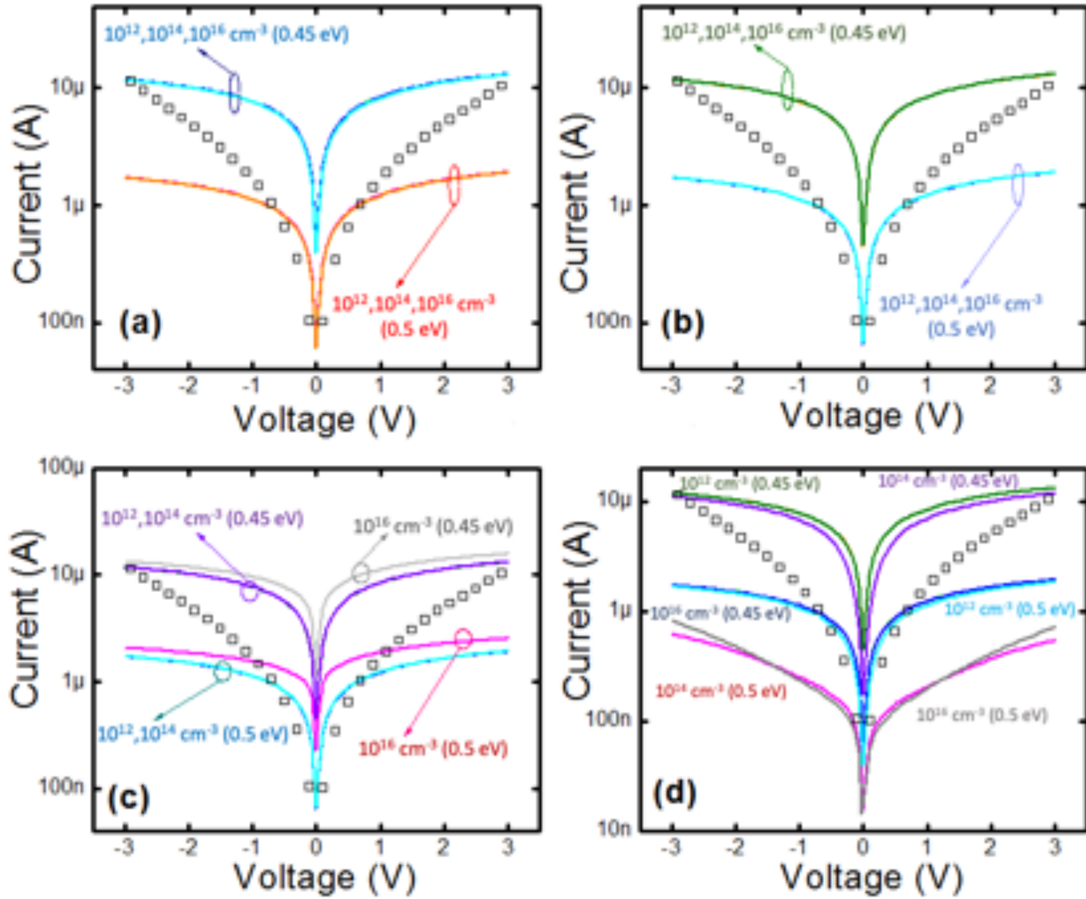

Figure 5.9: Effect of trap distribution on simulation results assuming Schottky model for Ti-Si contacts. (a) For exponential distribution of eNeutral traps spanning 0.1 eV from peak at conduction band minima. (b) For exponential distribution of hNeutral traps spanning 0.1 eV from peak at valance band maxima. (c) Considering the effect of (a) and (b) simultaneously. (d) Gaussian distribution of eNeutral traps spanning 0.1 eV from its peak at an energy 0.275 eV below conduction band minima together with Gaussian distribution of hNeutral traps spanning 0.1 eV from its peak at an energy 0.275 eV above valance band maxima. In all four cases (a)-(d), capture cross section of electrons and holes are considered as $10^{-12} cm^{-2}$. Barrier lowering due to image charge is considered. The metal-silicon contact barrier height used for each simulation is given within braces.

$$J_{Ohm} = J_{Dft} + J_{PF} \text{ ; } solid\ line \tag{5.14}$$

$$J_{Ohm} = J_{Dft} \text{ ; } dotted\ line \tag{5.15}$$

figure 5.8(b) exhibits the effect of using only ‘Schottky’ model for contacts during simulation. For this set of simulations, equation 5.11 will take the form of equation 5.16,

$$J_{Sch} = J_{Dft} \tag{5.16}$$

with calculation of J_{FN} at high electric field.

Figure 5.8(b) also exhibits the effect of changing barrier height (ϕ_B) and its effect on conformity between simulation and experiment. The simulation with these assumptions matches best with experimental results when ϕ_B is varied between 0.45 eV and 0.55 eV. The disagreement is quite visible in figure 5.8(b). The matching improves with introduction of mid-gap traps in the same simulation (figure 5.8(c)). In this case, the steady state boundary condition remains unchanged. The only difference is $R_{N_T(E)} \neq 0$ in equation 5.9. Several functions for distribution of $N_T(E)$ within the band gap have been tested and delta distribution with peak is found to be most apt along with gaussian distribution with peak at mid-gap which exhibited similar results. The results for Schottky model are exhibited in figure 5.9. To understand the effect of tunneling separately, a set of simulations have been carried out, the result of which is exhibited in figure 5.8(d). In that case equation 5.11 takes the form of equation 5.17.

$$J_{Tun} = J_{Dft} \tag{5.17}$$

Here J_{Tun} accounts for all possible tunneling mechanisms including trap assisted tunneling (TAT). Nevertheless, the IV using these models have been found invariable with addition of traps to the interface. Which means tunneling mechanisms other than TAT dominate under test condition. Continuity equation in ‘NLM’ solution region becomes equation 5.10 with $J_{PF} = 0$. Doing so, reveals the nature of tunneling currents. In figure 5.8(d), shape of the IV curve changes as the metal to semiconductor barrier height is gradually increased from 0.45 eV to 0.55 eV. Referring to figure 5.5(b) one can argue that this happens as the tunneling current drops below the current in silicon nanowire channel, J_{Dft} with increase in barrier height. With inclusion of J_{Sch} to LHS, these effects go away as the current never drops below J_{Dft}.

5.6 Temperature dependent electrical characterisation

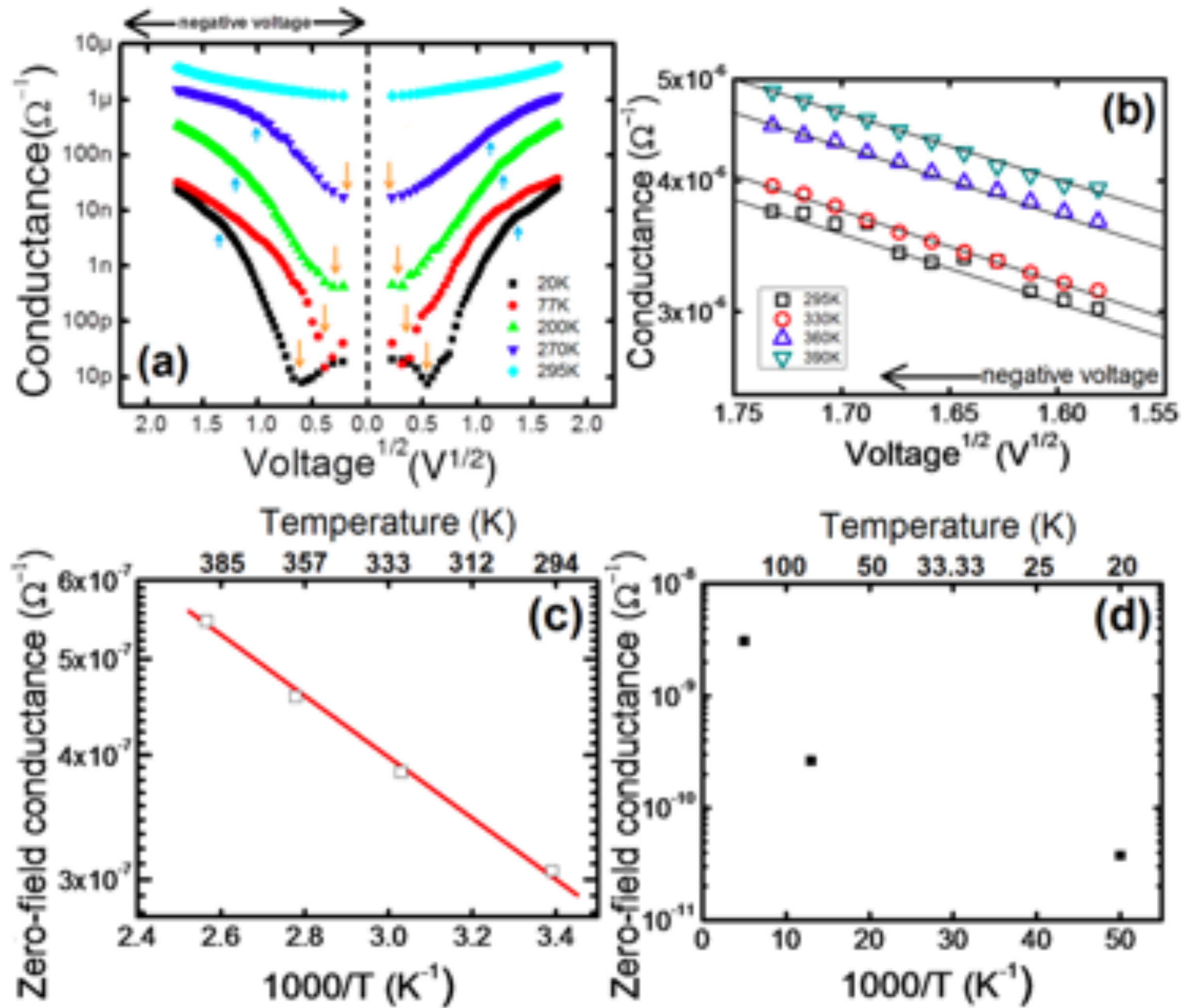

Figure 5.10: (a) Low temperature conductance (current/voltage) vs $V^{\frac{1}{2}}$ characteristics obtained through experiment to confirm dominance of Poole-Frenkel transport in gold catalyzed, wide diameter, VLS grown silicon nanowires. The measurement was performed on the device shown in figure 5.2(b). (b) High temperature conductance vs $V^{\frac{1}{2}}$ characteristics to obtain plot of zero-field conductance. (c) Arrhenius plot to obtain the activation energy for de-trapping from the Coulomb traps. (d) Low temperature Arrhenius plot.

The results of the simulations have clearly pointed out PF transport to be the dominant mechanism behind charge carrier transport in VLS grown silicon nanowires. PF transport is form of hopping transport, in which, charge carriers responsible for current periodically move in and out of coulomb traps. This process is greatly impacted by the change of temperature. Increase or decrease of temperature results in increase or decrease of average thermal energy. This changes the energy required for a charge carrier to move out of a trap (detrapping). Therefore, by performing low temperature measurements, the onset of PF transport can be observed. On

the other hand, by performing high temperature measurements, information about the average energy required for detrapping can be obtained. The low temperature IV curves shown in figure 5.10(a) can be roughly divided into three parts separated by the arrow marks. This property, however, disappears for IV curves measured at room-temperature (295 K) or higher. The IV curves become straight line after certain $\sqrt{V}$ marked by orange arrows pointing downwards. At higher $\sqrt{V}$ value marked by cyan arrows pointing upwards, slope of the curves reduces. This reduction of slope at higher $\sqrt{V}$ is discussed later in this chapter. Anyway, it is clear from the characteristics that the region between orange and cyan arrow marks and the region beyond cyan arrow marks form straight lines when conductivity is plotted in log scale vs $\sqrt{V}$. For room-temperature the entire curve consists of a single straight line. This is a clear trait of PF transport happening in the silicon nanowires. The fact that the orange down-arrows shift to lower $\sqrt{V}$ values with rise in temperature and finally approaches zero at room-temperature reinforces the hypothesis. On top of that, what makes the orange and cyan arrows different, is the fact that the slope of the curves changed polarity at orange arrows, marking a clear change in the type of the transport. This observation can be backed by simulation results of figure 5.8(a) from which it is apparent that conductance in lower voltages (the exact value of the voltage is dependent on E_A of equation 5.7), determined by equation 5.6 can be approximated as $q(\mu_n n + \mu_p p)$. For our intrinsic silicon nanowire, this can be further approximated to $qn_i(\mu_n + \mu_p)$ with n_i being the intrinsic carrier concentration. Now, if we consider the low voltage conductance at 295 K and 200 K in figure 5.10(a), we can observe a more than four orders of magnitude decrease. This is because, even though mobility increases by a factor of 2-3 by going from 295 K to 200 K, intrinsic carrier concentrations drop almost by five orders of magnitude [87]. If the dominant mechanism of current conduction is via Poole-Frenkel transport at some region of IV characteristics, then according to equation 5.7, plot of conductance, G in logarithmic scale vs $\sqrt{V}$ will form a straight line. However, this cannot be said of the transport dominated by other relevant mechanisms described by equations 5.1, 5.2, 5.4, 5.5, 5.6 or any other form of tunneling (functional form not discussed). Some portion of the curves becoming straight line, therefore, clearly establishes PF dominated transport of charge carriers in those regimes. The orange arrows approach zero because, with reduction in temperature, the de-trapping mechanism became more dependant on the applied electric field. At lower temperatures, average thermal energy ($k_B T$ of equation 5.7) of the system has dropped, making it easier for us to observe the transition to Poole-Frenkel transport. This explains the three distinct regions observed in IV characteristics

recorded in temperatures lower than 200 K.

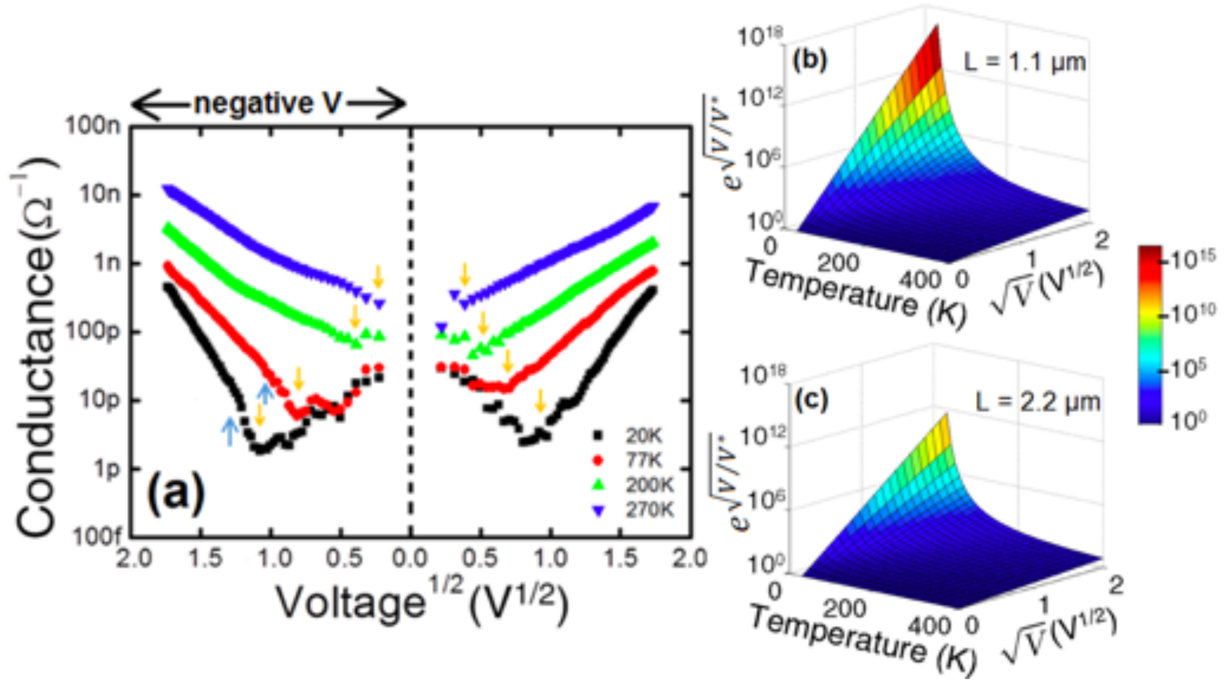

Figure 5.11: (a) Low temperature conductance vs $V^{\frac{1}{2}}$ characteristics of a long channel (2.2 μm) silicon nanowire device. (b) Plot of voltage exponent of the Poole-Frenkel expression with respect to temperature and $\sqrt{V}$ for the device with channel length of 1.1 μm. (c) Same plot for device with channel length of 2.2 μm.

VLS grown silicon nanowires are reported to have catalyst (used to grow the nanowire) all over its surface [13] and volume [61] which could be the origin of the traps. To extract the activation energy of this de-trapping process, zero-field conductance (linear extrapolation of conductance to $\sqrt{V}$=0) is plotted against inverse temperature (figure 5.10(c)) from high temperature, high electric field conductance vs $\sqrt{V}$ characteristics shown in figure 5.10(b). Higher $\sqrt{V}$ values (1.55 - 1.75) were used to make sure that the obtained activation energy is for PF transport. Higher temperatures (295 K - 390 K) were used to make sure that experimental zero-field conductance values represented by open squares in figure 5.10(c) can fit a straight line in Arrhenius plot. A similar plot (separate plot was needed to keep X-axis linear) shown in figure 5.10(d) exhibits why straight line fitting is not possible for lower temperatures (200 K, 77 K and 20 K). This behavior can also be observed from the data published by Weisse et al. [63] but to a lesser degree as the temperatures were not this low (only till 200 K). The value of activation energy obtained from figure 5.10(c) is 60 meV. A single value of activation energy is contradictory to the low temperature measurements where the slope of conductance vs $\sqrt{V}$ curves have been observed to reduce at higher $\sqrt{V}$ (cyan arrows in figure 5.10(a)). This effect can't be

attributed to the presence of Coulomb traps with different activation energies as the behaviour disappeared with increase in temperature. To investigate this reduction of slope of conductance vs $\sqrt{V}$ in figure 5.10(a) at higher voltages, a similar device but with channel length of 2.2 μm, was fabricated and characterised (matching with PF model, presented in figure 5.8(a)). The longer channel device does not exhibit reduction of slope at higher voltages (figure 5.11(a)) like the shorter channel device (figure 5.10(a)). As a matter of fact, the longer channel (2.2 μm) device characteristics has shown slight reduction in slope in only two places (marked using cyan arrows in figure 5.11(a)) exhibiting contrast to the shorter channel (1.1 μm) device. At some places the slope is even increased slightly as reported by Ben-Chorin et al. [88]. The effect of increasing channel length can be speculated by looking at equation 5.7 and 5.8. V^* is the parameter which is directly effected by changing L which, in turn, effects $e^{\sqrt{V/V^*}}$, the voltage exponent of equation 5.7. A plot of the value of this voltage exponent at different temperature and $\sqrt{V}$ is presented in figure 5.11(b) for $L = 1.1\mu m$ and in figure 5.11(c) for $L = 2.2\mu m$. These plots show that for low temperature and high voltages, the value of the voltage exponent becomes orders of magnitude higher in case of the shorter channel length device. This could lead to a change in the deterministic term of equation 5.7 and in that case the large $e^{\sqrt{V/V^*}}$ could dominate conductance thereafter. In order to support our hypothesis about gold clusters,

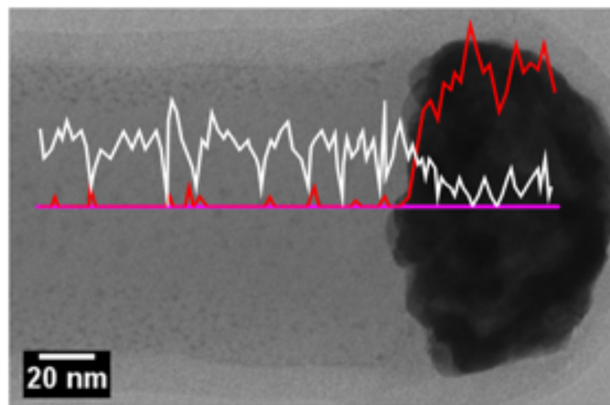

Figure 5.12: TEM image of a silicon nanowire with EDX line-scan. The purple line represents the path of the scan. White and red curves represent counts of silicon and gold respectively in arbitrary unit. The black region on the right-side of the image is the alloy nanoparticle used to grow the silicon nanowire. The gold count shows occasional small peaks before shooting-up at the nanowire to catalyst boundary.

TEM image of a silicon nanowire with Energy-Dispersive X-ray spectroscopy (EDX) line-scan has been presented in figure 5.12. The line-scan (purple straight line) spans from a point in silicon nanowire to a point in the catalyst nanoparticle, used for VLS growth. As expected,

silicon count (white curve) drops and gold count (red curve) increases sharply at the boundary of the materials. Additionally, occasional drops can be observed in silicon count along with occasional peaks in gold count. Metal catalysts other than gold may exhibit similar phenomenon. However, our experimental results provided us with scope to comment on gold catalyst only. Point defects [89] or stacking fault [90] found inside VLS grown silicon nanowires by previous studies, could also contribute to PF transport in silicon nanowires.

5.7 Conclusion

In summary, with experimental results and simulations, we have presented the evidence of Poole-Frenkel effect dominating current transport in gold catalyzed, VLS grown silicon nanowires. This could be because of the presence of residual gold catalyst inside the silicon nanowires from VLS growth process and the presence of point defects and stacking faults in resultant nanowires, acting as coulomb traps from which charge carriers were de-trapped by the applied voltage. In chapter 6 we present a detailed explanation of the origin of the traps using extensive physical characterisation of the nanowires.

Chapter 6

Physical origin of Poole-Frenkel transport in VLS grown silicon nanowires

6.1 Introduction

One of the principal advantages of VLS method is incorporation of less defects compared to other methods of silicon nanowire synthesis [6]. Because of this reason, VLS is often compared to Czochralski method [91] with the relative motion of solid and liquid phases reversed [28]. This 'Czochralski method for nanoscale' analogy became the driving force for research in VLS grown silicon nanowires. Reports of microelectronic devices made with VLS grown silicon nanowires became commonplace [92, 57, 93] in the last decade. In chapter 5, we have studied gold catalysed VLS growth of undoped (intrinsic) silicon nanowires. The results are published in a journal article [94]. To avoid any surface or confinement related effects and to understand whether any characteristic peculiarity is induced due to gold-catalysed VLS growth process itself, wide diameter ($>$ 250nm) nanowires were studied. Several test devices were made and their electrical characteristics were recorded at several temperatures between 20 K to 390 K. After that, experimental results were compared with equivalent TCAD simulations. Through that exercise, exact method of current transport through the grown nanowires were found. It has been demonstrated that charge carrier transport in these nanowires is dominated by Poole-Frenkel (PF) mechanism. Prior to this, PF transport has been reported in compound semiconductor nanowires [77], perovskite nanowires [78], field emission through nanowires [79], even transport through random networks of nanowires [80]. In fact, PF transport is always associated with transport through disordered materials or pre-breakdown conduction of

dielectrics [95]. In chapter 5, we hypothesised either one, or both of the following two factors are responsible for the phenomenon. (1) Due to the presence of gold-silicon clusters inside the volume of the silicon nanowires, acting as coulomb traps, capturing and releasing charge carriers, or (2) crystal defects formed inside silicon nanowires during VLS growth process doing the same. There are several reports that indirectly point towards either one of the hypotheses.

To support the presence of gold clusters, conclusions from one of the earliest works in this field [28] can be cited. Also, in chapter 5, we have presented the result of Energy-Dispersive X-ray spectroscopy (EDX) from a TEM . The results exhibited occasional increase in gold concentration with corresponding decrease in silicon concentration. However, anything conclusive could not be said about the placement of these gold clusters. Werner et al. used HRTEM to exhibit the presence of gold on the surface of VLS grown silicon nanowire [96]. This is supported by Sang Ho et al. [89], Hertog et al. [13] and Lee et al. [97] by their High-Angle Annular Dark Field (HAADF) Scanning Transmission Electron Microscope (STEM) results. Pioneering works in the field support the presence of crystal defects in VLS grown silicon nanowires as well. Wagner et al., also studied crystal defects in gold catalysed, VLS grown silicon nanowires throughout 1960s [28, 98]. These studies have claimed to find existence of crystal defects such as dislocations, stacking-fault, impurity striation and second phase regions using X-ray topography by Lang technique [99]. The authors also concluded that most of these defects are located near the base of the silicon nanowires and the region away from the base of the nanowire is 'perfectly' crystalline. Instability of the eutectic droplet during growth is presented as probable cause of this observation. Later, with the help of the more advanced structural characterisation technique, Transmission Electron Microscopy (TEM), Westwater et al. have reported the presence of twin-defect and stacking-fault in gold catalysed VLS grown silicon nanowires [100, 101]. However, these defects are always discussed in the context of bending or kinking. The TEM used for these studies [100, 101] had only line resolution and lacked the capability of detecting many other defects. A decade later, Akhtar et al., reported diameter dependent defect formation in gold catalysed, VLS grown silicon nanowires [102]. According to their study, silicon nanowires with diameter around 5-6 nm were observed to be free of any crystal defects. Nanowires with diameter around 16 nm were observed to have a single axial twin boundary. Nanowires with diameter larger than 20 nm were observed to have large number of twin boundaries. For nanowires grown in the [111] direction, these boundaries were found to be periodic, while for the [110] direction, these boundaries exist along the entire

length of the nanowire. Francisco et al. reported similar results with multiple stacking-faults through VLS grown silicon nanowire axis for nanowires grown in [111] and [112] direction [90]. Lee et al. [97] studied the same defects using High-Resolution Transmission Electron Microscopy (HRTEM). In that, twin defects are observed to be formed as diagonal lines across the entire nanowires (body diagonals). This omnipresence of twin defects is understandable from energetic point of view as the required energy for twin formation per bond is much lower than the average thermal energy at the temperature required for VLS growth process [103]. Later, Shin et al. were able to introduce twin boundaries and stacking-faults in gold catalysed, VLS grown silicon nanowires in a user-programmable way by rapidly changing the energetic condition (temperature and pressure) inside the reaction chamber [104].

In this chapter, we have investigated the physical origin of PF transport in VLS grown silicon nanowire presented in chapter 5. We have also tried to conclude the discussion with concrete physical evidences. To test our hypothesis, we have executed a thorough structural characterisation of the material. The results are exhibited in section 6.2. Through TEM and selected area electron diffraction (SAED), the nanowires have been found to be of perfect single crystal nature. However, we have found crystallographic misorientation throughout the nanowire and multiple regions with twin boundaries (TB) through HRTEM and HAADF. This type of 3D defect is demonstrated for the first time in VLS grown silicon nanowires. It has been shown that local crystallographic misorientation inside VLS grown silicon nanowires can result in contrast difference, resembling phase/atomic number difference in TEM. These defects comprise of small ($< 25\ nm^2$) regions of misorientation inside (111) oriented, otherwise perfectly crystalline, silicon nanowires. Analysing these results, and results from TCAD simulations, a concluding argument has been presented in section 6.3 to account for the coulomb trap mediated transport in VLS grown silicon nanowires.

6.2 Physical characterisation

Planer SEM image of a substrate after VLS growth is exhibited in figure 6.1. Most of the nanowires have grown in $\langle 111 \rangle$ direction. This is typical of silicon nanowires grown in (100) wafers with diameter in this range [27]. A portion of many nanowires has grown in arbitrary shape, as a consequence of instability of gold-silicon alloy droplet during growth. However, most of the nanowires have 8-12μm long, $\langle 111 \rangle$ oriented straight portions, as a result of en-

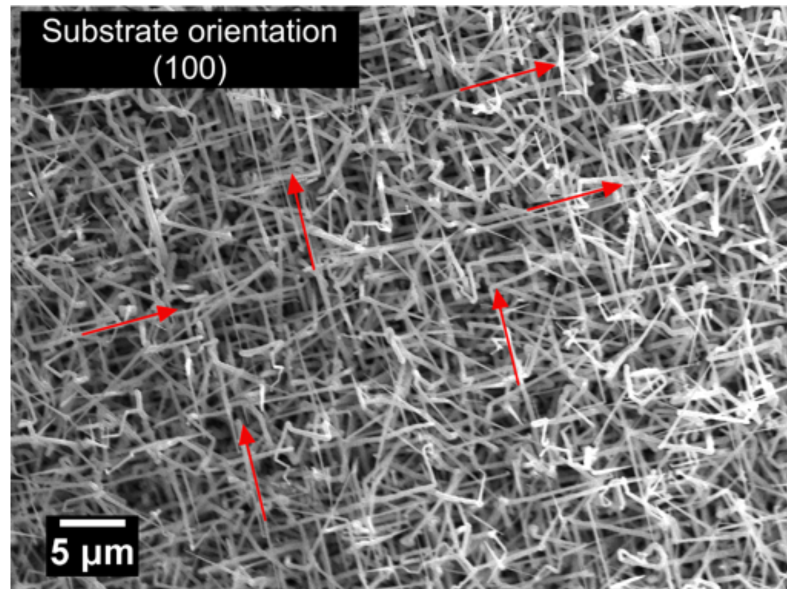

Figure 6.1: Planer Scanning Electron Microscope (SEM) image of a silicon (100) substrate after silicon nanowire growth. The red arrows indicate equivalent $\langle 111 \rangle$ directions.

ergetic condition inside reaction vessel (temperature and pressure) favouring growth in that direction, selectively increasing stability. The straight part can be separated from the rest of the nanowire, and nanowires from the substrate, by ultrasonication. The devices reported in this work are made using these straight parts selectively. This is facilitated during exploratory SEM scan of the substrate prior to device fabrication. Well defined growth direction is indicative of single crystals.

Figure 6.2 exhibits detailed bright field (BF) TEM characterisation of a silicon nanowire at different magnifications. At relatively low magnification (figure 6.2(a)), lot of dark patches on the silicon nanowire can be seen. Figure 6.2(b) and (c) shows these patches in higher magnification for two different regions. The region shown in figure 6.2(b) is marked using the dashed yellow square in figure 6.2(a). This is a region close to the boundary of the nanowire. The region shown in figure 6.2(c) is from inside the dashed orange square of figure 6.2(a). This region is near the centre of the nanowire. Both images exhibit dark patches. In figure 6.2(b) the density of the patches can be observed to increase when moving closer to the surface of the nanowire. Figure 6.2(d) shows a grayscale plot through the dashed cyan arrow in figure 6.2(b). Before taking the scan, the image was inverted (bright regions are mapped to dark, and dark regions are mapped to bright), so the spikes in the plot actually represent the presence of a dark patch (bright region in the inverted image). The size distribution of these patches in figure 6.2(c) is plotted in figure 6.2(e). Other studies have reached a conclusion that this contrast difference is

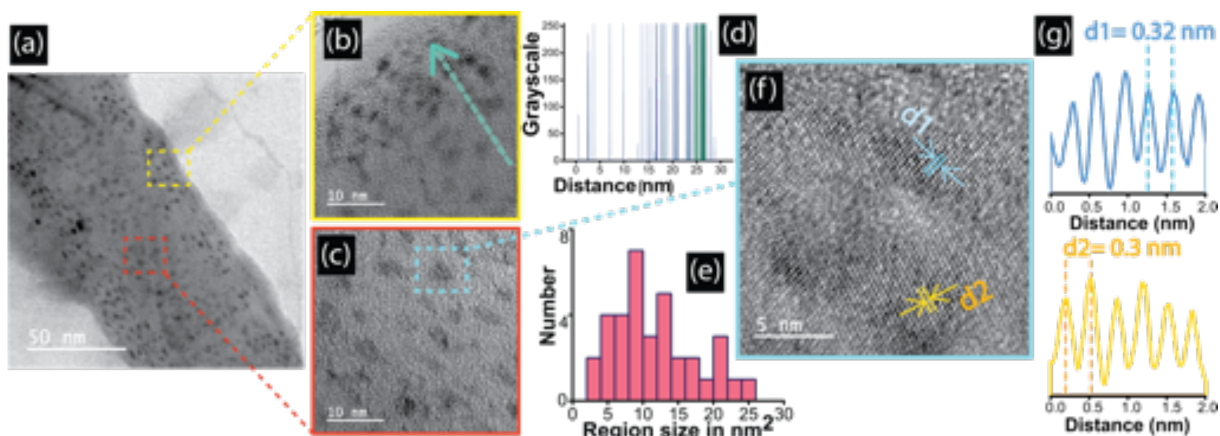

Figure 6.2: (a) TEM image of a gold catalysed, VLS grown silicon nanowire. Dark patches are visible on the nanowire. (b) The region inside the dashed yellow square in (a) at a higher magnification. (c) The region inside dashed orange square in (a) at a higher magnification. (d) A scan along the dashed cyan arrow showing how the frequency of the dark patches increases when moving towards the shell of the nanowire. In this graph, a spike in grayscale represents presence of a dark patch as the image is vectorised and inverted before taking this measurement. (e) Size distribution of the dark patches in (c). (f) HRTEM of the region inside the dashed sky blue square in (c) showing that the patches in images a-c appear due to the local presence of crystallographic misorientation on an otherwise single crystal silicon nanowire. (g) Scan showing the presence of two different d-spacing (d1 and d2) in HRTEM.

a result of phase difference [105]. However, in HRTEM (figure 6.2(f)) these spots transform into small pockets of misorientation in an otherwise perfect crystal matrix. Figure 6.2(f) exhibits HRTEM image from the region inside the dashed sky blue square in figure 6.2(c). The dark patches, therefore, can be a result of reaching near-Bragg condition. Figure 6.2(g) exhibits the d-spacings found in this region. The values of d-spacing obtained from this region is 0.32 nm and 0.3 nm which are close to the bulk d-spacing, 0.313 nm of silicon (111) planes [106]. Similar results have been found from all over the sample. Regions which appeared darker in low magnification, turned into small regions with crystallographic misorientation.

This, however, could not be captured in the SAED. Figure 6.3 exhibits diffraction from the region shown in figure 6.2(c). Even though the TEM images exhibit high density of dark patches in an area, as if the diffraction patterns appeared to be taken from a single crystal only. This suggests that, the overall misorientation should be within 5° deviation from exact s-vector [65]. Such morphology is indicative of local residual stress during VLS growth process. This is different from the findings of previous studies [96, 89, 13, 97], in which, it was concluded that the origin of contrast is indeed phase difference (atomic number contrast) and hence presented as a proof of the presence of gold. EDX results from SEM and TEM can be used to gain

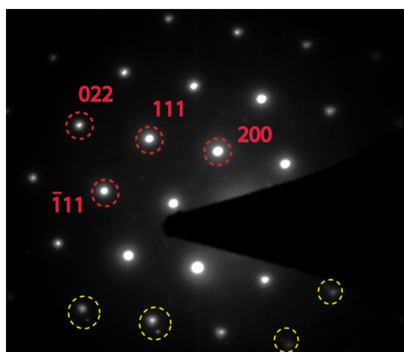

Figure 6.3: Selected area electron diffraction (SAED) of a silicon nanowire grown using VLS method. The image suggest that the grown nanowires are single crystalline. Indexed spots are marked using dashed red circle. Twin spots are marked using dashed yellow circle.

additional insight.

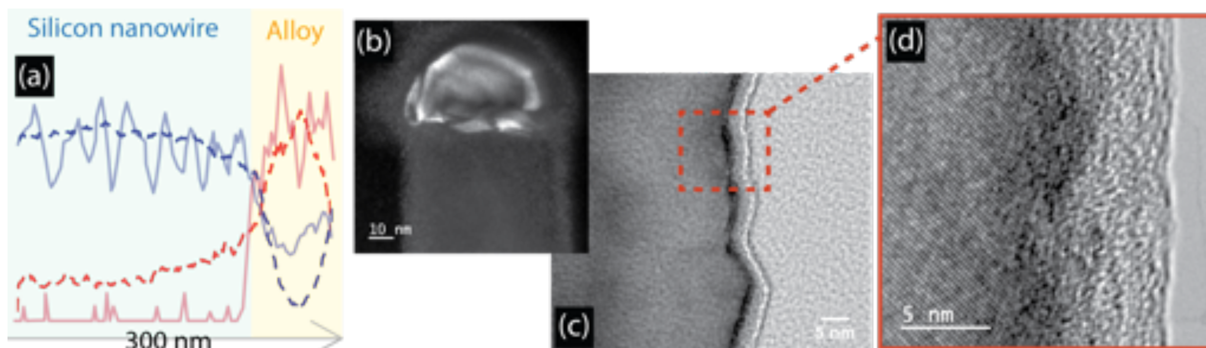

Figure 6.4: (a) EDX line-scan from FESEM and TEM of the VLS grown silicon nanowires. The dashed blue curve represents silicon concentration obtained from FESEM tool with an accelerating voltage of 20 kV. The same obtained from TEM with accelerating voltage of 200 kV is represented by the solid blue line. The dashed red curve represents gold concentration obtained from FESEM tool with 20 kV and the same obtained by 200 kV TEM is represented by the solid red line. The regions from which the data is taken are marked by the hues. Sky blue region represents the silicon nanowire and yellow tint represents the alloy nanoparticle on top of it. (b) Dark field TEM image near the tip of the silicon nanowire. The bright hemisphere on top of the nanowire is the catalyst nanoparticle. (c) TEM image exhibiting the sawtooth faceting of the nanowires. The native oxide shell of the nanowire can be seen in this image. A dark region can be seen just below the native oxide. (d) The region inside the dashed brick red square in (c) in higher magnification.

Figure 6.4(a) exhibits EDX line-scans of VLS grown silicon nanowires. Similar data is also presented in chapter 4 and chapter 5. The red curves in the image represent gold concentration and the blue curves represent silicon concentration. The solid lines are for data taken from a TEM tool and the dashed lines are for data taken from a FESEM tool. Other than the TEM data being more noisy, the main difference between the data collected using these two methods is in the concentration of gold in the silicon nanowire. In figure 6.4(a), the data from silicon

nanowire and catalyst alloy are separated using blue and yellow hue. It can be seen that, upon crossing the boundary from silicon nanowire to the alloy, the gold concentration shoots up and silicon concentration dips down. This creates a difference in contrast in the dark field TEM image presented in figure 6.4(b). In this image, the Au-Si alloy nanoparticle can be seen as the bright region on top of the nanowire. The difference in gold concentration in silicon nanowire region might give some additional insight to the position of gold within the nanowire. The EDX from TEM is taken using an accelerating voltage of 200 kV and the EDX from SEM is taken using an accelerating voltage of 20 kV. Therefore, the EDX results from SEM tool will represent data collected from near surface as the electrons have much less energy in this case and hence a much lower penetration depth [107]. This difference is observed to be repeated through several measurements in this study. To investigate further, a TEM image from (110) zone axis is presented in figure 6.4(c). In this image, a dark region can be seen between the amorphous native oxide shell and crystalline silicon nanowire core. In higher magnification, the difference in crystallinity clearly proves the presence of a different phase.

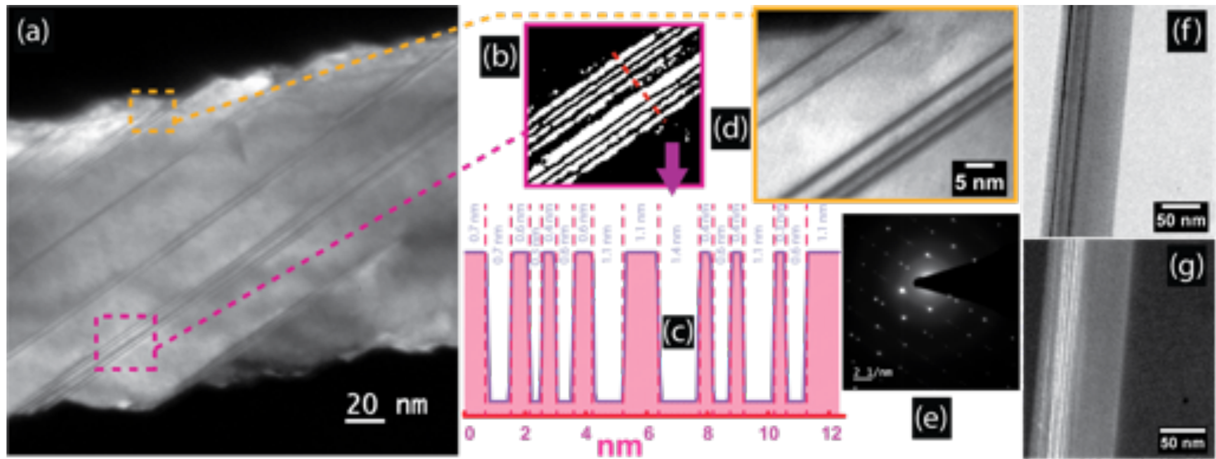

Figure 6.5: (a) Dark field TEM image of a silicon nanowire showing multiple twin boundaries spanning as diagonals on silicon nanowires. (b) Vectorised image for analysis from the region inside the dashed magenta square in (a). (c) Line scan along the dashed red line in (b) to investigate the periodicity of the defects. (d) The region inside dashed yellow square in (a) in higher magnification. One of the twin boundaries can be seen to terminate before reaching the shell of the nanowire in this image. (e) Electron diffraction showing patterns from a region with twin boundaries. (f) Axial twin bounderies spanning throughout the length of silicon nanowire. (g) The image of (f) in dark field and in slightly higher magnification.

Other than the small regions of crystallographic misorientation, similar to previous studies, twin boundaries were also found to be present in the nanowires. Figure 6.5(a) exhibits a region with multiple twin boundaries spanning as body diagonals of the nanowire. Previous studies

have anticipated these twin boundaries to be periodic [102, 108]. These types of defects are known as lamellar defects. To investigate that, the region inside the dashed violet square is analysed using image processing. Figure 6.5(b) and figure 6.5(c) exhibit the results. Even though some order in the frequency of appearance of these defects were found, we did not observe twin boundaries arranged in lamellae anywhere in the samples we analysed. However, we have observed some of these diagonal twin boundaries terminate before reaching the faceted surface of the nanowire. One such twin boundary can be seen by observing the region marked using the dashed yellow square in high magnification. The result is exhibited in figure 6.5(d). SAED from this region is presented in figure 6.5(e). The diffraction clearly exhibits presence of growth twins. Other than the diagonal twin boundaries, we did observe some twin boundaries spanning throughout the length of the nanowires. One such nanowire is exhibited in figure 6.5(f) and figure 6.5(g) in bright field and dark field. However, unlike the previous reports [102, 108] this type of defects are found in nanowires grown in [111] direction instead of [110] direction. The effect, these defects have, on electron transport is discussed in section 6.3.

6.3 Effect of defects on transport

Figure 6.6(a) shows the SEM image of a silicon nanowire device which is exhibiting PF transport. 2D cross section along its axis is simulated in Sentaurus TCAD environment to obtain information about electrostatics and carrier action inside the nanowire. Figure 6.6(b) exhibits electrostatic potential inside the silicon nanowire, when a 3V potential difference is applied between its metal contacts. Circuit symbols in figure 6.6(a) mark positive potential applied to the left metal contact and connection of ground terminal to the right contact. As expected, the region covered by metal contacts are almost equipotential. The plot of electric field in figure 6.6(c) shows the highest value of absolute electric field near the edges of metal contact. High electric field is also present in the entire channel region. This means, at this bias condition, any electron (hole) in the channel region should be quickly swept away to the left (right) contact. Figure 6.6(d) presents the current density plot in this bias condition. From the plot, it can be observed that the majority of the current in this nanowire is contributed by the subsurface region. To understand the current more, a band diagram is drawn (figure 6.6(e)) along the path, through which most of the current flows. Dashed white line in figure 6.6(a) and (d) represent the x-axis of the band diagram. The red box represents the metal contact where 3V positive

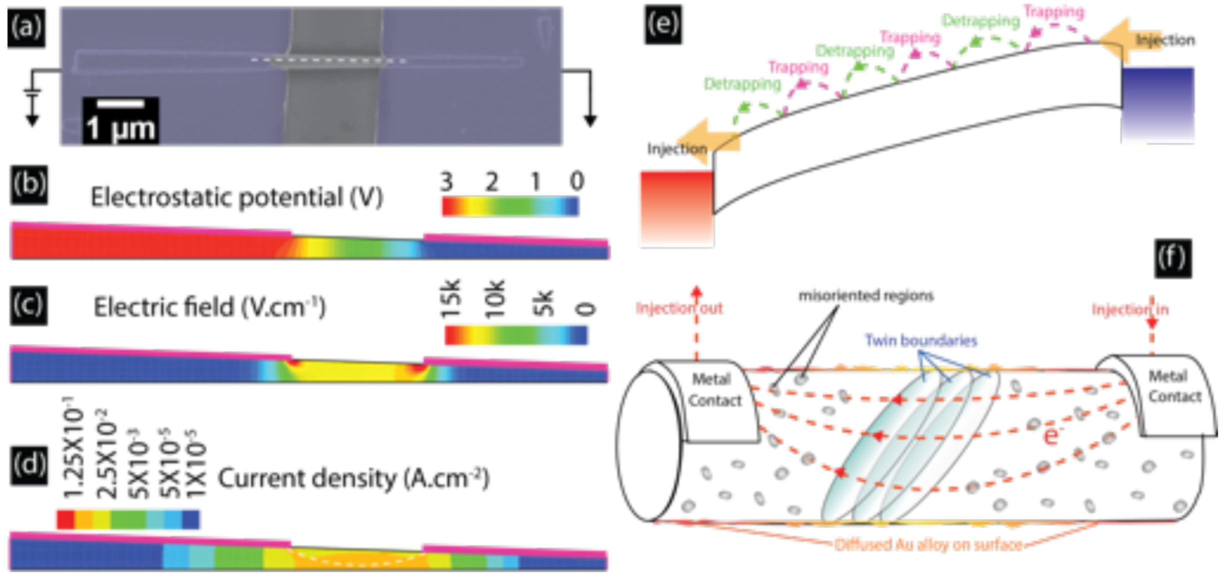

Figure 6.6: (a) SEM image of the device exhibiting PF transport. The circuit symbols represent connections to external measurement circuit and connections in simulation. Positive bias is applied to the contact on left. Ground is connected to the contact on right. (b) Sentaurus TCAD simulation result from a test structure identical to the one shown is (a). The plot exhibits electrostatic potential inside the nanowire. Magenta lines on the plot represent the positions of the metal contacts. (c) Plot of absolute value of electric field inside the nanowire under the biasing condition described by (a)-(b). (d) Total current density inside the nanowire. The condition at which the plot is taken is same as (a)-(c). (e) Band diagram along the dotted white line shown in (a) and (d). (f) A schematic diagram explaining the effect of different defects, found in this work, on electron transport.

bias is applied and the blue box represents the grounded metal contact. It can be observed from the band diagram that even though the electric field in the channel region aids electron and hole current both, the current in the device will be mostly contributed by electrons due to electron injection from the metal. Because of this, number of electrons available at any moment, in the channel region, will be orders of magnitude higher than the available holes. However, because of the presence of defects, the dominant mode of current transport has been shifted to PF instead of drift. This is conceptually represented by the dotted arrows on the band diagram. The physical interpretation of PF transport involves periodic trapping and detrapping of charge carriers in response to the applied potential. Figure 6.6(f) schematically explains this for electrons. After injection from one metal contact, the electrons rush to the other contact in response to the electric field present in the channel region (figure 6.6(c)). However, instead of drifting through a perfectly crystalline silicon, it encounters numerous misoriented regions and twin boundaries on its path. As a result, the electrons traverse through a sequence of trapping and detrapping events before finally reaching to the other metal contact. Since the simulation shows majority

of the current is subsurface (figure 6.6(d)), the gold-silicon alloy trapped on the surface of the nanowire has very little effect on the overall current. In that case, the locally misoriented regions (dark patches in TEM) should have the biggest effect on the current because of their high density. On the other hand, axial twin boundaries shown in figure 6.5(f) and (g) should have the least effect on the transport as they are mostly aligned to the direction of flow of charge carriers. This is analogous to the grain boundary effect in polycrystalline silicon solar cells [109].

6.4 Conclusion

In summary, we have successfully concluded the argument started in chapter 5, in which Poole-Frenkel transport is established as the dominant mechanism of current transport through VLS grown silicon nanowires. As anticipated in chapter 5, through thorough structural study of the material, we have found evidence of catalyst clusters and crystal defects in these silicon nanowires. It has been also exhibited that, the catalyst clusters are only present on the surface of the nanowires. Through TCAD simulations, it has been shown that majority of the current in these silicon nanowire devices are from subsurface region. Also, the study of defects suggest, not all defects contribute to the periodic trapping-detrapping of charge carriers responsible for the manifestation of PF transport. For instance, some twin boundaries appear as body diagonal of the silicon nanowires, while some are oriented along the direction of current flow in these devices. Even though occurrence of both these defects are almost periodic, because of the way they are oriented, the former type of defect will have more severe impact on the electron transport in the fabricated devices of this work. However, small ($<25\ nm^2$) regions of crystallographic misorientation inside the otherwise perfectly crystalline silicon nanowires are reported, for the first time. Their high frequency and omnipresence in the grown nanowires led to our strong belief that they are the single most important type of defect contributing towards the manifestation of PF transports in VLS grown silicon nanowires.

Chapter 7

Conclusions and future work

The main objective of this work is to pave the way for bottom-up preparation of silicon nanowire devices. In this work, the entire process of silicon nanowire device preparation is discussed. From material synthesis, to optimisation of device parameters, which impact electrical characteristics. In chapter 4, the most promising method of bottom-up process of silicon nanowire synthesis, VLS method is studied. The growth is executed in a simple, low cost, spherical, cold-wall catalytic chemical vapour deposition tool. Relative simplicity of the setup, should make VLS growth accessible to a wider group of researchers. Also, the low cost of the components required to assemble such a tool, should bring down the cost of silicon nanowire production. Moreover, use of this tool should abruptly bring down the thermal budget as, instead of the entire process chamber, heat is applied to the sample only. This would lead to much lower energy consumption for the process, which will lower the cost further. Each step of recipe optimisation for the tool is documented in chapter 4. Details of the growth process are provided in appendix A. The next step in electronic device production, transfer of silicon nanowire to a foreign substrate and fabrication of test devices using lithography, is exhibited in chapter 4. The process details are given in appendix A. After that, using several electrical characterisation techniques and TCAD simulations, the mechanism of charge carrier transport in the VLS grown silicon nanowires is studied in chapter 5. It has been found that the dominant method of charge carrier transport is through Poole-Frenkel mechanism. Previous studies could not find this because of the state of doping and contact formation. It is important to note that, to observe PF dominated electrical characteristics, the resistance of the silicon nanowire channel has to be higher compared to the resistance of the reverse biased contact at that bias condition. This makes it highly unlikely for this behaviour to be observed in doped nanowires. Also, in thin-

ner nanowires (diameter 10 nm), PF transport is masked by surface induced effects because of relatively high surface to volume ratio. Electrical characteristics to exhibit the onset of PF transport have been presented in chapter 6. Prior to this work, PF transport is always associated with disordered materials, not single crystals such as VLS grown silicon nanowires. It has been anticipated that either residue gold clusters or crystal defects were responsible for the manifestation of PF transport. To investigate this, detailed physical characterisations are presented in chapter 6. With the help of the outcome of the physical characterisations and TCAD simulations, a concluding theory of charge carrier transport through VLS grown silicon nanowires is presented at the end of the work.

Even though concluding remarks are presented at the end of this work, we believe the following future works to be important.

- Even though use of the simple equipment described in chapter 4 should have a major impact in cost and complexity of VLS growth of silicon nanowires, production costs can be reduced even further. The precursor used in the VLS growth process is SiH_4, which is quite expensive. In the process explained in chapter 4, 10 sccm silane is flown through the reactor. Only a small fraction of the precursor could come in contact with liquid FECA nanoparticles and take part in dissociation reaction to form solid silicon. The rest of the precursor is blown out of the chamber by the exhaust. To make the process even more commercially viable, a feedback has to be designed so that the SiH_4 from the exhaust can be harvested.

- In this work, it has been discovered that VLS grown silicon nanowires have small (< 25 nm^2) regions of crystallographic misorientation, within 5° deviation from exact s-vector, all over its volume. This is indicative of local residual stress during VLS growth process. It is also discussed in this work, the impact these and other form of defects have in the transport of charge carriers through VLS grown nanowires. However, it should be of enormous interest, if the actual physical mechanism of creation of these defects can be identified. In that case, the defects can be added or removed in a user programmable way. Doing that will allow researchers to either avoid or exploit the presence of these defects for various applications.

- Study of the optical and electron-optical properties of these nanowires should be of interest to researchers in several fields.

- A study of the thermoelectric properties of these nanowires would be interesting. To achieve good thermoelectric property, a material must hinder the transport of phonon through some mechanism. The small misoriented regions within the volume of the silicon nanowires should impact the phonon transport within the material. Well planned experiments and simulations are required to gain practical understanding of the effect.

- Since silicon nanowires are already proven to be bioresorbable and non-cytotoxic, substrates with dense mesh of nanowires could be used to create composite materials with living biological organisms. One such composite would be with filamentous algae such as spirogyra. The shape and size of the algae should allow the composite to form spontaneously in Murashige and Skoog medium (MS0). Once formed, the electrical characteristics of the composite device can be studied to obtain understanding of the intracellular processes that involve transfer of charge carriers. This composite can also be used to influence behaviour of the living cells. Additionally, the composite can be used as sensors in aqueous medium.

Appendices

Appendix A

Methods

A.1 Optimisation of catalyst nanoparticle formation

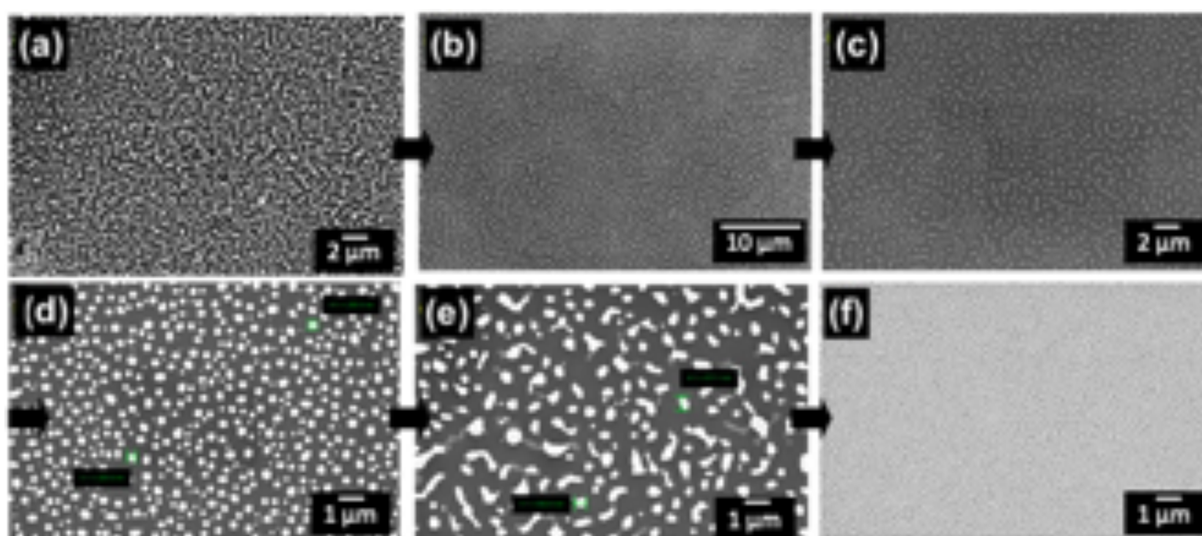

Figure A.1: (a) 20 nm Au film annealed for 1 minute at 550°C. (b) 20 nm Au film annealed for 1 minute at 650°C. (c) 20 nm Au film annealed for 1 minute at 800°C. (d) 20 nm Au film annealed for 2 min at 800°C. (e) 20 nm Au film annealed for 5 min at 800°C. (f) 5 nm Au film annealed for 2min at 800°C.

The first step of growing silicon nanowires using VLS method is optimisation of the catalyst nanoparticles. The target is to have well separated, circular nanoparticles on the surface of the substrate. If the surface of the substrate between the nanoparticles is not devoid of catalyst, during VLS growth, unwanted artefacts grow on the substrate. This can seriously obscure the observations of experiments. On the other hand, directional, anisotropic growth is hindered if the nanoparticles are not circular. The diameter of these particles is important as well. It defines

the temperature and pressure required for the growth. Also, diameter of the grown nanowire is defined by the diameter of the nanoparticle. Therefore, optimising the diameter of the nanoparticles leads to optimisation of the diameter of the nanowires. In figure A.1, key aspects of the optimisation process is exhibited. In figure A.1(a)-(c), the effect of annealing temperature is shown. In figure A.1(c)-(e), the effect of annealing duration is shown. In figure A.1(d) and (f), the effect of initial film thickness is shown.

Optimised recipe: Deposit 5 nm gold thin film using Orion sputter. Verify film thickness with quartz crystal in situ as well as physical characterisation techniques. After that, transfer the wafer to AnnealSys AS-ONE 150, rapid thermal annealing system. If the substrate is small, make sure it covers the pyrometer underneath the sample, which is used to control the temperature of the chamber, real time, using a PID controller. Set temperature ramp rate as 100°C/sec. This high ramp rate is important to avoid Ostwald ripening, which creates larger catalyst particles in the expense of small particles. Pass 900 sccm N_2 as the ambient gas for the annealing process. Anneal for 2 min at 800°C.

A.2 Silicon nanowire growth

Silicon nanowires were grown in a spherical cat-CVD chamber. The precursor gas (SiH_4) was flown into the chamber using mass flow controllers. The (100) silicon wafers, used to prepare substrate for VLS growth, were cleaned by standard RCA cleaning procedure ending with a 2% HF dip for chemical oxide removal. After that, 5 nm thick gold thin film was deposited on top of the substrates using thermal evaporation. Thickness of the gold thin film was monitored by a quartz crystal during evaporation. The thickness was also confirmed using cross-section Scanning Electron Microscopy (SEM). To make nanoparticles from the film, the substrates were annealed at 800°C for 2 minutes. After that, silane (SiH_4) was passed at 10 sccm for 4 hours while the substrate was kept at 600°C. Optimisation process of the recipes are detailed in our previous work [81].

Optimised recipe: Use the optimised recipe to make silicon-Au eutectic nanoparticles on (100) silicon substrate. Before loading the sample into HWCVD tool, dip the sample vertically into 2% HF solution for 15 second at room temperature. After that, quickly dip the sample couple of times in de-ionised water and place it into the load lock chamber at the centre of the instrument. The vacuum of the load lock chamber will dry the sample. After vacuum

is reached, transfer the sample to the i-poly chamber of the tool. After the base vacuum is achieved, set substrate temperature as 750°C. In this tool, the temperature is measured using a thermocouple connected to the heating element. The substrate is kept at a distance above the heating element. There is no physical connection. However, a chart is available in the laboratory to find out the exact temperature of the substrate. This chart is prepared by recording data from a pyrometer. 750°C at the heating element results in 600°C at the substrate. After the temperature is reached (750°C at the thermocouple), pass 100 sccm H_2 for 5 minutes and close the lid covering the sample. Stop H_2 flow and start 10 sccm SiH_4 flow. When SiH_4 flow is stabilised, stop closing the gate valve between the chamber and exhaust. While doing this, keep an eye on the pressure gauge to see the reading. The pressure will rise as you keep closing the gate valve. Stop when pressure reaches 5×10^{-2} mbar. Open the lead covering the sample and start timer. Continue this for 4 hours. During this time keep checking the pressure inside the chamber. The absence of any automatic pressure control leaves it to the user to maintain the pressure inside the chamber. The quality of the nanowire depends on how precisely the pressure is maintained. Any fluctuation in the pressure, during the 4 hours of growth, will result in bent and kinked nanowires.

A.3 Physical characterisation

The plane view of the substrates after growth and device fabrication were taken using a Jeol JSM-7600F, (Field Emission Gun) FEG-SEM tool with an accelerating voltage of 8 kV. For EDX line scans, 20 kV accelerating voltage was used in the same tool. To take TEM images, substrates with silicon nanowires were immersed in de-ionised (DI) water and sonicated for 10 minutes. After that the suspended solution was drop-casted and dried on copper grids. After that, the grids were used to take the TEM images using a FEI Tecnai G2 F30 tool at an accelerating voltage of 300 kV. EDX scans were taken using 200 kV accelerating voltage in Jeol JEM 2100F HRTEM.

A.4 Device fabrication

Substrates were prepared by 100nm dry oxidation of (100) silicon wafers. To fabricate test structures, substrates with silicon nanowires were sonicated and the resultant solution was dis-

persed on SiO_2 substrate. After gentle drying of the solution, silicon nanowires were located and marked by SEM imaging. RAITH 150 Two electron-beam lithography (EBL) tool was used to pattern contacts on silicon nanowires through PMMA (polymethyl methacrylate). Substrates with PMMA were developed using a 1:3 MIBK/IPA developer solution. After development, metals were deposited using thermal evaporator and the samples were kept immersed in acetone for lift-off.

A.5 Device characterisation

Agilent B1500 Semiconductor Device Analyzer was used to study and record the electrical characteristics. The metal contacts were probed via contact pins connected to a Keithley switch matrix. To avoid any transient effect, each data point is integrated over 6 power line cycles (PLC).

A.6 Details of simulation

TCAD simulations were carried out using Synopsys TCAD Structure editor and Device simulation tools. A 2D structure has been constructed in the simulation environment considering the symmetries of the device structure. The structures were then divided into meshes to solve Poisson's equation and continuity equations iteratively. The mesh sizes are optimised to reach a balance between accuracy and computation time. The results were normalised with a multiplier named as 'area factor' to convert the 2D result into 3D. For Poole-Frenkel (PF) model, value of the activation energy (E_a) was probed as 60 meV according to the results of our previous study.

Appendix B

Codes for simulation

B.1 Structure editor: to create the device structure

```
(sde:clear)
   (define nm 1e-3)

   (define xAlow (* -5.0))
   (define xAhigh (* 5.0 ))
   (define yAlow (* -5.0 ))
   (define yAhigh (* 0.0 ))

   (define xSlow (* -4.0))
   (define xShigh (* -2.5 ))
   (define ySlow (* -0.45 ))
   (define yShigh (* 0.0 ))

   (define xDlow (* -1.5))
   (define xDhigh (* 4.0 ))
   (define yDlow (* -0.45 ))
   (define yDhigh (* 0.0 ))

   (define xDLlow (* -3.0 ))
   (define xDLhigh (* 3.0 ))
   (define yDLlow (* -0.35 ))
   (define yDLhigh (* 0.00 ))
```

```
(define xOXlow (* -5.0))
(define xOXhigh (* 5.0 ))
(define yOXlow (* 0.00 ))
(define yOXhigh (* 0.1 ))

(define xSUBlow (* -5.0 ))
(define xSUBhigh (* 5.0 ))
(define ySUBlow (* 0.1 ))
(define ySUBhigh (* 5.0 ))

(sdegeo:set-default-boolean "ABA")
(sdegeo:create-rectangle (position xAlow yAlow 0) (position xAhigh yAhigh 0) "Vacuum"
"Air")
(sdegeo:create-polygon (list (position -4 0 0) (position -4 -0.450 0) (position -2.5 -0.450 0)
(position -2.5 0 0))
"Aluminum" "SOURCE")
(sdegeo:create-polygon (list (position -1.5 0 0) (position -1.5 -0.450 0) (position 4 -0.450 0)
(position 4 0 0))
"Aluminum" "DRAIN")
(sdegeo:create-polygon (list (position -3 0 0) (position -3 -0.350 0) (position 3 -0.350 0)
(position 3 0 0))
"Silicon" "DEVICE LAYER")
(sdegeo:create-rectangle (position xOXlow yOXlow 0) (position xOXhigh yOXhigh 0) "Ox-
ide" "OXIDE")
(sdegeo:create-rectangle (position xSUBlow ySUBlow 0) (position xSUBhigh ySUBhigh
0) "Silicon" "SUBSTRATE")

(sdegeo:define-contact-set "source" 4.0 (color:rgb 1.0 0.0 0.0 ) "")
(sdegeo:define-contact-set "drain" 4.0 (color:rgb 0.0 1.0 0.0 ) "")
(sdegeo:define-contact-set "gate" 4.0 (color:rgb 0.0 0.0 1.0 ) "<><>")

(sdegeo:set-current-contact-set "source")
(sdegeo:set-contact-edges (find-edge-id (position -3.9 -0.45 0)) "source")

(sdegeo:set-current-contact-set "drain")
```

(sdegeo:set-contact-edges (find-edge-id (position 3.9 -0.45 0)) "drain")

(sdedr:define-constant-profile "SUBSTRATE" "BoronConcentration" 0)

(sdedr:define-refeval-window "SUBSTRATE_window" "Rectangle" (position -4.0 0.1 0) (position 4.0 5.0 0))

(sdedr:define-constant-profile-placement "SUBSTRATE_Def" "SUBSTRATE" "SUBSTRATE_window

(define mesh1 (* 0.001))

(define mesh3 (* 0.1))

(define mesh4 (* 0.05))

(sdedr:define-refeval-window "RefEvalWin$_1$"”$Rectange$”$(position-300)(position3-0.350))$

(sdedr:define-multibox-size "MultiboxDefinition$_1$”$0.0050.0050.00010.0001-1.1-1.1)$

(sdedr:define-multibox-placement "MultiboxPlacement_1" "MultiboxDefinition_1" "RefEvalWin$_1$”)

(sdedr:define-refinement-function "MultiboxDefinition_1" "DopingConcentration" "MaxTrans-Diff" 1)

(sde:build-mesh "mesh" "-F tdr " "NW")

B.2 Device simulation: to obtain the IV characteristics

File {

Grid= "NW$_m sh.tdr$”

Current= "NW.plt"

Plot= "NW$_I dVg.tdr$”

Output= "NW$_I dVg.log$”

Parameter= "nwiv.par"

}

Electrode {

{ name="drain" Voltage=0.0 }

{ name="source" Voltage=0.0 }

}

```
Physics {
EffectiveIntrinsicDensity( OldSlotboom )
Recombination(
SRH(DopingDep)
Band2Band(E2)
Avalanche(CarrierTempDrive)
)
}

Physics(Material="Silicon") {

Mobility(
PhuMob
PFMob
HighFieldsaturation
Enormal
)
EffectiveIntrinsicDensity(OldSlotboom)

Recombination(
SRH( DopingDep )
Band2Band(E2)
Avalanche(CarrierTempDrive)
)
}

Physics (MaterialInterface="Titanium/Silicon") {
Traps((FixedCharge Conc=4.5e+10))
Schottky eRecVelocity=2.573e6 hRecVelocity=1.93e6
Schottky BarrierLowering
Schottky
Thermionic
HeteroInterface
Schottky DistResist=1e-6
```

```
Recombination(
Radiative
SRH
Avalanche(CarrierTempDrive)
eBarrierTunneling "NLM"
hBarrierTunneling "NLM"
Band2Band(E2)
)
}

Plot {
eDensity hDensity
eDriftVelocity hDriftVelocity
TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
eMobility hMobility
eVelocity hVelocity
eQuasiFermi hQuasiFermi
eTemperature * Temperature hTemperature
hTemperature
ElectricField/Vector Potential SpaceCharge
Doping DonorConcentration AcceptorConcentration
SRH Band2Band * Auger
AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eEparallel hEparallel eENormal hENormal
BandGap
BandGapNarrowing
Affinity
ConductionBand ValenceBand
* eTrappedCharge hTrappedCharge
* eGapStatesRecombination hGapStatesRecombination
}
```

```
Math {
Extrapolate
Avalderivatives
RelErrControl
Digits=5
ErRef(electron)=1.e10
ErRef(hole)=1.e10
Notdamped=50
Iterations=20
DirectCurrent

NonLocal "NLM" (
MaterialInterface="Titanium/Silicon"
Length=10e-7
Permeation=100e-7
Direction=(0 1 0) MaxAngle=5
-Transparent(Material="Titanium")
)
}

Solve {
Poisson
Coupled { Poisson Electron }
Coupled { Poisson Electron Hole}
save(FilePrefix="initial")

load(FilePrefix="initial")
NewCurrentPrefix="idvg_vs_0.0"
QuasiStationary
( InitialStep=1e-4 Increment=1.3 Maxstep=1e-2 MinStep=1e-6
Goal { name="drain" voltage=-3.0 }
)
{ Coupled { Poisson Electron Hole}}
NewCurrentPrefix="idvg_vs_5.0"
```

QuasiStationary

(InitialStep=1e-4 Increment=1.3 Maxstep=1e-2 MinStep=1e-6

Goal { name="drain" voltage=3.0 }

)

{Coupled { Poisson Electron Hole}}

Plot (FilePrefix="idvg$_{v}s_{0}$.0”$Time = (0;0.5;1)NoOverwrite$)

Coupled { Poisson Electron Hole}

}

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Publications

1. S. Acharya and A. Kottantharayil, “VLS Growth of Silicon Nanowires in Cold Wall Cat-CVD Chamber", IEEE 2nd International Conference on Emerging Electronics (ICEE). DOI: 10.1109/ICEmElec.2014.7151169

2. S. Acharya and A. Kottantharayil, “Poole–Frenkel Transport in Gold Catalyzed VLS Grown Silicon Nanowires." IEEE Transactions on Electron Devices 65, no. 5 (2018): 1685-1691. DOI: 10.1109/TED.2018.2817544

3. S. Acharya, B. Tongbram, I. Samajdar and A. Kottantharayil, “What causes Poole-Frenkel transport in VLS grown silicon nanowires?”, *Under review*.

Publication not related to thesis:

4. S. Acharya, A. V. Babu, R. A. Khadar and A. Kottantharayil, “Mobility improvement in CVD graphene by using Local Metal Side-Gate”, *manuscript under preparation*.