Novel plasma processes for surface passivation and light trapping in crystalline silicon solar cells

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by

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under the guidance of

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2016

Dedicated to

my Amma, Achan

Brother and Gudia

Thesis Approval

This thesis entitled

Novel plasma processes for surface passivation and light trapping in crystalline silicon solar cells

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Declaration

I declare that this written submission represents my ideas in my own words and where others ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that Chapter 5 of this thesis contains the work we have published in IEEE Electron Device Letters, vol. 34, no. 7, pp. 918 - 920, 2013 and in the proceedings of the 28^{th} European Photovoltaic Solar Energy Conference and Exhibition, pp. 1899 - 1902, 2013. Chapter 6 contains the work that has been submitted to the Journal of applied physics and is under review. Chapter 7 of this thesis contains the work we have published in IEEE Journal of Photovoltaics, vol. 6, no. 1, pp. 74 - 78, 2016. Chapter 8 contains the work we have published in IEEE Journal of Photovoltaics, vol. 5, no. 3, pp. 819 - 825, 2015 and in the proceedings of the 40^{th} IEEE Photovoltaic Specialists Conference, pp. 1244 - 1247, 2014.

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Abstract

Improving the solar cell efficiency while maintaining the cost of production or lowering the cost of production while maintaining the solar cell efficiency are the desiderata in case of the crystalline silicon solar cell industry. In the late 1990's, efficiency levels $\sim$ 25% have been demonstrated for crystalline silicon solar cells based on novel device architectures. The processing cost involved in manufacturing these cells were prohibitively high that the solar cell industry had not adopted it for mass production. However, the processing of these high efficiency devices involve some of the best practices that needs to be adopted in pursuit of higher solar cell efficiencies.

Thermal oxidation of silicon is one of these best practices adopted in the high efficiency silicon solar cell fabrication. Thermally grown SiO_2 film is known to form high quality interface with silicon, making it an ideal candidate as a surface passivation layer. The thick (105 nm) SiO_2 film also serves as the anti-reflective coating. The high temperature of processing, coupled with its low growth rate and hence low throughput have made this technology expensive and unviable for the industry. In this thesis, a process for growing silicon oxide/silicon oxy-nitride films on silicon at temperatures $< 400^oC$ is discussed. The process involves exposing the silicon surface to an oxidising plasma ambient. Thin silicon oxy-nitride films are capped with silicon nitride and their surface passivation potential is investigated. Surface recombination velocity less than 50 cm/s was obtained for the stack of silicon oxy-nitride/silicon nitride. The growth of an interfacial silicon oxy-nitride prior to silicon nitride deposition was also found to improve the thermal stability of the silicon nitride passivation. The emitter surface passivation in case of c - Si solar cells was seen to improve when the stack of silicon oxy-nitride/silicon nitride was used as the passivation layer, resulting in 5 mV improvement in open circuit voltage. Comparable emitter passivation performance was observed when the plasma grown silicon oxy-nitride (380^oC) film was benchmarked with that of a thin thermally grown (600^oC) silicon oxide film. The stack is thus an alternative option for emitter surface passivation in case of p-type silicon

solar cells.

Silver contacts used in silicon solar cells adds significantly to the cost of solar cells. To lower the cost of production, alternative metallisation schemes based on electroplated Ni - Cu contacts is being investigated. Electroplating of Ni - Cu contacts in silicon results in unwanted/residual plating in pin holes present in silicon nitride films. Modification of the silicon nitride layer or surface treatments to lower the pin hole density in silicon nitride is mandated, during technology development of Ni - Cu metallisation processes. One such surface treatment process involves treating the silicon nitride film in Ar + N_2O plasma ambient. However, the surface passivation quality of plasma enhanced chemical vapour deposited (PECVD) silicon nitride film is reported to degrade with plasma treatment. A detailed investigation on the impact of Ar + N_2O plasma post treatment process on the surface passivation properties of the silicon nitride film is discussed in this thesis. On exposing a PECVD silicon nitride film to an Ar + N_2O plasma the effective minority carrier lifetime is seen to improve from 266 μs to 863 μs at a minority carried density (MCD) of $10^{15}cm^{-3}$. This correlates with an order of magnitude decrease in interface state density at the silicon - silicon nitride interface which is likely due to the enhanced passivation of the interface. The improvement in effective lifetime is seen for both n-type, p-type as well as n^+ emitter surfaces. The improvement in effective lifetime was also observed for different plasma ambient like Ar, He and Ar + N_2O. The enhancement in passivation is also seen to be stable for annealing up to 450^oC. Coupled with its potential for reducing background plating, the proposed process is a promising candidate for developing passivation layers for cell technologies with low temperature metallisation schemes.

Inverted pyramidal texturing is yet another best practice adopted in high efficiency silicon solar cells. The process results in lower reflectance and leads to lower number of defects on the wafer surface. The process however is not adopted by the silicon solar cell industry owing to the expensive photolithography steps required for this process. In this thesis, a novel process for the fabrication of inverted pyramids on silicon is discussed. The process replaces the photolithography step with a thin film deposition step and thermal annealing. The process involves using open blisters formed in silicon nitride films as an etch mask to fabricate inverted pyramids in silicon. The mechanism behind the formation of blisters as well as the impact of various process conditions on blister formation in silicon nitride is investigated in this thesis. By tailoring the blister formation process, a blister surface coverage of 51% was obtained for a low temperature annealing at 550^oC. When etched in anisotropic etchant, this resulted in a

weighted average reflectance of 17.3%, indicating that the process can be a viable alternative for inverted pyramid fabrication with further improvement in surface coverage of blisters. The process can also be used to generate blisters of sub micron dimensions, making the process a potential candidate for fabrication of nano pyramids.

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My career would have taken another track, had it not been for my parents and my brother, who had convinced me to stay back at IIT Bombay to pursue my higher studies way back in 2009. A similar "awakening" happened in Oct, 2012 and it was Sreetama, my wife, (my good friend then), who convinced me in the nick of time to pursue a PhD. None of this would have been possible without their encouragement, blessings and unconditional love. Their contribution in shaping my life and my research career is beyond words, and it is to them that I dedicate my thesis.

Sandeep S. S.

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List of Abbreviations

AFM	Atomic force microscope
ALD	Atomic layer deposition
ARC	Anti reflective coating
ARXPS	Angle resolved x-ray photoelectron spectroscopy
BHF	Buffered hydrofluoric acid
BSF	Back surface field
c - Si	Crystalline silicon
CVD	Chemical vapour deposition
Cz	Czochralski
EELS	Electron energy loss spectroscopy
EHP	Electron hole pair
EQE	External quantum efficiency
FF	Fill factor
FTIR	Fourier transform infrared spectroscopy
FZ	Float zone
HFCV	High frequency capacitance voltage
HFGV	High frequency conductance voltage
HRTEM	High resolution transmission electron microscope
IBC	Interdigitated back contact
ICP - CVD	Inductively coupled plasma chemical vapour deposition
IE	Iodine ethanol
IPA	Isopropyl alcohol
IQE	Internal quantum efficiency
ITRPV	International technology roadmap for photovoltaics
IV	Current - voltage

iV_{oc}	Implied open circuit voltage
J_{0e}	Emitter saturation current density
J_{sc}	Short circuit current density
LPCVD	Low pressure chemical vapour deposition
MCD	Minority carrier density
MIS	Metal insulator semiconductor
MOS	Metal oxide semiconductor
η	Efficiency
OES	Optical emission spectroscopy
PCD	Photo conductance decay
PECVD	Plasma enhanced chemical vapour deposition
PERC	Passivated emitter and rear contacts
PERL	Passivated emitter, rear locally diffused
PERT	Passivated emitter, rear totally diffused
pFF	pseudo fill factor
PIII	Plasma immersion ion implanter
PV	Photovoltaics
QM	Quinhydrone methanol
QSS	Quasi steady state
RF	Radio frequency
RI	Refractive index
R_s	Series resistance
R_{sh}	Shunt resistance
R_{sheet}	Sheet resistance
SCCM	Standard cubic centimetre per minute
SEM	Scanning electron microscope
S_{eff}	Effective surface recombination velocity
SLPM	Standard liter per minute
SRH	Shockley - Read - Hall
SRV	Surface recombination velocity
STC	Standard test conditions
τ_{bulk}	Bulk lifetime

τ_{eff}	Effective lifetime
TOF - SIMS	Time of flight secondary ion mass spectroscopy
V_{oc}	Open circuit voltage
W_{av}	Weighted average
XPS	X-ray photoelectron spectroscopy

Chapter 1

Introduction

Over the last decade, there has been an increasing thrust to move towards sustainable and clean energy sources. Renewable energy sources like solar, wind, hydro and tidal energy have been in the forefront of this tectonic shift away from fossil fuel based power plants. Solar photovoltaics (PV) have become a major player among renewable energy sources in terms of its global installed capacity. The installed capacity of solar PV has gone up from a meagre 1.4 GW in 2000 to 139 GW in 2013 [1]. Of the globally installed PV capacity, crystalline (mono crystalline, multi crystalline, ribbon, mono like) silicon PV has been the major contributor, with a market share of approximately 80% [2]. This massive growth in installed capacity of solar PV have been fuelled by advances in cell/module processing technology leading to higher cell/module efficiency, reduction in cost ($<$\$/W) and a slew of government policies. Further with a projected increase in the total installed capacity in the coming years, further reduction in production cost or efficiency enhancements (without significant increase in production cost), would be the driving force of the PV industry. Fig. 1.1 shows the data adapted from the International Technology Roadmap for Photovoltaics (ITRPV), 2014 report [3] shows the various components making up the total cost of a module.

In order to lower the cost of starting silicon material, one of the approaches involve reducing the thickness of the silicon wafer. With reducing thickness of silicon, maximum light needs to be absorbed within the thin silicon bulk to obtain the same short circuit currents. This would necessitate the need for developing alternative technologies for the enhancing the light absorption in c - Si solar cells. Conventional surface texturization processes may no longer be viable, as the process in itself would result in a significant loss of silicon (15 - 30 μm). This further lowers the thickness of bulk silicon wafer, thus necessitating the development of alternative

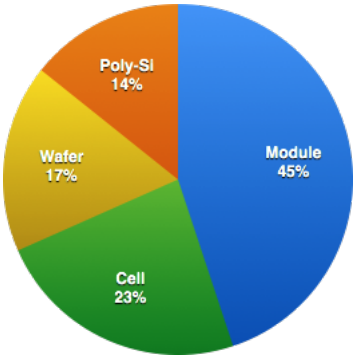


Fig. 1.1: Various components of module cost, data adapted from [3].

schemes for surface texturing, as the industry move towards thinner wafers. Wafer handling during processing is yet another challenge that is foreseen for thinner wafers.

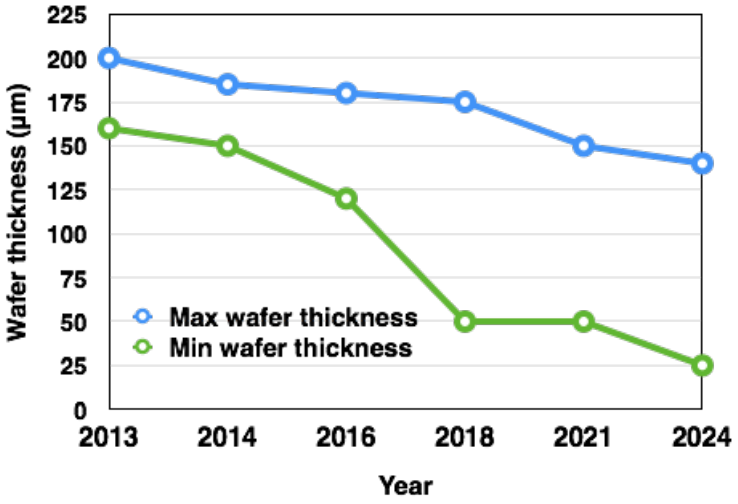


Fig. 1.2: Predicted maximum and minimum wafer thickness in coming years, data adapted from [3].

Silver based contacts used in c - Si solar cells adds significant cost to the solar cell fabrication process. Besides, reducing the amount of silver used in c - Si solar cells, there have been significant effort in replacing Ag contacts using Ni - Cu based electroplated contacts. Recently, a cell efficiency of 20.5% was demonstrated on 6" n-type passivated emitter rear totally diffused (PERT) solar cells, using Ni - Cu - Ag as the front contact [4]. One of the challenges associated with Ni - Cu metallisation is the residual plating in pin holes present in anti-reflective coating (silicon nitride) [5]. Many research groups have reportedly addressed this issue plating by modifying the anti-reflective coating [6]. Thus it maybe concluded, for widespread industrial adaptation of Ni - Cu contacts, specific processes and equipments needs to be developed.

Despite achieving an efficiency of 25.0% on c - Si solar cells based on the passivated emit-

ter locally diffused (PERL) architecture way back in the late 1990's, the current commercially available c - Si cells have efficiency levels hovering around the 20% mark [7]. The cell processing steps used for the PERL cell fabrication involved mulitple photolithography steps, high temperature oxidation and multiple dopant diffusion steps. This makes the processing scheme costly, and hence unviable for industry adoption. Additionally, the high efficiency was shown on small area devices (4 cm^2). At a cell level, the efficiency enhancement and/or cost reduction can be largely brought about by developing novel process alternatives in the areas of junction formation, light trapping, surface passivation, and metallisation. The PERL cell differs from the commercially available c - Si solar cells in the following ways:

1. PERL cell uses an inverted pyramid configuration for light trapping as compared to the random pyramids used in commercial c - Si solar cells. The fabrication of inverted pyramids requires photolithography steps and thin film growth which increases the cost and lowers the throughput in case of commercial c - Si solar cells. The inverted pyramids used in PERL cells are reported to result in better light trapping and results in lower number of defects upon depositing the surface passivation layer [8].

2. For passivation of front and rear surface in case of PERL cells, a thermally grown SiO_2 film of thickness $\sim$105 nm is used [9]. The film also serves as an anti-reflective coating (ARC) on the front surface of the solar cell. Despite the thermally grown oxide being well known for its high quality interface with silicon, the high temperature required for oxide growth makes it commercially non-viable. Low oxidation rates also lower the throughput which is also detrimental for c - Si solar cell industry. Besides, in case of solar cells based on multi-crystalline silicon wafers, high temperature processing can lead to activation of impurities in the bulk, and can degrade the device performance [10]. In case of commercial c - Si solar cells, a 70 nm thick plasma enhanced chemical vapour deposited silicon nitride film is used as the ARC and surface passivation layer on the front surface.

3. Locally diffused regions on both the rear side (p^+ for back surface field formation) as well as under the contact in the emitter region (for n^+ formation, to lower contact resistance) requires photolithography steps, making the process costly. However, recent technological advancements has seen the emergence of selective emitter technology have been developed in conjunction with screen printing [15]. Similarly laser fired contacts have been recently used for making selective contacts at the rear surface of the solar cell

through dielectrics or dielectric stacks (Al_2O_3, Al_2O_3 - SiN_x, SiO_2 - SiN_x) [4].

From the discussion above, it can be seen that some of the processes used in PERL cell fabrication have still not found its way towards the commercial production process. Despite potential benefits in terms of cell performance enhancement, thermal oxidation of silicon and inverted pyramidal texturing of silicon have are yet find its way to commercial production, owing to high cost and throughput issues. More recently, Sunpower has demonstrated 25% efficiency on large area crystalline silicon solar cells. The solar cell based on an all back contact platform is a successor of the Interdigitated back contact (IBC) solar cell [11]. However, the higher cost of production makes these modules expensive. High efficiency device structures like PERL, all back contact solar cells (from Sunpower) serves as guidelines for developing newer processes for industry. Bringing down the cost of production of high efficiency silicon solar cells is indeed an open and challenging problem, involving development of novel processes.

1.1 Thesis motivation

Thermal oxidation of silicon in oxygen ambient at high temperatures is known to result in high quality Si - SiO_2 interface. In high efficiency PERL cells, a 105 nm thick thermally grown silicon dioxide serves as surface passivation layer and anti-reflective coating. However, as previously discussed, the lower oxidation rate, coupled with the higher cost and lower throughput makes this process unviable for silicon solar cell industry. Hence, a 70 nm thick silicon nitride with a refractive index of 2.0 is widely used as the passivation layer and ARC in commercial crystalline silicon solar cells [9]. Low temperature growth of silicon dioxide based on wet chemical oxidation [12], steam based (wet) oxidation [13] is being looked at as potential alternatives for thermally grown dry SiO_2 films in crystalline silicon solar cells. Compared to dry oxidation, wet oxidation can be carried out at lower process temperatures (800 - 1000^{o}C) and has a higher growth rate [13]. Another approach to grow low temperature oxide is by exposing the silicon wafer to an oxidising plasma ambient. Silicon dioxide grown in plasmas were extensively studied as a potential replacement for thermal oxide in metal oxide semiconductor (MOS) devices. It is reported that various oxidising ambients like nitrous oxide, oxygen and these gases in combination with various inert gases like helium (He), argon (Ar), krypton (Kr), xenon (Xe) have been used for growing silicon oxide films [14]. However, the feasibility of using a plasma grown oxide film as a surface passivation layer in silicon solar cells is unknown.

This thesis discusses a process for low temperature growth of silicon oxide/silicon oxy-nitride film in an oxidising plasma ambient at temperatures less than 400^oC. The surface passivation potential of the plasma grown silicon oxy-nitride film is investigated by capping these films with hydrogenated silicon nitride film. The performance of the stack as a surface passivation layer is benchmarked against a low temperature oxidation carried out in a furnace at 600^oC. The process development of this low temperature oxidation step for surface passivation and its integration into crystalline silicon solar fabrication process forms the core part of this thesis.

In pursuit of lowering the cost of production, alternative metallisation schemes like Ni - Cu based front contacts are being extensively investigated. Some of the challenges associated with the integration of Ni - Cu metallisation into c - Si solar cells are Cu diffusion, lower adhesion, background plating and long term reliability [5]. Background plating (residual plating) is the unwanted deposition of Ni - Cu observed on pin holes present in the anti-reflective coating. This residual plating not only degrades the aesthetic value of the cell but also results in significant decrease in fill factor, and cell performance [16]. Mitigating this residual plating requires modification of the silicon nitride film [16]. Another approach to mitigating background plating involved the oxidation of the silicon nitride film [17]. One of the possible methods discussed included exposing the silicon nitride film to an oxidising plasma ambient. However, it is also reported that post deposition plasma treatment would lead to degradation of silicon - silicon nitride interface [18]. In this thesis, a post deposition plasma treatment process is developed to prevent background plating without sacrificing the passivation quality [19].

Random pyramidal texturing used currently in silicon solar cells may not be viable as the industry moves to thinner wafers. The process not only results in significant loss of bulk silicon material but also results in the formation of localised defects in solar cells [8]. Hence, there is a renewed interest in the fabrication of inverted pyramids on silicon, as the wafer thickness is being scaled down. As previously discussed, fabrication of inverted pyramids require expensive lithography process, which has stopped the solar cell industry from adopting it. In this thesis, a novel scheme relying on blisters formed in inductively coupled plasma chemical vapour deposited silicon nitride films is used for fabrication of inverted pyramids in silicon. The texturing process based on blister formation in silicon nitride is commercially attractive as it eliminates the photolithography steps and hence can be implemented in solar cell industry.

1.2 Organisation of the thesis

The thesis discusses three novel plasma based processes with potential application in crystalline silicon solar cell fabrication. Including the introduction, the contents of the thesis are organised into seven chapters. Chapter 2 introduces the concept of surface passivation using the extended Shockley - Read - Hall (SRH) theory, and also discusses the techniques used to determine the surface passivation quality of a dielectric film. This is followed by a literature survey reviewing the surface passivation quality of various dielectrics like silicon nitride, silicon oxide and aluminium oxide. The potential of low temperature chemically grown oxides as potential surface passivation layer is also reviewed in chapter 2, setting the tone for development of alternative low temperature techniques for growing oxides on silicon. Chapter 3 reviews the conventional surface texturing processes as well as some of the alternative processes used for surface texturing of silicon surfaces, thereby establishing the need for development of alternative processes for fabrication of inverted pyramids in silicon. Chapter 4 reviews some of the techniques used for characterisation of the samples prepared as part of the thesis.

Following a detailed literature review on plasma oxidation of silicon for various applications, Chapter 5 discusses the potential of a plasma grown silicon oxy-nitride film for surface passivation of silicon surfaces. The impact of various plasma ambient on the surface passivation quality is also discussed. The surface passivation of a stack of plasma grown silicon oxy-nitride is investigated after capping the film using a silicon nitride film. Impact of ammonia addition on the plasma oxidation process also forms part of chapter 5. Chapter 6 discusses the integration of plasma oxidation process into the c - Si solar cell fabrication flow. The impact of interstitial oxygen trapped in silicon during plasma oxidation on effective lifetime and solar cell performance is investigated. The benchmarking of the plasma oxidation process against a low temperature thermally grown oxide film is also discussed. Following a loss analysis of the solar cells, the chapter proposes a roadmap for further improvement in solar cell performance. The chapter also discusses the potential causes behind the shunts observed in the solar cells reported in this thesis.

Chapter 7, discusses the impact of an inert gas/N_2O plasma treatment on the surface passivation quality of PECVD silicon nitride film. The process, known to result in a decrease in residual plating in case of Ni - Cu metallisation, was seen to result in a significant enhancement in minority carrier lifetime. The chapter discusses in detail, the cause of the enhancement in

lifetime, as well as the thermal stability of the lifetime enhancement. The chapter concludes with a discussion on the potential of the proposed plasma treatment process for front/rear side passivation of silicon solar cells.

Chapter 8 discusses the fabrication of inverted pyramids in silicon through blisters in silicon nitride. The chapter investigates the fundamental mechanism behind the formation of blisters in silicon nitride and its dependence on process conditions. Subsequent to this discussion, a process for fabrication of micrometer scale inverted pyramids in silicon through blisters in silicon nitride is introduced. The impact of blister coverage, blister size, and the nature of the blister on the inverted pyramid formation is also discussed. The chapter concludes with a short discussion on two schemes which maybe used for the fabrication of inverted pyramids of sub micron dimensions in silicon.

Chapter 9, summarises the thesis, and provides a roadmap for future research work in relation to the processes listed in the previous chapters.

Chapter 2

Surface passivation in crystalline silicon solar cells

For any device to work efficiently as a solar cell, the device needs to perform three functions effectively: light trapping, carrier generation, carrier separation, and carrier collection. The various components present in a solar cell devices perform one or more of these functions. For example: The anti-reflective coating present in a silicon solar cell not only serves to minimise reflection, thereby improving the generation within the silicon, but also works as a surface passivation layer ensuring that the carriers generated on the front surface of the device are not lost to surface recombination. Efficient carrier generation, separation and collection would imply minimising the losses at various stages in a silicon solar cell. The losses in a solar cell device can be broadly categorised as optical and electrical losses. The electrical losses in solar cells combines the recombination losses as well as the resistive losses. The discussion on losses in solar cells in this section is restricted to crystalline silicon solar cells.

Optical losses in silicon solar cells are predominantly due to reflection of light from the silicon surface and shadowing as a result of the contact grid. In order to lower the reflection from the surface of a silicon solar cell, the surface of the wafer is textured by etching the wafer in anisotropic etchants like KOH/NaOH. The anisotropic etching results in the formation of sharp pryamidal structures on silicon which randomises the light falling on the surface, thereby lowering the reflection. In order to further lower the optical loss, an anti-reflective coating is used on the silicon surface. Silicon nitride is the anti-reflective coating currently used in silicon solar cells. By tailoring the thickness and refractive index (RI), the minima of reflectance can be tuned. Details on the choice of anti-reflective coating is discussed in an upcoming section. Metal

contacts used on silicon solar cells result in significant shadowing preventing light from entering the regions directly under the contact. However, lowering the number of fingers on a solar cell can lead to significant increase in ohmic losses. Therefore, the optimal number of fingers and bus bars in a solar cell is an optimisation between contact resistance and shading losses. Cell architectures based on all back contacts like the IBC, back contact - back junction eliminate the shading losses from the front contact grid used in more conventional cell architectures [2].

Recombination of carriers can take place in the emitter, bulk and surface regions of a solar cell. The recombination in the bulk of the silicon wafer is mainly due to the presence of bulk impurities (e.g.: Fe) in silicon [20]. The phosphorus diffusion process used for emitter formation in silicon can result in gettering of impurities, thus improving the bulk lifetime of the wafer. In case of poly or multi crystalline silicon, grain boundaries unless well passivated can serve as recombination centres as well. Major component of recombination in the emitter of a solar cell is dominated by Auger recombination. Higher the doping of the emitter, higher is the recombination in the emitter region. A heavily doped emitter can also lead to free carrier absorption which can decrease the generation within a solar cell. The surface of a silicon wafer is usually composed of a large number of silicon dangling bonds. The dangling bonds on the surface of a silicon wafer can act as recombination centres. Solar cell being a large area device has a large area of exposed silicon on both the front and rear surfaces of the solar cell. In commercial, silicon solar cells, the issue of surface recombination on the front surface is mitigated by coating it with a hydrogenated silicon nitride. On the rear side of the solar cell, an Al - back surface field is used to repel away the electrons arriving at the rear contact, thus passivating the rear surface. Additionally, recombination can also occur at the metal - silicon interface. In case of PERL cells [9], the contacts are formed over a thin tunnelling SiO_2 layer, which lowers the recombination under the contact.

This chapter begins with a short description of recombination mechanisms in semiconductors followed by a detailed introduction into the basic concepts of surface recombination and effective lifetime. This is followed by a short review of some of the passivation layers used in screen printed solar cells and high efficiency silicon solar cells. A short discussion on wet chemical oxidation of silicon is also included in this chapter. The chapter also includes a detailed review on oxidation of silicon in plasma ambient, setting the background for the various experiments discussed in this thesis.

2.1 Carrier recombination in semiconductors

Generation of excess carriers in a semiconductor as a result of light absorption or by other methods, results in disturbing the thermal equilibrium of the semiconductor. Recombination is the inverse process by which the carriers generated within a semiconductor are lost. The loss of carriers result in the release of energy either as phonons (lattice vibrations) or as photons. In thermal equilibrium, the generation and recombination rates are identical. In semiconductors, there are three main types of recombination mechanisms available namely, (i) radiative recombination, (ii) Auger recombination and (iii) Shockley - Read - Hall recombination. These are described below.

2.1.1 Radiative recombination

Radiative recombination, also known as direct recombination is a dominant recombination mechanism in case of direct band gap semiconductors. Direct recombination is a process wherein the electron in the conduction band of the semiconductor falls back into the valence band, and recombines with a hole. The energy released as a result of the recombination process, is typically emitted as a photon, whose energy will be equal to that of the band gap of the semiconductor. Since, the process involves two carriers, the recombination rate is proportional to the concentration of electrons and holes in the system. This gives rise to the equation for recombination rate as [21]:

$$U_{rad} = B(np - n_i^2) \tag{2.1}$$

where n and p represents the non equilibrium electron and hole densities (in cm^{-3}), while n_i represent the intrinsic carrier density in the semiconductor (in cm^{-3}). The constant B represents the probability of a direct band to band transition in the semiconductor (in cm^3/s). The constant B, would have a higher value for direct band gap semiconductors, while the value would be lower for indirect band gap semiconductors. For Si, the value of B = 1.1 x 10^{-14} cm^3/s [22]. In indirect band gap semiconductors like silicon, conservation of momentum and energy implies that a transition to valence band maximum would involve a phonon and a photon. The involvement of a phonon makes the probability of occurrence of this event much lower in an indirect band gap semiconductor. The radiative recombination lifetime, τ_{rad}, is given by the equation,

$$\tau_{rad} = \frac{1}{B(n_0 + p_0 + \Delta n)} \tag{2.2}$$

In case of low level injection, i.e. $\Delta n << n_0 + p_0$, Eqn. 2.2 transforms to:

$$\tau_{rad} = \frac{1}{B(n_0 + p_0)} \tag{2.3}$$

where as in case of high level injection, $\Delta n >> n_0 + p_0$, Eqn. 2.2 transforms to

$$\tau_{rad} = \frac{1}{B\Delta n} \tag{2.4}$$

2.1.2 Auger recombination

Auger recombination, also known as a three particle recombination, involves three particles during the recombination process. In this process, as an electron falls back into the valence band from the conduction band, the excess energy emitted is used to excite an electron in the conduction band to a higher energy level. This electron, then loses its energy as lattice vibrations and returns to its ground state. This Auger recombination mechanism is termed as *eeh* process. Auger recombination process can also involve two holes and an electron and is then called as the *ehh* process. The net recombination rate can be represented as [21]:

$$U_{Auger} = C_n(n^2 p - n_0^2 p^0) + C_p(np^2 - n_0 p_0^2) \tag{2.5}$$

where, C_n and C_p represent the Auger coefficients for *eeh* and *ehh* processes respectively (in cm^6/s). For Si, C_n is 1.1 x 10^{-30} cm^6/s and C_p is 0.3 x 10^{-30} cm^6/s at 300 K [22]. n and p are non equilibrium electron and hole concentrations respectively (in cm^{-3}), while n_0 and p_0 are equilibrium electron and hole concentrations respectively(in cm^{-3}). In case of low level injection, $\Delta n << n_0 + p_0$, simplification of Eqn. 2.5 results in

$$\tau_{Aug}(n,p) = \frac{1}{C_{n,p} N_{D,A}^2} \tag{2.6}$$

where, N represents the doping density of the semiconductor, with the subscripts D and A representing n-type and p-type semiconductors respectively. In case of high injection conditions, $\Delta n >> n_0 + p_0$, Eqn. 2.5 simplifies to

$$\tau_{Aug}(n,p) = \frac{1}{(C_n + C_p)\Delta n^2} \tag{2.7}$$

Comparing Eqn. 2.2 and Eqn. 2.5, it can be seen that the Auger recombination process has a strong dependence on the excess carrier density at high level injection than radiative recombination. This higher recombination rate for high level injection makes this process one of the dominant recombination processes in case of heavily doped surfaces.

2.1.3 Shockley - Read - Hall (SRH) recombination

Recombination of carriers through defect level in silicon is termed as Shockley - Read - Hall (SRH) recombination. The defect levels in the semiconductor can include metallic impurities and crystallographic defects. The defect can act as a recombination center, if it captures an electron from the conduction band (CB) and a hole from valence band (VB) resulting in the annihilation of the electron hole pair (EHP). It can also act as a transition level, where an electron from CB is captured before it is released to the VB, resulting in recombination with a hole in the VB. The single level trap recombination rate U_{SRH}, derived from SRH formalism can be written as [23]:

$$U_{SRH} = v_{th} N_T \frac{pn - n_i^2}{\frac{n+n_1}{\sigma_p} + \frac{p+p_1}{\sigma_n}} \tag{2.8}$$

where, $n_1 = n_i e^{\frac{E_t - E_i}{kT}}$, $p_1 = n_i e^{\frac{E_i - E_t}{kT}}$, N_T is the concentration of the trap centres (per cm^{-3}), σ_n and σ_p represent the capture cross section for electrons and holes respectively (expressed in cm^2), v_{th} is the thermal velocity (in cm/s), E_i represents the intrinsic level and E_t represents the trap energy level (in eV), and T is the temperature in ^oK.

2.1.4 Surface recombination in semiconductors

Surface of a semiconductor material represent an abrupt termination of the crystalline structure. This abrupt termination of the crystal structure results in a large density of dangling bonds at the silicon surface. Surface recombination is an extension of SRH recombination model, wherein a large number of traps are present at the surface of the semiconductor. The dangling bonds lead to trap states in the energy band diagram of the semiconductor at the surface. For the case of a continuum of traps, the SRH equation needs to be modified to include the large density of trap states. The number of traps centre represented as N_T in Eqn. 2.8 changes to $dN_T = D_{it}(E_T)dE_T$,

and is substituted in Eqn. 2.8, and integrated across the bandgap.

$$U_s = (p_s n_s - n_i^2) v_{th} \int_{E_v}^{E^c} \frac{D_{it}(E_T) dE_T}{\frac{n_s+n_1}{\sigma_p} + \frac{p_s+p_1}{\sigma_n}} \tag{2.9}$$

where $n_1 = n_i e^{\frac{E_t - E_i}{kT}}$, $p_1 = n_i e^{\frac{E_i - E_t}{kT}}$, D_{it} is the interface trap density (in cm^{-2} eV^{-1}), σ_n and σ_p represent the capture cross section for electrons and holes respectively (expressed in cm^2), v_{th} is the thermal velocity (in cm/s), E_i represents the intrinsic level and E_t represents the trap energy level (in eV), and T is the temperature in ^oK. Eqn. 2.9 assumes that the trap levels are non interacting, and the capture cross section is independent of the occupancy level of the trap. The following inferences can be made from Eqn. 2.9 regarding the surface recombination rate, U_s.

1. U_s can be lowered by reducing the number of interface trap states, i.e. by lowering the interface state density. This forms the basis of *chemical passivation*, wherein the dangling bonds at the interface are terminated by hydrogen or by growing a thermal oxide, as shown in Fig. 2.1(a). Another method of chemically passivating the silicon surface is by using an iodine - ethanol solution or quinhydrone methanol solution to passivate the silicon wafer [24].

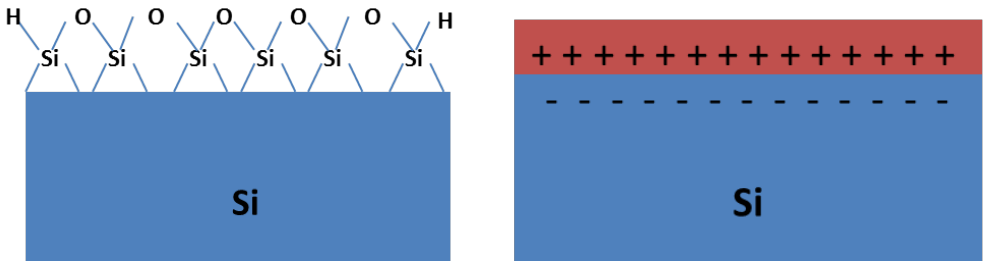
2. Lowering p_s or n_s, the surface hole or electron concentration densities can bring down the surface recombination rate, U_s. This forms the basis of *field effect passivation* and can achieved in the following ways: (a) using a doping profile to create a field to repel the minority carriers away from the interface, (b) using the charge in the dielectric at interface to repel the minority carriers away from the interface, as shown in Fig. 2.1(b), and (c) applying an external voltage to repel the minority carriers away from the interface.

2.1.5 Effective lifetime and surface recombination velocity

Eqn. 2.9 represents the surface recombination flux at the surface of a material or at the interface. The equation can be rewritten as:

$$U_s = \frac{pn - n_i^2}{\frac{n+n_1}{S_p} + \frac{p+p_1}{S_n}} \tag{2.10}$$

where $S_n = \sigma_n N_{it} v_{th}$ and $S_p = \sigma_p N_{it} v_{th}$, where N_{it} represents the trap density at the surface in cm^{-2}. S_n, S_p are the surface recombination velocity for electrons and holes respectively.



(a) (b)

Fig. 2.1: Schematic representation of two surface passivation mechanisms (a) Chemical passivation (b) Field effect passivation

Being a surface phenomenon, the unit of surface recombination in $cm^{-2}s^{-1}$, unlike $cm^{-3}s^{-1}$ for the bulk recombination rate shown in Eqn. 2.8. Hence a new quantity, surface recombination velocity (SRV) defined by the relation, $S = U_s/\Delta n$ is introduce to represent the flux of the carriers towards the surface of the semiconductor. Lower the flux of minority carriers towards the interface, lesser is the recombination, and hence lesser the value of surface recombination velocity. The maximum value of surface recombination velocity cannot exceed the thermal velocity (10^7 cm/s) at room temperature. For the best quality interfaces, SRV should be as low as possible. SRV is measured from the lifetime measured in a lifetime tester using the following equation.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S_{front}}{W} + \frac{S_{rear}}{W} \tag{2.11}$$

τ_{eff} is the effective lifetime, τ_{bulk} is the bulk lifetime, S_{front}, S_{rear} is the surface recombination velocity (in cm/s) at the front and back side of the wafer, and W is the thickness of the wafer (in cm). This equation is used through out this thesis to measure the surface recombination velocity. The bulk lifetime (τ_{bulk}) of the wafer comprises of the following components, τ_{rad}, τ_{Aug}, τ_{SRH}. It is given by the relation

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}} \tag{2.12}$$

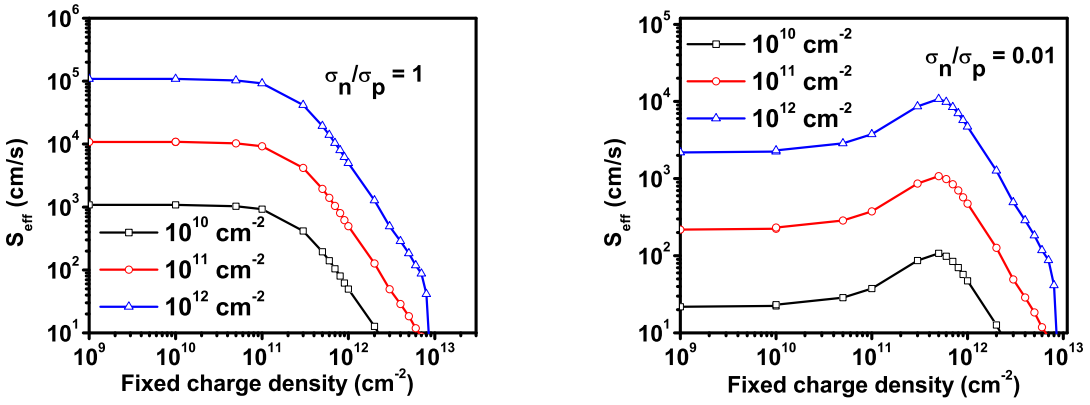
If the same passivation layer is used on both sides of the silicon wafer, then Eqn. 2.11 can be rewritten as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W} \tag{2.13}$$

In order to minimize the impact of τ_{bulk} on the measured τ_{eff}, typically float zone (FZ) wafers with high lifetimes are used for the measurement.

2.1.6 Simulation of surface passivation

The influence of chemical and field effect passivation on the effective surface recombination velocity was simulated using the methodology described by Dingemans et al. [10]. The excess carrier density at steady state was calculated for a specific wavelength and a specific fixed charge density using PC1D. PC1D is solves the poisson and continuity equations to simulate one dimensional carrier transport in semiconductors. The tool has been widely used for simulating and modelling silicon solar cells. In the simulation discussed in this section, a n-type wafer with resistivity of 2 Ω cm and bulk lifetime of 1 ms was chosen as the starting material. A steady illumination at 300 nm, with an intensity of 0.1 W/cm^2 was used to simulate the generation of carriers. Positive fixed charges were applied to the top surface of the wafer and the corresponding excess carrier densities were calculated using PC1D. For the excess carrier densities (n_s, p_s) obtained, the net surface recombination rate (U_s) was calculated by solving the SRH equation with interface trap density (N_{it} in cm^{-2}) and capture cross sections as additional inputs. S_{eff} was calculated at an injection level of 10^{15} cm^{-3}. The methodology used for computation as well as the MATLAB code used for computing the S_{eff} is included in Appendix A. The impact of the interface parameters, N_{it} (governing chemical passivation) and Q_{ox} (governing field effect passivation) on the surface recombination velocity (S_{eff}) is shown in Fig. 2.2.



(a) (b)

Fig. 2.2: Impact of N_{it} and positive Q_f on S_{eff} for two different capture cross section ratios (a) $\sigma_n/\sigma_p = 1$ (b) $\sigma_n/\sigma_p = 0.01$ on n - type wafer with τ_{bulk} = 1ms.

For the simulation with $\sigma_n/\sigma_p = 1$, it can be seen that the effect of field effect passivation starts to become evident for $Q_f > 10^{11}$ cm^{-2}. It can also been seen that S_{eff} (chemical pas-

sivation) has a strong dependency on N_{it}. The dependency of S_{eff} on the electron and hole capture cross sections is also shown in Fig. 2.2(b). For the ratio of σ_n/σ_p = 0.01, maximum value of S_{eff} is observed close to Q_f ~8x10^{11} cm^{-2}. This corresponds to a point of maximum recombination where the ratio of excess carrier density (p_s/n_s) is approximately equal to σ_n/σ_p [25]. The capture cross section of electrons and holes are dependent on the processing conditions as well as the type of dielectric used for the passivation. The plots shown in Fig. 2.2 gives a qualitative understanding on the impact of various interface parameters like Q_f, D_{it}, σ_n and σ_p on the surface recombination velocity. Additionally, Fig. 2.3 shows the impact of field

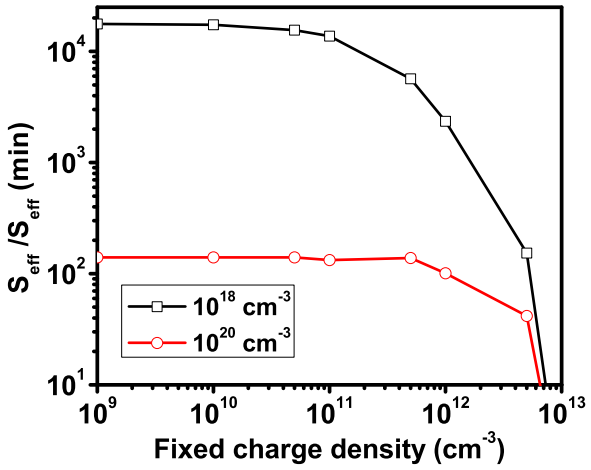


Fig. 2.3: S_{eff} normalised with S_{eff} (min) for two different doping densities. N_{it} of 10^{10} cm^{-2} and σ_n/σ_p = 1 was assumed for this simulation.

effect passivation on wafers with two different doping densities of 10^{18} cm^{-3} and 10^{20} cm^{-3}. Simulated S_{eff} is normalised to the minimum S_{eff} (S_{eff} (min)). It can be seen that an increase in positive Q_f (higher field effect passivation) is seen to have a minimal impact on a wafer with higher doping density than a wafer with lower doping density. N_{it} of 10^{10} cm^{-2} was assumed for these simulations, and σ_n/σ_p = 1 was maintained. It was also observed from simulations that the impact of N_{it} on S_{eff}/S_{eff} (min) did not have any bearing on the doping density of the wafer. Thus it maybe concluded that in case of heavily doped surfaces like that of the n^+ emitter in c - Si solar cells, the interface state density may play a major role in determining the net S_{eff} than the positive fixed charge density. The result shown in Fig. 2.3 agrees qualitatively with what was previously reported by Glunz et al. [27].

2.1.7 Photo conductance decay measurements

The fundamental principle behind the measurement of effective carrier lifetime is outlined in this section. Uniform illumination of a block of silicon will result in the generation of excess carriers in silicon. As the source of light is switched OFF, the carriers decay over time. Measuring the decay rate of the excess carriers in the block of silicon will give an estimate of the carrier lifetime [22]. A higher recombination rate results in faster decay of generated carriers , thereby resulting in lower the carrier lifetimes. The dynamics of this recombination process can be mathematically modelled using the continuity equation:

$$\frac{\delta \Delta n}{\delta t} = G(t,x) - U(t,x) + \frac{1}{q}\frac{\delta J_n}{\delta x} \tag{2.14}$$

where G and U are the generation and recombination rates respectively (in cm^{-3}) in the block of silicon under investigation, and Δn is the excess carrier density in cm^{-3}. J_n is the electron current due to spatial variation in generation rate. Spatially uniform generation would imply that the third term on the right hand side of Eqn. 2.14 will become zero. Uniform generation in the bulk of the silicon wafer is ensured by illuminating the sample with an IR source. Substituting U = Δn/τ_{bulk}, and replacing $\tau_{bulk} = \tau_{eff}$, Eqn. 2.14 modifies to

$$\tau_{eff} = \frac{\Delta n}{G - \frac{\delta \Delta n}{\delta t}} \tag{2.15}$$

which is the generalized expression for measurement of carrier lifetime. In case of transient measurements, a light pulse is rapidly turned off, following which the decay of excess carriers take place. This would imply, G = 0, and Eqn. 2.15 is modified to yield the relation for lifetime measurement in transient mode.

$$\tau_{eff}(tr) = \frac{\Delta n}{\frac{\delta \Delta n}{\delta t}} \tag{2.16}$$

The transient mode is typically used for measuring higher lifetime samples. In steady state (quasi steady state) mode, $\delta\Delta$n/δt = 0, and Eqn. 2.15 is modified to yield the lifetime.

$$\tau_{eff}(qss) = \frac{\Delta n}{G} \tag{2.17}$$

As seen from Eqns. 2.16, 2.17, the effective lifetime in a semiconductor can be computed by finding the time dependent variation of excess carrier density and generation rate. The variation

in the carrier density with time is measured using a photo conductance decay measurement system [26]. The system consists of a tuned RF bridge, which is detuned as the conductivity of the sample changes with illumination. The change in conductivity ($\Delta\sigma$) brought about by the excess carrier generation is given by the relation:

$$\Delta\sigma = q(\mu_n + \mu_p)\Delta nW \tag{2.18}$$

where μ_n, μ_p are the electron and hole mobilities in the semiconductor, W is the width of the sample and q is the electronic charge. A calibrated reference solar cell is used to estimate the time dependent illumination intensity, which is used to compute the generation rate using the equation [26]

$$J_{ph} = \frac{q\Delta nW}{\tau_{eff}} \tag{2.19}$$

where J_{ph} is the photo generated current for a given irradiation. Combining Eqn. 2.18, 2.19, effective lifetime can be computed using the relation,

$$\tau_{eff} = \frac{\Delta\sigma}{J_{ph}(\mu_n + \mu_p)} \tag{2.20}$$

2.2 Surface passivation layers in silicon solar cells

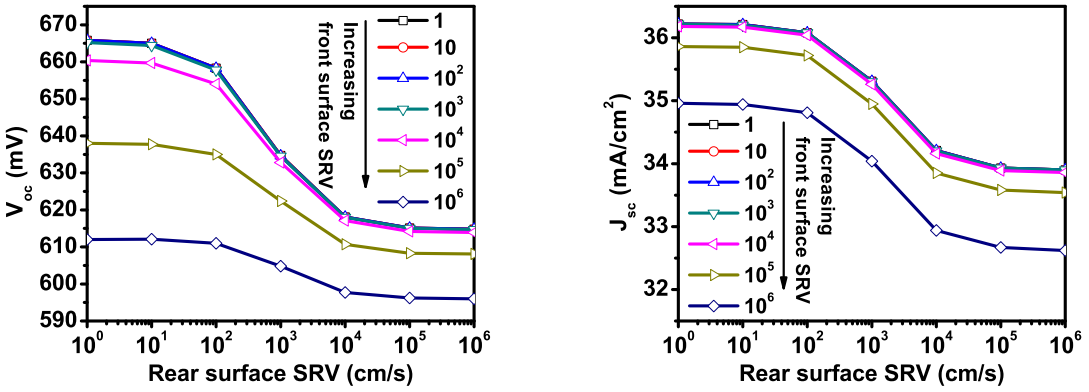
The impact of surface passivation on the performance of a c - Si solar cell is discussed in this section through simulations. A solar cell with an efficiency in excess of 20% was simulated using PC1D. The parameters used for the simulation of the solar cell are listed in Table 2.1. The impact of front and rear surface recombination velocity on the performance of the simulated solar cell parameters was studied by varying the front and rear surface SRV.

The results of the simulation are summarised in Fig. 2.4. The open circuit voltage (V_{oc}) is shown to degrade significantly for front surface SRV's greater than 10^4 cm/s as shown in Fig. 2.4(a). The emitter doping on the front surface makes it more tolerant to the variation in front surface recombination velocity [27]. However, for a given front surface SRV, V_{oc} degrades significantly as the rear surface SRV increases from 10 to 100 cm/s. Thus from the simulated results, it maybe concluded that the front surface of the silicon solar cell is more tolerant to SRV variations, while a poor passivation of the rear surface can degrade the solar cell performance significantly. As the front surface SRV increases from 1 cm/s to 10^6 cm/s, the V_{oc} is seen come

Table 2.1: Parameters used for simulating a p-type Si solar cell with efficiency $> 20\%$

Parameter	Value
Wafer thickness	180 μm
Front surface texture	5 μm
Anti-reflective coating	75 nm, RI - 2.0
Emitter contact resistance	1 mΩ
Base contact resistance	1 mΩ
Shunt resistance	∞
P - type substrate doping	1.513x10^{16} cm^{-3}
Emitter doping	1.843x10^{20} cm^{-3}
Junction depth	0.316 μm
Bulk lifetime	1 ms
Front SRV	1 - 10^6 cm/s (varied)
Rear SRV	1 - 10^6 cm/s (varied)

down by almost 55 mV (at a rear surface SRV of 100 cm/s). Fig. 2.4(b) shows the variation in short circuit current density (J_{sc}) with the front and rear surface SRVs. J_{sc} is seen to have a weak dependency on the front and rear surface SRV's. As the front surface SRV increases from 1 cm/s to 10^6 cm/s, the J_{osc} is seen come down by 1.4 mA/cm^2 (at a rear surface SRV of 100 cm/s). In this context, it maybe concluded that estimating the V_{oc} of a solar cell can give a fair understanding of the passivation quality of a dielectric film applied on the front or rear surface of a solar cell.



(a) (b)

Fig. 2.4: PC1D simulation results showing the impact of front and rear surface recombination velocities (a) open circuit voltage (b) short circuit current density. The impact of surface recombination velocity (front and rear) is seen to be more dramatic on the open circuit voltage than on short circuit current density.

Passivating a silicon surface can be carried out using both organic and inorganic methods.

Some of the commonly used organic compounds for passivating the silicon surfaces are Quinhydrone methanol (QM) and iodine ethanol (IE). The dominating passivation mechanism in these solutions is the chemical passivation wherein the dangling bonds are passivated by the various components present in the respective solution. In case of IE and QM solutions, the silicon dangling bonds are passivated by - O - CH_2 - CH_3 and - O - CH_3 groups respectively [28, 29]. More recently, there have been reports suggesting that the surface passivation brought about by QM solution also includes a component of molecular field effect passivation [24]. Inspite of the very low SRV values yielded by organic compound based surface passivation, these schemes are not implemented in solar cells. However, these organic solutions are typically used for measuring the bulk lifetime of the wafers used for the solar cell processing. Hydrofluoric acid is another solution used for passivating the silicon surface. In case of HF based passivation, the dangling bonds are reportedly passivated by hydrogen [28].

In case of crystalline silicon solar cells, inorganic thin films like silicon nitride, silicon oxide and Al_2O_3 are widely used for surface passivation of front and rear surface of the solar cells. Silicon nitride films with positive charges are well suited for passivating n-type silicon surfaces, and is widely used for passivation of n-type emitters in silicon solar cells. Besides electrically passivating a surface, a passivation layer when implemented on a solar cell should also have long term stability and should be robust to long term exposure to light. Passivation schemes based on silicon nitride films have been reported to exhibit excellent long term stability as well as UV stability [30, 31] and has hence been one of the widely used dielectric for emitter surface passivation in c - Si solar cells. Besides, it also serves as an antireflective coating in c - Si solar cells. However, using silicon nitride films to passivate the rear surface of a p-type passivated emitter and rear contacts (PERC) solar cell can result in parasitic shunting [32] and is one of the reason why alternative dielectrics like Al_2O_3 are looked at, for passivating rear surface in p-type c - Si solar cells.

Al_2O_3 with negative charges is suitable for passivating p-type silicon surfaces. For example, p-type base in conventional cell front n^+ emitter architecture on p-type wafers, or p-type emitter on n-type wafers. Al_2O_3 films have exhibited long term stability as well as UV stability making it an ideal candidate for implementation in silicon solar cells [33]. In this section, some of the commonly used surface passivation layers in both commercial as well as high efficiency solar cells based on PERC, PERT, and PERL architectures are reviewed.

2.2.1 Screen printed silicon solar cells

The discussion included in this section covers some of the surface passivation approaches used in screen printed crystalline silicon solar cells where the front and rear contacts are screen printed and co-fired. The solar cell comprises of a p-type substrate with a heavily doped n^+ emitter surface on the front surface. Silicon nitride is deposited on the front surface which serves as a surface passivation and anti-reflective coating. Screen printed Ag and Al are used as the front and rear surface contacts, which is co-fired in a rapid thermal annealing furnace to make contact to silicon. The rear surface is completely covered with screen printed Aluminium, which diffuses into silicon during co-firing. The diffused Al form a p+ doped silicon layer and the p^+-Si - p-Si junction produces a back surface field (BSF). The Al - BSF serves as the rear passivation layer in case of most of the commercially available screen printed solar cells. Table. 2.2 lists some of the reported surface passivation layers used in large area solar cells with screen printed contacts on the front and rear surfaces.

Table 2.2: Summary of surface passivation layers used in screen printed solar cells.

Substrate	Front surface	Rear surface
P	SiN	Al - BSF
P[34]	SiN	a - Si
P[35]	Wet chemical oxide - SiN	Al - BSF
P[36]	Thermal SiO_2 - SiN	Al - BSF
P[37]	Rapid thermal oxide (SiO_2) - SiN	Al - BSF
N[38]	Thermal SiO_2 - SiN	Thermal SiO_2 - SiN, n^+ BSF
N[39]	Thermal SiO_2 - SiN, n^+ FSF	p^+ Al
N[40]	SiN	p^+ Al
N[35]	Wet chemical oxide - SiN	Wet chemical oxide - SiN

One of most commonly used front surface passivation layer is silicon nitride film. A film of 75 nm thickness, and refractive index of 2.0 is typically used as the anti - reflective coating and surface passivation layer. Stacks of silicon oxide/silicon nitride have also been used for surface passivation applications, wherein, the thin layer of silicon oxide have been grown using conventional furnace oxidation or using rapid thermal oxidation (RTO). Low temperature oxidation processes involving nitric acid, referred to as wet chemical oxide in Table. 2.2, are also reported to result in an improvement in solar cell surface passivation. These low temperature grown oxides are seen as alternatives to the furnace grown or RTO grown silicon oxide films. One such approach to growing silicon oxide films is by exposing a silicon wafer to an oxidising

plasma ambient. The proposed process and its feasibility for application in silicon solar cells is discussed in great detail in chapter 5 and 6 of this thesis.

2.2.2 High efficiency solar cell architectures

High efficiency solar cell architectures discussed in this section include the PERL, PERC and PERT solar cells. In case of PERL and PERC solar cells, the rear contact is locally diffused at certain regions using photo lithography [41] or laser firing [45]. In case of PERT solar cells, the rear surface is totally diffused, and a passivation layer is used all over the rear surface. Table 2.3 summarises some of the dielectric layers used for surface passivation in these high efficiency solar cells.

Table 2.3: Surface passivation layers used in high efficiency solar cell architectures.

Cell architecture	Front surface	Rear surface
p - PERL[41]	Thermal SiO_2	Thermal SiO_2
p - PERL[4]	Thermal SiO_2 - SiN	Thermal SiO_2 - PECVD SiO_x - SiN
p - PERC[42],[67]	SiN	Thermal SiO_2 (wet)
p - PERC[43]	Thermal SiO_2	PECVD a-Si - SiO_x
p - PERC[44]	SiN	Double layer SiN
p - PERC[45]	Bilayer SiN	ALD Al_2O_3 - PECVD SiN
p - PERC[46]	Thermal SiO_2 - SiN	Thermal SiO_2 - AlO_x - SiN
p - PERC[47]	SiN	Al_2O_3 - SiN
n- PERT[4]	Thermal SiO_2 - SiN	Thermal SiO_2 - PECVD SiO_x - SiN
n- PERT[48]	Thermal SiO_2 - SiN	Thermal SiO_2 - SiN

The list shown in Table 2.3 though not exhaustive, is representative of some of the commonly used dielectrics for surface passivation of high efficiency silicon solar cells. One of the commonly used dielectric layer for surface passivation in high efficiency silicon solar cells is the thermally grown silicon oxide film. The film has been used independently or in tandem with other dielectrics for front surface as well as rear surface passivation, once again reiterating the need for developing silicon oxide films at low temperatures. Stacks of Al_2O_3 - SiN films have also been seen to be widely used for rear surface passivation in PERC solar cells. Al_2O_3 deposited by ALD (thermal and plasma) [45], reactive sputter deposition [49] and spray coating [50] have been investigated for potential rear surface passivation. Field effect passivation is found to be one of the dominating mechanism in case of Al_2O_3 based surface passivation. However, very low interface state density ($<10^{11}$ $eV^{-1}cm^{-2}$) have been reported for Al_2O_3 films

deposited by atomic layer deposition (ALD), making it an ideal candidate for surface passivation of both n and p-type silicon surfaces as well as n^+ and p^+ emitter surfaces [10]. A detailed discussion on Al_2O_3 based surface passivation schemes is beyond the scope of this thesis and has been restricted to only silicon nitride and silicon oxide films as they form the crux of the work discussed in this thesis.

2.3 Silicon nitride films for surface passivation of silicon

Silicon nitride films have been widely used in silicon solar cells as a surface passivation layer and as an anti-reflective coating. The films serves as an excellent passivation layer and is known to be stable over long periods of time and also exhibit excellent UV stability [31]. Typically silicon nitride films with a refractive index (RI) of 2.0 and thickness of 75 nm is used as the passivation layer as well as anti-reflective coating. Silicon nitride is predominantly deposited using a plasma CVD (remote, direct) technique, though there are reports of other techniques like Low Pressure CVD (LPCVD) and Atmospheric Pressure CVD. The low temperature ($<450^oC$) used in case of plasma CVD technique has made it a very popular technique in the PV industry. Plasma deposited silicon nitride films are known to have a large amount of hydrogen present in them. The hydrogen present in the film not only passivates the surface but also passivates bulk defects in case of multi-crystalline silicon wafers. The film properties can be varied by varying the deposition conditions, and thus by tuning the thickness and RI of the silicon nitride film, the reflectance characteristics as well as surface passivation quality of these films can be varied. This section includes a review on the surface passivation properties of plasma CVD and LPCVD based silicon nitride films.

2.3.1 Plasma deposited silicon nitride films

Deposition of silicon nitride in a plasma CVD chamber involves using silane and ammonia as the process gases. There are also some deposition processes, where the ammonia is replaced by nitrogen. The silane gas used for the deposition is usually diluted in nitrogen or inert gas ambient. By varying the ratio of silane to ammonia, the deposition rate, refractive index and carrier lifetime in PECVD silicon nitride films can be varied. This was reported by Kerr et al. who had demonstrated a carrier lifetime of 900 μs for the best recipe on planar 1 Ω cm p - type FZ wafer [51]. Good quality of surface passivation was obtained for silicon nitride films

with refractive index (RI) ranging from 1.9 to 2.1 [51]. The effective lifetime was also seen to strongly depend on the deposition temperature. Surface recombination velocities of 4 cm/s and 20 cm/s was demonstrated by Lauinger et al. for remote plasma (2.45 GHz) CVD deposited silicon nitride films on 1 Ω cm and 0.7 Ω cm planar p - type FZ wafers respectively [52]. SRV was reported to be strongly correlated to the deposition conditions, and stable passivation layers were obtained at a RI of 2.3 [53]. Very recently, Duttagupta et al. have demonstrated very high τ_{eff} of 950 μs for silicon nitride film (RI = 2.05) deposited using an inline PECVD reactor [54]. Following a high temperature firing in a belt furnace, τ_{eff} increased further to 1470 μs on n-type 1 - 2 Ω cm FZ wafers. Silicon rich silicon nitride films (RI = 2.5) exhibited very high τ_{eff} of 2500 μs which degraded to 435 μs after the high temperature firing step.

Higher RI films are reported to result in very high τ_{eff}, but τ_{eff} is seen to degrade significantly following the high temperature firing step at temperatures above 800^{o}C. The degradation in τ_{eff} is attributed to the hydrogen effusion from silicon nitride. The degradation in τ_{eff} is reported to have a correlation to refractive index of the silicon nitride film [55]. To improve the thermal stability and to reduce the parasitic shunting effects seen in conventional silicon nitride films, a bilayer silicon nitride is used. The stack comprises of a silicon rich (RI$\sim$ 3.46 - 4.16) nitride layer at the bottom capped with a nitrogen rich silicon nitride(RI$\sim$ 1.9 - 2.0). The films exhibited an SRV of 12 cm/s and the SRV was found to be stable to the firing process [44]. However, the net refractive index of the stack was 3.6, and hence the parasitic absorption would be higher in these films.

The high quality of surface passivation in silicon nitride is the result of a combination of the positive fixed charge present in the film and the lower interface state density, contributing to the field effect and chemical passivation respectively. The hydrogen present in silicon nitride passivates the dangling bonds at the silicon - silicon nitride interface [56]. The amount of hydrogen trapped in PECVD silicon nitride film varies from 15 - 30% [57]. The hydrogen is trapped in the film during the deposition of the film using silane and ammonia as the reactant gases. The positive charge in silicon nitride is brought about by the presence of K centre, which is a silicon atom back bonded to three nitrogen atoms i.e. $N_3{\equiv}Si.$. The K centres can be neutral, positively charged or negatively charged. The charge can be modulated by varying the refractive index of the film. For films rich in nitrogen, the positive fixed charge density is reported to increase [58]. Lamers et al. had also reported that by using plasma pre-treatment steps, silicon - silicon nitride interface can be modified, and thus the surface passivation quality

of the silicon nitride film can be modulated independent of the bulk properties of the silicon nitride film [58]. Electron energy loss spectroscopy (EELS) on silicon - silicon nitride interface indicated nitrogen trapping within $\sim$1nm of the silicon surface during silicon nitride deposition. This nitrogen trapping was reported to result in significant strain at the silicon - silicon nitride interface, which can have a detrimental impact on the passivation quality [59].

2.3.2 Low pressure CVD silicon nitride films

Low Pressure CVD (LPCVD) silicon nitride films have also been previously investigated for potential application in silicon solar cell technology. These films are known to be very resistant to etch solutions, and are used as a diffusion barriers in silicon CMOS technology. The films exhibited poor surface passivation quality when deposited directly on a bare silicon wafer. The hydrogen content in LPCVD films (2 - 10%) is significantly lower than those for PECVD silicon nitride films (20 - 25%), resulting in its poorer passivation quality [60]. However, when deposited over a thermally grown thin silicon oxide film, these LPCVD silicon nitride films exhibited high effective lifetime [57]. However, these films have not been used in silicon solar cells because of the high deposition temperature and its incompatibility to high temperature contact firing processes. Weber et al. had demonstrated very low surface recombination velocities ($<$ 2 cm/s) for LPCVD films deposited on p-type FZ wafers with a sheet resistance of 100 $\Omega/\square$ [61]. A corona charging method was used to deposit negative charge on the dielectric, which resulted in low SRV.

2.3.3 Impact of post deposition plasma treatments on surface passivation of silicon nitride films

Degradation of surface passivation quality of silicon nitride films have been reported by various others [18, 62]. Bose et al. had exposed a PECVD silicon nitride film to a N2O plasma at 250^{o}C for 20 min. Following N_2O plasma exposure, the interface state density as well as positive fixed charge density was seen to increase for different silicon nitride films investigated in [18]. The increasing defects within the film as a result of plasma damage was suggested as a potential cause for the increase in D_{it}. Similar results was obtained by Wan et al. when a silicon nitride film was exposed to NH_3 plasma at room temperature [62]. A significant increase in SRV was observed upon exposing the films to NH_3 plasma. Longer the duration of plasma exposure,

greater was the extent of degradation in surface passivation quality. The increase in D_{it} was attributed to an incorporation of N - H radicals into the bulk of the SiN film which may have resulted in generation of additional defects. Wan et al. had also demonstrated similar degradation in passivation quality for a-Si films as well [62]. Post deposition treatment of silicon nitride films assumes significance owing to its potential application in case of Ni - Cu based metallisation in silicon solar cells. By treating the film is various oxidising ambients (including plasma), the residual plating of Ni/Cu on silicon nitride films can be minimised. Optimal process development would require a study on the impact of such a post deposition plasma treatment on the surface passivation quality of the respective SiN film. In Chapter 7 of this thesis, one such post deposition plasma treatment process capable of minimising background plating and improving the surface passivation quality is discussed. The results reported in chapter 7 contradicts some of the previously published results [18, 62] and also discusses the potential mechanism behind the improvement in passivation quality.

2.4 Silicon oxide films for surface passivation of silicon

Thermally grown silicon dioxide films are known to form the best quality interface with silicon and has been used as a surface passivation layer in high efficiency silicon solar cells. The process have not been widely adopted by the solar cell industry owing to cost and throughput considerations. In this light, silicon oxide films grown or deposited by other methods have invited a lot of attention from the solar cell community. One of the candidate is silicon oxide films deposited using PECVD. However, stand alone PECVD deposited SiO_x films have not shown good surface passivation quality [43]. Stacks of SiO_x - SiN_x have thus evoked a lot of attention from the PV community and are known to yield high quality of surface passivation. This section reviews some of the stacks of SiO_x - SiN_x films used for surface passivation. The section also reviews some of the available literature on silicon oxide films grown through wet chemical oxidation as well as plasma oxidation.

2.4.1 Stacks of SiO_x - SiN films for surface passivation

Hofmann et al. [43] had reported that PECVD SiO_x cannot effectively passivate silicon surfaces. It was proposed that stack systems based on SiO_x - SiN_x can result in improved surface passivation properties. A minimum SRV of 60 cm/s was measured on p-type 1 Ω cm FZ wafers,

for a stack of PECVD SiO_x - SiN_x after a firing step at 850^{o}C for 3 s. Dingemans et al. [63] had shown surface recombination velocity of 6 cm/s and 11 cm/s for a stack comprising of PECVD SiO_x - SiN_x:H for n-type and p-type FZ wafers after a post deposition anneal at 400^{o}C for 30 mins. The surface passivation quality was found to remain same even after annealing the film at 850^{o}C for 30 secs. Mack et al. had demonstrated an S_{eff} of $\sim$ 8 cm/s on p-type FZ wafers after depositing 90 nm of PECVD SiO_x film on 9 nm of thermally grown SiO_2 [64]. Larianova et al. demonstrated S_{eff} of 2.4 cm/s on 2.5 Ω cm n-type FZ wafer for a stack of thin thermally grown SiO_2 - SiN films. S_{eff} was reported to be strongly correlated to the thickness of the SiO_2 film [65]. Extremely low S_{eff} reported for the stack was at par with what was observed for annealed SiO_2 films [65]. Similar enhancement in lifetime for stacks of thermally grown SiO_2 - SiN have been reported by many other authors [51, 66]. Stacks of SiO_2 - SiN films find extensive application in rear surface passivation of PERC solar cells not only because of the high quality of surface passivation but it also eliminates the parasitic shunting problem associated with silicon nitride films when used on the rear surface [32]. However, as previously discussed, the major bottleneck of using thermally grown SiO_2 films is the high temperature (hence higher cost) used for the growth, and the associated throughput problems owing to the lower oxidation rate.

In order to integrate the thermal oxidation process into solar cell process flow, approaches for lowering the oxidation temperature and improving the oxidation rate is actively investigated. One of the approach involves oxidation in a steam ambient [67, 42]. For silicon oxide film grown in steam ambient at 950^{o}C, Mack et al. have demonstrated S_{eff} of 25 cm/s on p-type 1.25 Ω- cm FZ wafer following a forming gas anneal. S_{eff} for the as grown oxide film was found to be $\sim$ 125 cm/s. The thermally grown SiO_2 film was used to passivate the rear surface of p-type PERC solar cells. The wet oxidation process reported in [42, 67] still uses a high temperature for the processes, but mitigates the problem of low oxidation rate observed for oxidation in dry O_2 ambient.

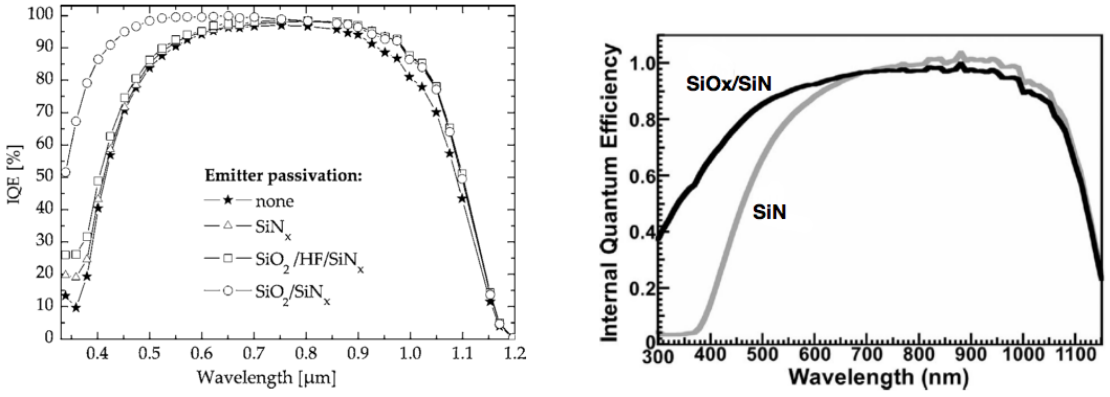
2.4.2 Wet chemical oxidation of silicon

A widely reported low temperature oxidation process is chemical oxidation of silicon in oxidising solutions. Nitric acid has been used for growing thin SiO_2 films on silicon for surface passivation. Grant et al. demonstrated a SRV of 40 cm/s for a 5 nm SiO_2 film grown using nitric acid. However, the desirable passivation levels were obtained only after a high temper-

ature anneal (800^{o}C - 1100^{o}C), thus eliminating any potential advantage in terms of thermal budget [12]. More recently, Anamaria et al. demonstrated that silicon oxide films grown in an O_3 + UV ambient prior to deposition of Al_2O_3 - SiN_x and AlN - SiN_x stacks can result in an improvement in emitter surface passivation quality [68]. Silicon oxide films grown in O_3 + UV ambient was also reported to improve the wettability of silicon surfaces resulting in better uniformity for inline phosphorus diffusion process [69].

Electrochemical oxidation of silicon eliminates the high temperature anneal step and yields SRV of 15 cm/s but is plagued by long oxidation time, and non uniformity [70]. Recently, light induced anodic oxidation is reported to improve the oxidation rate and uniformity of the grown oxide file [71]. The process reported by Cui et al. is used to oxidise p-type surfaces and requires the formation of a n^+ emitter and a thermally grown SiO_2 film at 950^{o}C to protect the n^+ emitter surface during the anodic oxidation process [71].

Chowdhury et al. had investigated the potential of native oxide for surface passivation [72]. They had shown a minimum SRV of 8 cm/s for an oxide thickness of 1 nm, after capping it with a SiN_x:H films. The native oxide growth was carried out for 4 months. However, the very long oxide growth times makes the process less interesting from a commercial point of view. However, there is no comment on the firing stability and long term stability of the stack. A SRV of 18 cm/s is also reported for an oxide grown in nitric acid and capped with SiN_x:H [72].



(a) (b)

Fig. 2.5: (a), (b) IQE for n-type Si solar cells with wet chemical grown SiO_2/PECVD SiN_x films used for emitter surface passivation [73, 74]

Oxidation of silicon in HNO_3 is a self limiting process ($\sim$1.6 nm) and hence can only be used for growing ultra thin silicon oxide films. Hence these wet chemical oxides need to be capped with other dielectrics like silicon nitride, for application as passivation layers in c - Si

solar cells. Stacks of wet chemical grown SiO_2 - PECVD SiN_x films was used for emitter surface passivation of n-type silicon solar cells [73] The films were grown by oxidising the silicon in nitric acid. The V_{oc} was found to improve by 27 mV following the use of wet chemical grown SiO_2 - PECVD SiN_x for emitter surface passivation. The corresponding internal quantum efficiency (IQE) curves are shown in Fig. 2.5(a). A significant improvement in emitter surface passivation can be inferred from the IQE curves. The same was confirmed by means of effective lifetime measurements [73]. More recently, Matsumoto had demonstrated similar improvement in solar cell performance on both n - type and p - type silicon solar cells. A V_{oc} improvement of 10 mV was demonstrated for p-type silicon solar cells [35]. On n-type silicon solar cells, a 4 mA/cm^2 improvement in J_{sc}, and a 3.4 mV improvement in V_{oc} was reported [35, 74]. The corresponding IQE curves for the n-type silicon solar cells are shown in Fig. 2.5(b) [74]. The nitric acid grown SiO_2 film was reported to shield the silicon surface from plasma damage resulting in an improvement in emitter surface passivation [35, 74]. These results clearly demonstrates the potential of stacks of silicon oxide/silicon nitride films for surface passivation applications in silicon solar cells.

2.4.3 Growth of silicon oxide films in plasma ambient

Silicon oxide can be grown by exposing Si wafer to a plasma struck in O_2 ambient [14]. Bright et al. have shown that a two step plasma oxidation/deposition can result in high quality interfaces [75]. A 0.5 nm thick SiO_2 layer was grown by exposing the Si wafer to a He + O_2 plasma for 15 s at a temperature of 200 - 300^oC. They report that this thin oxide layer removes carbon from the surface and prevents nitrogen incorporation at the interface, resulting in D_{it} in the order of $10^{10}eV^{-1}cm^{-2}$ [75]. Sekine et al. has reported radical based oxidation of silicon resulting in high quality oxides [14]. These plasma grown oxides have better interface properties when compared to thermal oxidation. These plasma oxides were grown at 400^oC in an microwave plasma system using Kr + O_2 as the process gas, and MOS transistors were fabricated using the plasma grown oxide [14].

Nitrous oxide plasma have been investigated for growth of plasma oxides. Garduno et al. have reported the growth of oxide using nitrous oxide in a PECVD chamber. It is reported that by using nitrogen as process gas, silicon nitride films can also be grown [76]. Diniz et al. have reported the growth of silicon oxy-nitride films by low energy implantation of NO^+ ions into silicon [77]. A dielectric constant of 5.5 and a positive fixed charge density of $7x10^{10}$

cm^{-2} was obtained, and the authors report the films as a potential candidate for gate oxide applications. However, the interface state density was not reported [77]. It is reported that using N_2O plasma can result in lower ion damage as compared to O_2 based plasma, resulting in improved interface properties. The oxide films grown in nitrous oxide ambient were reported to have lower surface roughness as compared to films grown in oxygen plasma. Additionally, incorporation of nitrogen at the interface is also reported to contribute to lower interface state density [78].

In the sections below, a detailed study of the growth dynamics of plasma oxides in capacitively coupled and inductively coupled plasma systems is reported. Additionally, the role of inert gas in the plasma oxidation process is also looked into. Finally, the application of plasma oxides on MOS devices is also reviewed.

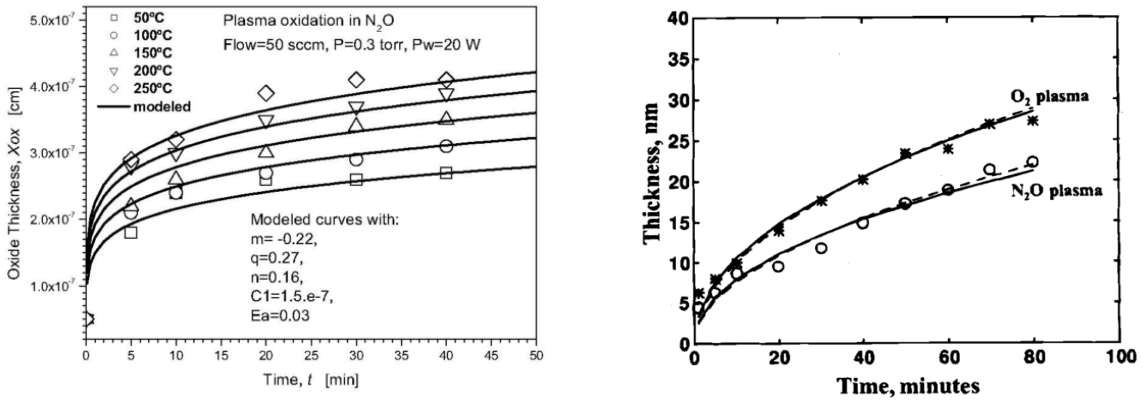
Growth dynamics

The oxidation kinetics in an inductively coupled plasma system using an oxygen plasma was reported by Choi et al. [79]. Si substrate with a chemically grown oxide was used for their studies. The oxide growth process was modelled by a linear parabolic law with a negative linear growth rate constant. However, the initial growth rate is reported as a rapid growth process. The diffusion coefficient of the oxidising species in the growing oxide on the surface is higher when the oxide is thin and lower when the oxide is thick, resulting in a rapid oxide growth during the initial phase. However as the thickness of the oxide increases, the process becomes diffusion limited, similar to the case of thermally grown dry or wet oxides [79]. Activation energy of the linear rate constant was computed as 0.35 eV and parabolic rate constant as 0.37 eV, which is much lesser than those for thermally grown oxides. The growth process is modelled by Eqn. 2.21.

$$\frac{X^2}{k_P} + \frac{X}{k_L} = t + \tau \tag{2.21}$$

where X is the oxide thickness, t is the oxidation time, k_P and k_L are parabolic and linear rate constant respectively, and τ is the time constant. Fig. 2.6(b) shows the growth rate for films grown in ICP [80] and PECVD based plasma system [76].

High density plasma oxidation using O_2 is faster as compared to N_2O based plasma oxidation. This difference in oxidation rate is likely due to decreased electron density and presence of different oxidising species in N_2O plasma compared to the O_2 plasma. Furnace oxidation based



(a) (b)

Fig. 2.6: (a) Modified power law based model for PECVD grown oxides [76] (b) Parabolic growth rate model for oxide films grown in ICP chamber [80].

on N_2O also has lower oxidation rate as the nitrogen incorporation at the interface restricts the flow of oxidising species into the interface, thereby limiting the growth process [80].

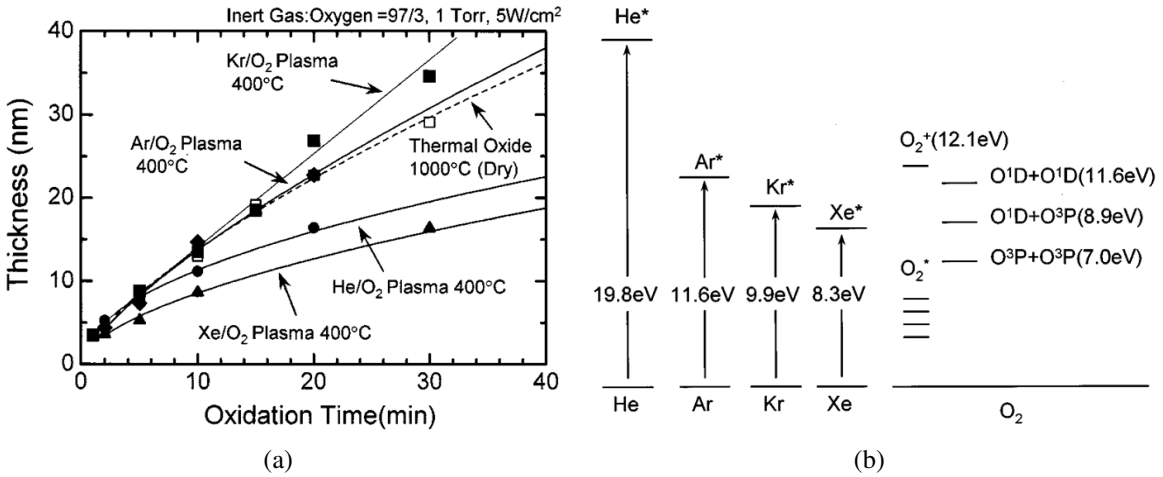
Garduno et al. modelled the growth of oxides in N_2O or O_2 ambient by using a modified power law, taking into account the pressure and time dependence of the growth process. The growth process was carried out in a capacitively coupled chamber of a PECVD equipment. Ion energy is known to play a key role in the oxidation reaction and transporting the reactive species to the interface. The oxidation process was modelled by Eqn. 2.22.

$$X_{ox} = A_0.P^{-m}.e^{-E_a/KT}.P_w^q.(t+t_o)^n \tag{2.22}$$

where P is the pressure (in Torr), P_w is the power (in W), and T is the temperature (in K). Parameter n depends on the gas being used for the process and is 0.2 for O_2 and 0.16 for N_2O. Parameters, A_0, q, E_a, and m are determined from experiments, and varies according to equipment used for growing the oxide [76]. Fig. 2.6(a) shows the oxide growth modelled using the proposed modified square law.

Role of inert gas on oxidation process

One issue with plasma oxidation is the surface damage brought about by bombardment of energetic ions during the oxide growth process. However, in order to minimize the damage, inert gas + O_2 mixtures are used to reduced the amount of energetic oxygen ions. In the above section, the growth dynamics was modelled for plasma oxides/oxy-nitrides grown in a pure O_2 or



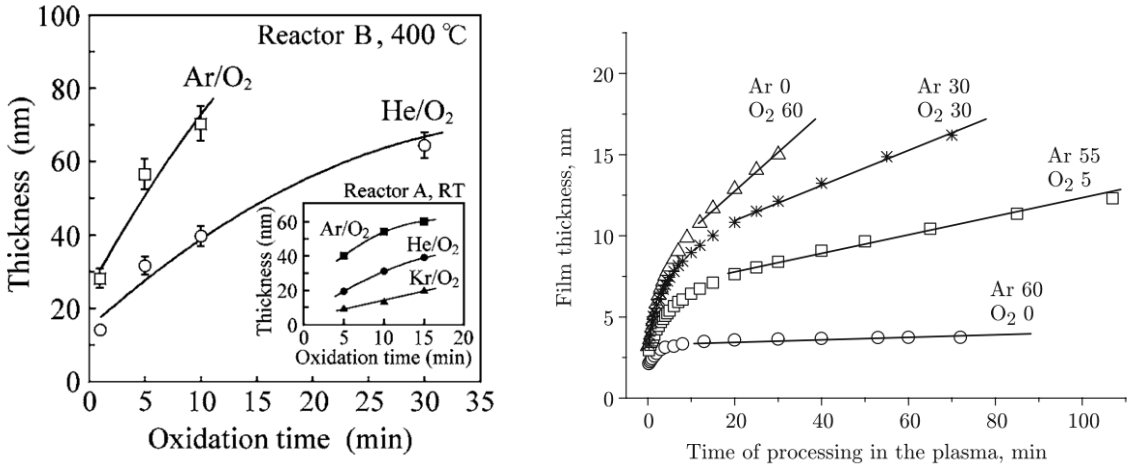
(a) (b)

Fig. 2.7: (a) Growth rate in inert gas - oxygen mixture (b)Energy diagram of inert gas and oxygen [14].

N_2O ambient. Addition of inert gas to oxygen is reported to enhance the oxidation rate, and improve the electrical properties of the grown oxides [14]. The oxidation rates are better than those reported for thermal oxides when a mixture of Kr + O_2 is used for growing the silicon oxide. The oxidation rates for various oxygen/inert gas combinations is shown in Fig. 2.7(a). Addition of krypton to oxygen resulted in a stoichiometric silicon dioxide with stoichiometry identical as film thermal oxide. The low temperature of growth makes this a very promising alternative for thermally grown silicon dioxide.

Sekine et al. [14] explained the increased oxidation rate on the basis of the energy of ionized inert gas with respect to oxygen. This is illustrated in Fig. 2.7(b). O^1D + O^1D is the highly reactive state of oxygen and can lead to bond forming reactions. The inert gas helium with higher energy for its first metastable state results in generation of more $O_2{}^+$ species, which is less reactive. The first metastable state of Ar^* is at 11.6 eV and can result in more higher number of $O_2{}^+$ species than O^1D + O^1D, while Kr^* with an energy level of 9.9 eV can lead to more number of reactive species and leads to an increased oxidation rate. However, Kaspar et al. reported that O^1D species lead to an enhanced oxidation, only for thickness of $\sim$2 nm. Beyond that, continuous exposure to O^1D radicals did not yield thicker oxides. The enhanced oxidation in inert gas require other reactive species which would contribute to the diffusion of reactive species into the oxide [81].

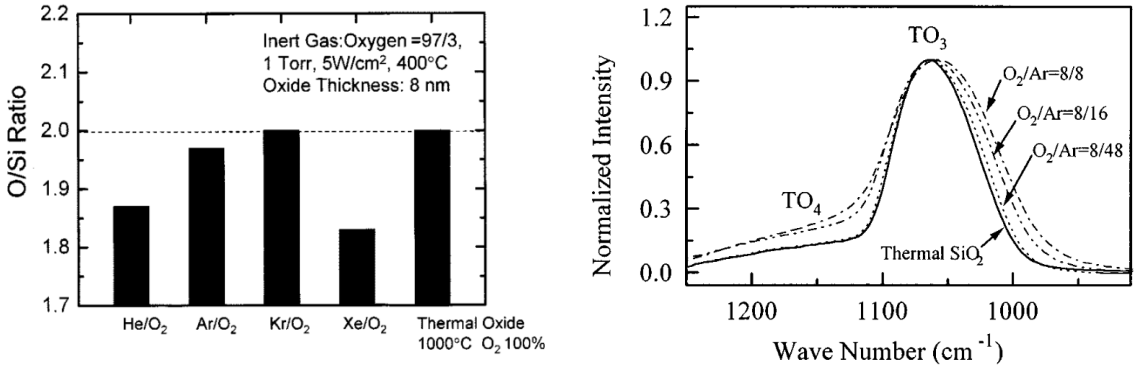
In reported literature, the oxidation rates for combinations of inert gas - oxygen was found to have a strong dependence on the nature of the system used for the experiments. Kakiuchi et al. used an atmospheric pressure plasma reactor [82]. Very high oxidation rates in the order of 28



(a) (b)

Fig. 2.8: (a) Oxidation in atmospheric pressure plasma chamber [82] (b) Oxidation rate for different O_2/Ar ratios[83].

nm/min was reported for oxidation in Ar + O_2 ambient [82]. However, the results presented by Kakiuchi et al. indicate that oxidation in Kr + O_2 plasma ambient has the lowest oxidation rate at room temperature in comparison to oxidation rates in He + O_2 and Ar + O_2 plasma ambients, as shown in Fig. 2.8(a). This result contradicts the results reported in [14] possibly due to the difference in the plasma systems used for the respective experiments. Fig. 2.8(b) shows the oxidation rate in an ICP plasma system for different Ar + O_2 ratios. Higher oxidation rate was observed for an O_2 plasma than their diluted counterparts [83].



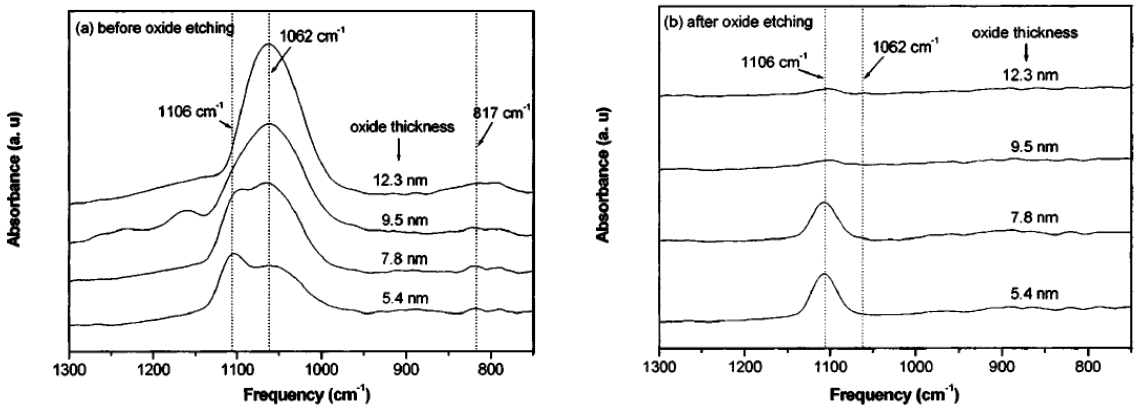
(a) (b)

Fig. 2.9: (a) O/Si ratio from XPS measurements [14] (b) FTIR spectrum showing Si - O - Si vibrations for different O_2/Ar ratios [84].

Films grown in different plasma ambient were reported to have different physical compositions as indicated in Fig. 2.9(a). The film grown in Kr + O_2 ambient had a similar stoichiometry as a thermally grown SiO_2 films. The enhanced oxidation rate in Kr + O_2 ambient may have

contributed to the stoichiometric nature of the plasma grown film [14]. Liu et al. studied the impact of different Ar + O_2 ratios on the physical composition of the films. FTIR investigations on different films revealed that, for the same O_2 gas flow rate, and increase in Ar flow rate shifted the FTIR peak corresponding to Si - O - Si vibrations from 1057 cm^{-1} to 1065 cm^{-1}. This was closer to that observed for ultra thin thermally grown SiO_2 films as shown in Fig. 2.9(b). The densification of the plasma grown film as a result of large Ar concentration in plasma is stated to be the reason behind the shift in FTIR peak.

Interstitial oxygen in ultra thin plasma grown silicon oxide films



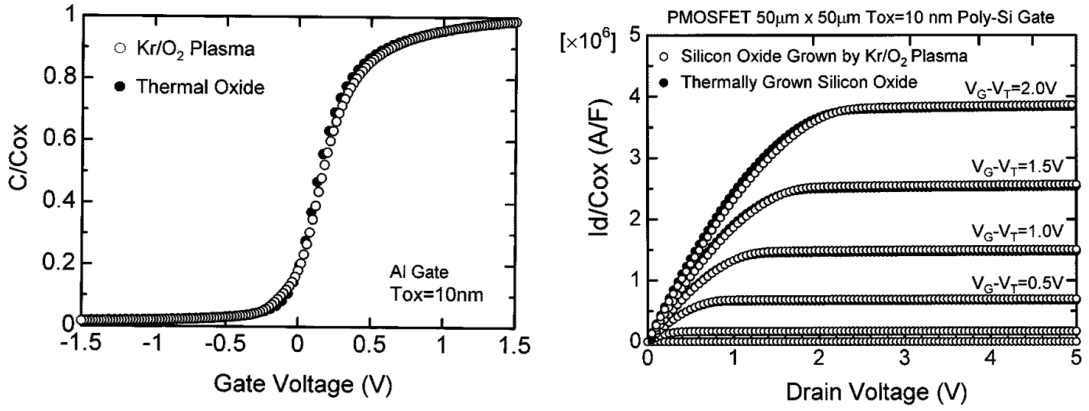
(a) (b)

Fig. 2.10: FTIR spectrum for plasma grown oxide films of different thickness (a) before and (b) after etching in HF solution [85].

Oxidation of silicon carried out at low temperatures can lead to trapping of interstitial oxygen within silicon [85]. FTIR measurements were used to evaluate the presence of interstitial oxygen within silicon. Fig. 2.10(a) shows the FTIR spectrum for the different oxide thickness. The peaks at 1060 cm^{-1} and 817 cm^{-1} are due to Si - O stretching and bending mode vibrations. The peak at 1106 cm^{-1} is attributed to interstitial oxygen within silicon. FTIR measurements following an oxide etch in HF solution, indicated the presence of interstitial oxygen for oxide thickness of 5.4 nm and 7.8 nm, as shown in Fig. 2.10(b). The interstitial oxygen disappears for thicker films because the silicon layer (with the trapped interstitial oxygen) is consumed during the oxidation process [85]. Kim et al. called this interstitial oxygen trapped in silicon as plasma damage. Further experiments using both O_2 and N_2O as process gases also indicated the trapping of interstitial oxygen in silicon. From plasma characterisation using optical emission

spectroscopy (OES), it was concluded that atomic oxygen plays a crucial role in the trapping of interstitial oxygen within silicon. Oxygen in silicon or interstitial oxygen leads to other absorption peaks apart from 1106 cm^{-1}. The peak at 515 cm^{-1} is attributed to bending mode vibrations of Si - O - Si defect molecule [86]. There are similar reports assigning this band to interstitial oxygen in silicon [86].

Device applications



(a) (b)

Fig. 2.11: (a) HFCV characteristics of MOS capacitor with Al gate (b) IV characteristics of p-MOS transistor [14].

MOS capacitors and transistors were fabricated using plasma grown oxide as gate oxide [14]. The device performance was compared with those using thermally grown oxides as the gate oxide. Plasma oxides grown in Kr + O_2 ambient resulted in a D_{it} less than 10^{10} $eV^{-1}cm^{-2}$, which was lower than what was obtained for a thermal oxide grown in O_2 ambient at 1000^oC. High frequency capacitance - voltage (HFCV) characteristics at 1 MHz for metal oxide semiconductor (MOS) capacitors fabricated on n-type substrates with resistivity 3 - 5 Ω cm is shown in Fig. 2.11(a). I_d - V_d characteristics of MOS transistors fabricated on n-type substrate is also shown in Fig. 2.11(b). A sub threshold swing of 69.5 mV/decade was reported for Kr + O_2 plasma oxide as compared to 68.3 mV/decade obtained for thermal oxides [14]. As can be seen,the device performance rendered by plasma grown oxide, which was grown at 400^oC is equivalent to or better than what was obtained for thermal oxides grown at 1000^oC. This exhibits the potential of plasma grown oxides for device applications. There are very few reports on using plasma oxidation for solar cell passivation. The role of nitrous oxide plasma exposure

on solar cells was investigated by Mahanama et al. [87]. An improved cell performance was reported after N_2O plasma exposure on solar cells having a micro crystalline Si emitter [87].

2.5 Summary of the chapter

Starting from the fundamentals of recombination in semiconductors, this chapter discussed the fundamental concepts behinds surface passivation of silicon surfaces. The impact of the semiconductor - dielectric interface parameters like D_{it} and Q_f on the surface recombination rate was discussed through simulations performed using PC1D. The impact of surface recombination at the front and the rear surface of a solar cell on the overall solar cell performance was also discussed through simulations. A comprehensive review of some of the passivation layers used on screen printed solar cells as well as high efficiency solar cells were presented. The chapter also discussed the impact of post deposition plasma treatment on the surface passivation quality of silicon nitride. The chapter concluded with a detailed review of some of the schemes used for low temperature growth of silicon oxide films. The potential application of these films on semiconductor devices was also discussed.

From the review of the existing literature on plasma oxidation processes discussed in this chapter, it was found that there has been no reported study on the potential of plasma grown silicon oxide films for passivating crystalline silicon surfaces. Plasma oxidation process, despite being reported to yield equivalent performance as that of a thermally grown SiO_2 film, have not made its way towards solar cell fabrication process. In this thesis a larger focus is given to these two aspects. One is the evaluation of plasma oxidation process for surface passivation of silicon surfaces which is discussed in chapter 5. Chapter 6 discusses the other aspect of integrating the plasma oxidation process into the solar cell fabrication line. The impact of the plasma oxidation process on the overall solar cell performance is also discussed in chapter 6.

Chapter 3

Surface texturing processes for light trapping in crystalline silicon solar cells

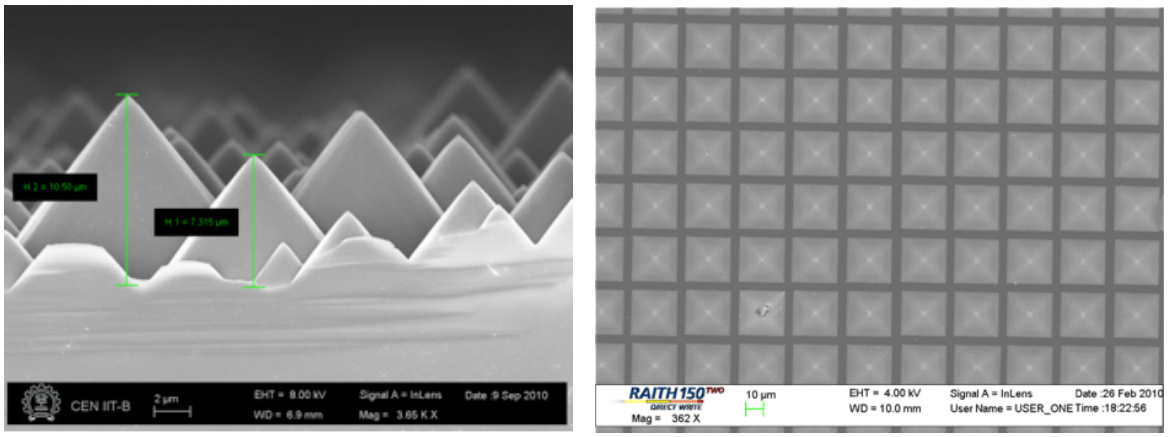
The optical losses in c-Si solar cells are primarily due to the reflection of light from the front surface of the silicon wafer and reflection of light from the contact grids used on solar cells. Further the photons of energy less than the band gap of silicon, 1.12 eV (corresponding to wavelength of 1100 nm) passes through the wafer without resulting in carrier generation. In order to mitigate the optical losses in mono crystalline silicon solar cells, the surface of the silicon wafer is textured by etching the wafer in anisotropic etchants like KOH/NaOH. This process is seen to bring down the weighted average (W_{av}) reflectance (300 - 1000 nm) to approximately 10 - 11% [88]. Further reduction in reflection is brought about by using a silicon nitride film (75 nm, RI = 2.0) as an anti reflective coating (ARC) on the textured silicon surface, which further brings down the W_{av} reflectance to 2 - 3 % [88]. Random pyramidal texturing and inverted pyramidal texturing are the two main approaches used for surface texturing of mono crystalline silicon. Of the two, random pyramidal texturing is widely used in commercial crystalline silicon solar cells owing to its simplicity and cost effectiveness. Inverted pyramidal texturing process requires expensive photolithography process thereby restricting its usage to laboratory scale high efficiency PERL solar cells [7]. In multi crystalline silicon wafers isotropic etch solutions based on HF + HNO_3 + H_2O are used for surface texturing [89]. Other etching schemes based on alkaline (NaOH, KOH) solutions, NaOH - NaClO solutions and reactive ion etching (RIE) are also reportedly used for surface texturing multi crystalline silicon wafers [90, 91]. Wav reflectance of 27% was reported for an acidic texturing scheme based on HF + HNO_3 solution, which can down to 8% on depositing an ARC [90].

This chapter discusses the pros and cons of both random pyramidal texturing as well as inverted pyramidal texturing, thereby establishing the need for development of alternative processes for fabrication of inverted pyramids in silicon. Some of the alternative processes reviewed in this chapter include laser texturing, plasma texturing, texturing schemes based on nano imprint lithography, colloidal lithography and inkjet printing. The chapter also discusses some of the mask free processes used for fabricating inverted pyramids on mono crystalline silicon surfaces.

3.1 Conventional surface texturing processes

Optical losses in crystalline silicon solar cells are mitigated by means of surface texturing and an anti reflective coating. A wet chemical process based on anisotropic etchants like KOH/IPA or NaOH/IPA is widely used for surface texturing of mono crystalline silicon in the solar cell industry [9]. Random pyramidal texturing of silicon is widely used in case of commercially available mono crystalline silicon solar cells, and is reported to yield a weighted average reflectance value of 11.7% [92]. Random pyramidal texturing process involves exposing the silicon wafer to an anisotropic etch solution at 80 - 90^{o}C. The variation in etch rates between the $<111>$ and $<100>$ planes results in the formation of pyramid like structures on $<100>$ silicon wafers after etching. Fig. 3.1(a) shows the surface of the wafer after etching. Sharp pyramids can be seen to be formed. The process is simple to implement and has been widely adopted in the commercial mono crystalline silicon solar cell manufacturing process. However, the random pyramidal texturing process is known to consume 10 - 20 μm of silicon from the wafer [93], making the process less attractive for lower wafer thicknesses. Also random pyramids with its sharp edges and corners are known to result in increased stress on the overlying dielectric [94]. This paves the way for patterned texturing process based on conventional lithography techniques.

Inverted pyramidal texturing used in high efficiency laboratory scale PERL solar cells is reported to yield lower reflectance values of 10.2% but involves cumbersome photolithography processes [92]. Fig. 3.1(b) shows the surface of a $<100>$ silicon wafer with inverted pyramids fabricated on it. The pyramids have a regular arrangement, and the size of the pyramid can be varied by changing the dimensions on the patterning mask. Fig. 3.2 shows the process flow used for the fabrication of inverted pyramids in silicon. The fabrication process involves a large number of steps and involves photolithography. The use of photolithography makes this



(a) (b)

Fig. 3.1: Two different surface texturing schemes demonstrated on <100> wafers (a) Random pyramidal texturing (b) Inverted pyramidal texturing.

process not only expensive, but also results in a lower throughput in case of commercial silicon solar cell production lines. Hence inverted pyramidal texturing process has not found its way towards commercial solar cell production. This necessitates the need for alternative techniques for texturing of silicon solar cells.

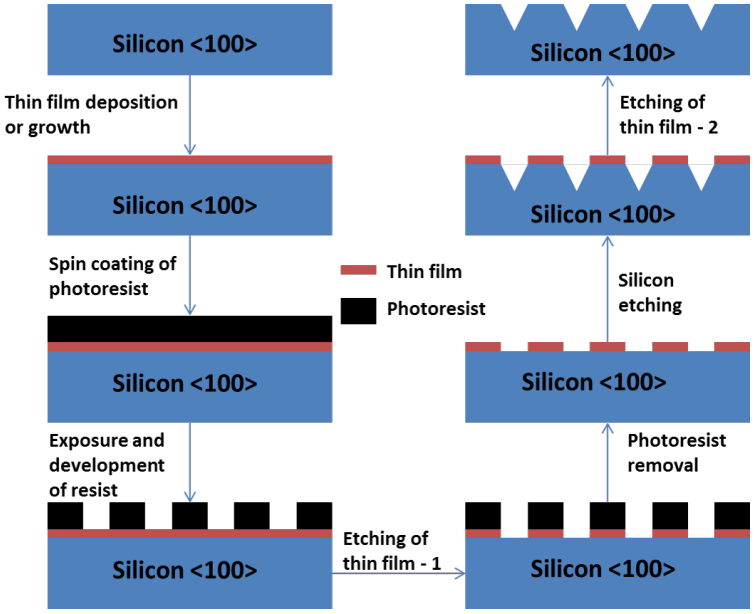
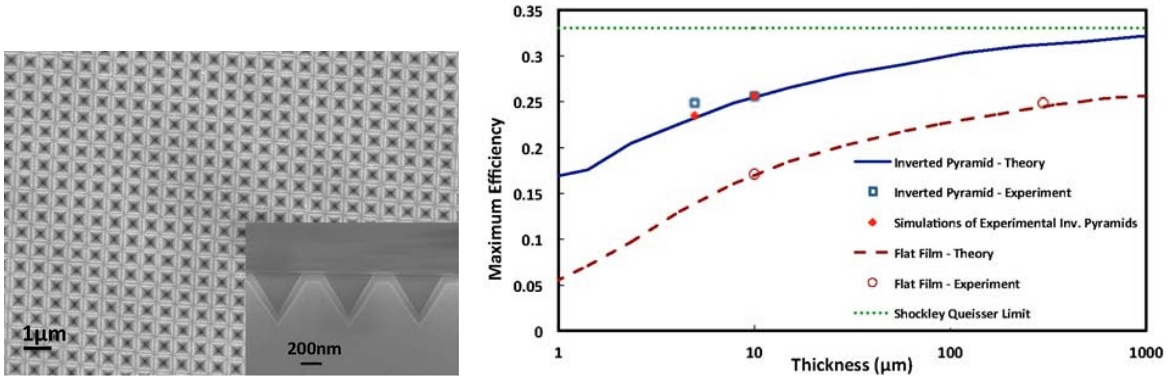


Fig. 3.2: Process flow for fabrication of inverted pyramids in crystalline silicon, adapted from [9].

Nano structuring approaches based on nanowires [95], nanocones [96], nanoholes [97] are also reported as potential schemes for improving light absorption in silicon, as the thickness of the wafer scales. These approaches yield low reflectance values, but falls short in terms of cell performance owing to large surface recombination losses associated with these struc-

tures. Inverted nanopyramids are reported to yield high levels of absorption in thin c - Si films, while minimizing the increase in surface area to 1.7 times, thus potentially lowering the loss of carriers to surface recombination [98]. By using a thin film c - Si of thickness 10 μm in conjunction with nanopyramid texturing, absorption comparable to 300 μm thick silicon was reported. Fig. 3.3(a) shows the nanotextured silicon surface, while Fig. 3.3(b) shows the maximum achievable efficiency for varying thickness of silicon. As can be seen, the theoretical simulation of nanopyramids on 5 and 10 μm thick Si predicted an improvement in the efficiency as compared to a flat silicon of thickness 10 μm and 300 μm. The same was corroborated by experimental data as shown in Fig. 3.3(b). Thus by moving to nanopyramids, not only can significant saving in bulk Si material be achieved but also a significant decrease in surface recombination losses can be brought about. However in the reported work, the nanopyramid texturing was carried out using interference lithography. The technique is not commercially viable for solar cell industry owing to higher production costs and lower wafer throughput. Thus finding novel and alternative means for fabricating inverted pyramids in silicon is an open and challenging problem.



(a) (b)

Fig. 3.3: Potential of nano texturing on ultra thin silicon wafers (a) Inverted nano pyramids fabricated on silicon using immersion lithography (b) 5 μm thick wafer shows an equivalent performance as compared to a 300 μm thick wafer [98].

The chapter begins with a discussion on some of the already reported techniques for fabrication of lithography free micro and nano scale inverted pyramids.

3.2 Novel processes for fabricating inverted pyramids on crystalline silicon surfaces

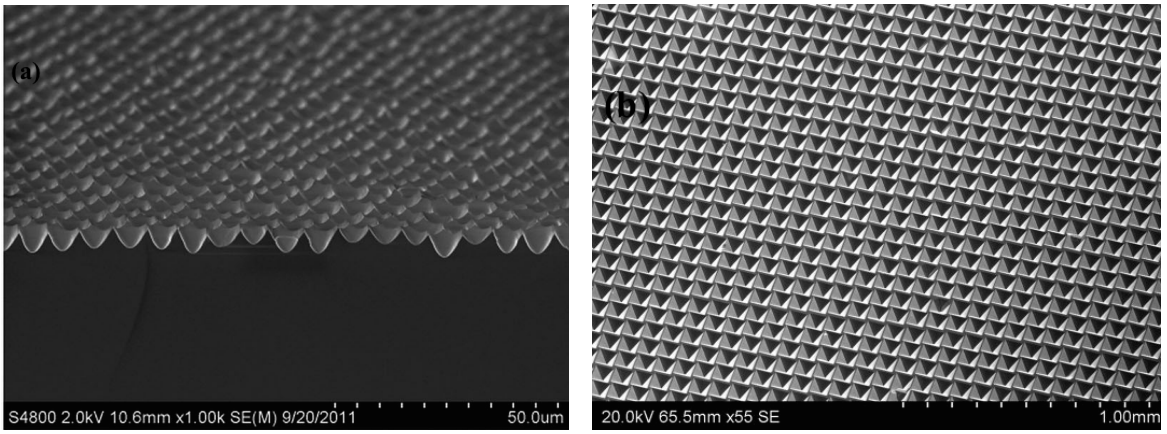
This section discusses some of the alternative techniques that have been proposed for the fabrication of inverted pyramids on silicon.

3.2.1 Reactive ion etching

Hauser et al. had reported the usage of a nanoimprint lithography technique for the fabrication of honeycomb texture on multi crystalline silicon wafers [99]. The process involves the fabrication of a polydimethylsiloxane (PDMS) stamp based on an interference lithography technique. The stamp is further used to fabricate the honeycomb patterns onto the silicon surface. After transferring the pattern onto the photoresist on the silicon wafer, the sample is etched in two different RIE chambers to obtain the required pattern. The proposed process, though very promising, involves expensive techniques like immersion lithography and nano imprint lithography and also suffers from low throughput. Moreno et al. had reported a texturing process based on reactive ion etching using SF_6 + O_2 plasma [100]. By tailoring the process power, inverted pyramid like structures were fabricated on the silicon surface. The process however, resulted in the a weighted average reflectance of 6%. However, presence of various SiO_xF_y complexes on the surface of the silicon wafer after the RIE process was confirmed by Raman spectroscopy. The impact of this complex on the device performance was not investigated. Usage of a reactive ion etch process is also reported to result in an irreversible degradation of bulk lifetime of the silicon wafer [101]. This may lead to a degradation in device performance, necessitating further studies before implementing this technology in commercial production.

3.2.2 Laser texturing and Inkjet printing

Zeilke et al. had used a laser texturing based process for the fabrication of inverted pyramids on periodic textures on the silicon wafer [45]. Very high short circuit current of 39.3 mA/cm^2 was obtained on a multi crystalline wafer as a result of the direct laser texturing process. Kumar et al. had also used laser to ablate a dielectric [102]. The ablated dielectric region serves as a template for the fabrication of inverted pyramids in silicon. However, the throughput for these laser processes may need further improvement before it is put into commercial production



(a) (b)

Fig. 3.4: Alternate surface texturing schemes demonstrated on <100> wafers (a) Laser texturing of silicon [45] (b) Inverted pyramidal texturing using inkjet printing [8].

[99, 102]. There is a recent report of a process based on inkjet printing for the fabrication of inverted pyramids on silicon [8]. The process resulted in an ordered array of inverted pyramids, but the base of the pyramid was about 65 μm wide, thus consuming a large quantity of silicon during the etch process. For fabricating inverted pyramids of smaller dimensions, the print dimensions need to be lowered. With further improvement in inkjet printing technology, the process in [8] may become commercially viable.

3.2.3 Colloidal lithography

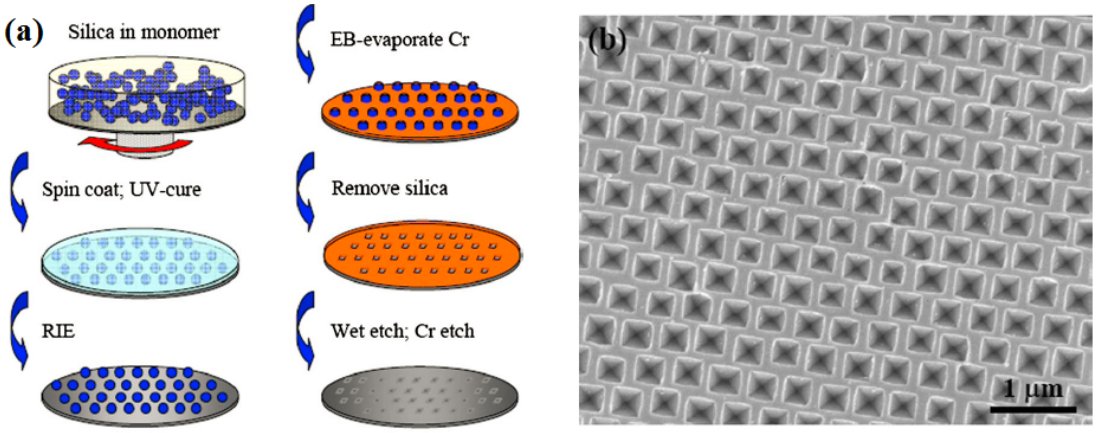


Fig. 3.5: (a) Process flow for fabricating inverted pyramids using colloidal lithography (b) Inverted pyramids fabricated using technique mentioned in (a) [103].

A very promising and commercially viable method for the fabrication of inverted pyramids on silicon is by using colloidal lithography. Sub-wavelength inverted pyramids were fabricated

by Sun et al. using colloidal lithography [103]. The schematic of the process sequence is shown in Fig. 3.5. Colloidal silica particles are spun coated onto a silicon wafer surface. A metal film is deposited on the wafer surface. The silica particles serve as a shadow mask during the metal deposition process. Upon lift off of the silica particles, the etch would happen in the voids and the remaining metal on the wafer surface act as an etch mask. After the etching process, the metal is removed and subsequent processes can be carried out on the wafer. The process resulted in the formation of periodic sub wavelength inverted pyramids as shown in Fig. 3.5. One of the potential drawback of this work is the usage of a metal mask which can degrade the bulk lifetime of the wafer. Replacing the metal deposition step with a dielectric can potentially mitigate this issue.

3.2.4 Maskless fabrication of inverted pyramids

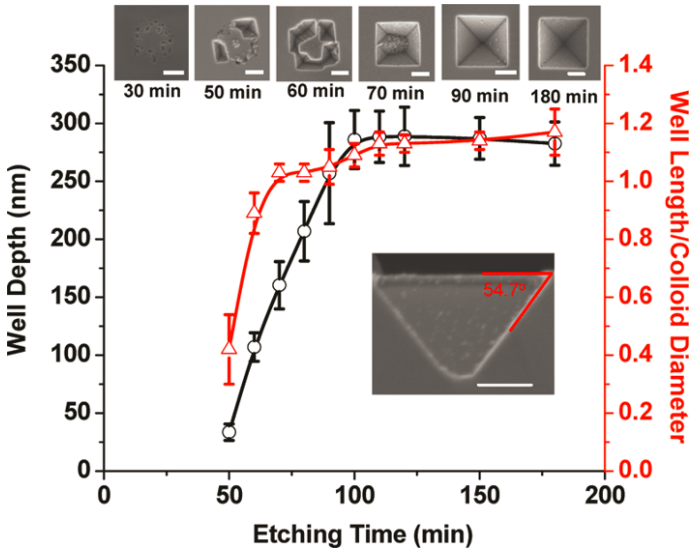


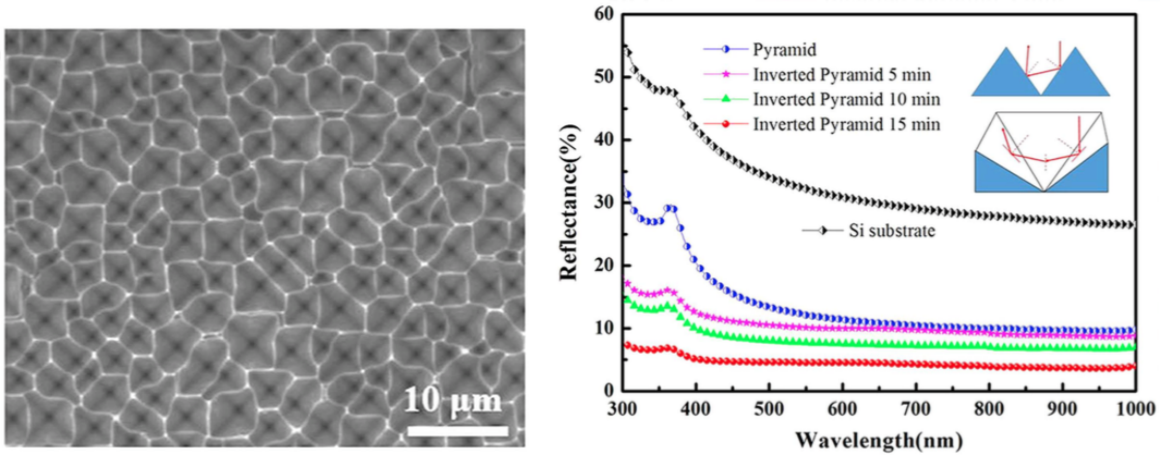
Fig. 3.6: Etched depth (well depth) versus etching time, indicating a large amount of etch for longer etch durations; inset shows the SEM images showing the evolution of the pyramids with time [105].

Maskless fabrication of inverted pyramids using chemically reactive colloidal particles was reported by Chaturvedi et al. [105]. Amidine functionalised poly styrene beads were used as the colloid in the experiment [105]. The bead, upon heating in an autoclave at 150^{o}C, results in localised formation of ammonium hydroxide, which results in the anisotropic etching of silicon. The reported process is very promising as inverted pyramids of various dimensions can be fabricated in an autoclave using super heated steam. However the surface coverage of the inverted pyramids was seen to be low. Fig. 3.6 shows the nano pyramid depth with increasing

etch time. As can be seen for 30 min, no pyramid formation is found, and it is seen to commence beyond 50 min. The initial period of the process is used to etch out the thin chemically grown silicon dioxide film and hence the etch rate is slow in the initial phase of the process. As the time increases, the silicon dioxide film is etched out, and the silicon etching is seen to commence, and fully formed inverted pyramids can be found after 90 min. However the spacing behind the beads are quite high, resulting in lower surface coverage and hence high reflectance.

A novel texturization scheme based on a LPCVD silicon nitride was reported by Weber et al., where a thin film (2 - 3 nm) of LPCVD silicon nitride was isotropically etched in HF:HNO_3 solution to generate pits of 5 μm [104]. The process was reported to consume less quantity of silicon as compared to conventional etching process. However, the process had a higher reflectance value as compared to conventional random pyramids. Low density SiO_2 films deposited at low temperature was also used as an etch mask for anisotropic etching [106]. In this process, the pin holes present in the silicon oxide film served as a mask for fabrication of inverted pyramids. Here again, the surface coverage of the inverted pyramids was found to be low resulting in higher reflectance [106]. Self assembly of CsCl is another technique used for fabricating inverted pyramids on silicon [107]. After depositing titanium on top of the self assembled CsCl nanoparticles, CsCl was lifted off leaving behind Ti on the wafer surface. Further etching of Si in NaOH/KOH resulted in the formation of inverted pyramids on the silicon surface, with Ti acting as the etch mask [107]. The process yielded inverted pyramids of sub micron dimensions. However, the process involved two thermal evaporation steps for the deposition of CsCl and Ti respectively, thereby increasing the cost.

More recently, Wang et al. has reported a novel process for maskless fabrication of inverted pyramids [108]. Regularly arranged inverted pyramids are fabricated by etching a <100> Si wafer in a solution of $Cu(NO_3)_2$/HF/H_2O_2/H_2O at 50^oC. The etch mechanism is based on an electrochemical reaction brought about by the difference in electrochemical potential between Si and Cu^{2+}, and is similar to the concept of metal assisted chemical etching. The selectivity of etch process is reported to be the result of a difference in surface bond densities for the <100> and <111> planes. It is argued that the <100> plane may have more number of electrons available for capture by Cu^{2+}. Weighted average (W_{av}) reflectance of 4.4% is reported after the etch process, which is significantly lower than some of the reported values for random as well as inverted pyramidal texturing. The wafer surface after the etch process and the corresponding W_{av} reflectance are shown in Fig. 3.7. Despite the ground breaking results, one of the major



(a) (b)

Fig. 3.7: Maskless inverted pyramid fabrication using $Cu(NO_3)_2/HF/H_2O_2/H_2O$ as etch solution (a) Inverted pyramids after etching in solution (b) W_{av} reflectance for different time durations compared with random texturing process. [108].

bottleneck of the proposed process is the use of Cu, which is a fast diffuser in Si. Cu diffusion into Si can result in a significant reduction in bulk lifetime of the wafer, which may prove detrimental for a solar cell process. However, detailed investigation into the carrier lifetime degradation as a result of the proposed process needs to be carried out, before adopting this process for texturing process in c - Si solar cell fabrication. An alternative option would be to replace $Cu(NO_3)_2$ with another salt which can replicate the same effect.

3.3 Summary of the chapter

Inverted pyramidal texturing process, despite the cumbersome lithography processes involved, was seen to have a significant advantage over random pyramid texturing in terms of the amount of silicon consumed during the process. The larger consumption of silicon bulk during random pyramidal texturing can become a deal breaker as the wafer thickness scales over the coming years. However, the hallmark of random pyramidal texturing process is its simplicity, making it the widely adopted technique for texturing silicon surfaces in commercially available silicon solar cells. In order to replace the photolithography process involved in inverted pyramid fabrication, various alternative processes for fabrication of inverted pyramids were discussed in this chapter. In light of the discussion in this chapter, it can be concluded that there is still a lot of scope for designing and developing novel processes for fabricating inverted pyramids on crystalline silicon surfaces. One such alternative process for fabricating inverted pyramids on

silicon surfaces is discussed in chapter 8 of this thesis.

Chapter 4

Experimental Techniques

This chapter discusses the basic theory behind some the characterisation techniques widely used during the experiments discussed in this thesis.

4.1 Fourier transform infrared spectroscopy

Fourier Transform Infrared (FTIR) Spectroscopy is used to investigate the various fundamental vibrational modes of a material. FTIR measurements have been extensively used to understand the presence of various bonds within the dielectrics discussed through out this thesis. When a sample is exposed to infra red (IR) radiation, the molecules absorb the energy. The molecular vibrational energy levels of the sample moves from ground state to excited state. Each molecule absorbs specific energy levels, and hence is a signature of the material under investigation. The IR radiation thus transmitted through the sample will indicate the extent of absorption within the sample. Some of the vibrational modes of the molecules are stretching (symmetric and asymmetric) mode, rocking mode, scissoring mode, twisting mode, and wagging mode. Analysis of peaks (shape, intensity and position) present in the resultant spectrum can provide information regarding the bonding structure of the material under investigation. Some of the vibrational modes relevant to the discussions in the thesis are indicated in the Table. 4.1.

In this thesis, FTIR system from Perkin Elmer (Spectrum BX II) was used. Single side polished <100> Cz - Si wafers with 4 - 7 Ω cm resistivity was used for the experiments. The dielectric films were deposited on the polished surface of the wafer. A wafer with no deposition was used as the reference sample. The measurements were carried out in transmission mode at room temperature. A resolution of 4 cm^{-1} was used. 16 - 32 scans were carried out per sample

Table 4.1: Different bonding arrangements in FTIR spectrum and corresponding wavenumber.

FTIR Vibration modes		
Bond	Wavenumber (cm^{-1})	Vibrational mode
Si- N [109, 110]	490 875 - 896 2335 - 2360	N- Si_3 Si - N Stretching - asymmetric Si - N_2 stretching
Si - O [86, 111]	810 1071 1105	Si - O - Si bending Si -O - Si stretching Si - O - Si stretching - asymmetric
Si - H [112]	2140 2175 2220	H - Si - SiN_2 H_2 - Si - N_2 H - Si - N_3
N - H [112]	3445 1540	N - H stretching NH_2 bending

to improve the accuracy of the measurements.

4.2 X-ray photoelectron spectroscopy

X-ray Photoelectron Spectroscopy (XPS) is a surface analytical technique used to characterize the chemical composition of a material. Basic operating principle of XPS is the photoelectric effect. On irradiating a sample with an X-ray (1 - 2 KeV), electrons are ejected out from the material. By measuring the energy of the emitted electron (E_{emit}), the binding energy (E_{bind}) of the electron can be calculated as $E_{bind} = h\nu - (E_{emit} + q\phi_p)$. $h\nu$ is the energy of the incident X-rays, ϕ_p is the work function of the spectrometer and E_{emit} is the energy of the emitted electron [113]. A typical XPS spectrum has count of emitted electrons on the Y - axis and binding energy on the X-axis. Each element has its own characteristic binding energy, and thus XPS can identify the elements as well as its chemical state. A shift in binding energy observed in a XPS spectrum is typically attributed to a change in bonding state of the element in question. e.g. The binding energy for SiO_2 in Si2p XPS spectrum is 103.3 eV, whereas the incorporation of nitrogen shifts the Si2p XPS spectrum to 102 eV [114]. In XPS, the photoelectrons are emitted from the top 0.5 - 5 nm of the surface, making it a surface sensitive analytical technique. X-rays can penetrate deeper into the material, but the emitted electrons are lost due to lower mean free path of the electrons. Angle resolved XPS (ARXPS) is a technique where the sample is titled with respect to the X-ray, as a result of which a depth profiling of the sample can be done.

In this thesis, both surface and ARXPS techniques have been extensively used to investigate

the stoichiometry of the plasma grown films. The data included in this thesis have been obtained from an XPS system from ULVAC - PHI, Model: PHI5000 Versa Probe II. Al Kα, X-ray source was used for the measurements.

4.3 Optical emission spectroscopy

The transition of an electron from an excited state to a lower energy state can result in the emission of photons. Emission spectroscopy is a spectroscopic technique used to analyse these emissions. Optical emission spectroscopy (OES) is widely used for analysing reactive plasmas. In plasmas, the emissions result from the various excited states of the reactive species present in the plasma. The emissions are specific to each atomic species present within the plasma. However, each atomic species can have multiple emissions which depends on the nature of electronic transitions. The plasma emission intensity depends on the degree of ionisation and the electron energy distribution of the plasma [115]. This technique can be used to investigate the presence or absence of any reactive species within the plasma. One of the major benefit of OES spectroscopy for plasma diagnosis is that it is a non intrusive technique, and has been widely used for end point detection in plasma etch systems.

OES is used in this thesis to analyse the plasma employed for the oxidation process. A spectrometer from Princeton Instruments was used for the measurements shown in this study.

4.4 Time of flight secondary ion mass spectroscopy

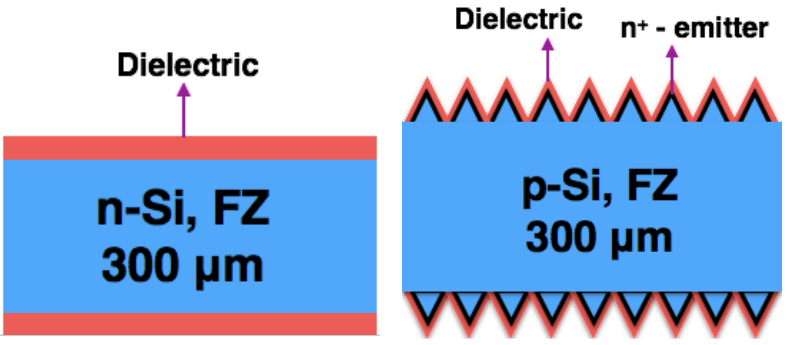
Time of flight secondary ion spectroscopy (TOF-SIMS) is used to analyse the chemical composition (elemental and molecular) at the surface of a material. A pulsed ion beam (Cs/Ga/O_2) is directed at the sample under investigation. This results in the emission of secondary ions and ion clusters from the sample surface. The ejected species travels through a "flight column" and reaches the detector. The time taken for the secondary ions ejected from sample to travel from the sample surface to the detector is used to identify the elements. The sensitivity of TOF-SIMS is in the ppm range. A depth resolution of 1 nm and a spatial resolution of 0.1 μm is possible with the TOF-SIMS used for analysis in this thesis. Besides surface analysis, TOF-SIMS can be used for generating depth profiles. By repeatedly sputtering and analysing the sample, the depth profile of the element under investigation can be generated. Different materials have different

sputtering yields for an ion beam. The raw data for a depth profile would have the counts on the Y - axis and sputtering time on the X - axis. Using a surface profilometer, the sputtered crated depth is measured and is then used to estimate the sputter rate. Converting counts to concentration requires the use of relative sensitivity factor (RSF).

In this thesis, TOF - SIMS is used for depth profiling of hydrogen and nitrogen. Due to the absence of standard samples, the raw data (count versus time) is presented in this thesis. TOF - SIMS measurements were carried out at SAIF IIT Bombay using phi nanoTOF II from ULVAC - PHI.

4.5 Effective lifetime measurements

Effective lifetime measurements are carried out to investigate the quality of surface passivation. Illuminating a block of semiconductor results in generation of carriers. By measuring the decay rate of carriers, the effective lifetime of carriers can be estimated. The wafer under test is placed near an inductive coil and the generation and decay of carriers results in a change in conductance of the wafer. The change in conductance is analysed and the effective lifetime is measured. From lifetime measurements, surface recombination velocity, S (cm/s) and emitter saturation current, J_{0e} (fA/cm^2), can be extracted. The schematic of the device used for extraction of τ_{eff} and J_{0e} are shown in Fig. 4.1(a) and Fig. 4.1(b) respectively. For accurate estimation of τ_{eff}, FZ wafers are used to mitigate the impact of bulk lifetime on τ_{eff} measurement. In case of J_{0e} measurements, an emitter is diffused on the wafer and is then capped with silicon nitride on both sides.



(a) (b)

Fig. 4.1: Device schematic used for (a) τ_{eff} measurement (b) J_{0e} measurement.

The extraction of effective surface recombination velocity (S_{eff}) from τ_{eff} is given by the

following equation.

$$\frac{1}{\tau_{eff}} = \frac{2S_{eff}}{W} \tag{4.1}$$

where W represents the thickness of the wafer. Eqn 4.1 is obtained from Eqn. 2.13 by assuming τ_{bulk} to be ∞. Thus the calculated S_{eff} is the highest SRV obtainable for the dielectric under investigation. In this thesis, Eqn. 4.1 is used for calculating SRV. Lifetime measurements were carried out in WCT -120 lifetime tester from Sinton instruments. For $\tau_{eff} < 200\ \mu$s, QSS mode was used for the measurements, whereas transient mode was used for higher τ_{eff} reported in this thesis.

J_{0e} value is computed from τ_{eff} using the equation

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2J_{0e}(N_{dop} + \Delta n)}{qn_i^2 W} \tag{4.2}$$

where N_{dop} (in cm^{-3}) is the wafer doping level, q is the electronic charge, W (in cm) is the thickness of the wafer, $n_i{}^2$ (in cm^{-3}) is the intrinsic carrier density and Δn (in cm^{-3}) is the excess carrier density. Typically, J_{0e} measurements are carried out using high resistivity wafers to ensure that the wafer goes into high injection regime ($\Delta n >> N_{dop}$) following illumination. By calculating the slope of the curve, $\frac{1}{\tau_{eff}}$ - $\frac{1}{\tau_{bulk}}$ versus Δn, J_{0e} can be extracted [116]. In case of low injection regime ($\Delta n << N_{dop}$), the term on the right side of the Eqn. 4.2 is a constant. Hence, it can be rewritten as:

$$S_{eff} = \frac{2J_{0e}(N_{dop} + \Delta n)}{qn_i^2 W} \tag{4.3}$$

where S_{eff} is the surface recombination velocity in cm/s. In this thesis, J_{0e} measurements were carried out on double side phosphorus diffused p-type FZ and Cz wafers. Device schematic used for this measurement is shown in Fig. 4.1(b).

4.6 Metal insulator semiconductor capacitance - voltage measurements

Metal insulator semiconductor (MIS) capacitor is a two terminal device used to study various electrical properties of the dielectric and the nature of interface between the dielectric and semiconductor. Analysis of the capacitance - voltage (CV) curves can give a whole host of information regarding the dielectric like the breakdown field and its interface parameters like

fixed charge density (Q_f) and interface state density (D_{it}). Fig. 4.2 shows the process used for fabrication of MIS capacitors discussed in this thesis. Thermally evaporated aluminium (150 nm) have been used for making the top and bottom contact in the MIS capacitors discussed in this thesis. Al was evaporated using shadow mask with circular holes of 200 μm and 400 μm diameter.

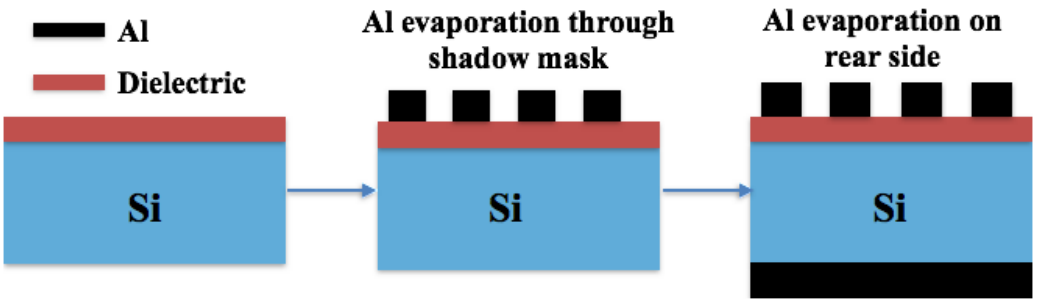


Fig. 4.2: Process flow for fabricating MIS capacitors.

Fig. 4.3 shows the high frequency CV (HFCV) and high frequency conductance - voltage (HFGV) curves measured on a p-type substrate. Depending on the applied gate voltage, three regimes of operation namely accumulation, depletion and are labeled in Fig. 4.3. The resultant HFCV curve measured from a MIS capacitor is strongly dependent on the Q_f and D_{it}. An increase in positive Q_f shifts CV curve to the left, while an increase in negative Q_f shifts the CV curve to the right. An increase in D_{it} can result in a larger skew for the HFCV curve in the depletion region.

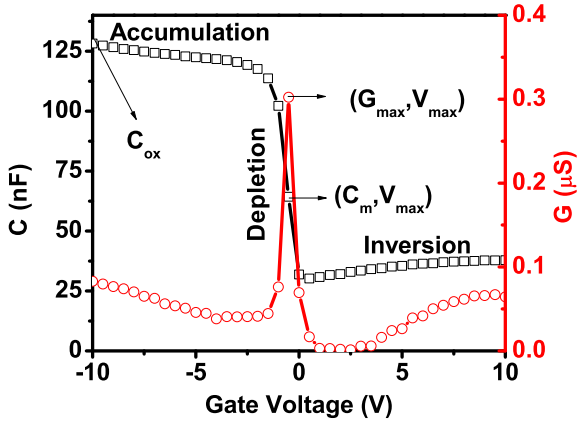


Fig. 4.3: HFCV and HFGV for an MIS capacitor on a p-type Si substrate.

In order to extract the Q_f from the HFCV curve, the shift in mid - gap voltage (V_{mg}) from its ideal value ($V_{mg,ideal}$) is computed. V_{mg} is the voltage corresponding to the mid - gap capacitance (C_{mg}) extracted from the HFCV curve. $V_{mg,ideal}$ and C_{mg} are computed using the

following relations [117]:

$$V_{mg,ideal} = \phi_{ms} + \phi_B + \frac{qN_aX_{mg}}{C_{ox}} \tag{4.4}$$

where ϕ_{ms} is the metal semiconductor work function difference (in volts), ϕ_B is the bulk potential (in volts), q is the electronic charge, N_a is the doping concentration of Si (in cm^{-3})and X_{mg} is depletion width at mid-gap (in cm).

$$\frac{1}{C_{mg}} = \frac{1}{C_{ox}} + \frac{1}{C_{s,mg}} \tag{4.5}$$

where $C_{s,mg} = \varepsilon_s/X_{mg}$. Further, the fixed charge density Q_f is given by:

$$Q_f = C_{ox}(V_{mg,ideal} - V_{mg}) \tag{4.6}$$

where V_{mg} is the voltage corresponding to mid gap capacitance C_{mg}.

D_{it} was extracted from HFCV and HFGV curves using the single frequency approximation method described by Hill et al. [118], using the following relation:

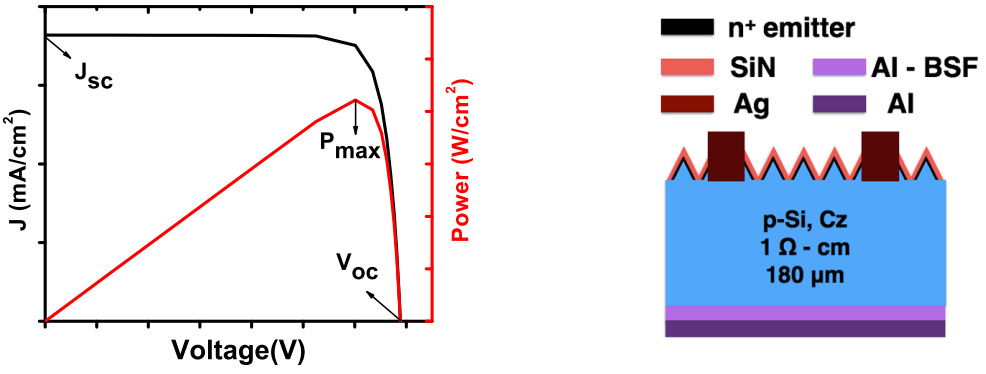
$$D_{it} = \frac{2}{qA} \frac{G_{max}/\omega}{(G_{max}/\omega C_{ox})^2 + (1 - C_{max}/C_{ox})^2} \tag{4.7}$$

The HFCV curves reported in this thesis, have been measured using Keithley 4200 SCS at 50 - 100 KHz. The bias was applied to the bottom contact while the gate contact was grounded during measurements. The MATLAB codes used for extraction of D_{it} and Q_f are included in Appendix A.

4.7 Solar cell current - voltage measurements

Performance of a solar cell is quantified by measuring the illuminated IV under standard test conditions (STC) as defined under International Electrotechnical Commission (IEC) standard 60904 [119]. One of the primary condition is that the illumination spectrum used for measurement should match with the AM 1.5G spectrum. The illumination intensity should be 1000 W/m^2 and temperature of measurement should be 25^oC. Further, an array of contacts should be used to probe the bus bar in order to reduce the impact of series resistance on the measurement. Fig. 4.4(a) shows the illuminated IV and power - voltage (PV) curve for a silicon solar cell. The maximum power point on the curve is labelled as P_{max}. Open circuit voltage (V_{oc}) and short

circuit density (J_{sc}) are also labelled in Fig. 4.4(a). Fig. 4.4(b) shows the schematic of the screen printed solar cell used in the experiments discussed in this thesis. The detailed process flow and the recipes used for fabricating the solar cell shown in Fig. 4.4(b) is given in Appendix B.



(a) (b)

Fig. 4.4: (a) IV and PV curve of a solar cell (b) schematic of a screen printed p-type silicon solar cell used for experiments.

From the IV and PV curve, the solar cell efficiency and fill factor are calculated using the following relations:

$$FF = \frac{P_{max}}{V_{oc} * J_{sc}} \tag{4.8}$$

where P_{max} is the maximum power generated out of a solar cell (in W/cm^2), V_{oc} is the open circuit voltage (in V), and J_{sc} is the short circuit current density (in A/cm^2)

$$\eta = \frac{P_{max}}{P_{in}} \tag{4.9}$$

where P_{in} is the power incident on the solar cell under test. At 1 sun illumination, P_{in} is 0.1 W/cm^2.

In this thesis, the illuminated IV measurements were carried out using a solar simulator from ABET instruments. The measurement temperature was maintained at 25^{o}C using a water cooling system. Series resistance (R_s) of the solar cell was measured using Bowden method [120], while shunt resistance (R_{sh}) was measured from the reverse biased dark IV curve [121].

4.8 Quantum efficiency measurements

Quantum efficiency (QE) refers to the ratio of the number of electrons that are collected from a solar cell to the number of photons incident on the solar cell. Depending on the number of photons that are considered for calculating QE, it is classified as external and internal. External QE (EQE) takes into account the total number of photons incident on the device, whereas Internal QE (IQE) considers the total number of photons entering the device. This would imply that IQE eliminates the effect of reflectance from the measurement. IQE is given by the relation, IQE = EQE/(1 - R - T), where R and T represent the reflection and transmission losses on the device respectively.

QE of a device is measured by illuminating the device with photons of different wavelengths. e.g.: For the c - Si silicon solar cells discussed in this thesis, QE measurements are carried out from 300 nm to 1100 nm. An ideal IQE curve would have a value equal to one for the wavelengths under investigation. In case of c - Si solar cell, a sharp fall in IQE for short wavelength range (300 - 500 nm) is representative of carrier loss due to recombination in the emitter and the surface region. Similarly for long wavelength range (900 - 1100 nm), a fall in IQE represents carrier loss due to recombination at the rear surface. A fall in IQE in the mid wavelength range is representative of a low bulk lifetime. Therefore, QE measurements can be used to diagnose the diagnose the recombination mechanisms responsible for the losses in a solar cell. QE measurements shown in this thesis, were carried out using Bentham PVE300 from Bentham Instruments in transformer mode. A wavelength resolution of 5 nm was used during measurements.

Chapter 5

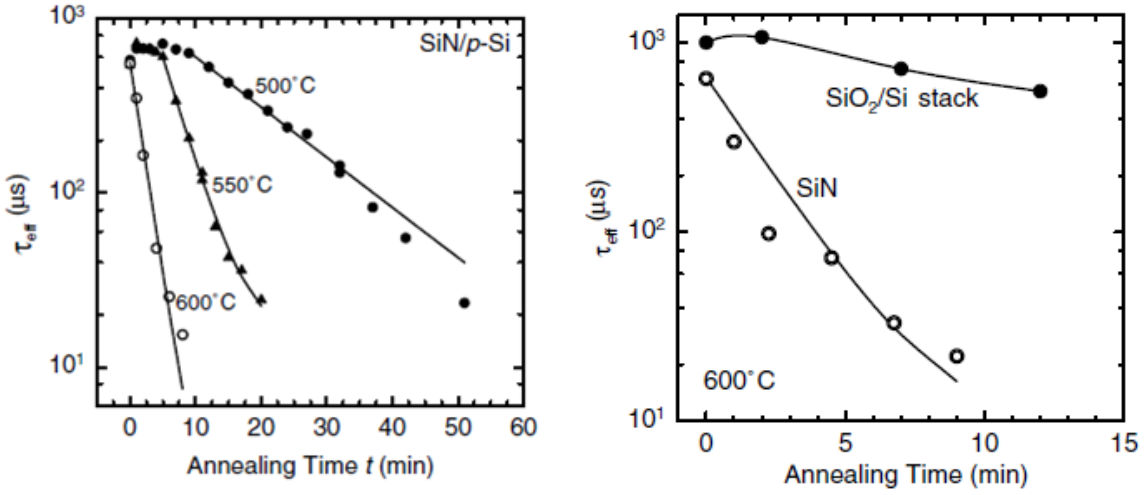
Potential of plasma grown films for silicon surface passivation

5.1 Motivation

Hydrogenated silicon nitride (SiN_x:H) is widely used in commercially available crystalline silicon solar cells, as an anti reflective coating and as a surface passivation layer. Schmidt et al.had demonstrated a minority carrier lifetime of 900 μs on 1 Ω cm p-type FZ wafers, indicating very high surface passivation quality for the silicon nitride film [51]. However, the minority carrier lifetime decreased to $\sim$20 μs upon annealing at 600^oC, as shown in Fig. 5.1(a). Lauinger et al. had shown record low SRV of 4 cm/s and 20 cm/s on p-type 1.5 Ω cm and 0.7 Ω cm FZ wafers using a silicon nitride film deposited in high density remote PECVD system [52]. Low RI (1.9 - 2.0) films have been reported to be thermally stable, and rich in fixed charges, whereas high RI (2.2) films yields very low interface state density. However, the passivation quality of the high RI films are reported to degrade with firing. Additionally, it is also reported that, using SiN_x:H film for rear surface passivation can lead to parasitic shunting, thereby degrading solar cell performance [32].

Thermally grown SiO_2 is known to offer high quality interfaces with c - Si for MOS technology, as it yields very low D_{it} in the order of 10^9 - 10^{10} $eV^{-1}cm^{-2}$ after a forming gas annealing at 420^oC. However in case of crystalline silicon solar cells, thermally grown SiO_2 films offer similar passivation quality for emitters, with different phosphorus doping concentrations [51]. It also offers good quality passivation for p-type substrates of varying resistivity. Owing to the high quality surface passivation offered by thermally grown SiO_2 films they have been used for

passivating the front and the rear surface of high efficiency PERL cells [7]. The passivation quality of as grown SiO_2 film is improved by a forming gas annealing (FGA) or by capping the SiO_2 layer with SiN_x:H film. Very low SRV of 2.4 cm/s and 11.8 cm/s were reported for stacks of thermally grown SiO_2 - PECVD SiN_x:H films, which was comparable to what was obtained for alnealed SiO_2 films [65]. However, the high temperature required for the growth of SiO_2 forbids it application in commercial crystalline silicon solar cells. High temperature leads to higher production cost, lower throughput, and can also lead to activation of impurities in multi crystalline silicon wafers, and hence there is a need for low temperature processes for growth of silicon oxide films.



(a) (b)

Fig. 5.1: (a) Thermal degradation of silicon nitride film on annealing (b) Improved thermal stability of SiO_2 - SiN stack [51].

As previously discussed, stacks of SiO_2 - SiN_x:H films are known to yield very low SRV [65]. Not only is the quality of surface passivation improved but It is also reported that stacks of SiO_2 - SiN_x:H have an improved thermal stability [51]. Fig. 5.1(b), illustrates the improvement in thermal stability upon using a stack of SiO_2 - SiN_x:H [51]. Rohatgi et al. reported that a stack of a rapid thermal oxide (RTO) grown SiO_2 film capped with SiN_x:H resulted in 'exceptional' emitter surface passivation following a contact firing process [122]. SRV of less than 10 cm/s was reported by Narasimha et al. on p-type 1.25 Ω cm wafer after firing a stack of RTO - SiN_x:H [66]. Additionally it was also reported that surface passivation quality of SiO_2 - SiN_x:H stack was found to be independent of the silicon nitride deposition conditions, which eliminated the need for a thorough optimisation of SiN_x:H films [51].

From the above discussions, it can be concluded that the surface passivation quality of silicon nitride films degrades with firing, and can also result in parasitic shunting when used for rear surface passivation. Thermally grown SiO_2 films offer excellent surface passivation upon alnealing, for both n and p-type substrates. However the high temperature required for the growth (800^oC - 1100^oC) of SiO_2 films make it less attractive for industrial adoption, thereby restricting its usage in commercial crystalline solar cells. However, stacks of SiO_2 - SiN_x:H offers the following advantages:

- Improved surface passivation with improved thermal stability as compared to single layer SiO_2 or SiN_x:H films
- Tedious optimisation of the top silicon nitride layer can be done away with in case of SiO_2 - SiN stacks

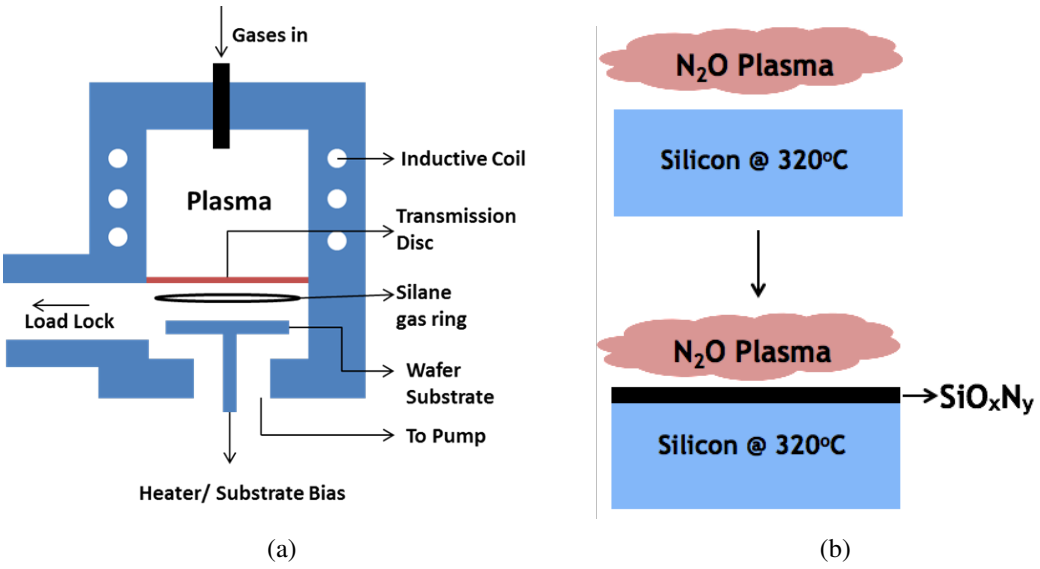
By lowering the growth temperature of SiO_2 films, SiO_2 - SiN_x:H stack can become a potent technology for passivating the front and rear surface of c - Si solar cells. It is in this light that low temperature oxide growth processes like wet chemical oxidation and plasma oxidation assumes significance. By tailoring the process conditions, high quality oxides may be grown, which when capped with SiN_x:H can result in better surface passivation. This chapter discusses the process development of a plasma oxidation process for potential surface passivation of n - type Si surfaces.The chapter starts of with a discussion on the impact of different plasma ambient on the surface passivation quality of plasma grown films. The surface passivation quality was investigated after capping the films with SiN_x:H films. This is followed by a detailed investigation on the surface passivation properties of films grown in N_2O plasma ambient. The final part of the chapter assesses the impact of NH_3 addition on the plasma oxidation process. The chapter concludes with a short discussion on the potential trapping of interstitial oxygen within silicon during the low temperature plasma oxidation process.

5.2 Impact of plasma ambient on surface passivation quality of plasma grown films

This section explores the plasma oxidation process in O_2 and N_2O plasma ambient. The surface passivation quality of the respective plasma grown films are evaluated after capping them with a SiN_y:H film. FTIR measurements are used to study the chemical composition of the films grown

in different plasma ambients. Plasma analysis using OES was used to compare the intensity of oxygen radicals present in different plasma ambients. For films grown in O_2 plasma, addition of argon is reported to improve the interface, and enhance the oxidation rate [82], while addition of nitrogen (N_2) is known to result in lower defect density [127]. In this light, the plasma oxidation process in Ar + O_2 and N_2 + O_2 ambients are also discussed in this section. The surface passivation quality of the respective plasma grown films are also evaluated after capping them with a SiN_y:H film.

5.2.1 Experiment details



(a) (b)

Fig. 5.2: (a) Schematic of ICP system used for experiments (b) Schematic of plasma oxidation process.

P-type, Cz <100> Si wafers with resistivity of 4 - 7 Ω cm was used as the starting material for the experiment. The wafers were subjected to 2% HF last, Radio Corporation of America (RCA) cleaning procedure. An inductively coupled plasma chamber was used for growing the plasma oxides under the following conditions: temperature of 320^{o}C, pressure of 25 mTorr, oxygen flow of 50 sccm and ICP power of 1000 W. The substrate power was kept at 5 W. Growth was carried out for 10 mins. Argon and nitrogen with a flow rate of 50 sccm was optionally introduced to the chamber to assess the impact of these gases on the plasma oxidation process. For the nitrous oxide based experiments, all process conditions were kept identical, but N_2O at a flow rate of 50 sccm was used for generating the plasma. The plasma characteristics for different plasma ambients were studied using an optical emission spectroscope, and the

chemical composition of the thin oxide films was studied using FTIR measurements carried out in transmission mode. 75 nm thick SiN_x:H film deposited using an ICP - CVD process was used for capping the thin plasma grown oxide films. The interface trap density and fixed charge density of the thin oxide films and stacks were studied using MOS capacitors fabricated on p-type Si substrates. Aluminium was used as the top and bottom contact. Lifetime measurements were carried out on n-type FZ wafers with 1 Ω cm resistivity, and 300 μm thickness. The thermal stability of the surface passivation was studied by measuring the effective lifetime after annealing the samples in a rapid thermal annealing chamber in N_2 ambient, for 2 s.

5.2.2 Plasma characterisation using optical emission spectroscopy

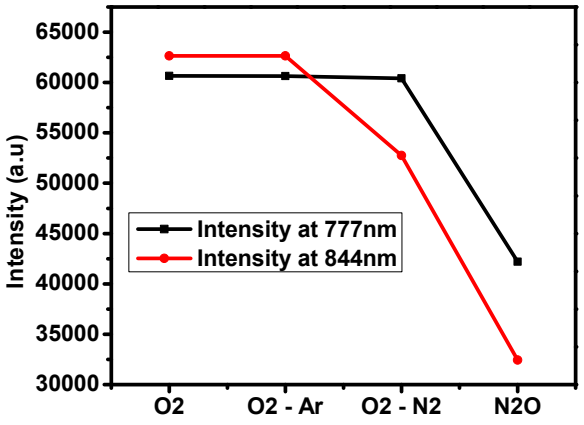


Fig. 5.3: Comparison of oxygen line intensities for different plasma ambient, showing a lower atomic oxygen content for N_2O plasma.

Fig. 5.3 compares the OES intensity for the various gas combinations, with nitrous oxide showing minimum intensity and oxygen showing the maximum intensity. OES for an oxygen plasma exhibited two distinct atomic lines at 777 nm and 844 nm corresponding to the atomic transitions $3p^5P$ - $3s^5S$ and $3p^3P$ - $3s^3S$ respectively [128], and is shown in Fig. 5.4. When Ar was introduced into the process chamber along with oxygen, the intensity of the oxygen related peaks remained almost the same, though additional lines corresponding to argon species could be seen. However, on introducing nitrogen, the intensity of 844 nm spectral line decreases. The intensity of the oxygen related spectral lines are seen to be the lowest for N_2O plasma, as shown in Fig. 5.3. The larger atomic oxygen content in the plasma can lead to larger incorporation of interstitial oxygen within the silicon [85] .

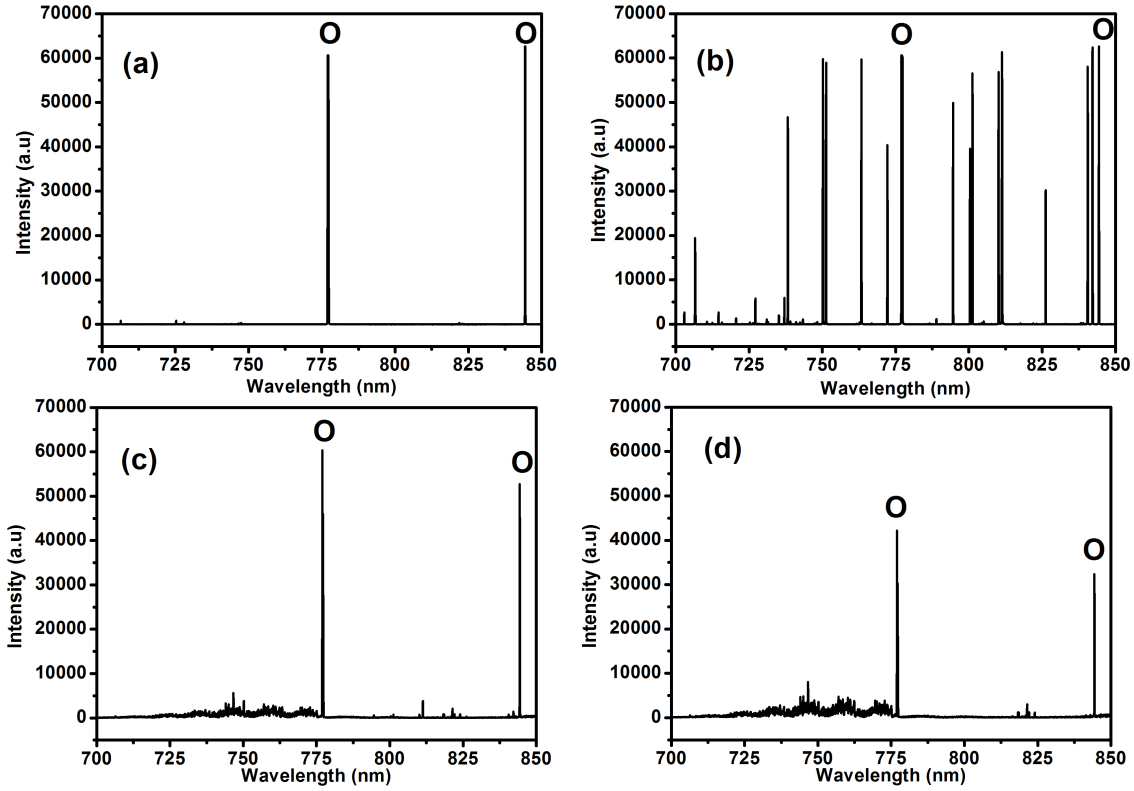


Fig. 5.4: Optical emission spectra for various plasma ambient (a) O_2 (b) Ar + O_2 (c) N_2 + O_2 (d) N_2O.

5.2.3 Physical characterisation of plasma grown films

FTIR data for films grown in different plasma ambients are shown in Fig. 5.5. The trough at 1106 cm^{-1} corresponds to interstitial oxygen trapped within silicon. On addition of argon or nitrogen, a sharp trough was found at 1060 cm^{-1}, which corresponds to Si - O - Si stretching mode vibrations. For the samples grown in oxygen ambient, a prominent peak at 510 cm^{-1} can also be seen, which corresponds to SiO_4 bending mode vibrations [86]. Upon adding argon, the concentration of SiO_4 bonds comes down, while a trough indicating Si - Si unsaturated bonds at 615 cm^{-1} is seen to emerge [129]. This signature observed for the Ar + O_2 sample maybe due to the enhanced oxidation making these vibrations more easier [14, 129]. For samples grown in O_2 + N_2 ambient, the trough at 510 cm^{-1} is absent, while a deeper trough at 610 cm^{-1} is observed. However for samples grown in N_2O ambient, there are no troughs seen at 510 cm^{-1} or 615 cm^{-1}. However for films grown in N_2 + O_2 and Ar + O_2 ambient, a sharp peak is seen in place of a trough. The reason for this anomaly is not clearly understood.

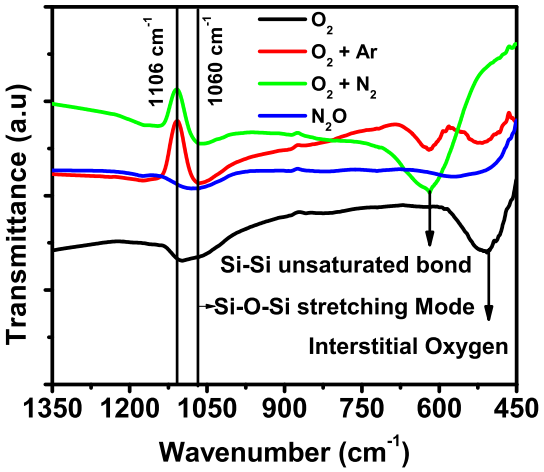


Fig. 5.5: FTIR spectrum for plasma grown films in different ambient.

5.2.4 Lifetime and capacitance - voltage measurements

The interface properties at the silicon - dielectric interface was probed using MIS capacitors. Interface state density was calculated using single frequency approximation method [118], while the fixed charge density was computed from the shift in mid-gap voltage from its ideal value [117]. For the as grown samples, it was observed that the D_{it} was in excess of 10^{12} $eV^{-1}cm^{-2}$. In order to improve the passivation, a SiN_x:H film was deposited on the as-grown plasma oxide films. HFCV measurements on the stack revealed D_{it} in the range of 5 - 7x10^{11} $eV^{-1}cm^{-2}$ for samples grown in O_2, O_2 + N_2 and O_2 + Ar ambient. For samples grown in N_2O ambient, the D_{it} was found to be 1.6x10^{11} eV^{-1} cm^{-2}. However, the Q_{ox} varied from 1.8 - 3x10^{12} cm^{-2}, as can be seen in Fig. 5.6.

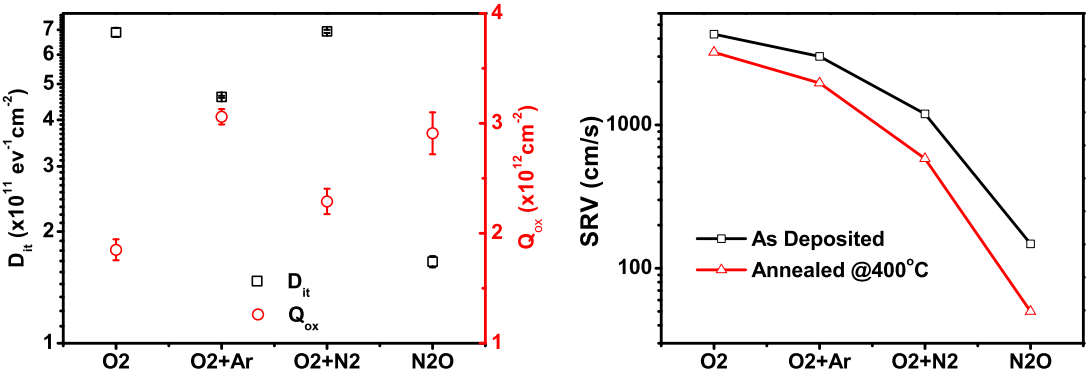


Fig. 5.6: Electrical Characteristics of film grown in different ambient.

SRV was calculated from the measured effective lifetime, assuming infinite bulk lifetime,

at a minority carrier density of 10^{15} cm^{-3}. It was seen that the films grown in O_2, O_2 + Ar, O_2 + N_2 ambient had SRVs $>$ 1000 cm/s as shown in Fig. 5.6. On annealing the samples at 400^{o}C, passivation was seen to improve, with the sample grown in O_2 + N_2 ambient showing a SRV of 582 cm/s. However for samples grown in N_2O ambient, the SRV was found to be 148 cm/s which came down to 50 cm/s upon annealing at 400^{o}C in N_2 ambient, indicating a well passivated surface. It is speculated that the higher SRV for films grown in O_2 based plasma ambients maybe due to the role played by interstitial oxygen trapped during the plasma oxidation process, as was seen from the FTIR data. Plasma oxidation in O_2 ambient is also reported to result in higher plasma damage as compared to oxidation in N_2O ambient [78]. This higher plasma damage along with the larger interstitial oxygen may have resulted in poorer passivation quality for the O_2 based plasma grown oxide films. The improvement in passivation upon annealing can be attributed to the diffusion of hydrogen from the bulk of SiN_x:H towards the interface. The firing stability of the film was investigated by annealing the stacks to 800^{o}C,

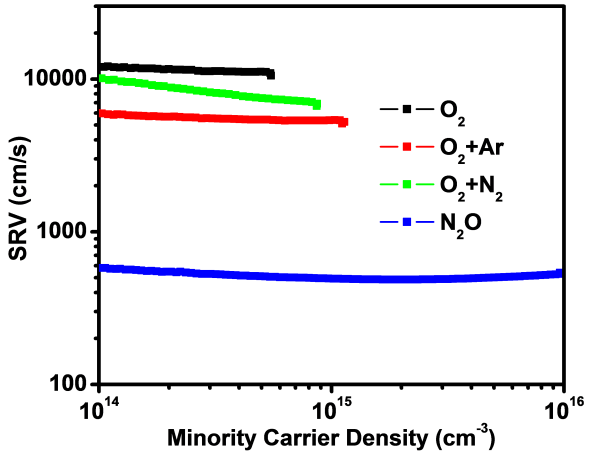


Fig. 5.7: SRV variation across samples after firing the stacks at 800^{o}C.

as can be appreciated by comparing Fig. 5.6 and Fig. 5.7. It was observed that the passivation quality degraded significantly for all films grown in oxygen ambient. However, the film grown in nitrous oxide exhibited a much better passivation as compared to the films grown in oxygen ambient even after firing at 800^{o}C. The degradation in lifetime upon high temperature firing can also be the result of a degradation in bulk lifetime brought about by oxygen diffusion into the bulk of the silicon wafer.

5.2.5 Conclusion

In the previous section, plasma oxidation process was discussed as a promising route towards growing low temperature SiO_x films for passivation of silicon surfaces. Of the different plasma ambients investigated in this section, N_2O was found to result in better surface passivation compared to its oxygen based counterparts. Chemical composition studies using FTIR revealed an increased amount of interstitial oxygen and unsaturated Si - Si bonds for films grown in oxygen ambient. The atomic oxygen present in the plasma is also seen to be playing a major role in determining the amount of interstitial oxygen in silicon. The poor quality of surface passivation observed for films grown in O_2 based ambient maybe due to a combined effect of higher plasma damage and trapping of larger interstitial oxygen content during plasma oxidation process [85]. A detailed discussion on the role of interstitial oxygen and its impact of surface passivation quality is provided in chapter 6.

5.3 N_2O plasma oxidation for silicon surface passivation

In the previous section, it was seen that carrying out plasma oxidation in a nitrous oxide ambient resulted in better surface passivation quality as compared to oxygen based plasma ambients. Oxidation in nitrous oxide ambient is known to result in lower amount of plasma damage on silicon surface as compared to plasma oxidation carried out in oxygen based plasma ambient. This combined with the lower amount of interstitial oxygen may have resulted in lower SRV for the films grown in N_2O plasma ambient. This section investigates the plasma oxidation process in N_2O ambient in detail. A detailed investigation on the chemical as well as surface passivation characteristics of the plasma grown films is discussed in this section.

5.3.1 Experiment details

RCA cleaned, p-type, Cz <100> Si wafers with resistivity of 4 - 7 Ω cm was chosen as the substrate for the experiments. An inductively coupled plasma chamber (ICP - CVD, plasma lab system 100, Oxford instruments) was used for growing the plasma oxides at an ICP power of 1000 W and temperature of 320^oC. Chamber pressures of 4 mTorr and 25 mTorr was used in the experiments. The substrate power was kept at 5 W. N_2O flow rate was varied from 20 to 50 sccm. Chemical composition of the as grown silicon oxy-nitride films were investigated using

FTIR and XPS measurements. Silicon nitride (SiN_y:H) film deposited using a silane (SiH_4) - nitrogen (N_2) mixture in an ICP - CVD was used as a capping layer [123]. The interface state density and the fixed oxide charges were studied by using MIS capacitors fabricated on p-type silicon wafers, with aluminium as the front and back contacts. Carrier lifetime studies were carried out on n-type FZ wafers with a resistivity of 1 Ω cm and a thickness of 300 μm using a WCT lifetime tester from Sinton instruments. Annealing of the samples was carried out in N_2 ambient using a rapid thermal processing system at different temperatures.

5.3.2 Physical characterisation of plasma grown film

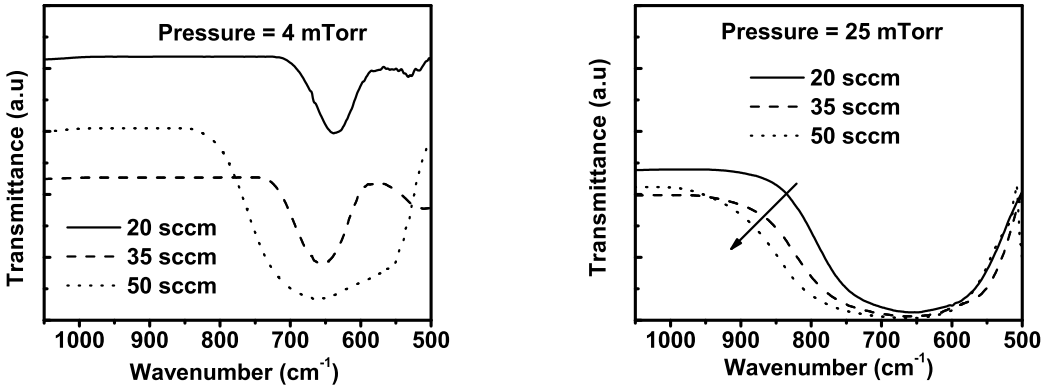


Fig. 5.8: FTIR spectrum at two different chamber pressures (a) 4 mTorr (b) 25 mTorr showing the variation in film composition with change in N_2O gas flow rates.

The impact of gas flow rates and chamber pressure on the chemical composition of the film were investigated using FTIR measurements in transmission mode. As can be seen from Fig. 5.8, in samples grown at 4 mTorr pressure a trough is seen at 640 cm^{-1} - 656 cm^{-1}, which was mainly contributed by the Si - Si dangling bonds (oxygen vacancies), which has a theoretical peak at 610 cm^{-1} [77]. However, for the 50 sccm sample, the trough was broader, and it can be attributed to an increased amount of Si - Si dangling bonds (oxygen vacancies), and Si - O bending mode vibrations. As the process pressure was increased to 25 mTorr, it can be seen from Fig. 5.8 that the troughs are broad for all gas flows, and the tail of the trough shifts slightly to higher wavenumber with an increase in the gas flow from 20 sccm to 50 sccm as indicated by the arrow in Fig. 5.8. This incremental increase in the trough width may arise from an increased amount of Si-N-O-Si bridges [77]. It is reported that the presence of Si - N -

O - Si reduces the density of strained bonds, and lowers the Si dangling bonds at the interface [77]. Hence it was confirmed from FTIR measurements, that a N_2O flow rate of 50 sccm and a chamber pressure of 25 mTorr was an optimum choice for growing the films.

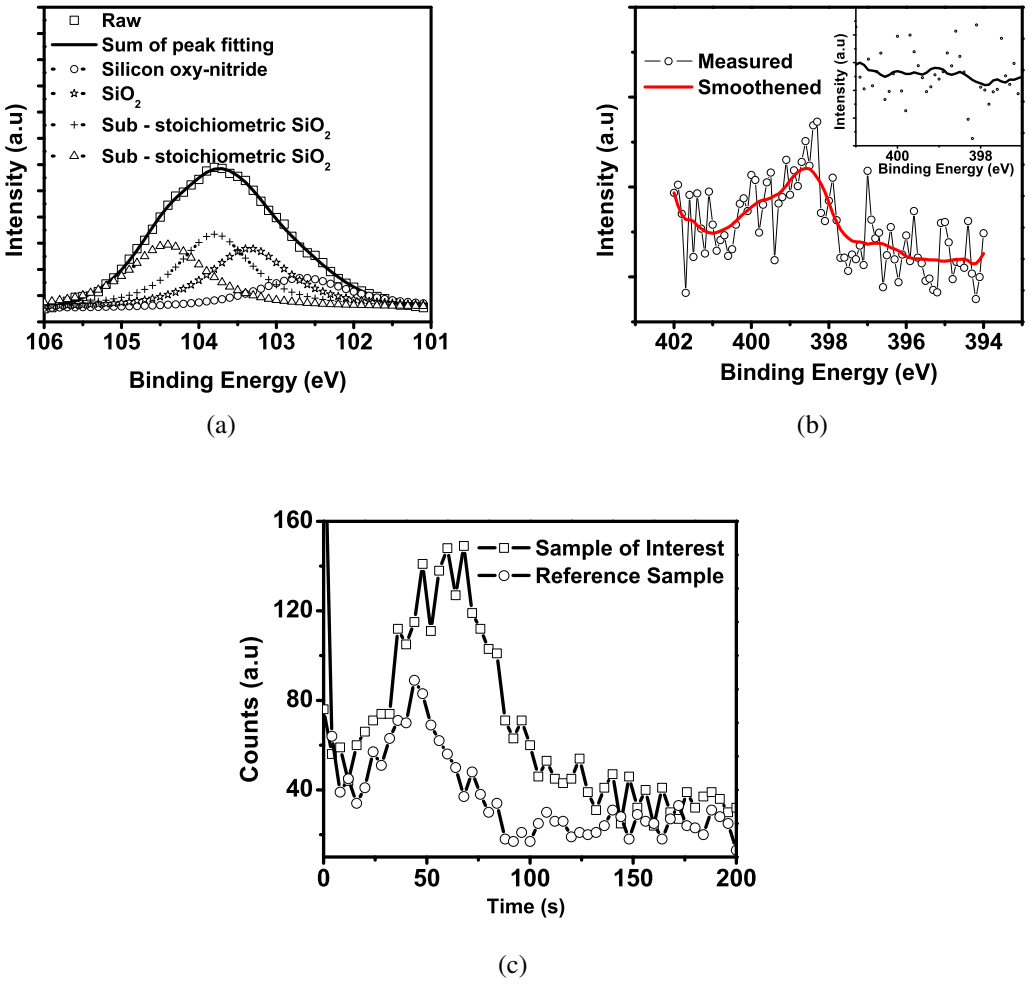


Fig. 5.9: Physical characterisation of the plasma grown film (a) Si2p XPS spectrum showing different oxide phases as well as oxy-nitride phase (b) N1s XPS spectrum showing raw and smoothed data, inset shows N1s spectrum for a film without nitrogen (c) SIMS profile showing nitrogen counts for plasma grown film.

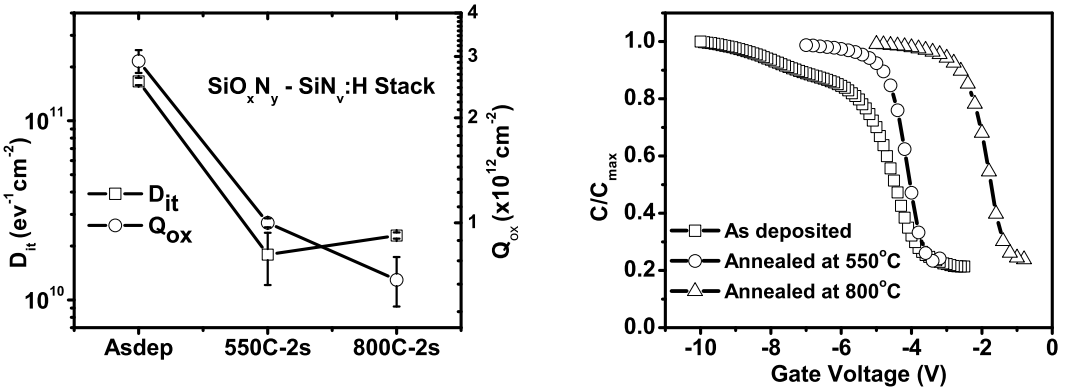
For films used for the surface passivation studies, the substrate power was lowered to 5 W to reduce the energy of ions moving from the plasma towards the wafer surface. Fig. 5.9(a) shows the deconvoluted Si2p XPS spectrum for the plasma grown film. As indicated in Fig. 5.9(a), four different peaks can be seen for the film grown at 25 mTorr, with a N_2O flow of 50 sccm. The peak at 102.66 eV corresponds to the oxy-nitride phase, SiO_2N_2 [124], while the peak at 103.35 eV corresponds to stoichiometric SiO_2, and peaks at 103.8 eV and 104.4 eV corresponds to sub-stoichiometric phases of SiO_2 [124]. Presence of nitrogen in the grown film is confirmed by the

smoothened N1s XPS spectrum, as seen in Fig. 5.9(b). N1s spectrum was smoothened using Savitzky - Golay filtering and 10 point adjacent averaging technique [125]. Inset of Fig. 5.9(b) shows the N1s XPS spectra for a film with no nitrogen incorporation for comparison. An ultra thin SiO_2 film grown in a RTP chamber at 1000^oC in O_2 ambient was used for this purpose. This confirms that the film grown in N_2O ambient with a substrate power of 5 W is an oxy-nitride and not an oxide.The presence of nitrogen in the plasma grown film was further confirmed by means of TOF - SIMS analysis. TOF - SIMS was carried out on the film grown at 5 W substrate power and 0 W substrate power. There was a clear difference in the nitrogen profile for both the cases, indicating the presence of nitrogen for the film grown using 5 W substrate power, which is labelled as sample of interest in Fig. 5.9(c). The sample grown at 0 W substrate power is considered as the reference sample.

5.3.3 Lifetime and capacitance - voltage measurements

High frequency capacitance and conductance as a function of gate voltage (HFCV and HFGV) were measured at 100 KHz on the silicon oxy-nitride films developed using a N_2O flow of 50 sccm. The mid-gap interface state density (D_{it}) was extracted from the conductance plot, using the single frequency approximation method [118]. The fixed charge density (Q_f) was calculated from the shift in the mid-gap voltage from the theoretical value [117]. For plasma grown silicon oxy-nitride films, D_{it} was found to be high in the order of 10^{12} $eV^{-1}cm^{-2}$, and was almost two orders of magnitude higher as compared to thermally grown dry oxides. In order to improve the interface properties, the silicon oxy-nitride film was capped with a 70 nm thick silicon nitride film deposited at 320^oC and a process pressure of 20 mTorr. On capping it with a silicon nitride film, D_{it} came down to $\sim 10^{11}eV^{-1}cm^{-2}$ for the silicon oxy-nitride film grown at 25 mTorr, as shown in Fig. 5.10(a). The sharp decrease in interface state density may be due to the passivation of the interface by hydrogen diffusing to the interface, during silicon nitride deposition.

In order to understand the role of annealing on the interface properties, the stack was annealed at two different temperatures of 550^oC and 800^oC for 2 s in N_2 ambient. Upon annealing the silicon oxy-nitride - silicon nitride (SiO_xN_y - SiN_v:H) stack at 550^oC, the mid-gap D_{it} came down further by an order of magnitude to 1.8 x 10^{10} $eV^{-1}cm^{-2}$ with a positive fixed charge density of 1 x 10^{12} cm^{-2}. This D_{it} value is comparable to the D_{it} values ($\sim 10^{10}$ $eV^{-1}cm^{-2}$) reported for thermally grown dry SiO_2 films. On annealing the SiO_xN_y - SiN_v:H stack at 800^oC,

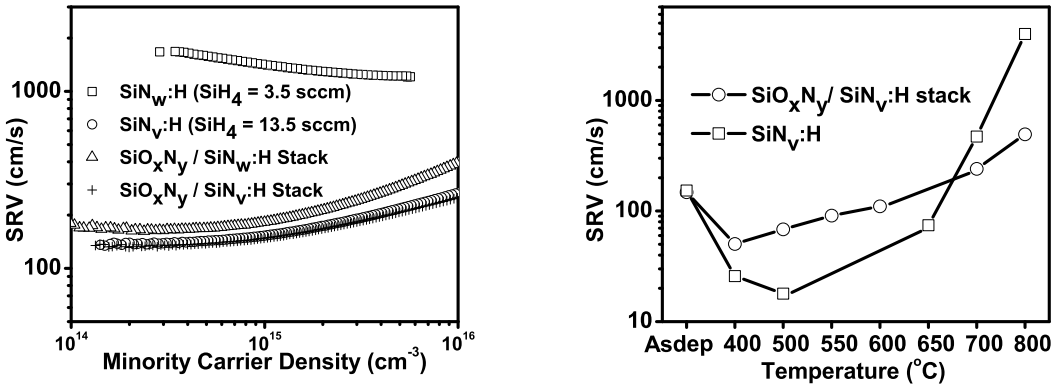


(a)

(b) HFCV curve of the stack for various anneal temperatures.

Fig. 5.10: HFCV Analysis of silicon oxy-nitride - silicon nitride stack at different annealing temperatures (a) Variation in D_{it} and Q_f for the stack and (b) respective HFCV curves.

the mid-gap D_{it} increased marginally to 2.3 x 10^{10} $eV^{-1}cm^{-2}$, with a substantial decrease in the positive fixed charge density to 6.8 x $10^{11}cm^{-2}$, as seen in Fig. 3.2(b). As can be seen in Fig. 5.10(b), the decrease in D_{it} is manifested as a decrease in the stretch out in HFCV for the samples annealed at 550^{o}C and 800^{o}C. The decrease in positive fixed charge for the sample annealed at 800^{o}C is manifested as a right shift in HFCV, as seen in Fig. 5.10(b). The improvement in interface properties upon annealing could be due to the migration of hydrogen atoms from the silicon nitride film towards the interface.



(a)

(b)

Fig. 5.11: (a) SRV for various silicon nitride layers and corresponding stacks (b) Thermal stability of stack compared with silicon nitride.

The surface passivation quality of the stack was investigated by measuring effective minor-

ity carrier lifetime. The SiO_xN_y - SiN_v:H stack provides only a marginal improvement in the lifetime compared to SiN_v:H passivation in the as deposited form. However it was seen that a reduction in the hydrogen content in the nitride (SiN_w:H), obtained by lowering the SiH_4 flow rate to 3.5 sccm, resulted in significant difference between the nitride only passivation and passivation by the silicon oxy-nitride - silicon nitride stack. Further it was seen that the passivation quality of the stack had a weak dependence on the hydrogen content of the capping silicon nitride film. The comparison between SiO_xN_y - SiN_v:H and SiO_xN_y - SiN_w:H in Fig. 5.11(a) points to the role of an interfacial silicon oxide - oxy-nitride layer in eliminating the need for a thorough optimisation of the capping silicon nitride. Similar observation was made by Schmidt et al. [51] for stacks of SiO_2 - SiN films as well as by Bordihn et al. [126] for stacks of SiO_2 - Al_2O_3 films [126]. The thermal stability of the SiO_xN_y - SiN_v:H stack was further investigated and it was compared with that of SiN_v:H.

Thermal stability study of the SiO_xN_y - SiN_v:H stack showed a minimum SRV of 50 cm/s after annealing at 400^oC, see Fig. 5.11(b). The SRV degraded to 493 cm/s after annealing at 800^oC, a typical contact firing temperature for screen printed solar cell fabrication. SiO_xN_y - SiN_v:H exhibited much higher thermal stability as compared to a single layer SiN_v:H film, as shown in Fig. 5.11(b). A similar improvement in thermal stability of SiN layer was reported on rapid thermal oxide/conventional furnace oxide + PECVD SiN stacks [66]. The SRV reported here, though higher, was obtained for a film grown at a lower thermal budget (320^oC versus 900^oC). The degradation in surface passivation upon the increase in anneal temperature is due to the marginal increase in D_{it} (degradation of chemical passivation) and decrease in Q_f (degradation of field effect passivation). The degradation in passivation quality may be attributed to an out diffusion of hydrogen from the interface [122].

5.3.4 Conclusion

In this section, a detailed investigation on the surface passivation properties of a stack of plasma grown SiO_xN_y - SiN_v:H film was discussed. Detailed physical characterisation using XPS and TOF - SIMS confirmed that the film grown in N_2O ambient is a silicon oxy-nitride and not an oxide due to the presence of nitrogen within the film. Upon capping the SiO_xN_y film with SiN_v:H, very low interface state density in the order of 10^{10} $eV^{-1}cm^{-2}$ was obtained after annealing. The stack exhibited a minimum surface recombination velocity of 50 cm/s upon annealing at 400^oC, and the thermal stability at higher temperature (800^oC) was much superior

when compared to that of a single layer silicon nitride film. This result is in line with what was previously reported by Narasimha et al. [66], where a similar behaviour was observed when a thin thermally grown silicon oxide film was capped with silicon nitride film [66]. It was also found that a thorough optimisation of the capping silicon nitride layer could be avoided when a thin plasma grown oxide was grown prior to the silicon nitride deposition. This maybe the outcome of the fact that the interface properties are governed by the plasma grown SiO_xN_y layer than the silicon nitride layer. This result is similar to what was previously observed by various groups [51, 68, 126].

5.4 Can addition of ammonia during plasma oxidation result in an improvement in surface passivation?

It is reported that using an ammonia plasma treatment prior to silicon nitride deposition leads to interface state density in the order of 10^{10} $eV^{-1}cm^{-2}$ [131]. This improvement in interface properties was attributed to a nitridation of the interface prior to silicon nitride deposition. On the other hand, room temperature ammonia plasma exposure on thermally grown SiO_2 - Si interface was also reported to result in increased interface state density and surface charges [130]. Further, an ammonia plasma could contain atomic hydrogen which may potentially improve the surface passivation. In order to investigate these aspects, an experiment was carried out, to study the effect of ammonia addition during the plasma oxidation process in N_2O ambient. The variation in plasma characteristics, chemical composition and electrical properties of silicon oxy-nitride films grown in N_2O + NH_3 ambient is investigated. The surface passivation properties of the film is also investigated after capping it with a hydrogenated silicon nitride film (SiN_y:H). The thermal evolution of the surface passivation is also discussed in this section.

5.4.1 Experiment details

The plasma exposure was done on p-type <100> Cz wafers, with 4 - 7 Ω cm resistivity. The exposure was done in two different ambients (a) Nitrous oxide (N_2O) (b) mixture of N_2O + NH_3. Two different substrate powers of 10 W and 0 W were tried out during the experiments. The reactant species present in the plasma was analysed using an OES, and thickness of the films was measured using a spectroscopic ellipsometer. Angle resolved XPS (ARXPS) mea-

surements were carried out to investigate the nitrogen incorporation into films grown in both N_2O and N_2O + NH_3 ambients. In order to study the electrical properties of the films, HFCV measurements were carried out on MIS capacitors. MIS capacitors were fabricated after capping the plasma grown film with hydrogenated silicon nitride film deposited using an ICP - CVD system. Aluminium was used as the gate metal for the MIS capacitors. MIS capacitors were fabricated for films before and after annealing in nitrogen ambient at 400^oC for 2 s. HFCV analysis was carried out and D_{it} was extracted using single frequency approximation method [118], while the fixed charge density was extracted by calculating the shift in mid - gap voltage from its ideal value [117]. Photo conductance decay measurements were carried out on 3 Ω cm n-type FZ wafers, using a Sinton WCT lifetime tester. These measurements were done after depositing the stacks on both sides of the FZ wafer. The thermal evolution of the surface passivation was evaluated by annealing the stacks in a rapid thermal annealing chamber in nitrogen ambient, for 2 s each.

5.4.2 Plasma characterisation using optical emission spectroscopy

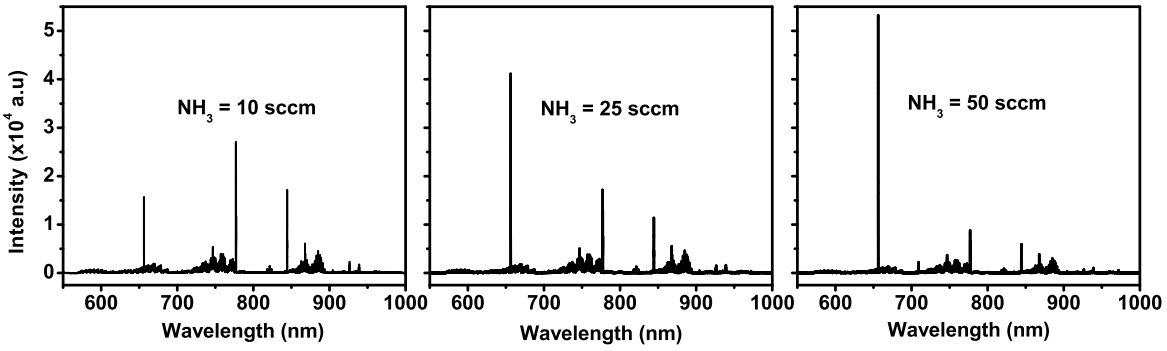
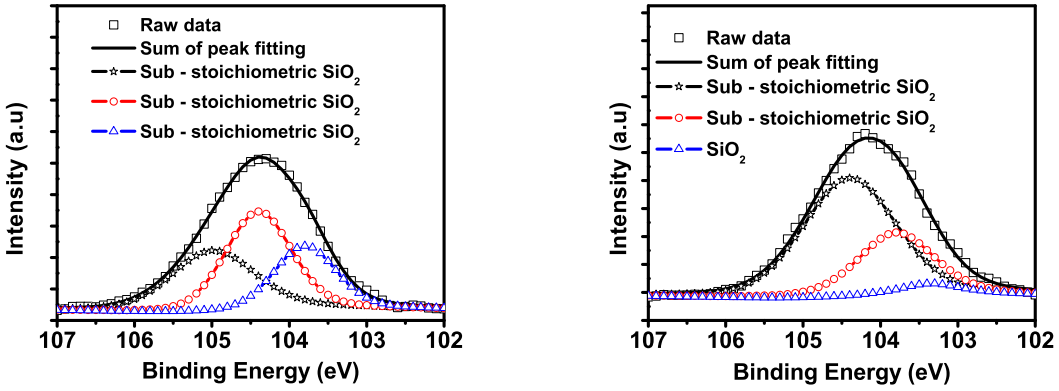


Fig. 5.12: Optical emission characteristics of N_2O + NH_3 plasma for varying ammonia flow rates.

The emission lines for N_2O + NH_3 plasma generated with a RF power of 1000 W, and with a substrate power of 10 W, are shown in Fig. 5.12. The N_2O flow rate was kept constant at 50 sccm, while the ammonia flow rate was varied from 10 sccm to 50 sccm. The excited states of oxygen in plasma are mostly comprised of atomic transitions from $3p^5P$ to $3s^5S$ resulting in an emission line at 777 nm. The atomic transition from $3p^3P$ to $3s^3S$ results in another emission line at 844 nm [128]. As was seen in Fig. 5.4(d), nitrous oxide plasma comprises of excited oxygen states resulting in strong emissions at 777 nm and 844 nm. Upon adding ammonia into the chamber, the intensity of oxygen emission comes down, and a strong peak corresponding

to the hydrogen emission line at 656 nm is visible as can be seen in Fig. 5.12. Similar optical emission spectrographs were obtained for films grown at lower substrate power. However, as the substrate power was decreased, the thickness of the as grown film decreased. It was observed that as the intensity of the oxygen emission lines came down for higher ammonia flow rates, the thickness of the film grown in the $N_2O + NH_3$ plasma ambient also came down from 5 nm (for 10 sccm of NH_3) to 4.4 nm (for 50 sccm of NH_3).

5.4.3 Physical characterisation of plasma grown films

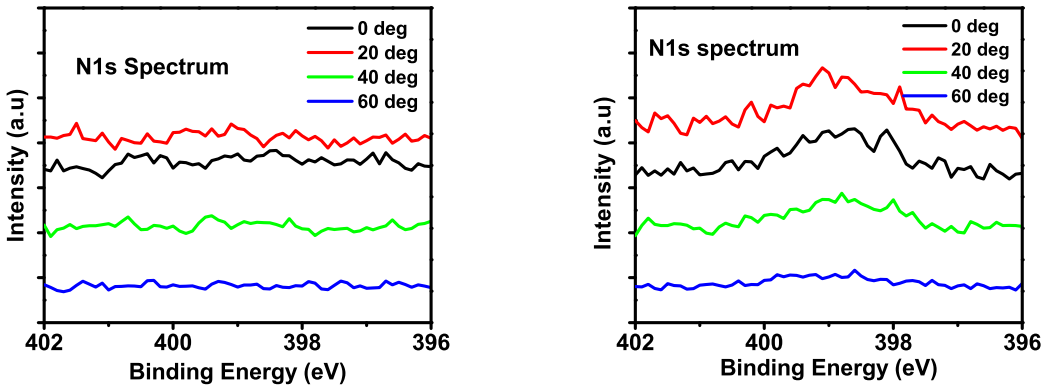


(a) (b)

Fig. 5.13: Si2p XPS spectrum for films grown in (a) N_2O and (b) $N_2O + NH_3$ ambient. A large amount of sub - stoichiometric phases of silicon oxide can be seen for both the films.

In order to understand how the physical composition of the plasma grown film changes with ammonia exposure, X-ray photoelectron spectroscopy was carried out on the samples. Fig. 5.13 compares the Si2p spectrum for the sample grown in N_2O and $N_2O + NH_3$ plasma. It is reported that a binding energy of 103.3 eV corresponds to SiO_2 peak while a binding energy of 102 eV corresponds to Si_3N_4 [124]. The binding energies between these values are reported to represent silicon oxy - nitride phases. The Si2p spectrum for $N_2O + NH_3$ ambient had a broader peak, indicating significant presence of nitrogen within the film. A higher intensity for the O1s spectrum was observed for film grown in N_2O plasma indicating a film with higher oxygen content. Upon de-convolution of Si2p peak for film grown in N_2O ambient, it was observed that the film comprised mainly of sub stoichiometric oxides, with peaks at 105 eV, 104.4 eV, and 103.8 eV. However, for the film grown in $N_2O + NH_3$ ambient, upon de-convolution, peaks indicating sub-stoichiometric oxides at 104.4 eV and 103.8 eV along with a stoichiometric

silicon dioxide peak at 103.3 eV can be seen, as indicated in Fig. 5.13(b).



(a) (b)

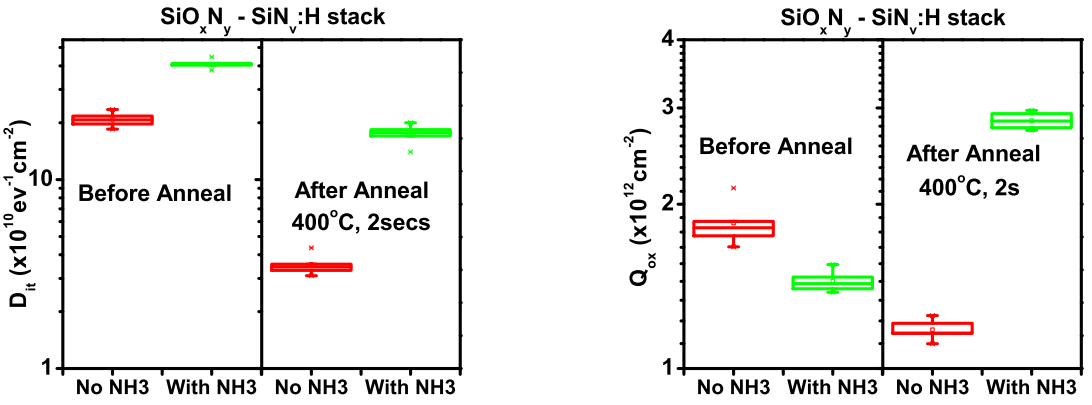
Fig. 5.14: ARXPS N1S spectrum for films grown in (a) N_2O and (b) N_2O + NH_3 ambient. Presence of nitrogen is seen for sample grown in N_2O + NH_3 plasma ambient.

On comparing the N1s spectrum for both the samples, presence of nitrogen was found in case of sample grown in N_2O + NH_3 ambient. Angle resolved XPS was carried out to determine the position of the nitrogen within the as grown film. As can be seen in Fig. 5.14(a), the film grown in N_2O ambient did not result in any nitrogen incorporation, whereas the film grown in N_2O + NH_3 ambient indicated the presence of nitrogen within the film. As can be seen from Fig. 5.14(b), nitrogen was found closer to the interface, as indicated by the takeoff angle observed in the XPS. The absence of nitrogen within the film grown in N_2O ambient contradicts with the previously discussed results in Section 3.3. The difference stems from the lower substrate power used in this experiment. A lower substrate power was chosen to eliminate any potential nitrogen pile up in the film grown in N_2O ambient. Thus by tailoring the substrate power, or by adding ammonia to the process chamber during the plasma oxidation process, thin silicon oxy-nitride films can be grown at low temperatures in an inductively coupled plasma chamber. The impact of the nitrogen pile up on the interface properties was investigated by fabricating MIS capacitors and symmetric test structures for lifetime measurements.

5.4.4 Lifetime and capacitance - voltage measurements

The electrical characteristics of the as grown plasma oxide/oxy-nitride films were studied by fabricating MIS capacitors with aluminium as the gate metal. For the plasma grown films, an interface state density in the order of 10^{12} $eV^{-1}cm^{-2}$ was observed, irrespective of the ambient

used for the growth. However, it was observed that the films grown in N_2O ambient had a lower D_{it}, and higher Q_{ox} value as compared to films grown in N_2O + NH_3 ambient. The interface properties were further investigated by means of HFCV and HFGV measurements after capping the plasma grown films with SiN deposited in a ICP - CVD. HFCV and HFGV curves for the stack were measured before and after annealing the stack in nitrogen ambient at 400^{o}C for 2 s. The temperature was chosen as it yielded the highest quality surface passivation in our previous experiments. The results of the HFCV analysis is summarised in Fig. 5.15.

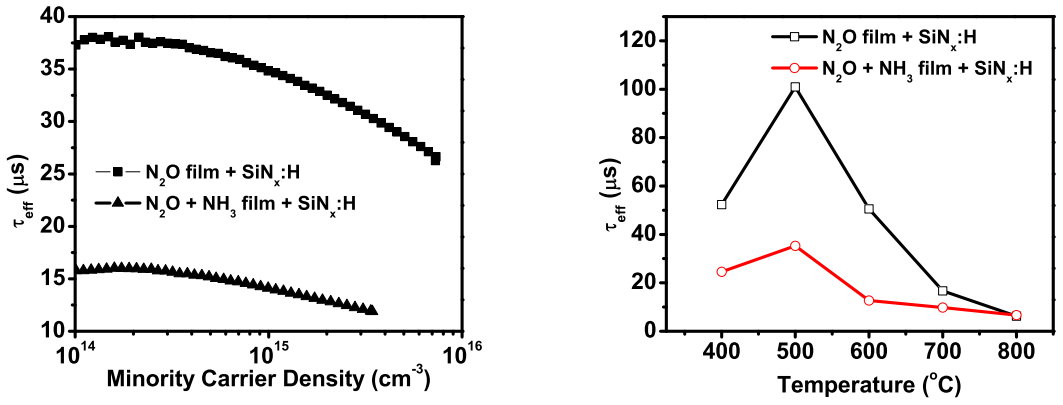


(a) (b)

Fig. 5.15: Variation in (a) D_{it} and (b) Q_f for SiO_xN_y - SiN_v:H stacks before and after annealing at 400^{o}C.

It was observed that for single layer films, the D_{it} remained above 10^{12} $eV^{-1}cm^{-2}$ and upon capping the film with silicon nitride, the interface state density came down by an order of magnitude, and was found to be $\sim$ 2x10^{11} $eV^{-1}cm^{-2}$ for samples grown in N_2O ambient, while it was found to be $\sim$4x10^{11} $eV^{-1}cm^{-2}$ for samples grown in N_2O + NH_3 ambient. However, upon annealing the stacks at 400^{o}C in nitrogen ambient, the D_{it} came down by an order of magnitude to $\sim$ 4x10^{10} $eV^{-1}cm^{-2}$ for the stack based on plasma oxide grown in N_2O ambient. However, for the stack based on N_2O + NH_3 ambient, the D_{it} was found to be $\sim$ 1.7x10^{11} $eV^{-1}cm^{-2}$ after annealing at 400^{o}C in N_2 ambient. It is reported that hydrogen plasma exposure at room temperature can also result in an increased interface state density [132]. As was seen from the optical emission spectrum for N_2O + NH_3 ambient, the atomic hydrogen within the plasma may also have contributed in creating a defective interface. The positive fixed charge density for the stack based on N_2O was found to be $\sim$ 1.8x10^{12} cm^{-2}, while for the stack based on N_2O + NH_3, it was found to be $\sim$ 1.4x10^{12} cm^{-2}.

From the capacitance - voltage studies, it could thus be seen that the film grown in an ambient of N_2O + NH_3 did not result in any improvement in terms of D_{it} before and after annealing. The addition of ammonia rather resulted in an increase in D_{it} at the Si - SiO_xN_y interface. The increase in D_{it} may have resulted from the nitrogen incorporation at the interface. Accumulation of nitrogen atoms at the interface may have resulted in an increased stress at the interface, which may have resulted in generation of larger amount of interface states [132]. The results discussed in this section confirmed that introducing NH_3 during plasma oxidation process resulted in lower growth rate and poorer interface with higher interface state density.



(a) (b)

Fig. 5.16: (a) τ_{eff} for the SiO_xN_y - SiN stack before annealing. Higher τ_{eff} observed for films grown in N_2O plasma ambient (b) Variation in τ_{eff} for SiO_xN_y - SiN stack for different annealing conditions. τ_{eff} was measured on 300 μm thick n-type FZ wafers with a resistivity of 3 Ω cm.

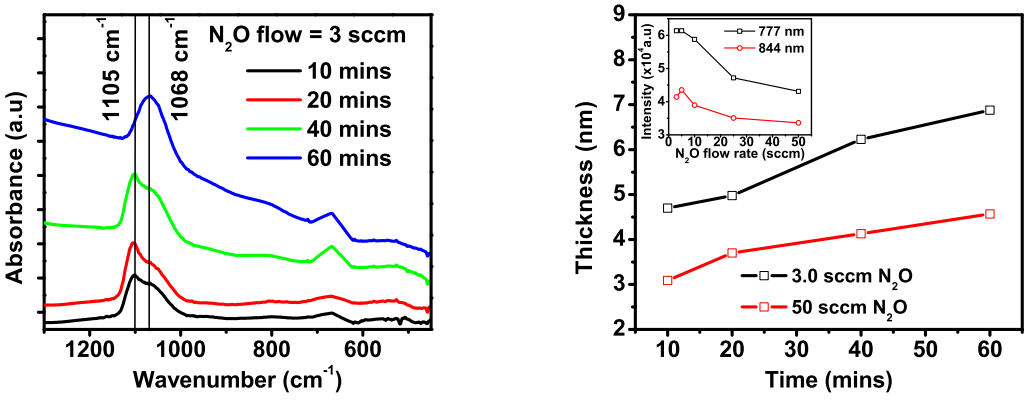
Minority carrier lifetime measurements were carried out on samples grown in N_2O and N_2O + NH_3 ambient on n-type FZ wafers, with a resistivity of 3 Ω cm. The films were capped with SiN film deposited using PECVD, and minority carrier lifetime was measured. The stack was annealed at various temperatures and the thermal stability of the lifetime was also measured. τ_{eff} of 35 μs was obtained for the stack of N_2O plasma grown film and silicon nitride, while for the stack of ammonia based plasma grown film and silicon nitride, it was found to be 14 μs, as shown in Fig. 5.16(a). Upon annealing the films for various temperatures, a maximum lifetime of 100 μs was obtained at 550^{o}C for N_2O based sample, while a maximum of 35 μs was obtained for N_2O + NH_3 sample at 550^{o}C as shown in Fig. 5.16(b). Lower τ_{eff} for samples grown in N_2O + NH_3 ambient may be due to the larger N - concentration at the interface. Similar reduction in τ_{eff} was reported by Yamashita et al. for increasing N - concentration

at the interface [133]. However, as the annealing temperature was increased further to 800^{o}C, both the films attained a minority carrier lifetime of 6 μs. This decrease in lifetime may have resulted from an out diffusion of hydrogen from the interface with annealing. The interstitial oxygen trapped during plasma oxidation may also have played a role in degradation of τ_{eff} after firing at 800^{o}C.

5.4.5 Conclusion

The addition of ammonia during the plasma oxidation process led to a decrease in the growth rate of the film. The hydrogen present in the plasma during the growth process did not play any part in improving the interface quality. However, ammonia plasma exposure led to an accumulation of nitrogen close to the interface, which may have resulted in an increase in interface state density at the Si - SiO_xN_y interface. Lifetime measurements carried out on the samples also confirmed that adding ammonia addition during the plasma oxidation process can be detrimental for the surface passivation quality.

5.5 Trapping of interstitial oxygen within silicon following plasma oxidation in N_2O ambient



(a) (b)

Fig. 5.17: (a) FTIR spectra for films grown in 3 sccm N_2O flow rate showing a decrease in interstitial oxygen at 1105 cm^{-1} for longer oxidation time (b) Ellipsometry data showing thickness versus growth duration for films grown in 3 sccm and 50 sccm N_2O flow. Inset shows the O line intensities measured using OES, higher O line intensity is observed for plasma struck at lower flow rates

Low temperature oxidation of silicon in oxygen plasma ambient is reported to result in oxygen incorporation in the bulk of the silicon [85]. According to Kim et al., the trapped oxygen in silicon is representative of the plasma damage incurred on the wafer during the plasma treatment. For larger thickness of the plasma grown oxide film, a decrease in interstitial oxygen content in silicon was observed [85]. An experiment was carried out in order to ascertain whether the same behaviour is replicated in case of the plasma oxidation process discussed in this thesis. Plasma oxidation was carried out at two different gas flow rates, 3 sccm and 50 sccm for different time durations. Fig. 5.17(a) shows the FTIR spectrum for films grown at 3 sccm N_2O flow rate. As the plasma exposure duration increased from 10 to 60 min (increasing film thickness), the interstitial oxygen peak at 1105 cm^{-1} is seen to come down, whereas, the peak at 1068 cm^{-1} corresponding to Si - O - Si stretching mode vibrations is seen to increase. The thickness of the film was also seen to increase for longer plasma exposure duration, as shown in Fig. 5.17(b). The results presented here are similar to what was previously reported by Kim et al., who had shown a correlation between film thickness and interstitial oxygen content [85]. Inset of Fig. 5.17(b) also shows the atomic O line intensities at 777 nm and 844 nm measured using OES. The atomic O line intensity is seen to come down for higher N_2O flow rates, resulting in lower film thickness, as shown in Fig. 5.17(b).

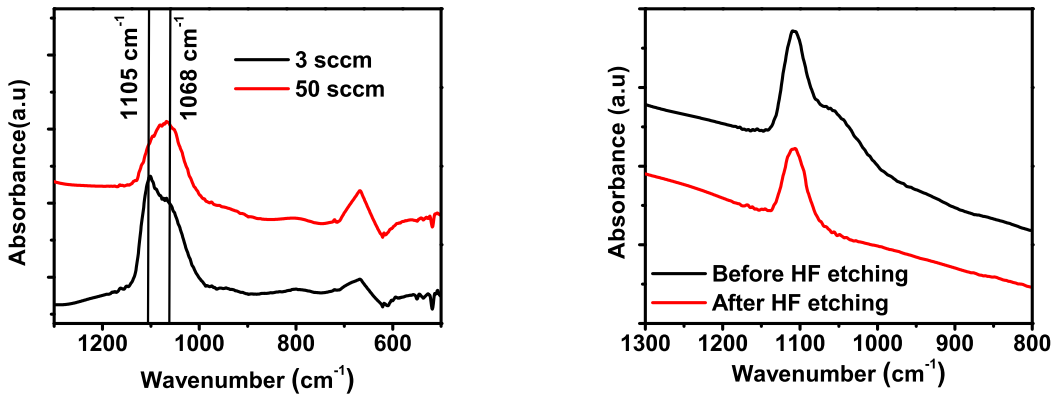


Fig. 5.18: (a) FTIR spectra comparing films grown at 3 sccm and 50 sccm N_2O flow rates. Time of growth was 10 min. Lower interstitial O content is observed for the 50 sccm sample (b) FTIR spectrum measured before and after removing the plasma grown film in 2% HF solution, confirming the trapping of interstitial oxygen within silicon.

From OES spectrum, higher oxygen plasma intensity was observed for 3 sccm plasma compared to 50 sccm plasma, and hence a better oxidation rate. Despite its lower thickness, the film

grown in 50 sccm N_2O plasma showed lower interstitial oxygen content at 1105 cm^{-1} when compared to a film grown in 3 sccm N_2O plasma. This is illustrated in Fig. 5.18(a), This difference in interstitial oxygen content stems from the higher amount of atomic oxygen observed for the 3 sccm N_2O plasma. Similar correlation between atomic oxygen intensity and interstitial oxygen content was also previously reported by Kim et al. [85].

In order to confirm whether the interstitial oxygen was present in the plasma grown film or inside the silicon surface, FTIR measurements were done on a sample before and after 2% HF dip for 60 s. A strong peak at 1105 cm-1 corresponding to interstitial oxygen was observed following the HF dip, as shown in Fig. 5.18(b). From this simple experiment, it was concluded that the interstitial oxygen is trapped within the silicon substrate. The detailed impact of the trapped interstitial oxygen on the surface passivation as well as solar cell performance is discussed in the next chapter.

5.6 Conclusions

In this chapter, the potential of a plasma oxidation for surface passivation of silicon surfaces was investigated. From HFCV and lifetime measurements it was observed that plasma oxidation process carried out in N_2O ambient was more suited for the surface passivation application. Lower interstitial oxygen content and plasma damage were the main reasons for choosing plasma oxidation process as the ambient for the future experiments. Films grown in N_2O plasma ambient was found to have small amount of nitrogen in it confirming it is a silicon oxy-nitride film. On capping the film with silicon nitride and subsequent annealing at 400^oC, SRV of 50 cm/s was obtained. The stack was also seen to exhibit superior thermal stability as compared to its silicon nitride counterpart. Compared to plasma oxidation in N_2O ambient, plasma oxidation in NH_3 + N_2O ambient resulted in significant pile up of nitrogen close to the interface of Si - SiO_xN_y. Pile up of nitrogen at the interface may have resulted in a higher interface state density and thereby resulting in lower effective lifetime. Plasma oxidation in N_2O ambient resulted in trapping of interstitial oxygen within silicon. Interstitial oxygen, representative of the plasma damage, came down for longer plasma exposure duration. Consumption of silicon during the growth of thicker films resulted in lower interstitial oxygen content for thicker plasma grown films.

Having investigated the potential of the N_2O based process for silicon surface passivation,

further efforts were directed towards integrating the plasma oxidation process in silicon solar cells. The process integration included porting of the process from an ICP based remote plasma system to a capacitive coupled direct plasma system. The process details, surface passivation studies and solar cell performance are discussed in detail in the next chapter.

Chapter 6

Plasma oxidation for emitter surface passivation in silicon solar cells

Thermally grown silicon dioxide (SiO_2) film of thickness $\sim$105 nm is used as the front surface passivation layer in case of high efficiency PERL solar cells [9]. Recently, Metal-Insulator-Semiconductor (MIS) architecture based solar cells employing a thin tunnel oxide resulted in a solar cell efficiency of 24.9%. The tunnel oxide replaces the amorphous Si layer used in conventional Heterojunction with Intrinsic Thin layer (HIT) structures, and yielded an improvement in short circuit current and fill factor [134]. However, thermal oxidation process is not industry compatible and hence low temperature oxidation of silicon has evoked interest of the solar cell community [35, 42, 74].

In the previous chapter, feasibility of plasma oxidation process for surface passivation of c - Si surfaces was discussed on test structures. It was seen that on using stacks of SiO_xN_y - SiN_v:H, thermal stability of the SiN_v:H layer improved significantly. This chapter discusses the integration of plasma oxidation process into the silicon solar cell fabrication process flow. First part of the chapter investigates plasma oxidation in N_2O ambient at 380^oC in a PECVD chamber and discusses the role of trapped interstitial oxygen on surface passivation quality and solar cell performance. The chapter also discusses the emitter surface passivation quality of films grown in Ar + N_2O plasma ambient, and benchmarks it efficacy with that of a SiO_x film grown in a furnace at 600^oC. The latter part of the chapter discusses the impact of the silicon nitride deposition conditions on the shunt formation in solar cells, and thereby providing a roadmap for further improvement in solar cell performance.

6.1 Role of interstitial oxygen trapped during plasma oxidation on surface passivation quality

Plasma oxidation of silicon at low temperature resulted in trapping of interstitial oxygen on the top layers of silicon substrate [85]. Atomic oxygen present in plasma ambient contributed to the interstitial oxygen trapped within silicon. As discussed previously in section. 5.5, for increasing oxide thickness, the amount of interstitial oxygen trapped within the silicon was seen to come down. It was suggested that the trapped interstitial oxygen may result in higher leakage current in case of MOS transistors [85]. However, no data correlating the role of interstitial oxygen to electrical performance of the device is available. Trapping of interstitial oxygen in silicon is thus inevitable in case of plasma oxidation in O_2 or N_2O ambient. An improved understanding on the role of interstitial oxygen in determining electrical performance, can result in designing and developing processes for replacing thermally grown SiO_2 films in crystalline silicon solar cells. In this section, role of interstitial oxygen trapped in silicon during plasma oxidation on the quality of surface passivation is investigated. By varying the plasma exposure time, films of different thickness were grown. The impact of plasma grown film thickness on the effective minority carrier lifetime, fixed charge density, interface state density and emitter passivation were investigated after capping the plasma grown films with PECVD silicon nitride film.

6.1.1 Experimental setup

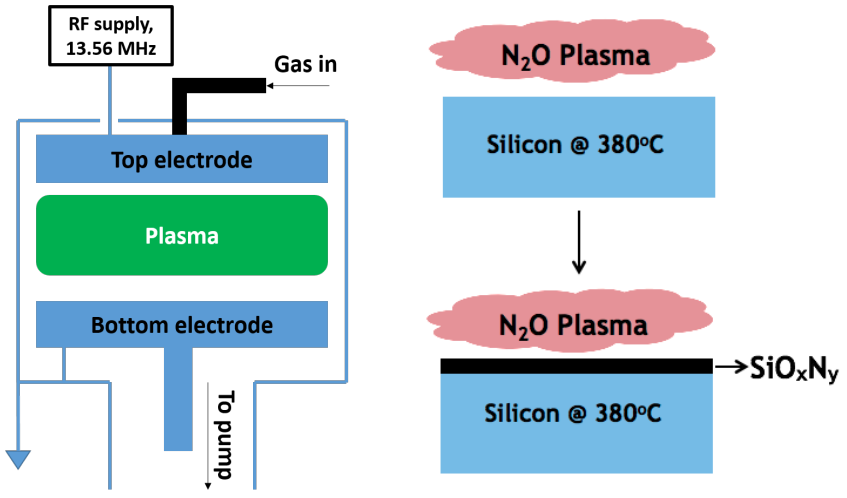


Fig. 6.1: (a) Schematic of PECVD system and (b) plasma oxidation process.

Thin silicon oxy-nitride (SiO_xN_y) films were grown in a capacitive coupled PECVD (Plasmalab 100, Oxford instruments) chamber at 380^{o}C in N_2O ambient.The schematic of the PECVD chamber, and the plasma oxidation process are shown in Fig. 6.1. Films of varying thickness were grown on RCA cleaned, p-type, polished Czochralski (Cz) <100> Si wafers with resistivity of 4 - 7 Ω cm by varying the plasma exposure time as 5, 10, 20 and 40 minutes. For the the growth of SiO_xN_y film, RF power was 10 W, chamber pressure was 1 Torr and N_2O flow rate was 200 sccm. Thickness of the oxynitride was measured using a spectroscopic ellipsometer (SE 800, Sentech Instruments). Film composition was determined using FTIR (Spectra 100, Perkin Elmer) and XPS (PHI5000VersaProbeII, ULVAC - PHI). For lifetime measurements, thin silicon oxy-nitride films were grown on both sides of n-type float zone (FZ) <100> wafer with 1 Ω cm resistivity. Hydrogenated silicon nitride film (SiN_v:H) film of $\sim$ 88 nm with a RI of 1.98, was deposited on SiO_xN_y on both sides of the wafer and minority carrier lifetime was measured using a Sinton WCT 120 lifetime tester. Interface properties of the stack of SiO_xN_y - SiN_v:H was investigated by fabricating Metal - Insulator - Semiconductor (MIS) capacitors on identical n-type FZ wafers. Thermally evaporated aluminium was used as the top and bottom contact. Thermal stability of SiO_xN_y - SiN_v:H stacks were investigated by firing the sample in a Rapid Thermal Annealing (RTA) chamber at 850^{o}C in N_2 + O_2 ambient for 1 s.

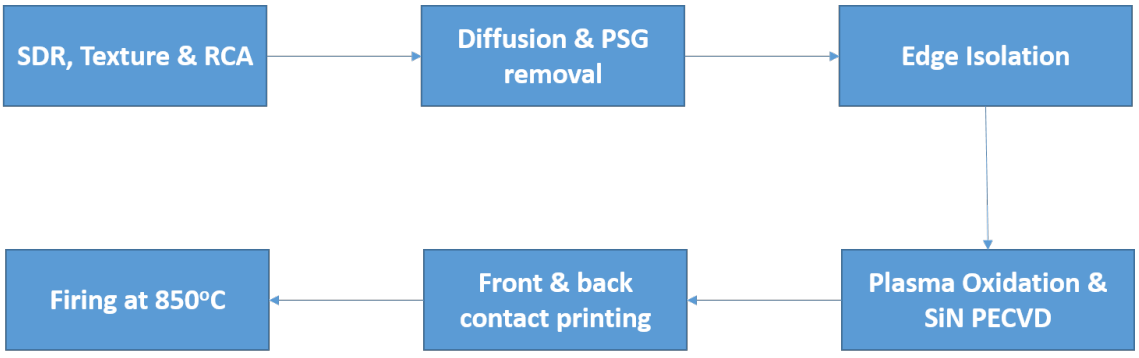
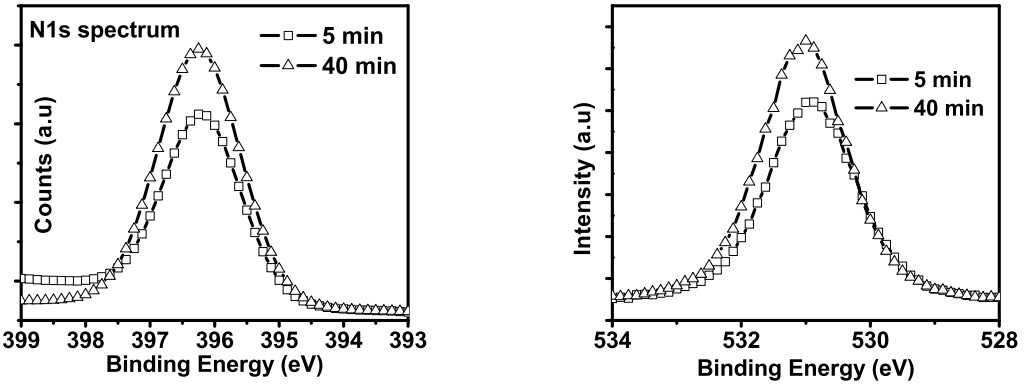


Fig. 6.2: Solar cell process flow.

Crystalline silicon solar cells were fabricated on textured 125 mm x 125 mm, 1 Ω cm p-type Cz wafers. Gas phase diffusion based on phosphorous oxy-chloride ($POCl_3$) was used for forming the n^+ emitter surface. Following phospho silicate glass (PSG) removal and plasma edge isolation, the surface passivation layer was grown/deposited using a capacitive coupled PECVD system at 380^{o}C. Screen printed silver was used as the front contact while screen printed aluminium was used as the rear contact, which were fired at 850 ^{o}C in a rapid thermal annealing chamber in N_2 + O_2 ambient. The schematic for the fabrication of silicon solar

cells is shown in Fig. 6.2. The quantum efficiency of the solar cell was measured to study the effect of plasma grown oxy-nitride films on the quality of emitter passivation. In order to study the quality of emitter passivation, lifetime measurements were carried out on 45 Ω/□ double side phosphorus diffused p-type 1 Ω cm Cz wafers. Stacks of SiO_xN_y - SiN_v:H were deposited on both sides of the diffused wafer and τ_{eff} was measured from quasi-steady state photo conductance measurements (QSSPC).

6.1.2 Physical characterization of plasma grown films



(a) (b)

Fig. 6.3: Physical characterisation of N_2O plasma grown films on Si (a) N1s XPS spectrum for SiO_xN_y film grown in N_2O ambient for 5 min and 40 min confirming presence of nitrogen (b) O1s XPS spectrum showing larger oxygen content for films grown for 40 min.

The variation in film composition was investigated using XPS. The longer plasma exposure time also resulted in an increase in nitrogen content in the film from 0.2% to 0.6%, as shown in Fig. 6.3(a). As the plasma exposure time was varied from 5 to 40 min, oxygen/silicon ratio changed from 1.56 to 2.74 indicating an increase in oxygen content within the film. The increasing O content within the plasma grown film is indicated in Fig. 6.3(b). The presence of nitrogen in the plasma grown film confirms that the plasma grown film is a silicon oxy-nitride film with small amounts of nitrogen.

Impact of interstitial oxygen on the electrical characteristics of the devices was investigated by growing thin oxy-nitride films in a PECVD chamber in N_2O ambient. Fig. 6.4(a) shows the FTIR spectrum for the plasma grown films in N_2O ambient in a PECVD chamber for varying plasma exposure times. Similar to the results obtained by Kim et al., the films grown in PECVD

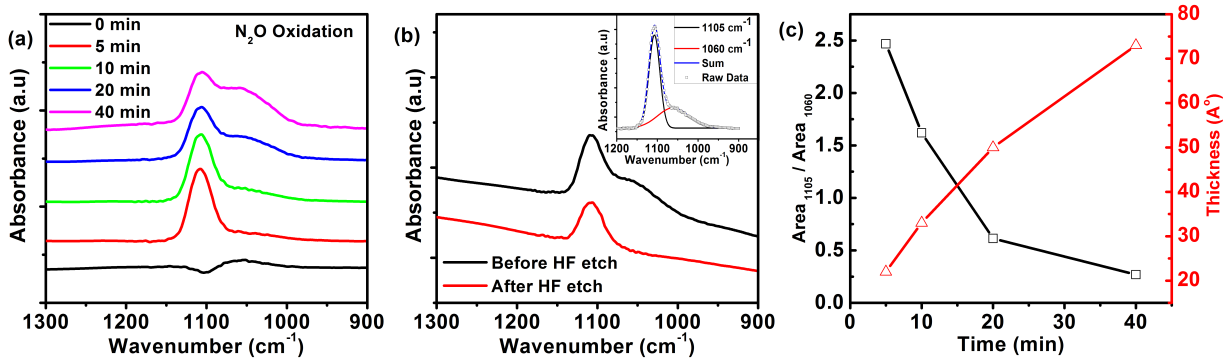
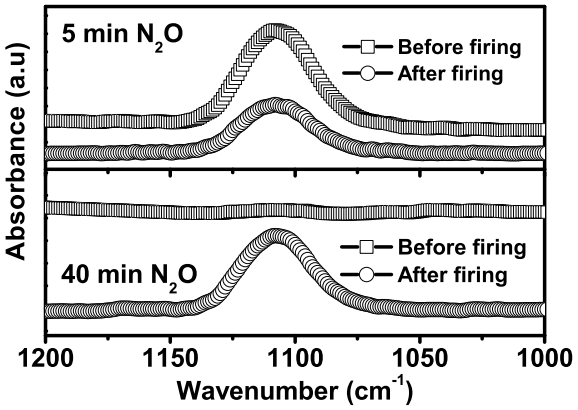


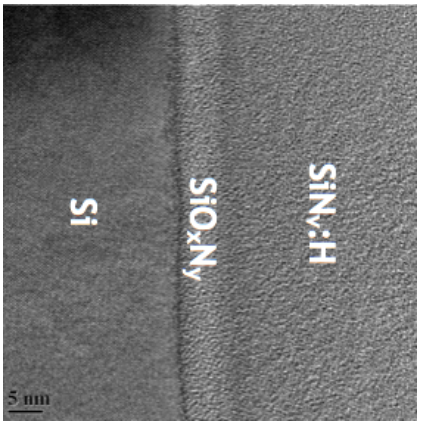
Fig. 6.4: (a) FTIR Spectra for films grown in PECVD chamber showing the emergence of Si - O - Si vibration mode at 1060 cm^{-1}, along with a decrease in interstitial oxygen peak at 1105 cm^{-1} with increasing plasma oxidation time (b) FTIR spectrum of plasma grown oxy-nitride film before and after removal of oxide in HF solution, a peak corresponding to interstitial oxygen is seen to remain indicating that it is within silicon. Inset shows the deconvolution of FTIR spectrum to obtain two peaks at 1105 cm^{-1} and 1060 cm^{-1} (c) Ratio of area under the 1105 cm^{-1} and 1060 cm^{-1} peaks is seen to decrease, which corresponds to an increase in film thickness.

chamber had peaks at 1105 cm^{-1}, which corresponds to interstitial oxygen trapped within silicon [85]. The film grown for 5 min had the strongest interstitial peak, while the films grown for longer duration started exhibiting a strong shoulder corresponding to the Si - O - Si stretching mode vibrations at 1060 cm^{-1}. The untreated sample (labelled as 0 min), correspond to a bare Si sample of same base resistivity measured after a 2% HF clean. FTIR measurements were repeated after etching the oxy-nitride film in buffered HF solution (5:1). The comparison of the FTIR spectrum before and after etching in buffered HF solution is shown in Fig. 6.4(b). Upon removing the oxy-nitride film, a FTIR peak corresponding to interstitial oxygen at 1105 cm^{-1} was seen, while the Si - O - Si shoulder at 1060 cm^{-1} was seen to disappear, indicating the removal of SiO_xN_y film, as shown in Fig. 6.4(b). The residual peak at 1105 cm^{-1} corresponds to interstitial oxygen within silicon [85]. The impact of plasma exposure time on the interstitial oxygen concentration can be seen clearly in Fig. 6.4(c). FTIR spectrum was de-convoluted and two Gaussian peaks corresponding to 1105 cm^{-1} and 1060 cm^{-1} were obtained as shown in inset of Fig. 6.4(b). The ratio of area under the 1105 cm^{-1} and 1060 cm^{-1} peaks is shown in Fig. 6.4(c), which is seen to decrease for increasing film thickness. Similar to the observations made by Kim et al. [85], the interstitial oxygen concentration in silicon due to plasma treatment came down for longer plasma treatment.

As shown in Fig. 6.4(c), a 7.3 nm film was obtained after treating the film in N_2O plasma ambient for 40 min. In order to use this thin layer as a surface passivation layer, it needs to be



(a)



(b)

Fig. 6.5: FTIR measurements carried out on Si wafer after stripping the as deposited and fired SiO_xN_y - SiN_v:H stacks in buffered HF solution. A significant increase in peak at 1105 cm^{-1} is seen for 40 min sample, after firing (b) HRTEM image of a (10 min) SiO_xN_y - SiN_v:H stack.

capped with another dielectric like silicon nitride. Stacks of SiO_xN_y - SiN_v:H would also have to undergo various thermal treatment steps like the high temperature firing step used in c - Si solar cell fabrication. In order to investigate the evolution of trapped interstitial oxygen to these processing steps, the silicon oxy-nitride films were capped with silicon nitride. One part of the sample was fired at 850^oC, simulating the typical firing condition, while the other sample was kept as reference. The stack of SiO_xN_y - SiN_v:H was then stripped off using buffered HF (5:1) solution, and FTIR measurements were carried out. The results of the measurement are shown in Fig. 6.5(a). For the 5 min sample, interstitial oxygen content was seen to remain within silicon even after silicon nitride deposition and firing step. However, for the 40 min sample, signal from the interstitial oxygen peak at 1105 cm^{-1} was very weak before firing, but was seen to increase dramatically after firing. This increase in interstitial content may have been the result of oxygen diffusion from the SiO_xN_y film into the silicon substrate. XPS measurements for the 40 min sample had confirmed that the SiO_xN_y film was rich in oxygen, see Fig. 6.3(b). Hence, it may act as a potential source of oxygen. The impact of this potential oxygen diffusion on the effective lifetime of the stack is investigated in detail in the sections below. Fig. 6.5(b) shows the HRTEM image showing the plasma grown film after 10 min of N_2O plasma exposure. The thickness of the film grown can be seen to be $\sim$ 5 nm.

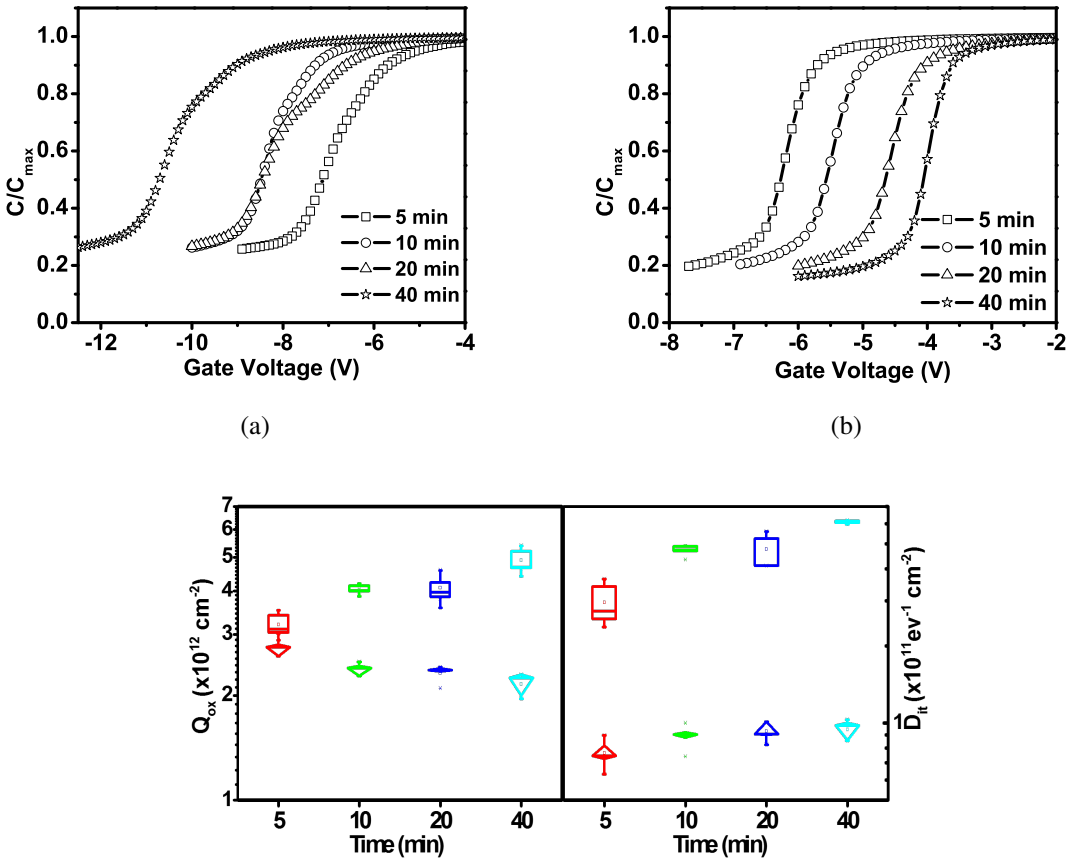


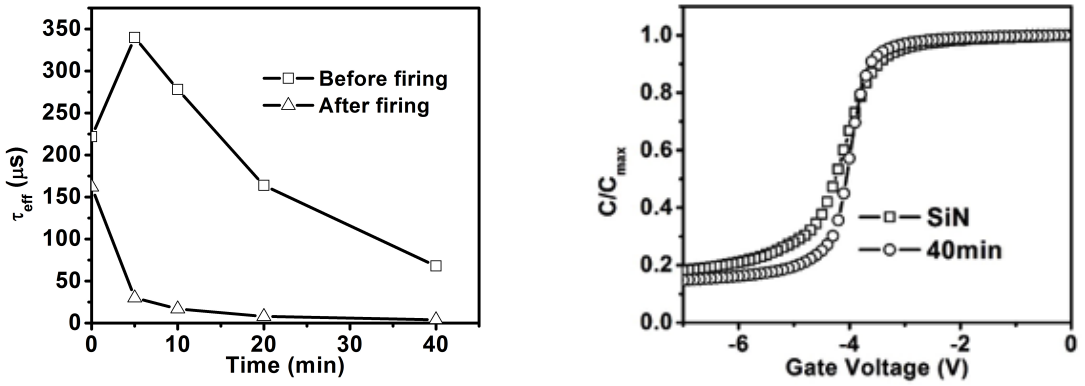
Fig. 6.6: HFCV curves for SiO_xN_y - SiN_v:H stacks (a) before firing (b) after firing (c) Q_{ox} and D_{it} versus plasma exposure time before (□) and after firing(◊).

6.1.3 Capacitance - Voltage and lifetime measurements

High frequency capacitance - voltage (HFCV) and High frequency conductance - voltage (HFGV) measurements were carried out on SiO_xN_y - SiN_v:H stacks grown/deposited on n-type FZ wafers. Aluminium was used as the top and bottom electrode. The measurements were carried out before and after firing the stack at 850^{o}C. The frequency of measurement was set at 50 KHz. The results of the HFCV measurements are shown in Fig. 6.6(a) and 6.6(b). Before firing, HFCV curves can be seen to shift to the left for increasing plasma exposure time, indicating an increase in fixed charge density (Q_{ox}). Q_{ox} was extracted by calculating the shift in mid-gap voltage from its ideal value [117]. Additionally for the 20 min and 40 min samples, a hump can been seen towards the accumulation region of the C-V curve as shown in Fig. 6.6(a), possibly due to generation of additional defects at the Si - SiO_xN_y interface. Before firing, Q_{ox} was seen to improve from 3.2x10^{12} cm^{-2} to 5x10^{12} cm^{-2} for increasing plasma exposure time.

However, upon firing, a significant decrease in Q_{ox} was shown by the 40 min sample, while almost no change in Q_{ox} was observed for 5 min sample. A progressive decrease in Q_{ox} was seen for samples after firing for longer plasma exposure time.

The interface state density (D_{it}) was extracted from HFGV and HFCV curves using single frequency approximation method [118]. D_{it} increased from 3 x10^{11} $eV^{-1}cm^{-2}$ to 6.5 x10^{11} $eV^{-1}cm^{-2}$ when the plasma exposure time was raised from 5 to 40 min. After firing the samples, D_{it} was seen to decrease significantly, as shown in Fig. 6.6(c). However, the value of D_{it} was comparable across all the four samples after firing.



(a) (b)

Fig. 6.7: (a) Variation in τ_{eff} versus growth time, for samples before and after firing. τ_{eff} for silicon nitride film (0 min) is also indicated in figure for comparison. τ_{eff} was measured on 300 μm thick n-type FZ wafers with a resistivity of 3 Ω cm. (b) C-V curves for SiN_y:H and 40 min SiO_xN_y - SiN_y:H stack after firing is shown for comparison. A larger stretch-out in HFCV curve can be seen for SiN_y:H sample.

Effective surface passivation would depend on two competing mechanisms: (i) field effect (Q_{ox}) passivation, and (ii) chemical (D_{it}) passivation [10]. In the case of as deposited samples, D_{it} and Q_{ox} are seen to increase with increasing thickness of the silicon oxy-nitride film. In this case, the field effect passivation is enhanced while the chemical passivation is degraded. However after firing while the D_{it} is fairly identical, Q_{ox} decreases with increasing thickness, indicating similar chemical passivation, but decreasing field effect passivation. Minority carrier lifetime measurements carried out on stacks of unannealed SiO_xN_y - SiN_y:H stacks, revealed a decreasing τ_{eff} for increasing plasma exposure time. As can be seen in Fig. 6.7(a) τ_{eff} decreased from 347 μs to 68 μs for longer plasma exposure time. Despite an enhancement in field effect passivation, the lower τ_{eff} for 40 min is attributed to its significant degradation in

chemical passivation, as was observed from C-V analysis. The τ_{eff} may also degrade significantly with a degradation in τ_{bulk}, as a result of the plasma treatment process. However, this aspect is discussed later on in this section. The lifetime obtained for 5 min SiO_xN_y - SiN_v:H stack (before firing) corresponds to a SRV of 43 cm/s (S_{eff}). For the short growth time, this result is at par with what was previously reported for low temperature grown silicon oxide films [12, 70, 72].

However, after firing, a sharp fall in τ_{eff} was observed for the SiO_xN_y - SiN_v:H stacks. On firing the SiO_xN_y - SiN_v:H stacks, τ_{eff} came down drastically from 347 μs to 30 μs for the 5 min sample. A similar decrease was seen for all the SiO_xN_y - SiN_v:H samples, with the 40 min sample showing a carrier lifetime of 8 μs after firing. However, after firing, τ_{eff} obtained for SiO_xN_y - SiN_v:H stacks were significantly lower than what was seen for silicon nitride sample (0 min) after firing. Fig. 6.7(b) compares the HFCV and HFGV curves for fired silicon nitride sample and SiO_xN_y(40 min)/SiN_v:H stack. The silicon nitride sample was seen to have a larger stretch out in HFCV than the SiO_xN_y(40 min)/SiN_v:H sample, implying a better quality interface for the stack. However, as previously shown, the corresponding lifetimes after firing were 168 μs and 8 μs for silicon nitride and SiO_xN_y - SiN_v:H stack respectively. Thus, it maybe concluded that the degradation in τ_{eff} may not be the result of degradation of Si - SiO_xN_y interface.

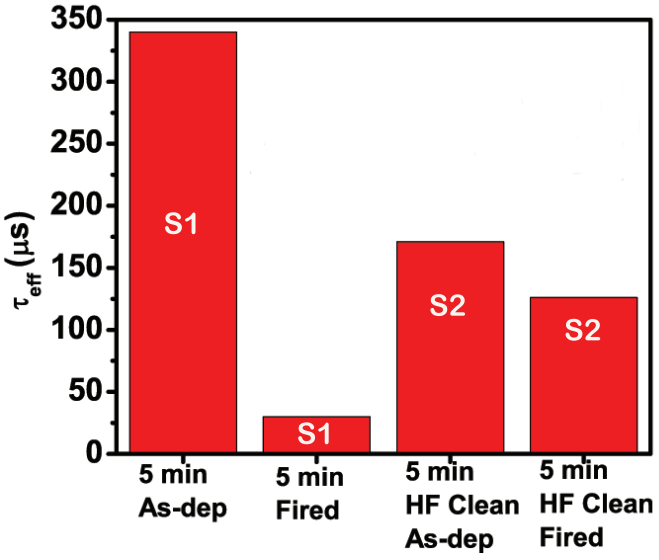


Fig. 6.8: Lifetime data on samples measured before and after firing. The samples differ in the fact that the plasma grown SiO_xN_y layer was etched out in 2% HF solution. After firing, a significant degradation in τ_{eff} can be seen, when the SiO_xN_y layer is present during firing process.

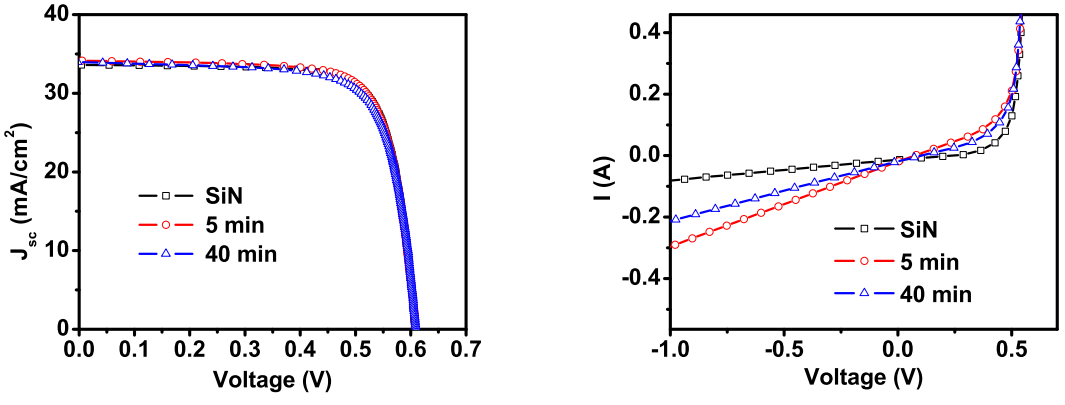
In order to ascertain the likely cause of this degradation, additional experiments were carried out on RCA cleaned, n-type 3 Ω cm FZ wafers. Silicon oxy-nitride film was grown on both sides of the wafer by exposing it in N_2O plasma ambient for 5 min. Subsequently SiN_v:H was deposited on both sides and this sample is labelled as S1. Lifetime was measured before and after firing the sample at 850^oC. Another set of samples labelled as S2 were prepared, wherein the SiO_xN_y was first grown using the same process as S1 and then it was subsequently etched in 2% HF. SiN_v:H was then deposited on both sides, and lifetime was measured before and after firing. In case of S1, SiO_xN_y layer is present near the interface, while it is absent in case of sample S2. For sample S2, τ_{eff} of 170 μs was measured in as deposited state, which degraded to 126 μs after firing. The quantum of decrease in τ_{eff} was $\sim$ 50 μs which was significantly lower than what was seen for sample S1 after firing, as shown in Fig. 6.8. In short, the firing process with the SiO_xN_y layer on the wafer has resulted in larger degradation in lifetime than without it. As seen from FTIR investigations, the transport of oxygen across the interface into the bulk of the wafer may have played a major role in degrading the measured τ_{eff} for the fired SiO_xN_y - SiN_v:H stacks due to potential degradation in bulk lifetime (τ_{bulk}).

To summarise, from HFCV and lifetime measurements, it maybe concluded that τ_{eff} was found to be determined by Q_{ox} and D_{it} at the Si - SiO_xN_y interface. Upon firing the SiO_xN_y - SiN_v:H stacks, τ_{eff} degraded severely. The degradation may have been the result of a degradation in τ_{bulk} potentially due to diffusion of oxygen from SiO_xN_y layer into the silicon substrate during firing, as was seen from FTIR measurements.

6.1.4 Can plasma grown silicon oxy-nitride films be used for emitter surface passivation?

As shown in the previous section, firing of SiO_xN_y - SiN_v:H stacks was seen to result in a severe degradation of τ_{eff} as compared to SiN_v:H films. The experiments were carried out on n-type FZ wafers, where the tolerance to oxygen impurities is low. Commercially available mono c - Si solar cells make use of Cz wafers in which the oxygen impurity concentration is almost two orders of magnitude higher than FZ wafers. This could imply that a Cz wafer would be more tolerant to potential oxygen diffusion from the plasma grown silicon oxy-nitride film. Thus the behaviour of plasma grown SiO_xN_y - SiN_v:H stacks can be inherently different in case of FZ and Cz wafers. Additionally, the diffusion process carried out using $POCl_3$ can also result in

some oxygen incorporation into the emitter of the solar cell. Additionally for emitters with low R_{sheet}, passivation is governed mainly by chemical passivation [135]. Thus an improved SiO_xN_y - Si interface as shown in Fig. 6.7(b) can potentially improve the emitter passivation. In order to investigate this aspect, c - Si solar cells were fabricated on textured p-type wafers of 1 Ω cm base resistivity and an emitter sheet resistance of 45 Ω/□. SiO_xN_y film was grown by exposing the emitter surface to an N_2O plasma for 5 min and 40 min. The SiO_xN_y film was capped with SiN_v:H and was used as the front surface passivation layer/anti-reflective coating. A solar cell with SiN_v:H film as surface passivation layer/anti-reflective coating was also fabricated for comparison. Illuminated and dark IV characteristics for the solar cells are shown in Fig. 6.9. It can be seen that the J_{sc} is higher for the solar cell passivated with the SiO_xN_y - SiN_v:H stack. Another noticeable feature is the larger reverse leakage current observed in the dark IV curve, as shown in Fig. 6.9(b). The increase in reverse leakage current can be attributed to an increase in the number of recombination centres, due to oxygen interstitials [136]. The reverse leakage current came down for longer plasma exposure duration, which was shown to result in lower interstitial oxygen in section 6.1.2, indicating the correlation between the trapped interstitial oxygen content and reverse leakage current. Similar increase in reverse leakage current was reported by Chen et al., who had found that larger the amount of oxygen precipitates in the wafer, larger is the reverse leakage current [136].



(a) (b)

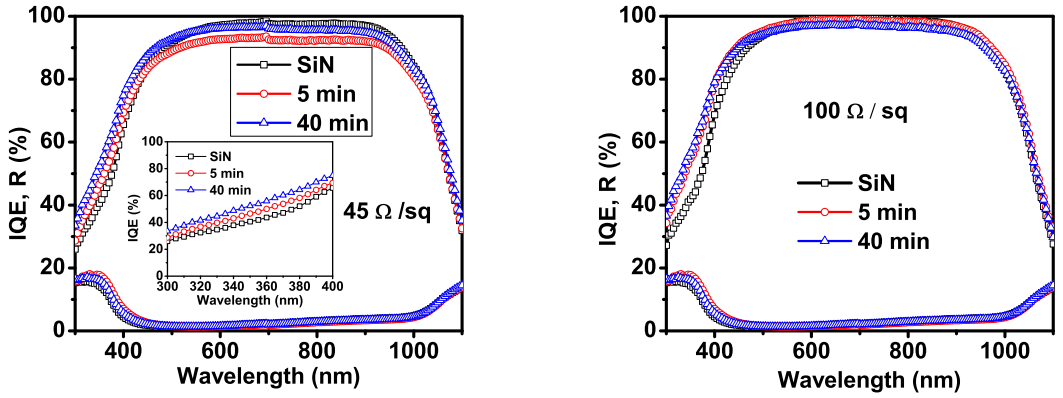
Fig. 6.9: (a) Illuminated and (b) dark IV curves for solar cell with and without plasma grown SiO_xN_y film.

The detailed solar cell characteristics are summarised in Table. 6.1. V_{oc} for all the solar cells were found to be almost identical. However, the short circuit current was seen to increase by

almost 0.6 mA/cm^2 for an oxidation time of 40 min. Yet another interesting observation is the lower R_{sh} observed for the films passivated with plasma grown SiO_xN_y - SiN_v:H stacks. The interstitial oxygen trapped within silicon can lead to an increase in the reverse leakage current, and hence lower R_{sh}. The lower R_{sh} and the higher R_s was also seen to have a bearing on the FF of the solar cells passivated with SiO_xN_y - SiN_v:H stacks.

Table 6.1: Illuminated IV parameters for solar cells fabricated with and without plasma grown oxy-nitride film.

Cell	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF(%)	η(%)	R_s(Ω cm^2)	R_{sh}(Ω cm^2)
Ref.	608	33.60	76.5	15.6	0.72	2973
5min	609	33.96	73.9	15.3	0.93	560
40 min	609	34.16	75.4	15.7	0.77	813



(a) (b)

Fig. 6.10: IQE and reflectance curves for two sets of solar cells with different emitter sheet resistances (a) 45 Ω/□ emitter (b) 100 Ω/□ emitter.

The internal quantum efficiency of the solar cells are shown in Fig. 6.10(a). As can be seen, cells with 5 min, 40 min SiO_xN_y had a better response in 300 - 500 nm wavelength range, indicating a potential improvement in emitter passivation as compared to the reference sample. The same is highlighted in the inset of Fig. 6.10(a). For the wavelength range from 550 nm to 950 nm, a marginal reduction in internal quantum efficiency (IQE) can be seen, most likely due to a degradation in τ_{bulk} of the wafer, as a result of possible diffusion of oxygen from the oxygen rich SiO_xN_y film after firing. The lower R_{sh} for the cells with the SiO_xN_y - SiN_v:H emitter surface passivation stacks may also have played a role in bringing down the IQE in the 550 nm to 950 nm range. The improvement in IQE for shorter wavelengths maybe the result of an

improvement in Si - SiO_xN_y interface quality. Glunz et al. had reported that the impact of positive charges on the SRV of emitter surfaces was low [27]. In this work, only positively charged dielectrics were used for emitter surface passivation, and hence, it maybe fair to conclude that a better SiO_xN_y - Si interface may have played a major role in determining the emitter surface passivation quality. The SiO_xN_y layer can shield the wafer surface from plasma damage during the silicon nitride deposition, which may have lead to an improvement in short wavelength response as seen from IQE. HFCV curves shown in Fig. 6.7(b) had indicated a better chemical passivation for the SiO_xN_y - SiN_v:H stacks as compared to SiN_v:H film. Similar shielding behaviour was reported to yield improved short wavelength response for wet chemical grown silicon oxide films [74]. Fig. 6.10(b) shows the quantum efficiency for solar cells fabricated on 100Ω/□ emitter. The improvement in emitter surface passivation quality for the SiO_xN_y - SiN_v:H stack was significantly better than their SiN_v:H counterpart, as is seen in Fig. 6.10(b).

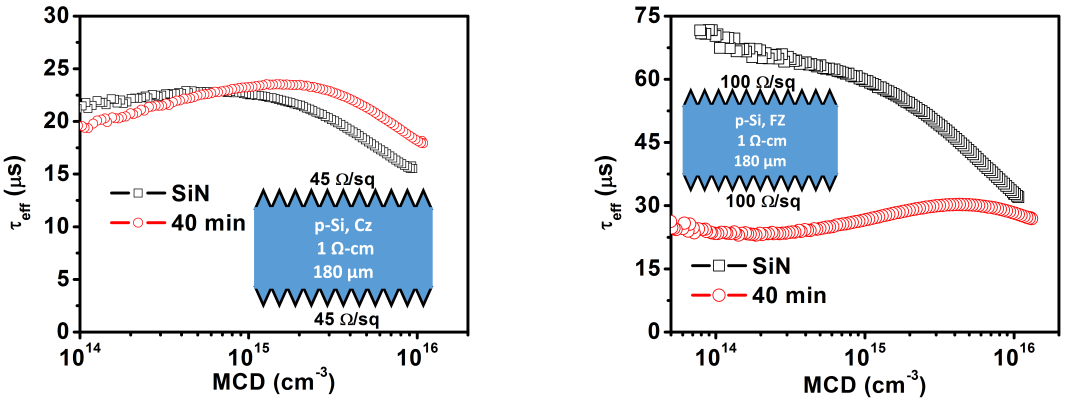


Fig. 6.11: Lifetime measurements on double side diffused emitters after firing at 850^{o}C (a) 45 Ω/□ emitter on Cz wafer (b) 100 Ω/□ emitter on FZ wafer.

In order to verify the improvement in emitter passivation quality across the samples, QSSPC measurements were carried out on 45 Ω/□ emitters diffused on both sides of textured p-type Cz wafer of resistivity 1 Ω cm. The lifetime measurements were carried out on the wafers after firing them at 850^{o}C in N_2 + O_2 for 1s. The results of the lifetime measurements are shown in Fig. 6.11(a). τ_{eff} for the both the samples were comparable with the SiO_xN_y - SiN_v:H stack showing marginally better τ_{eff} for higher minority carrier density. This result is in stark contrast with what was seen on n-type FZ wafers, as shown in Fig. 6.7(a). It maybe concluded from this result, that the Cz wafers with two orders of magnitude higher oxygen concentration than FZ

wafers and is less sensitive to bulk lifetime degradation due to oxygen diffusion from the plasma grown SiO_xN_y layer. The same fact was once again ascertained by repeating the experiment on a 100 Ω/□ emitter diffused on a p-type FZ wafer of resistivity 1 Ω cm. A significant decrease in τ_{eff} was observed for the SiO_xN_y - SiN_v:H stacks, as shown in Fig. 6.11(b), despite showing an improved short wavelength response on solar cells. Hence, the sharp fall in τ_{eff} is contemplated to be the result of a degradation in bulk lifetime of the wafer. The degradation in bulk lifetime is found to more severe in FZ wafers than in Cz wafers.

6.1.5 Conclusion

In this section, a capacitive coupled PECVD based process for the low temperature growth of silicon oxy-nitride films in nitrous oxide plasma ambient was discussed. For thinner plasma grown films, interstitial oxygen was seen to be trapped within the silicon, which was consumed as the films grew thicker. Stacks of SiO_xN_y - SiN_v:H with lower SiO_xN_y thickness was found to yield a τ_{eff} of 347 μs which was at par with what was previously reported for various low temperature grown silicon oxide films. τ_{eff} was seen to have a strong correlation to D_{it} and Q_{ox} at the interface. On firing, transport of oxygen across the interface into silicon was seen to result in a significant degradation in τ_{eff}, possibly due to degradation in τ_{bulk}. However, on silicon solar cells, the better interface properties for the SiO_xN_y - SiN_v:H stack resulted in an improved quantum efficiency for the short wavelength range, indicating an improvement in emitter surface passivation quality.

6.2 Plasma oxidation in Ar + N_2O ambient for silicon surface passivation

Plasma oxidation in N_2O ambient and its application on silicon solar cells were discussed extensively in the previous section. The solar cells exhibited an improvement in the short wavelength response leading to a marginal increase in J_{sc}, while the V_{oc} remained the same. The degradation in the bulk lifetime owing to oxygen diffusion during the firing process maybe the reason behind the lack of improvement in V_{oc}. Sekine et al. reported that, carrying out the oxidation process in Ar + O_2 and Kr + O_2 ambient resulted in an increase in oxidation rate and also resulted in an improvement in Si - SiO_2 interface quality [14]. In this section, the use of Ar in the

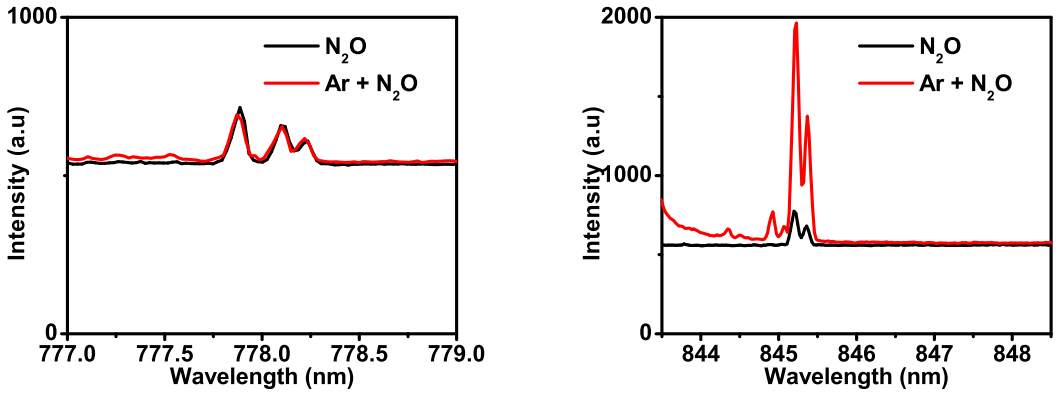
plasma oxidation process to improve the surface passivation in silicon solar cells is discussed. The variation in plasma composition, film composition and its impact of solar cell performance is discussed in detail. Efficacy of the Ar + N_2O plasma oxidation process for c - Si solar cell passivation is compared with that of a furnace grown low temperature silicon oxide film.

6.2.1 Experimental setup

RCA cleaned, p-type, polished Cz <100> Si wafers with resistivity of 4 - 7 Ω cm was chosen as the substrate for the experiments. Thin silicon oxy-nitride films were grown in Ar + N_2O ambient in a capacitively coupled plasma system. The ratio of N_2O:Ar was maintained at 1:9. The chamber pressure of 1 Torr, and RF power of 10 W was used for the experiments. The plasma exposure duration was varied from 5, 10, 20 and 40 mins, leading to films of different thickness. The thickness of the films were measured using spectroscopic ellipsometer. Plasma characterisation was carried out using an optical emission spectrometer. The film composition studies were carried out using FTIR in absorbance mode, with a resolution of 4 cm^{-1} and X-ray photoelectron spectroscopy (XPS). Silicon nitride (SiN_y:H) film of ∼80 nm was deposited on the silicon oxy-nitride film using PECVD. Crystalline silicon solar cells were fabricated on as cut 125 mm x 125 mm, p-type Cz <100> wafers with 1 - 3 Ω cm resistivity. Following saw damage removal, texturization and RCA cleaning, the wafers were loaded into a phosphorus diffusion furnace for emitter formation. After the junction isolation process and PSG removal, stacks of plasma grown oxy-nitride - silicon nitride films were used as the anti-reflective coating and emitter surface passivation layer. Screen printed silver was used as the front contact while screen printed Aluminium was used as the rear contact, and was fired at 850^oC in a rapid thermal annealing chamber in N_2 + O_2 ambient. The quantum efficiency of the solar cell was measured to study the effect of plasma grown silicon oxy-nitride films on the emitter surface passivation quality. Solar cell IV measurement was carried out in a class AAA solar simulator under AM 1.5G spectrum.

6.2.2 Plasma characterisation using optical emission spectroscopy

OES spectra indicating the oxygen related plasma species for N_2O and Ar + N_2O plasma is shown in Fig. 6.12. The peaks at 777 nm were seen to be similar for both the plasma ambients. However, a small increase in the oxygen peak intensity at 844 nm was observed for Ar + N_2O

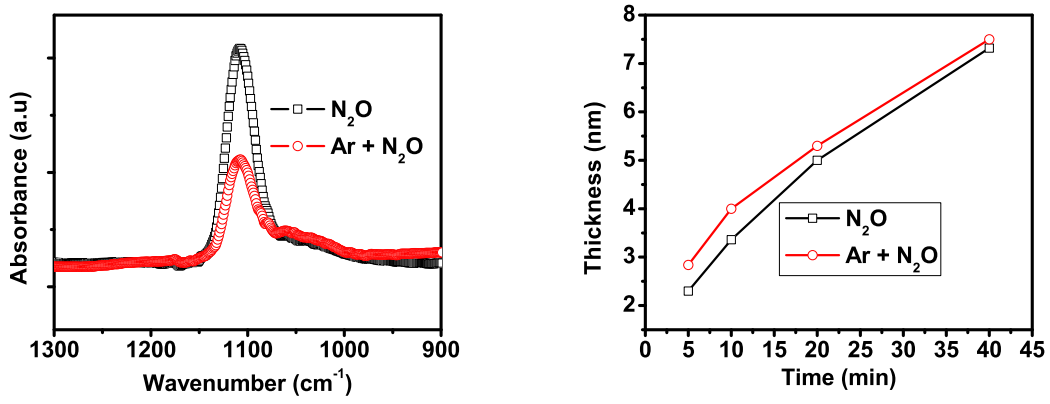


(a) (b)

Fig. 6.12: Comparison of OES spectra for N_2O and Ar + N_2O plasma at (a) 777 nm (b) 844 nm.

plasma ambient. From previous experiments, it was observed that an increase in oxygen content within the plasma was seen to result in an increase in growth rate. The increasing oxygen content in the plasma can also alter the physical composition of the film. The results of the film composition studies as well as ellipsometry results are discussed in detail in the section below.

6.2.3 Physical characterisation of plasma grown film

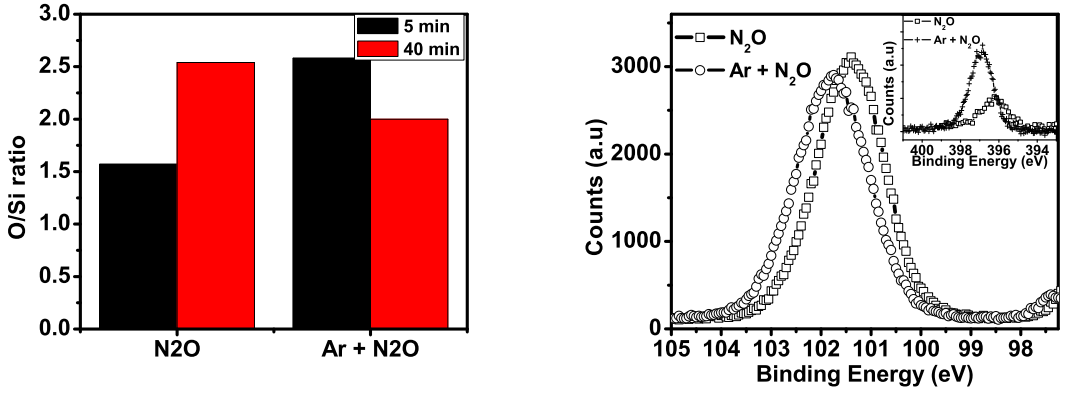


(a) (b)

Fig. 6.13: (a) FTIR spectrum and (b) ellipsometry data comparing films grown in N_2O and Ar + N_2O ambient for 5 min.

Fig. 6.13(a) compares the FTIR spectrum for two films grown in N_2O and Ar + N_2O ambient for 5 min. From the FTIR spectrum shown in Fig. 6.13(a), it can be observed that the area under the interstitial peak centred at 1105 cm^{-1} was lower for films grown in Ar + N_2O ambient as

compared to films grown in N_2O ambient. From elliposmetry results presented in Fig. 6.13(b), it can been seen that a marginally higher film thickness was obtained for oxidation carried out in Ar + N_2O as compared to oxidation in N_2O ambient. The growth rate was found to be higher for shorter duration, and was found to come down for longer oxidation times. The reduction in oxidation rate with increasing thickness may point out to a diffusion limited oxide growth mechanism as was reported by Choi et al. [79]. The enhanced oxidation rate in presence of an inert gas was found to be in agreement with what was reported previously by Sekine et al. [14]. The increased oxidation rate was explained on the basis of the energy of ionized inert gas with that of ionized oxygen. $O^1D + O^1D$ radicals are generated in an oxygen plasma and is the highly reactive state of oxygen and can lead to bond forming reactions. The first metastable state of Ar^* is at 11.6 eV and can result in $O_2{}^+$ species and $O^1D + O^1D$ species. However, Kaspar et al. reported that O^1D species lead to an enhanced oxidation, only for thickness of $\sim$ 2 nm. Beyond that, continuous exposure to O^1D radicals did not yield thicker oxides. The enhanced oxidation in inert gas require other reactive species which would contribute to the diffusion of reactive species into the oxide [81].



(a) (b)

Fig. 6.14: (a) O/Si ratio for various oxidation times in N_2O and Ar + N_2O ambient (b) Si2p spectrum for N_2O and Ar + N_2O oxidation for 40 min, inset shows N1s spectrum.

The chemical composition of the film was analysed further using XPS measurements. It was observed that oxygen to silicon ratio of 2.0 was obtained for films grown in Ar + N_2O for 40 min as compared to the 2.54 obtained for films grown in N_2O ambient for 40 min. The film was seen to move towards stoichiometry when a mixture of Ar + N_2O was used for the process. Additionally, the nitrogen content also increased from 2.6% for N_2O sample to 4.9% for the Ar

+ N_2O sample. From XPS measurements, it was observed that the film went from an O-rich state (2.58) to a stoichiometric state (2.0), as the oxidation time was increase from 5 min to 40 min. In comparison, the films grown in N_2O ambient, the stoichiometry changed from a Si-rich state to a O-rich state with increasing oxidation time. The same is illustrated in Fig. 6.14(a). The N1s spectrum showing the nitrogen content in the film is shown in inset of Fig. 6.14(b). Compared to N_2O based oxidation, films grown in Ar + N_2O ambient was found to result in higher nitrogen incorporation. Thus the growth of a film in an Ar + N_2O ambient resulted in the following advantages:

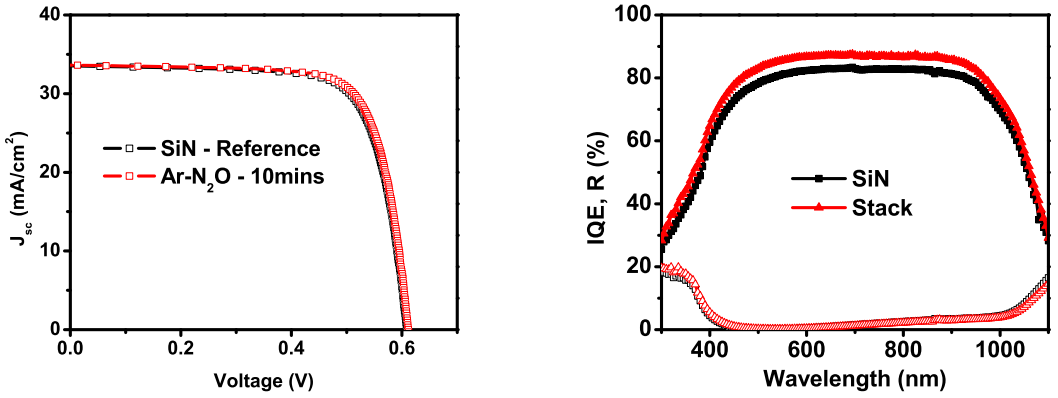
- The interstitial oxygen content trapped in silicon as a result of the plasma oxidation process came down as was seen from FTIR measurements.
- Oxygen to silicon ratio of 2.0 was obtained for films grown in Ar + N_2O for 40 min as compared to the 2.54 obtained for films grown in N_2O ambient for 40 min.

6.2.4 Solar cell results and discussion

In this section, the performance of the solar cells fabricated with the silicon nitride as the front surface passivation layer (baseline) is compared with solar cells having stack of silicon oxy-nitride/silicon nitride as the front surface passivation layer. Silicon oxy-nitride films are grown for 10 min in Ar + N_2O ambient at 380^oC. RF power was 10 W during the film growth, and chamber pressure was 1000 mTorr. As can be seen from Table 6.2, in comparison to the baseline solar cell, an improvement in V_{oc} was observed for the sample whose emitter was passivated by the SiO_xN_y - SiN_v:H stack. Compared to the data discussed in Table. 6.1, the solar cells discussed here shows a marginal improvement in V_{oc} as well as J_{sc}. Yet another point worth noting is the that the R_{sh} values for both the samples were comparable. Further, the lower R_s for the solar cell passivated with SiO_xN_y - SiN_v:H stack resulted in an improvement in FF and cell efficiency. However, the variation in R_s maybe due to process variations in contact printing and firing.

Table 6.2: Solar cell characteristics comparing Ar + N_2O oxidation (10 min) with baseline silicon nitride.

Cell Label	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF(%)	η(%)	R_s(Ω cm^2)	R_{sh}(Ω cm^2)
Baseline	608	33.59	74.4	15.20	1.10	702
10 min	611	33.68	75.1	15.50	0.98	784



(a) (b)

Fig. 6.15: (a) Illuminated IV and (b) internal quantum efficiency for solar cells fabricated with SiO_xN_y - SiN_v:H.

Fig. 6.15 shows the illuminated IV and internal quantum efficiency of the solar cells. An improvement in IQE was observed for the solar cell passivated with the stack. An improvement was seen in the short wavelength regime, which maybe attributed to the improvement in emitter passivation quality. However, the improvement in IQE in the mid-wavelength region is due to the higher R_{sh} observed for the solar cells passivated with the SiO_xN_y - SiN_v:H stack. Solar cell efficiency was seen to improve by 0.3% when SiO_xN_y - SiN_v:H stack was used for emitter surface passivation. The improvement in V_{oc} maybe attributed to an improvement in surface passivation quality. In order to confirm the improvement in emitter passivation quality, τ_{eff} measurements were carried out on test structures made on p-type Cz wafers. Phosphorus diffusion was carried out on both sides of a textured p-type Cz wafer, and the passivation layers were deposited on either side of the wafer. Fig. 6.16 summarises the results of the lifetime measurement. In the as deposited state, SiN_v:H and SiO_xN_y - SiN_v:H stack had comparable effective lifetimes. However, upon firing the samples at 850^{o}C in N_2 + O_2 ambient, a higher τ_{eff} was observed for the SiO_xN_y - SiN_v:H stack as compared to the SiN_v:H film, indicating an improvement in emitter passivation quality.

Table 6.3: Solar cell characteristics comparing Ar + N_2O oxidation (20 min) with baseline silicon nitride.

Cell Label	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF(%)	η(%)	R_s(Ω cm^2)	R_{sh}(Ω cm^2)
Baseline	611	33.03	75.4	15.20	0.962	867
20 min	614	33.42	75.4	15.50	0.915	2944

The repeatability of the Ar + N_2O oxidation process in enhancing the V_{oc} was further inves-

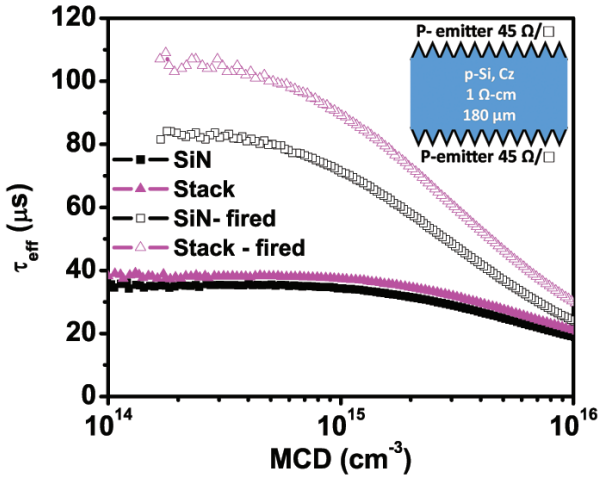


Fig. 6.16: Lifetime measurement on double side P-diffused p-type Cz wafers, before and after firing. Inset shows the test structure used for the measurement.

tigated, by increasing the oxidation time to 20 min. The results of this experiment is summarised in Table. 6.3. Here again, an increase in V_{oc} was observed compared to the reference solar cell. In addition to the V_{oc} improvement, a significant enhancement in R_{sh} was also observed. The quantum of improvement in R_{sh} was significantly more than what was observed for the case of a 10 min plasma oxidation. Thus it maybe concluded that a longer plasma oxidation process may improve the R_{sh} as well as result in a larger improvement in V_{oc}. To ascertain this hypothesis, solar cells were fabricated with their emitters passivated by a stack of SiO_xN_y - SiN_v:H. The SiO_xN_y film was grown in Ar + N_2O for 40 min. The results of this experiment is discussed in detail in the next section.

6.2.5 Conclusion

Silicon oxy-nitride films were grown in N_2O + Ar ambient. Similar to the case of N_2O based plasma oxidation, FTIR measurements indicated a decrease in interstitial oxygen content for increasing film thickness. O/Si ratio of the plasma grown film was found to approach 2.0 for an oxidation duration of 40 min. Improved c - Si solar cell performance was seen for solar cells with the stack of SiO_xN_y - SiN_v:H as the surface passivation layer. The improvement was observed in V_{oc} and was attributed to an improvement in emitter surface passivation. An improvement in R_{sh} was also observed when SiO_xN_y - SiN_v:H stacks were used for emitter surface passivation. Compared to solar cells fabricated using plasma oxides grown in N_2O ambient (without Ar), the following observations can be made.

- An improvement in R_{sh} was observed for plasma oxides grown in Ar + N_2O ambient, possibly due to the lower amount of trapped interstitial oxygen as was seen from the FTIR spectrum.

- An improvement in V_{oc} was observed in case of Ar + N_2O based plasma oxidation as compared to the improvement in J_{sc} observed in case of N_2O based plasma oxidation.

Therefore, plasma oxidation process based on Ar + N_2O ambient may be well suited for application in emitter passivation in case of c - Si solar cells. In the next section, SiO_xN_y - SiN_v:H stacks based on 40 min plasma oxidation is benchmarked against a low temperature furnace oxidation process for emitter surface passivation.

6.3 Benchmarking plasma oxidation against thermal oxidation at 600 ^oC

As discussed in the previous section, it was seen that, by using a plasma oxidation process based on Ar + N_2O for emitter surface passivation, resulted in a marginal improvement in solar cell performance. A higher V_{oc} and a higher R_{sh} were observed for solar cells when the emitter was passivated with SiO_xN_y - SiN_v:H stacks. It was seen that for a longer plasma oxidation duration, better R_{sh} was obtained. This section compares the emitter surface passivation quality of a plasma oxidation process in Ar + N_2O ambient at 380^{o}C with a thermal oxidation process at 600^{o}C. The films are capped with silicon nitride and is used as emitter surface passivation layer in screen printed solar cells. The performance of the solar cells is compared and the potential cause behind solar cell performance variation is also discussed in this section. The respective oxidation processes were carried out for 40 min, and the same PECVD SiN_v:H film was used for capping.

6.3.1 Experiment details

As cut, 125 mm x 125 mm, p-type Cz <100> wafers with 1 - 3 Ω cm resistivity were used as starting material. Following saw damage removal, texturization and RCA cleaning, the wafers were loaded into a phosphorus diffusion furnace. Following diffusion and PSG removal, the samples were taken for plasma oxidation process and the thermal oxidation process respectively.

Plasma oxidation process was carried out in Ar + N_2O ambient for 40 min. An RF power of 10 W was used for the process. Chamber temperature and pressure was maintained at 380^{o}C and 1000 mTorr respectively during the process. The thermal oxidation was carried out in N_2 + O_2 (2 : 3) ambient in a furnace maintained at 600 ^{o}C for 40 min. 600 ^{o}C was chosen so as to minimize the impact on the phosphorus diffusion profile during the oxidation step. Following the oxidation process, edge isolation process was carried out. The wafers were then capped with SiN_v:H film in a PECVD. Screen printed Ag and Al were used as top and bottom contacts, and were fired in a RTA at 850^{o}C. The solar cell IV was measured in a class AAA solar simulator under AM 1.5G spectrum. The detailed process flow is shown in Fig. 6.17. More details of the process flow are described in Appendix B. A modification is made to the process flow as compared to previous experiments. The edge isolation step is carried out after the thermal/plasma oxidation process prior to silicon nitride deposition. Suns - Voc measurements were carried out on finished solar cells to extract the pseudo fill factor (pFF), ideality factor (n) and emitter saturation currents, J_0 (J_{01}, J_{02}) at AM 1.5, 1 sun illumination.

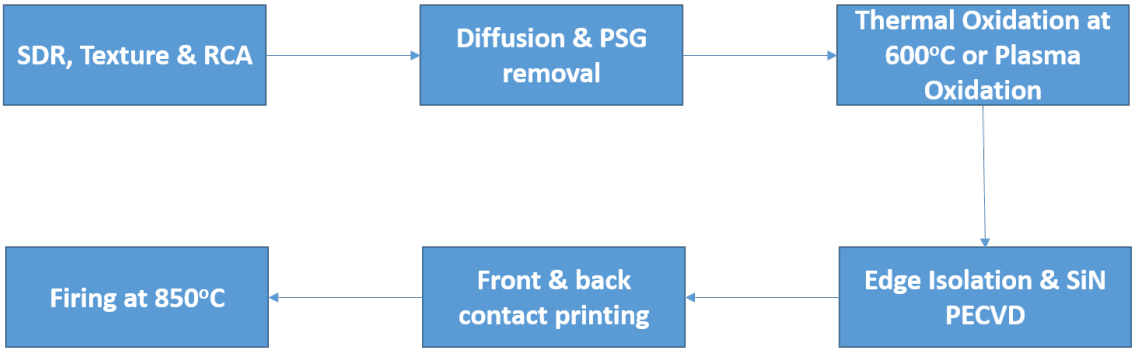


Fig. 6.17: Process flow used for solar cell fabrication.

6.3.2 Physical characterisation of thermally grown film

XPS measurements were carried out on the thermally grown SiO_x film. The spectrum of this film was compared with that of a film grown in Ar + N_2O plasma ambient for 40 min. The results are shown in Fig. 6.18. Two distinct peaks corresponding to the Si - Si signal coming from the substrate as well as signals corresponding to Si - O - Si bonds can be seen at binding energies of 97.5 eV and 101.8 eV respectively. However, as the thickness of the film increases, the XPS signal from the substrate becomes weaker. The lower intensity of the Si - Si signal corresponding to the substrate observed for the plasma grown film indicates that the thickness

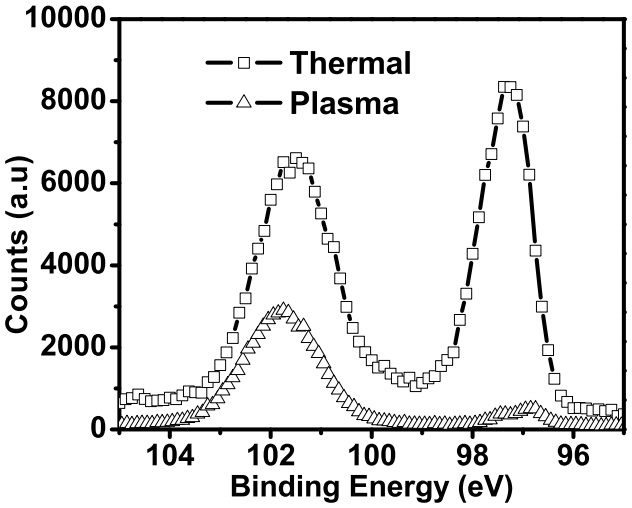


Fig. 6.18: Si2p spectrum for thermal and plasma grown films.

of the thermal grown film is significantly lower as compared to the plasma grown film. XPS measurement, confirms that a thin oxide film was grown as a result of annealing the sample at 600^{o}C in the furnace in $N_2 + O_2$ ambient. N1s spectrum for the corresponding film did not show any signal corresponding to nitrogen, indicating the absence of nitrogen within the thermally grown film.

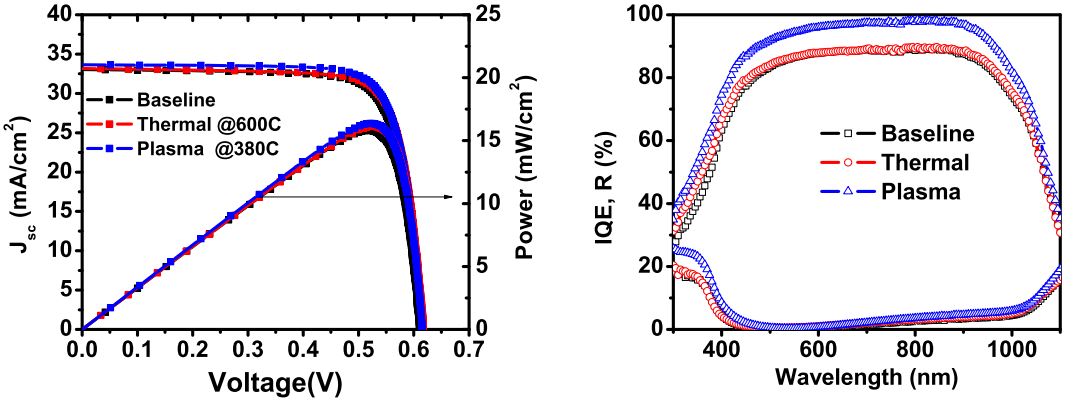
6.3.3 Solar cell results and discussion

The illuminated IV characteristics of the solar cells are summarised in Table 6.4. As can be seen, the best V_{oc} was obtained for the solar cell based on thermal oxide. V_{oc} for the plasma oxidised sample was 1 mV less than the thermal oxide sample, indicating that it can offer equivalent level of surface passivation as compared to the thermal oxide film grown at 600 ^{o}C. The samples grown with the plasma oxide was found to have a higher shunt resistance. The higher R_{sh} and lower R_s for the solar cell based on plasma oxidised sample, resulted in a higher fill factor, thereby pushing the efficiency beyond the thermal oxide sample. Similar to what was observed for other solar cells passivated with SiO_xN_y - SiN_v:H stack, a higher J_{sc} was observed for the plasma oxide sample.

The IV characteristics of the fabricated solar cells are shown in Fig. 6.19(a). Higher current and better fill factor can be seen for the solar cells with an emitter surface passivation based on plasma grown SiO_xN_y - SiN_v:H stack. The internal quantum efficiency for the cells are compared in Fig. 6.19(b). Solar cells passivated (front) with plasma grown SiO_xN_y - SiN_v:H

Table 6.4: Solar cell characteristics comparing plasma grown SiO_xN_y film with that of thermally grown SiO_x film.

Cell Label	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF(%)	η(%)	R_s(Ω cm^2)	R_{sh}(Ω cm^2)
Baseline	611	33.03	78.4	15.80	0.494	780
Thermal (CT)	617	33.17	78.8	16.20	0.452	867
Plasma (CP)	616	33.66	79.1	16.40	0.439	4727



(a) (b)

Fig. 6.19: (a) Illuminated IV and (b) IQE and reflectance curves, comparing the passivation quality of plasma grown SiO_xN_y film with that of thermally grown SiO_x film. The films are capped with baseline silicon nitride film. IQE, R for baseline SiN film is also shown in figure. The lower IQE for the mid wavelengths (450 - 900 nm) observed for two samples, is possibly due to the lower R_{sh}. An improvement in short wavelength response can be seen for plasma grown SiO_xN_y film film as well thermally grown SiO_x film.

stack demonstrated an improved internal quantum efficiency in the short wavelength (300 - 400 nm) region compared to solar cells passivated with thermally grown SiO_x - SiN_v:H stack. The better short wavelength response is representative of an improvement in the emitter passivation quality. The improved short wavelength response have resulted in a better current for the solar cells passivated with the plasma grown SiO_xN_y - SiN_v:H stack. The lower IQE in the mid wavelength regime (450 - 900 nm) can be due to the lower R_{sh} for the cells passivated with the thermally grown SiO_xN_y - SiN_v:H stack and baseline SiN_v:H film. Suns - V_{oc} measurements were used to further analyse the solar cells. The results are summarised in Table. 6.5

Table 6.5: Suns - V_{oc} data comparing solar cells based on plasma and thermal oxidation.

Cell Label	R_{sh}(Ω cm^2)	pFF(%)	pη(%)	n(1 sun)	J_{01}(A/cm^2)	J_{02}(A/cm^2)
Thermal (CT)	2037	80.7	16.40	1.02	$1.0\text{x}10^{-12}$	$3.0\text{x}10^{-8}$
Plasma (CP)	4042	82.1	16.60	0.98	$1.4\text{x}10^{-12}$	$1.2\text{x}10^{-8}$

From Suns - V_{oc} data, it can be seen that cell - CT have a lower J_{01} value compared to that of cell - CP, indicating better post processing lifetime for the solar cell passivated with SiO_x/SiN_y:H layer. However, the trend was reversed in case of J_{02}, wherein cell - CP showed a lower value compared to cell - CT, indicating a reduction in recombination. However it is also possible that the higher J_{02} for cell - CT may also be the result of non idealities brought about by the presence of localized shunts present in cell - CT. This improvement in J_{01} maybe attributed to an improvement in the bulk lifetime, potentially due to phosphorus induced gettering [137]. Thus from EQE and Suns - V_{oc} data, it can be concluded that the improvement in V_{oc} for solar cells passivated with thermal SiO_x based stack maybe the result of an improvement in bulk lifetime, where as the improvement in V_{oc} for the plasma grown SiO_xN_y based stack maybe due to an improvement in emitter surface passivation.

The increase in V_{oc} observed for the plasma grown SiO_xN_y - SiN_y:H stack was observed across different batches of solar cells. As the baseline process improved further, a 5 mV improvement in V_{oc} was still observed for solar cells passivated with the SiO_xN_y - SiN_y:H stack. In one of the batches, a texture additive was used during the texturization process, which improved the V_{oc} of the baseline (reference cell) to 614 mV. The corresponding V_{oc} for the cell with SiO_xN_y - SiN_y:H stack was 619 mV. The same is represented in Fig. 6.20, thereby confirming the repeatability of the process.

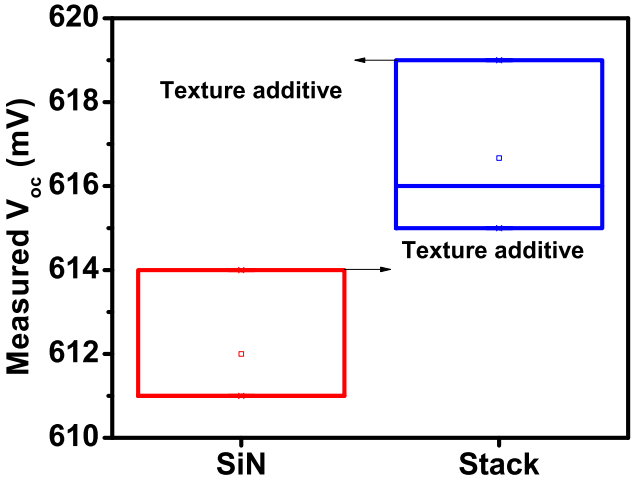


Fig. 6.20: Improvement in V_{oc} for the stack across different solar cell batches.

Loss analysis of the solar cell with 16.4% efficiency

A detailed loss analysis of the 16.4% efficient solar cell was carried out using the technique described by Aberle et al. [138]. The solar cells reported in [138] had a V_{oc} of 624.4 mV, J_{sc} of 37 mA/cm^2, FF of 78.6% and η of 18.1%. The results of the loss analysis carried out on the 16.4% efficient solar cell is summarised in Fig. 6.21. The major part of the loss was constituted by non perfect IQE, contributing 49% of the total loss compared to the 36% reported by Aberle et al. [138]. Non - perfect IQE is the result of the recombination losses on the front, rear and bulk of the silicon solar cell. Improving the emitter doping profile, and the quality of the surface passivation layer, the blue response of the solar cell can be improved. The next major component of the loss is constituted by metal shading and forward bias current at maximum power point (MPP). Lowering the contact dimensions can significantly improve the performance of the solar cell.

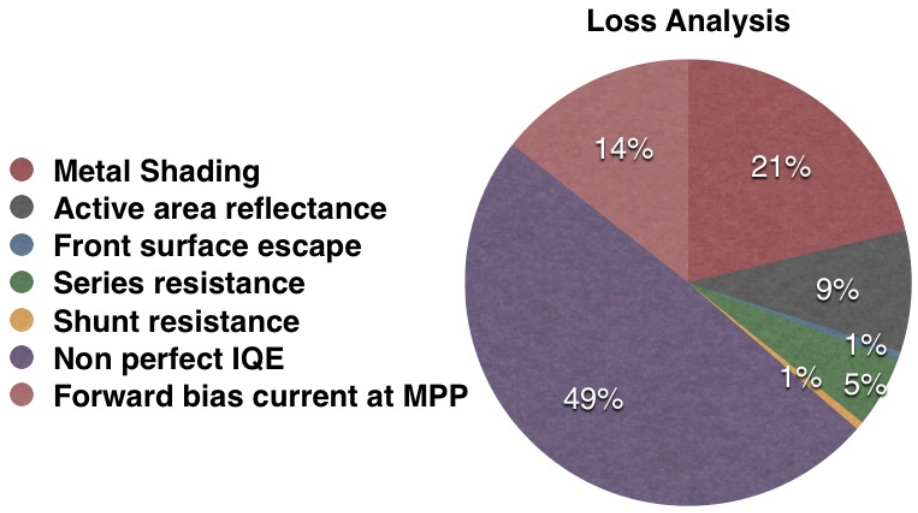
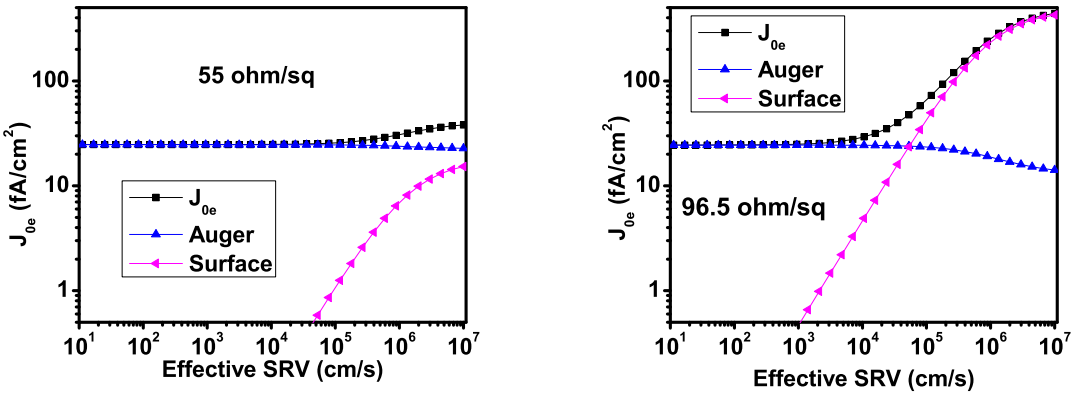


Fig. 6.21: Loss analysis carried out on the 16.4% solar cell. Non perfect IQE is seen to contribute close to 50% of the total loss in the solar cell under investigation.

As seen from the loss analysis, one of the key reasons for the poor performance of the solar cell is non perfect IQE of the solar cell. One of the possible reason is the presence of a dead layer in the emitter used for the fabrication of the solar cell. The solar cells discussed through out this thesis, have used a heavily doped emitter with a sheet resistance of 45 Ω/□ compared to the 70 Ω/□ sheet resistance reported in [138]. SIMS profiles for these emitters have indicated the presence of a dead layer, which can contribute significantly to emitter recombination [139]. Hence, the effect of an improved surface passivation may not be evident for such heavily doped

emitters. The contribution of surface recombination to the net emitter saturation current for two different emitters is shown in Fig. 6.22. Fig. 6.22 indicates the results of a simulation carried out using EDNA 2 simulator, available online on PVlighthouse.com. The simulation had assumed a p-type wafer with a resistivity of 1 Ω cm. The phosphorus emitter doping profiles were loaded from the previous SIMS results. The results of the simulation presents a qualitative picture on the impact of surface SRH on the net recombination/saturation current. The net emitter saturation current density indicated in Fig. 6.22 is the sum of recombination currents which includes Auger recombination, SRH recombination in bulk, radiative recombination and surface SRH recombination. In Fig. 6.22, only the components from surface and Auger recombination are indicated as the other two components were significantly lower. For heavily doped emitters, the impact of surface SRH recombination on the net emitter saturation current density is negligible, whereas Auger recombination within the emitter is seen to significantly dominate the emitter saturation current density. The scenario is reversed in case of lightly doped emitters. The contribution of surface recombination to net J_{0e} is significantly higher, while Auger recombination component dominates only for very low values of surface recombination velocities. The simulation gives a qualitative picture on the impact of the emitter doping profile on the effective surface recombination properties. The absolute values of J_{0e} measured in our samples are significantly higher than what was seen from the simulations.



(a) (b)

Fig. 6.22: Impact of surface SRH on different emitter sheet resistances (a) 55 Ω/□ (b) 100 Ω/□.

Looking ahead to the future, the improvement in emitter doping profile can bring about a significant improvement in the blue response of the solar cell. Etching a part of the emitter in isotropic etchants like HNA ($HF + HNO_3 + CH_3COOH$) is one of the possible options that may

be used to remove the dead layer present in the solar cells. Careful process development maybe needed before the process is implemented into the solar cell fabrication process. Reducing the contact area can also potentially improve the solar cell performance by further lowering the shadow losses resulting in an improvement in J_{sc}. The reduction in contact area can also bring about an improvement in the open circuit voltage thereby boosting the cell performance further.

6.3.4 Conclusion

A solar cell fabricated with a thermally grown oxide - SiN_y:H stack was found to have an equivalent performance as that of a solar cell fabricated with a plasma grown SiO_xN_y - SiN_y:H stack. However higher R_{sh} was observed for the the plasma grown SiO_xN_y - SiN_y:H stack. The advantage of the plasma process comes in from the low temperature of processing as compared to the thermally grown oxide. The performance improvement observed for the plasma grown SiO_xN_y - SiN_y:H stack was confirmed by fabricating solar cells across three different batches. Loss analysis carried out on solar cells indicated that the non perfect IQE was the major contributor to the loss in the solar cell. The presence of dead layer was concluded as one of the major causes behind the poor blue response of the solar cells. Dead layer removal as well as higher sheet resistance emitters are stated as potential options for improving the blue response. Lowering the shadowing losses due to the metal contacts can also result in an improvement in J_{sc}, and is also suggested as a scheme for further performance improvement. Another problem area for the solar cells reported in this thesis was the lower R_{sh} for the baseline (reference) solar cells. The next section discusses the optimisation of the front surface passivation and ARC layer for further enhancement in cell performance. The section includes a detailed discussion on some of the potential causes for the shunt formation in the solar cells discussed so far in this thesis. Some of the methods attempted towards the mitigation of shunts is also discussed in the next section.

6.4 Optimisation of the front surface passivation and ARC layers

From the loss analysis discussion in the previous section, it was seen that a non perfect IQE contributed to 49% of the loss in the solar cell described so far in this thesis. Compared to the

solar cells discussed so far in this thesis, industrial silicon solar cells have a higher V_{oc} and higher shunt resistance. This section discusses the further process optimisation of the silicon nitride front surface passivation layer in order to improve the shunt resistance as well as the V_{oc}.

Shunts in silicon solar cells can be the result of a wide range of reasons starting from a material defect to a process induced defect or crack on a wafer. Breitenstein et al. broadly classifies the the potential causes for shunts in single crystalline silicon solar cells as (a) process induced defects and (b) material induced shunts [140]. Process induced shunts include scratches, cracks on wafers, presence of residual Al on the front surface, shunts along the wafer edge and over firing of emitter contact, to name a few. Material induced shunts are mainly reported for multi crystalline silicon wafers and these include highly recombinative bulk defects and grain boundaries, silicon nitride inclusions etc. [140]. Lock In Thermography (LIT) is typically used for the investigation of localised shunts in solar cells [140]. However, due to the lack of availability of LIT set up, an elimination approach based on process modification, was used to deduce the potential cause of the shunts in the solar cells reported in this thesis.

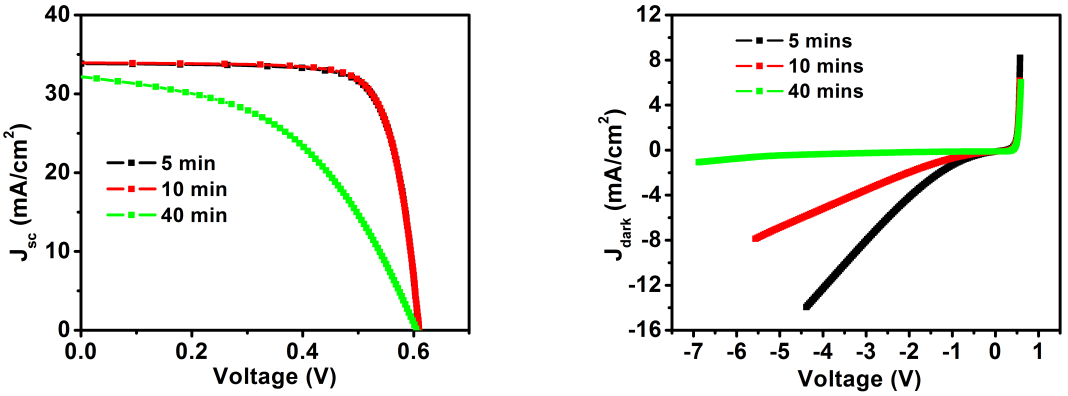
6.4.1 Role of contact firing process

One of the primary suspect was the over firing of Ag through the junction at localised points on bus bar and fingers. In order to investigate this aspect, crystalline silicon solar cells were fabricated using screen printing technology. Silicon oxy-nitride films were grown in Ar + N_2O ambient for 5, 10 and 40 min on the emitter side of the wafer. Silicon oxy-nitride films were capped with silicon nitride film which served as the anti-reflective coating. Screen printed Ag and Al were used as the front and rear contact respectively. All the solar cells were fired at 850^oC in N_2 ambient.

Table 6.6: Solar cell characteristics for varying Ar + N_2O plasma oxidation duration.

Cell Label	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF(%)	η(%)	R_s(Ω cm^2)	R_{sh}(Ω cm^2)
5 min	609	33.84	76.9	15.90	0.50	236
10 min	610	33.94	77.0	15.93	0.57	624
40 min	605	32.15	48.1	9.4	7.60	12000

From the solar cell characteristics listed in Table. 6.6, no significant variation between 5 and 10 min samples were seen apart from the marginal improvement in R_{sh}. For the 40 min sample, due to the thicker silicon oxy-nitride film, no proper contact could be made with silicon, resulting in a higher R_s. The performance of the sample was found to be below par as compared to

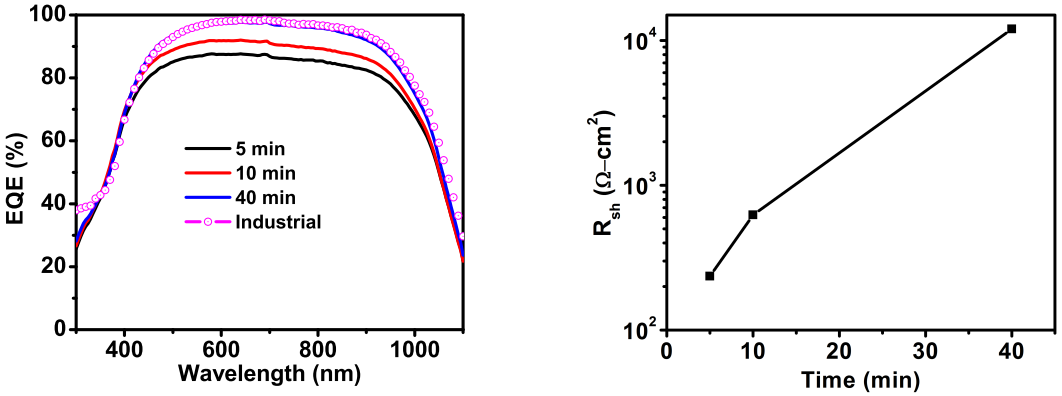


(a) (b)

Fig. 6.23: (a) Illuminated and (b) dark IV characteristics of solar cells fabricated with SiO_xN_y - SiN_y:H.

the other two samples which were properly contacted. Fig. 6.23(a) shows the illuminated IV characteristics for the three devices. The shunt resistance of the solar cell was extracted from the dark IV curve, shown in Fig. 6.23(b). In the reverse bias regime, the reverse saturation current was found to decrease with longer oxidation times. The 40 min sample was seen to have a shunt resistance, which was 20 times better than the other two samples. The reason for this improvement in shunt resistance could not be understood from the illuminated IV characteristics. This improvement in reverse saturation current was seen to translate into a larger shunt resistance. The genesis of the large leakage current in the reverse bias regime, has been attributed to shunts within the solar cells. The sharp increase in the reverse saturation current, at low reverse bias indicates the presence of defect levels, within the band gap of the p-n junction diode [141]. From our experiment, it maybe concluded that the contact firing process, seem to have played a significant role in the formation of shunts. The shunts can be formed under the bus bars as well as fingers present in the solar cell. It may thus be concluded that the shunts present in the devices reported in this thesis so far, maybe brought about by the localised diffusion of silver through the junction.

The effect of the shunts could be seen in the measured EQE plots for the solar cells as well. The currents measured during external quantum efficiency measurement is small and hence the impact of series resistance on external quantum efficiency is minimal. The localised shunts within the device resulted in the variation in EQE across the devices, especially in the mid wavelength region. Fig. 6.24(b) shows the variation in shunt resistance across the samples.



(a) (b)

Fig. 6.24: (a) External quantum efficiency of solar cells fabricated with SiO_xN_y - SiN_v:H for varying oxidation durations (b) Improvement in R_{sh} for increasing oxidation time.

However, it maybe noted that the difference in R_{sh} between 5 and 10 min samples is low as compared to what was observed for the 40 min. Despite the smaller variation in R_{sh}, a change in mid-wavelength EQE could be observed between these two samples. It may be thus concluded from the EQE curve in Fig. 6.24(a), that higher the R_{sh}, better the quantum efficiency measurement. EQE for 40 min (under fired) sample is seen to be at par with the industrial solar cell with cell efficiency in excess of 17%. The major impact of shunt resistance on the EQE is observed in the mid wavelength ranges of the visible spectrum.

6.4.2 Role of silicon nitride deposition conditions

Impact of RF power on R_{sh}

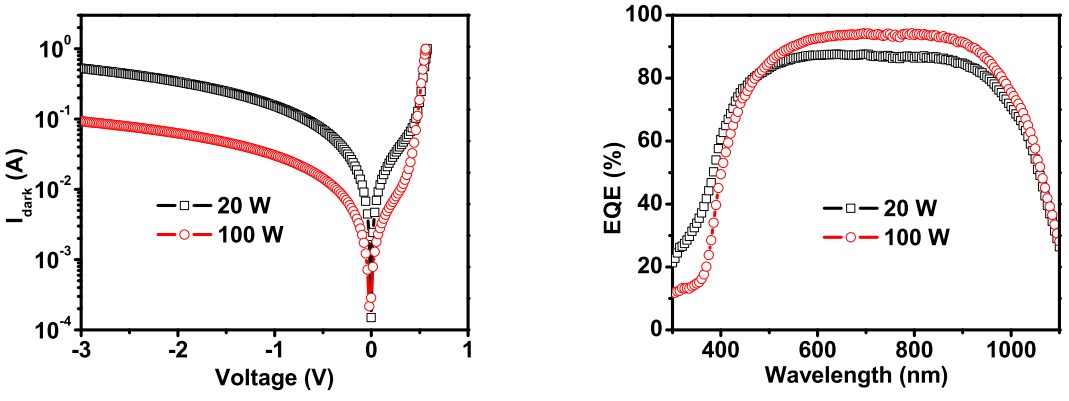
During contact formation on the emitter surface, the silver along with the glass frit melts and diffuses through the silicon nitride layer. At the Ag - Si interface a large number of crystallites are formed [142]. The crystallite formation is dependent on the firing conditions, emitter doping concentration and crystal orientation [143]. However, the diffusion process of the material can be controlled by varying the thickness as well as the density of the silicon nitride layer. Therefore, a denser silicon nitride film would lower the diffusion rate of Ag through the nitride, and this in turn has the potential to lower the shunts formed during contact firing in silicon solar cells. In order to test this hypothesis, the following experiment was carried out. Screen printed silicon solar cells with two different silicon nitride layers were fabricated. The solar cells differed in that the silicon nitride passivation layer was deposited at 20 W and 100 W

respectively on these cells. The deposition time was modified to ensure that both the solar cells had comparable thickness of ARC layer. The characteristics of the solar cells are summarised in Table 6.7.

Table 6.7: Solar cell characteristics for different plasma deposition power.

Cell Label	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF(%)	η(%)	R_s(Ω cm^2)	R_{sh}(Ω cm^2)
20 W	611	33.03	78.4	15.80	0.49	780
100 W	600	32.22	78.9	15.20	0.46	6782

A significant improvement in R_{sh} was observed when the RF power used for deposition was raised from 20 to 100 W. Higher RF power would imply more energetic collisions and hence higher density for silicon nitride films. However, the downside was the decrease in V_{oc} brought about by the increased plasma damage on the silicon surface during SiN deposition. Fig. 6.25(a) shows the dark IV curve for the two solar cells. Lower J_{dark} is observed in the reverse bias region for the 100 W sample, confirming the increase in shunt resistance. In the forward bias regime, the current for the 20 W sample was dominated by the leakage currents through the shunts. Fig. 6.25(b) shows a decreased external quantum efficiency on the emitter side for the 100 W sample, due to the higher plasma damage during deposition of the silicon nitride film.



(a) (b)

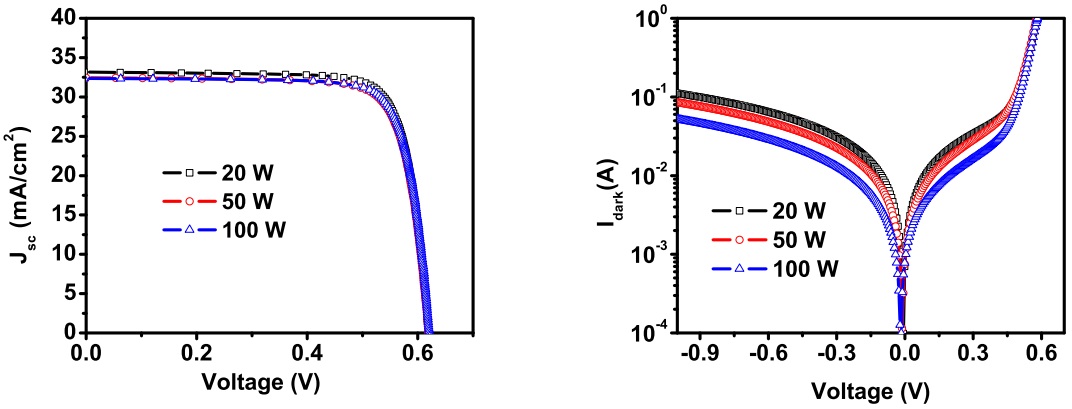
Fig. 6.25: (a) Dark IV and (b) external quantum efficiency for solar cells fabricated with two different silicon nitride films.

Higher plasma powers lead to a decrease in shunt resistance, but resulted in significant loss in V_{oc} due to the plasma damage on the Si surface. In order to mitigate the issue of plasma damage, the silicon nitride deposition was split into two steps. The first deposition was

carried out at 20 W power, followed by deposition at higher power. The hypothesis behind this experiment was that the bottom layer will act as a shield against plasma damage incurred during the high power deposition. Fig. 6.26 shows the illuminated and dark IV characteristics of solar cells fabricated using these bilayer silicon nitride films. 20 W represents the reference sample, while 50 W and 100 W represents the RF power used for depositing the capping layer. As expected, the shunt in the solar cells came down for higher plasma deposition conditions. The results are similar to what was shown in Fig. 6.25(a), with the higher power deposition showing a significantly higher shunt resistance. The splitting up of the deposition into two steps also lowered the plasma damage resulting in a similar V_{oc} for all the samples, as shown in Table. 6.8. Thus it maybe concluded that densifying the silicon nitride film may result in a significant improvement in R_{sh}.

Table 6.8: Solar cell characteristics for different plasma deposition power for the capping silicon nitride layer.

Cell Label	V_{oc}(mV)	J_{sc}(mA/cm^2)	FF(%)	η(%)	R_s(Ω cm^2)	R_{sh}(Ω cm^2)
20 W	619	33.22	79.2	16.30	0.490	1695
50 W	619	32.43	78.8	15.80	0.500	2000
100 W	621	32.36	79.60	16.00	0.488	3466



(a) (b)

Fig. 6.26: (a) Illuminated and (b) dark IV characteristics for solar cells fabricated with different silicon nitride films.

6.4.3 Thermally grown SiO_x films - bilayer silicon nitride films for improved front surface passivation

Based on the discussions in the previous section, it maybe concluded that, using a denser silicon nitride film resulted in a significant improvement in R_{sh}. However, high power deposition results in significant plasma damage, resulting in a loss in V_{oc}. A two step deposition process was proposed in order to eliminate the loss in V_{oc}, by mitigating the plasma damage. Using this approach, a bilayer silicon nitride film was developed, in order to improve the R_{sh}. The recipe details are given below:

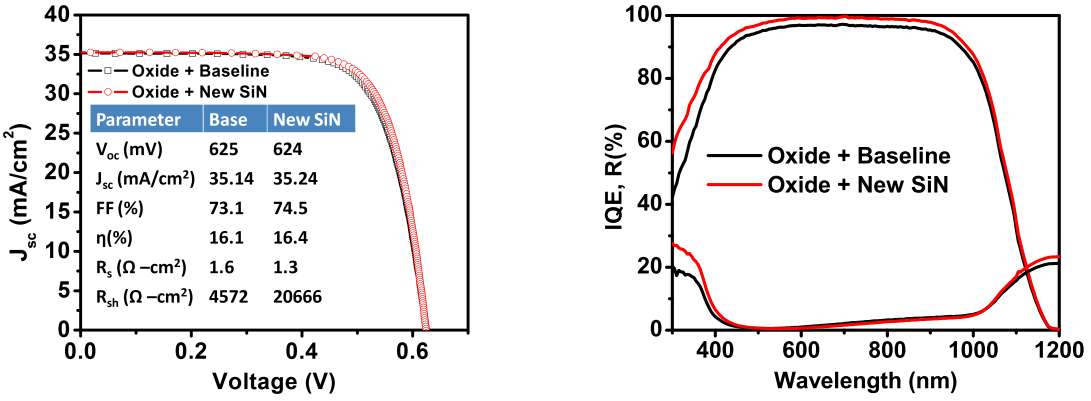
- Bottom layer: SiH_4: N_2 :: 20 sccm : 980 sccm, NH_3 = 20 sccm, Ar = 40 sccm, H_2 = 5 sccm, 220 s, 380^{o}C, 650 mTorr, 20 W.
- Capping layer: SiH_4: N_2 :: 18 sccm : 980 sccm, NH_3 = 20 sccm, Ar = 40 sccm, H_2 = 5 sccm, 50 s, 380^{o}C, 1000 mTorr, 100 W.

As shown in Fig. 6.20, further improvements in texturization process was found to improve the V_{oc} of the baseline process by almost 3 - 4 mV. Further, a thermal oxidation of the diffused silicon wafer at 600^{o}C in N_2 + O_2 ambient also resulted in an improvement in V_{oc}, as was discussed in section 6.3. Therefore by combining these two schemes a significant improvement in V_{oc} maybe obtained.

Based on the above hypothesis, an experiment was designed, wherein the cell fabrication process included the three schemes (one for R_{sh} improvement, two for V_{oc} improvement) discussed in this section. The process flow used for the fabrication of the solar cell remained same as the one described in Fig. 6.17. Following SDR and texturization the samples were loaded into a furnace for phosphorus diffusion. The sheet resistance of the samples after the phosphorus diffusion process was $\sim$ 65 Ω/□. Following PSG removal, samples were loaded into a furnace. The samples were oxidised in N_2 + O_2 ambient at 600^{o}C for 1 hour. This was followed by edge isolation and deposition of the silicon nitride layer. Two different silicon nitride films were deposited. On one sample, the baseline silicon nitride recipe was used and on the other sample, the new bilayer silicon nitride film was used. Subsequently, front and rear contacts were screen printed and cofired in a RTP chamber at 850^{o}C, in N_2 + O_2 ambient.

The results of the solar cell characterisation are indicated in Fig. 6.27. V_{oc} for the samples were found to increase significantly to $\sim$ 625 mV. As expected, a significantly higher R_{sh} was

observed for the solar cell fabricated with the new silicon nitride recipe. A higher R_s was seen for both the solar cells, thereby lowering the FF and hence the efficiency. Further, the new SiN film also resulted in an improvement in J_{sc}. IQE and reflectance curves for both the solar cells are shown in Fig. 6.27(b).



(a) (b)

Fig. 6.27: (a) Illuminated IV characteristics for solar cells fabricated with two different silicon nitride films. A higher R_{sh} and J_{sc} was observed for the new SiN film (b) IQE curves indicating a better passivation quality for the newly developed SiN film as compared to the baseline silicon nitride film.

6.4.4 Conclusion

Shunt formation in c - Si solar cells was found have a strong dependence on the nature of the silicon nitride film used as the anti-reflective coating. The lower R_{sh} value resulted in a loss of fill factor and hence solar cell performance. Additionally, it also resulted in inaccurate measurement of EQE, making data interpretation and analysis difficult. R_{sh} was improved for the solar cell by using a bilayer silicon nitride film, resulting in R_{sh} values as high as 20666 Ω cm^2. By incorporating a modified texturization process and a low temperature thermal oxidation step at 600^oC, V_{oc} as high as 625 mV was obtained.

6.5 Conclusions

The chapter discussed in detail about the integration of plasma oxidation process into the silicon solar cell process flow. Plasma oxidation in N_2O ambient was found to result in an improvement in blue response of the solar cell, but resulted in a lower R_{sh}. R_{sh} was however seen to

improve for longer plasma exposure duration possibly due to a decrease in interstitial oxygen content for longer plasma exposure. The improved blue response however resulted in a marginal improvement in J_{sc} of the solar cells fabricated with the SiO_xN_y - SiN_v:H stack as the emitter passivation layer. The improvement in blue response was attributed to the lower plasma damage on the wafer surface during silicon nitride deposition. However, a decrease in τ_{bulk} potentially due to interstitial oxygen was observed for both FZ and Cz wafers. The degradation in τ_{bulk} was more severe on FZ wafers than on P-doped Cz wafers. Upon addition of argon into the oxidation process,the improvement in blue response of the quantum efficiency resulted in an improvement in V_{oc} and R_{sh} was observed. The improvement in emitter passivation for Ar + N_2O oxidation was further confirmed by τ_{eff} measurements. A sharp increase in R_{sh} was observed for longer duration of growth in Ar + N_2O plasma ambient.

Compared to a thermal oxidation process carried out 600^oC, plasma oxidation process resulted in similar V_{oc} improvement for a given baseline process. However, at the high temperatures of growth of thermal oxides (800 - 1100 ^oC), the emitter doping profiles can also be modified leading to a loss of one to one correlation. Hence, a careful design of experiment maybe required to compare the plasma oxide with thermal oxides grown at higher temperatures.

The localised shunts in the solar cells discussed in the thesis, was found to have a strong dependence on the contact firing process as well as the silicon nitride deposition condition. Carrying out the silicon nitride deposition at a higher plasma power was found to bring down the shunts but resulted in a V_{oc} loss due to plasma damage on the emitter surface. A two step silicon nitride deposition process was found to minimise the impact of plasma damage on the emitter surface. Higher R_{sh} was obtained for solar cells passivated with these silicon nitride films. No loss in V_{oc} was observed, indicating that the emitter surface passivation quality remained unaffected.

Chapter 7

Impact of post deposition plasma treatment on surface passivation properties of silicon nitride films

7.1 Motivation

Hydrogenated silicon nitride films have been widely used as an anti-reflective coating (ARC) and a front surface passivation layer in c - Si solar cells. Silicon nitride (SiN_y:H) deposited using PECVD is known to yield very good surface passivation on low doped n-type and p-type wafers, as well as on n^+ emitters [51]. Replacing silver with copper for emitter contact metallisation is foreseen for industrial silicon solar cell technology [3]. Electroplating or light induced plating are leading candidates for deposition of copper. Compared to the existing screen printed Ag based metallisation processes for solar cells, not only is Cu cheaper, but also offers some other advantages. By using electroplated Ni - Cu contacts the aspect ratio of the front surface metal contact can be improved. This can reduce the metal shadowing losses and thereby improve the J_{sc} [144]. It is also reported that Ni - Cu contacts make a low contact resistivity with silicon, compared to screen printed Ag [144]. However, the low density of the PECVD silicon nitride films make it susceptible to the formation of pin holes [5]. Presence of foreign particles and scratches on the wafer surface can also further enhance the formation of pin holes in case of PECVD silicon nitride [5]. Pin holes in silicon nitride can act as nucleation centres during metal deposition process via suitable plating process. This undesired plating, referred to as background plating, can lead to additional recombination losses degrading solar

cell performance. Efforts to reduce background plating have focused on modifying the silicon nitride layer by altering the PECVD deposition conditions [16, 145] or by introducing various treatment steps on the silicon nitride. One such treatment step involves exposing the PECVD SiN_y:H film to an oxidising ambient. The oxidation of silicon under the pin holes is reported to bring about a reduction in background plating [17]. Also, stacks of SiO_2 - SiN [6], SiO_x(C) - SiN [146] have been used to reduce background plating. Inert gas plasma treatment of silicon nitride films is known to result in its densification, thereby lowering the pin hole density. An argon plasma treatment of silicon nitride films is known to lower pin hole density [147] and also improves moisture resistance in case of hot wire CVD silicon nitride films [148]. Therefore by treating a silicon nitride film in an inert gas + oxidising plasma ambient, not only can the SiN film be densified but also oxidise the silicon surface exposed under the pin holes. We have recently demonstrated a significant reduction in background plating using this approach [19]. The fill factor of the cells with post plasma treatment of the nitride was seen to improve over the case where no post deposition plasma treatment was applied. This has lead to the development of a Ni - Cu contact process with an active area efficiency of 18.2%. The silicon nitride film in question was treated in an Ar + N_2O plasma ambient for 10 min [19].

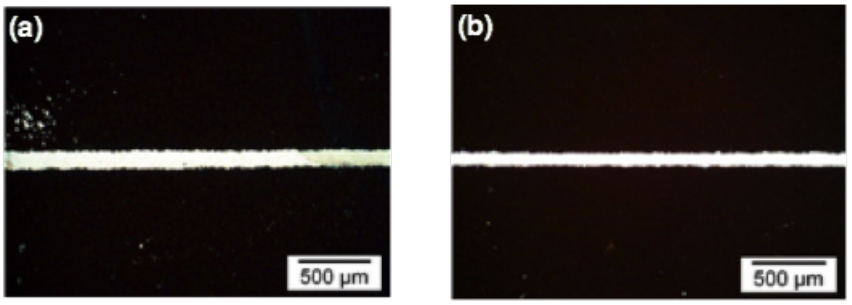


Fig. 7.1: (a) Background plating observed in untreated sample after Ni - Cu plating (b) Reduction in background plating in plasma treated sample after Ni - Cu plating[19].

Plasma treatment of silicon nitride in N_2O ambient was reported to result in an increase in D_{it} and Q_f at the Si - SiN interface [18]. The increase in interface state density was attributed to the damage incurred on the silicon nitride film as a result of plasma treatment. Similar degradation in passivation quality of PECVD silicon nitride films following ammonia plasma exposure at room temperature was reported by Wan et al. [62]. A significant change in the chemical composition was also observed [62]. Vernhes et al. reported that an argon plasma treatment on PECVD silicon nitride can lower the N - H bond density in silicon nitride films [149]. The bond breakage was attributed to an increase in temperature owing to the plasma

treatment. This rise in temperature is reported to result in annealing of bulk silicon nitride film, leading to breakage of N - H bonds within the film. FTIR spectroscopy confirmed a reduction in N - H bonds and a corresponding increase in the Si - N bond intensity. As reported by Vernhes et al., if the plasma treatment can result in a rise in temperature of the silicon nitride and subsequent release of hydrogen within the SiN bulk, it can significantly alter the Si - SiN interface characteristics. However, the focus of Vernhes et al. was to study the impact of plasma treatment on surface roughness of silicon nitride film, and hence no investigation of electrical characteristics of the Si - SiN interface was carried out [149]. Similar inert gas + nitrogen plasma treatment on silicon nitride was used to remove hydrogen from silicon nitride film, used as a charge trapping layer in floating gate memory devices [150].

In this chapter, the impact of a post deposition plasma treatment on PECVD SiN films and its interface with silicon is discussed. The plasma treatment process is carried out in a capacitively coupled PECVD chamber and is integrated with the silicon nitride deposition process. Following Ar + N_2O plasma treatment, effective lifetime (τ_{eff}) improved from 266 μs to 863 μs (at MCD of 10^{15} cm^{-3}) on an n-type FZ wafer. The underlying mechanism behind the improvement in τ_{eff} is investigated, and the results are summarised. The improvement in τ_{eff} was seen to be strongly correlated to a sharp decrease in D_{it} as well as an increase in Q_f. D_{it} decreased by an order of magnitude from 2.5x10^{11} $eV^{-1}cm^{-2}$ to 2.3x10^{10} $eV^{-1}cm^{-2}$, while Q_f increased from 1.2x10^{12} cm^{-2} to 1.7x10^{12} cm^{-2}. The enhancement in τ_{eff} was observed on n^+ emitter surfaces and p-type textured surfaces as well. τ_{eff} was seen to improve for different plasma ambients like He, Ar and Ar + N_2O. The thermal stability of the improvement in passivation is seen to be adequate for the thermal budgets typically used for post Cu metallisation anneals. From our experiments, it was concluded that the improvement in τ_{eff} was the combined effect of substrate induced thermal annealing and plasma exposure during the post deposition plasma treatment process of the silicon nitride film. Thus, an Ar + N_2O plasma treatment of silicon nitride not only results in a significant reduction in background plating but also improves the τ_{eff}, thereby making it a promising candidate for fabricating low temperature PERC/PERL solar cells with Ni - Cu based electroplated contacts [4].

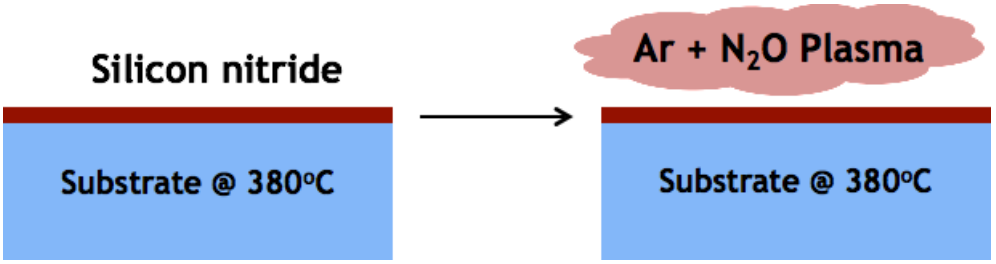


Fig. 7.2: Schematic of the plasma post treatment process of silicon nitride.

7.2 Experiment details

RCA cleaned, double side polished, 300 μm thick n-type, FZ <100> Si wafers with resistivity of 3 Ω cm was used for the experiments. Hydrogenated silicon nitride films were deposited in a PECVD tool (Plasmalab 100, Oxford instruments) using silane (diluted in N_2) and ammonia as process gases, at a temperature of 380^{o}C. RF power was kept at 20 W and chamber pressure was 650 mTorr. Following silicon nitride deposition, the samples were exposed to an Ar + N_2O plasma for 10 min in the same chamber without breaking the vacuum. An RF power of 10 W and chamber pressure of 1 Torr was used for the plasma treatment step. Lifetime measurements were carried out in a WCT lifetime tester from Sinton instruments after depositing the silicon nitride on both sides of the wafer. ARXPS and FTIR measurements were carried out to investigate the impact of plasma treatment on the surface and bulk chemical composition of silicon nitride film. MIS capacitors with aluminium as gate and bottom electrode were fabricated on n-type FZ wafers to investigate the silicon - silicon nitride interface properties. Firing of silicon nitride was carried out at 850^{o}C for 1 s in a rapid thermal annealing system in an N_2 + O_2 ambient. The thermal stability studies were carried out in an N_2 ambient in a furnace for 1 min in N_2 ambient at 450^{o}C, simulating the conditions used for sintering of Ni - Cu contacts.

7.3 Results and discussion

7.3.1 Physical characterisation of plasma treated silicon nitride film

FTIR measurements were carried out to investigate the impact of plasma treatment on the chemical composition of the silicon nitride film. The ratio of Si - H bond density before and after plasma treatment was found to be 1.01, while the corresponding ratio for N - H bond was found to be 1.02. The bond densities were calculated based on the technique described by Wan et al.

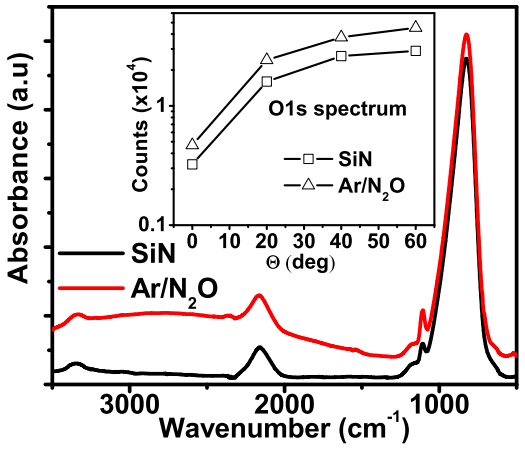
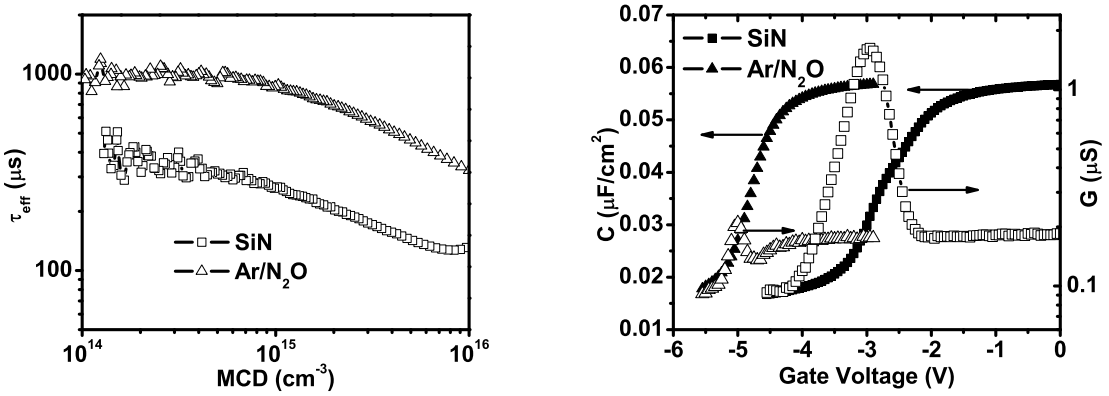


Fig. 7.3: FTIR spectrum showing no significant change in Si - H or N - H bond intensity following plasma treatment. Inset shows ARXPS O1s spectrum showing an increase in O-count after Ar + N_2O plasma post treatment.

[151]. Unlike what was reported by Vernhes et al., no significant change in Si - H or N - H bond intensity was seen following the plasma treatment [149]. An increase in Si - O bond density, centered at 1105 cm^{-1}, was the only difference between the post treated sample and its reference. The plasma power used in our experiment may have been too low to result in a change in chemical composition of the silicon nitride bulk. From ARXPS measurements on plasma treated and untreated samples, it was found that the amount of silicon and nitrogen for both the samples were identical. However, the oxygen signal intensity was seen to go up following the Ar + N_2O plasma treatment, indicating oxygen incorporation into the silicon nitride film as shown in Fig. 7.3. Similar oxygen incorporation in silicon nitride was reported by Bose et al. [18]. The oxygen present in the untreated sample may have been the result of exposing the sample surface to ambient. Thus from the FTIR and XPS measurements, it maybe concluded that the plasma treatment of silicon nitride modified only the near surface region and not its bulk chemical composition.

7.3.2 Capacitance - Voltage and effective lifetime measurements

Ar + N_2O plasma treatment was carried out on a bilayer silicon nitride (SiN) film composed of a thin (∼15nm) silicon rich silicon nitride at the bottom and a stoichiometric silicon nitride on the top (∼70 nm, RI = 2.0). τ_{eff} of sample increased significantly from 266 μs, before plasma treatment, to 864 μs after plasma treatment as shown in Fig. 7.4(a). The lifetimes are



(a) (b)

Fig. 7.4: (a) Improvement in τ_{eff} following Ar + N_2O plasma treatment of silicon nitride film. τ_{eff} measured on n-type FZ wafers (b) HFCV curves (closed symbols) and HFGV curves (open symbols) before and after plasma treatment. A significant improvement in τ_{eff} and a sharp reduction in D_{it} can be observed from the HFCV curves.

quoted at MCD of 10^{15} cm^{-3}. Low energy Ar plasma treatment of silicon nitride is reported to transfer its kinetic energy from the plasma to the silicon nitride film [148]. The transfer of energy from the plasma can result in densification of the film as a result of bond breaking and rearrangement. However, from FTIR studies shown in Fig. 7.3, no changes in N-H or Si-H bond intensity was observed after plasma treatment. Thus by treating silicon nitride films with an Ar + N_2O plasma, not only can the background plating be reduced but an enhancement in minority carrier lifetime can also be attained.

The electrical characteristics of the silicon - silicon nitride interface was investigated by fabricating MIS capacitors. High frequency capacitance and conductance were measured as a function of gate voltage (HFCV and HFGV) at a frequency of 50 KHz. From the HFCV curve in Fig. 7.4(b) it can be seen that the Ar + N_2O treatment resulted in a decrease in skew in HFCV curve indicating a net reduction in interface trap density (D_{it}). The conductance also decreased by an order of magnitude following the Ar + N_2O plasma treatment. Mid-gap D_{it} was extracted using the single frequency approximation method [118]. D_{it} was seen to come down from 2.5x10^{11} eV^{-1}cm^{-2} to 2.3x10^{10} eV^{-1}cm^{-2} upon plasma treatment. The improvement in D_{it} may have been the result of an enhancement in hydrogenation of the Si - SiN interface following the plasma treatment. The HFCV curve was also seen to shift to the left indicating an increase in positive fixed charge density (Q_f) as well. It was found that the Q_f increased from 1.2x10^{12} cm^{-2} to 1.7x10^{12} cm^{-2}. The combined effect of improvement in Q_f as well as a

drastic reduction in D_{it} may have resulted in higher τ_{eff} following Ar + N_2O plasma treatment.

Thermal stability of the enhancement in τ_{eff} was investigated for temperatures typically used for Ni - Cu contact sintering in c - Si solar cells [4]. As shown Fig. 7.5, a significant improvement in τ_{eff} was observed following a 450^{o}C anneal. τ_{eff} of 1239 μs was measured for the sample after annealing it in N_2 ambient at 450^{o}C for 1 min. For the untreated sample, τ_{eff} was 489 μs. Thus it maybe concluded that the improvement in surface passivation quality

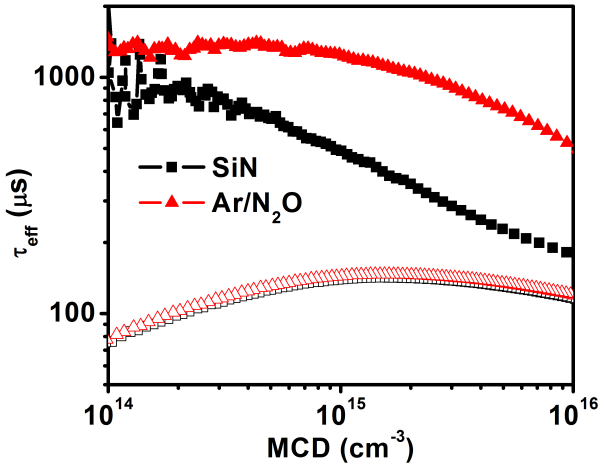


Fig. 7.5: Thermal stability of surface passivation quality for two different annealing conditions. Closed symbols represent 450^{o}C anneal in furnace typically used for Ni - Cu contact sintering, while open symbols represent 850^{o}C firing in RTA typically used for screen printed silver contacts.

was seen to be stable for temperatures used typically for Ni - Cu sintering. Coupled with its potential to reduce background plating, the plasma treatment process maybe an ideal candidate for fabricating low temperature processed c - Si solar cells based on PERC/PERL architectures [4]. Upon firing the samples at 850^{o}C, which is typical of a co-firing step in a screen printed Al - back surface field solar cell, τ_{eff} decreased to 150 μs for both samples, as can be seen in Fig. 7.5, likely due to out diffusion of hydrogen during the firing process. However, similar τ_{eff} obtained following firing indicates that the plasma treatment process does not lead to any deterioration in surface passivation quality of the silicon nitride film. Hence, the plasma treatment process can also be used for reducing background plating in high temperature processed solar cells with electroplated Ni - Cu contacts on the front surface [5].

UV- stability studies of the passivation layers were also carried out in a UV exposure chamber. The films were not annealed prior to UV exposure. The samples were exposed to a 365 nm UV light for varying time duration. The lifetime was measured for each time interval. The

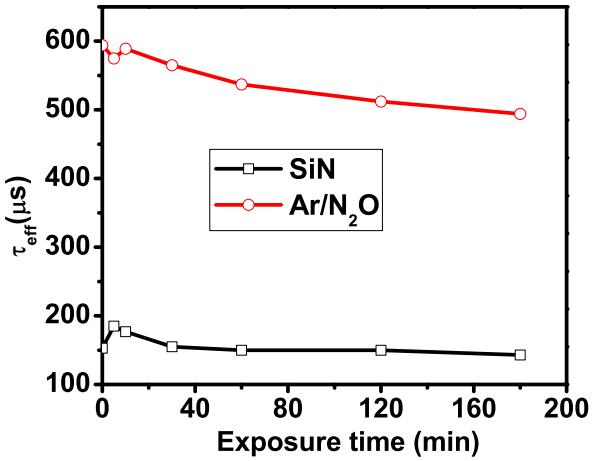


Fig. 7.6: Reduction in τ_{eff} following UV exposure. For longer duration, τ_{eff} can be seen to saturate. τ_{eff} was measured on 300 μm thick n-type FZ wafers with a resistivity of 3 Ω cm.

results of the experiment is summarised as shown in Fig. 7.6. τ_{eff} is observed to decrease for increasing time duration of UV radiation exposure. The fall in τ_{eff} may have been the result of breakage of Si - H bonds at the Si - silicon nitride interface [31]. However, after 150 min of UV exposure, τ_{eff} for both samples was seen to saturate as can be seen in Fig. 7.6.

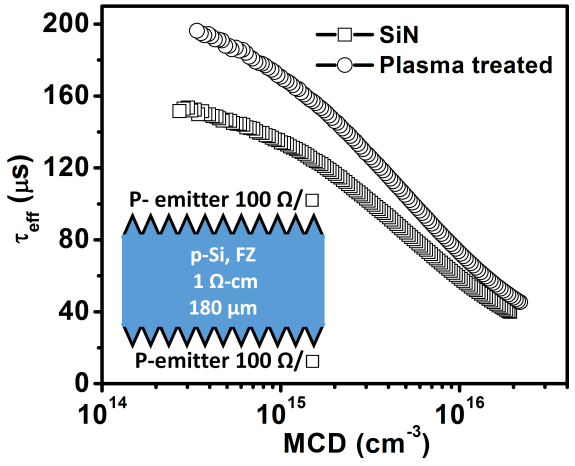


Fig. 7.7: Improvement in τ_{eff} observed following plasma treatment of silicon nitride on an n-type phosphorus diffused emitter. Inset shows the schematic of the device used for the experiment.

Having seen an improvement in minority carrier lifetime on n-type FZ wafers, the next step was to investigate how the plasma treatment impacted the emitter passivation quality. The same was investigated on 1 Ω cm p-type textured FZ wafers. Gas phase phosphorus diffusion was carried out on both sides to form symmetric test structures. The sheet resistance after diffusion

was measured to be $\sim$ 100 Ω/□. Silicon nitride was deposited on both sides of the wafer, and Ar + N_2O plasma treatment was carried out on both sides of the wafer. The schematic of the device used for measurement is shown in the inset of Fig. 7.7. Sample without any Ar + N_2O post treatment was used as reference sample. The implied V_{oc} was measured using photo conductance decay (PCD) measurements. As shown in Fig. 7.7, an improvement in τ_{eff} can be seen, which resulted in an improvement in implied V_{oc} from 682 mV to 687 mV.

Lifetime investigation on textured p - type Cz wafer

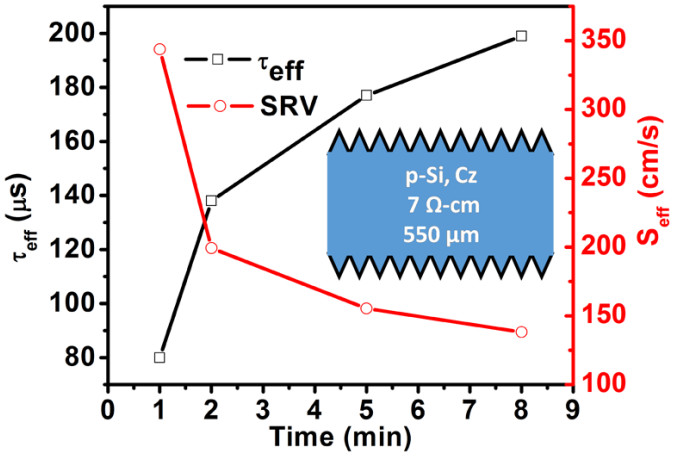
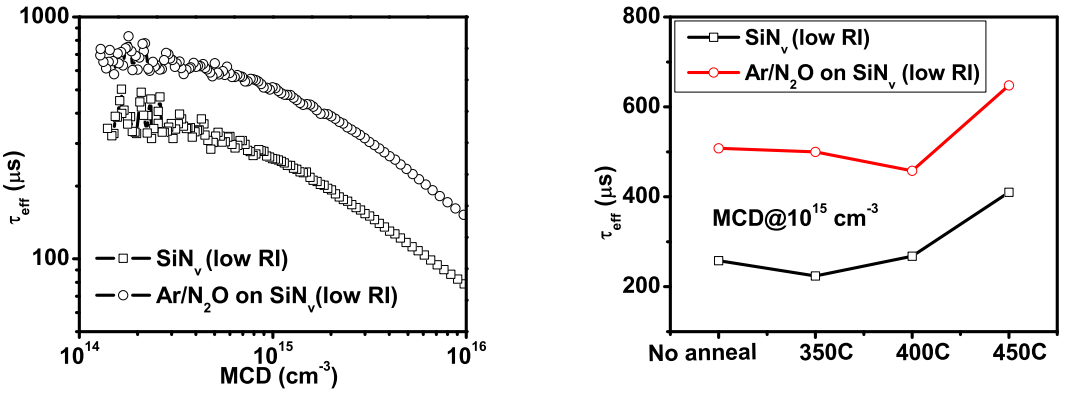


Fig. 7.8: Variation in τ_{eff} for different plasma exposure durations for a p-type Cz wafer.

The impact of a post deposition plasma treatment was investigated on a 7 Ω cm textured p-type Cz wafer. Silicon nitride film was deposited on both sides of the wafer, and the plasma treatment was carried out for different time durations of 1, 2, 5 and 8 min. As shown in Fig. 7.8, an improvement in τ_{eff} was seen for longer exposure duration. However, the rate of increase in lifetime is seen to be higher for shorter duration of time. The rate of improvement in τ_{eff} following Ar + N_2O post treatment is seen to come down for longer exposure duration. For longer duration of time, the improvement in lifetime maybe limited by the amount of hydrogen available in the film and by the number of interface trap states available at the interface of Si - SiN.

In order to check whether the lifetime improvement was specific to a silicon nitride film, Ar + N_2O plasma treatment was also carried out on a single layer silicon nitride film, labelled as SiN_y to distinguish it from the SiN film that was used in previous experiments. The silicon nitride film had a lower hydrogen content as compared to the film used in above experiments.



(a) (b)

Fig. 7.9: (a) τ_{eff} enhancement observed for plasma treated single layer silicon nitride film (b) Variation in τ_{eff} for different annealing temperatures for plasma treated single layer silicon nitride (SiN_v) film. τ_{eff} was measured on 300 μm thick n-type FZ wafers with a resistivity of 3 Ω cm.

The minority carrier lifetime was seen to improve from 260 μs to 506 μs (@MCD = 10^{15} cm^{-3}) after the plasma treatment as shown in Fig. 7.9(a). In comparison to the silicon nitride film shown in Fig. 7.4(a), the quantum of improvement was seen to be lower. The lower H content at the silicon - silicon nitride interface may have limited the enhancement in τ_{eff}. Thermal stability of surface passivation was investigated same as the above experiments at temperatures typically used for Ni - Cu contact sintering in c - Si solar cells [4]. As shown in Fig. 7.9(b), enhancement in passivation was seen to be stable for temperatures used in our experiments, making the process a suitable candidate for c - Si solar cells based on PERC/PERL architectures [4]. From this experiment, it maybe concluded that the enhancement in lifetime following plasma treatment is not specific to one type of SiN film but is applicable for both lower RI and higher RI SiN films.

7.4 Understanding the physical mechanism behind minority carrier lifetime improvement

From numerous experiments, it was seen that the τ_{eff} was seen to improve after Ar + N_2O plasma post treatment. HFCV measurements, confirmed that the plasma treatment led to a decrease in interface state density and an increase in positive fixed charge density. The quantum of improvement in τ_{eff} was seen to have a bearing on the hydrogen content within the silicon

nitride film. However, the exact physical mechanism behind the improvement in τ_{eff} is not clearly understood. This section investigates the potential mechanism behind the enhancement in τ_{eff} after Ar + N_2O plasma treatment.

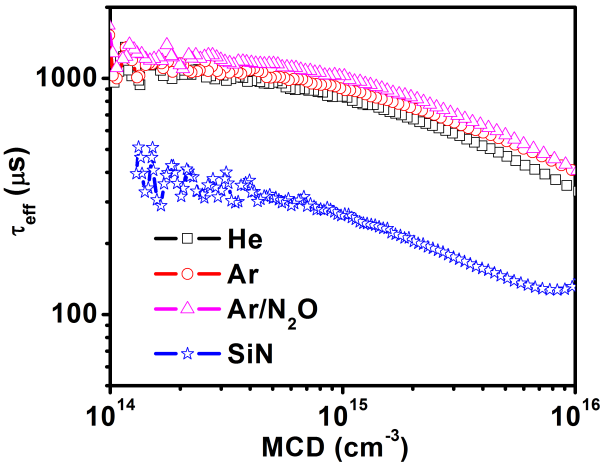


Fig. 7.10: Enhancement in τ_{eff} for different plasma ambient. No significant difference in τ_{eff} was seen for treatment in different plasma ambients. τ_{eff} was measured on 300 μm thick n-type FZ wafers with a resistivity of 3 Ω cm.

Vernhes et al. reported that, plasma treatment of silicon nitride films can result in an annealing of the silicon nitride [149]. The kinetic energy of the ionised species is dissipated as it bombards the silicon nitride, resulting in a rise in temperature, leading to the annealing. However, this would imply that, on using a lighter species like He, the amount of energy transferred onto the silicon nitride film would be less, and hence the annealing effect would be lower. In order to test this hypothesis, an experiment was carried out by treating the silicon nitride film in different plasma ambient. The impact of various plasma ambient on τ_{eff} was studied. Silicon nitride was deposited on both sides of n-type FZ wafers (3 Ω cm). The samples were then treated in He, Ar and Ar + N_2O ambient for 10 min respectively on both sides of the wafer. The result of the experiment is shown in Fig. 7.10. As compared to the reference sample, there was significant enhancement in τ_{eff}. However, τ_{eff} across the samples were comparable. Ar + N_2O plasma treatment resulted in best τ_{eff}, followed by Ar and He plasma treatments. However, the difference in τ_{eff} for different plasma ambient was not significant. This indicated that though the plasma ambient plays a role in determining τ_{eff}, the cause for the significant enhancement in τ_{eff} following plasma treatment lies elsewhere.

Another possible cause for the improvement in lifetime may have been the annealing of the sample as a result of the high substrate temperature. For annealing temperatures above

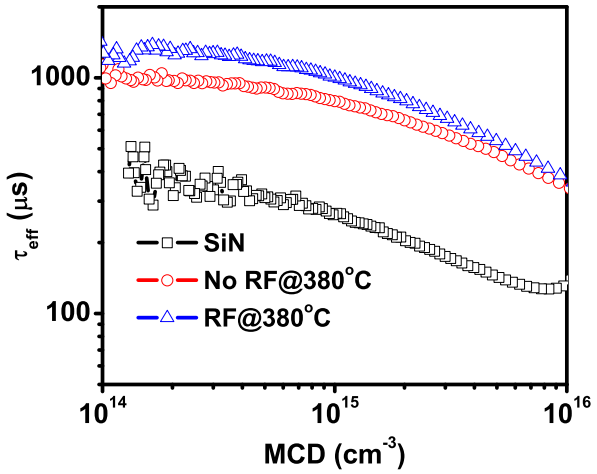
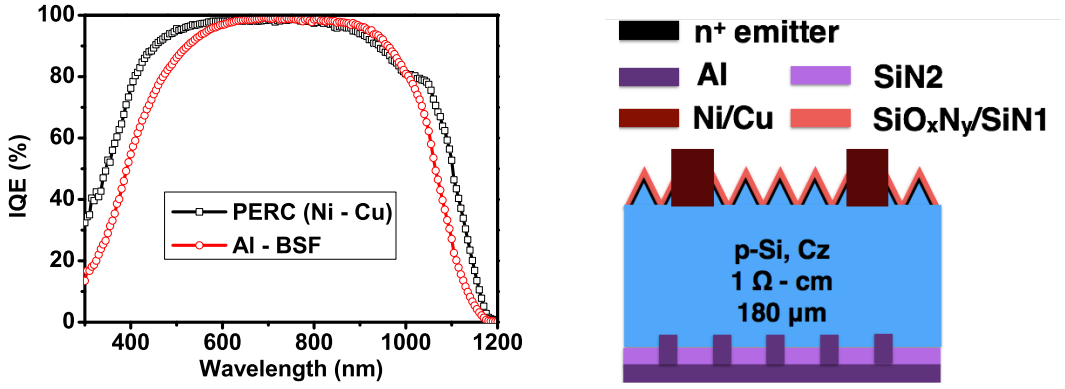


Fig. 7.11: τ_{eff} measurement on n-type FZ wafers, before and after plasma (RF) treatment. No RF corresponds to the sample kept in the chamber without turning ON the RF supply.

350^{o}C, Cai et al. had reported that the trapped atomic hydrogen in PECVD SiN films can act as a source of hydrogen leading to an improvement in surface and bulk passivation in multi crystalline solar cells [152]. During the Ar + N_2O plasma treatment reported here, the sample resides on the substrate for an additional 10 min at 380^{o}C. This in situ annealing during the plasma treatment may have an impact on the final effective lifetime. To investigate the impact of substrate annealing on the measured effective lifetime, an experiment was carried out on n-type FZ wafers of 3 Ω cm resistivity. SiN was deposited on both sides of the wafer. The sample was then kept inside the RF chamber at 380^{o}C in Ar + N_2O ambient keeping the RF supply OFF. Gas flow rate and chamber pressure used were same as those used for the post treatment process. The sample was placed in chamber for 10 min. As shown in Fig. 7.11, τ_{eff} increases when the sample was kept in chamber without any RF supply. Upon turning the RF supply ON, τ_{eff} was seen to increase further, indicating an improvement in passivation quality. This experiment clearly demonstrates and decouples the effect of the substrate annealing effect and plasma treatment on the effective minority carrier lifetime. The results presented here are in contrast to what was reported by Bose et al., who had reported an increase in D_{it} following N_2O plasma treatment at 250^{o}C [18]. The higher substrate temperature (380^{o}C) used in our experiments may have contributed to this difference. The improvement in surface passivation quality after the plasma treatment process, is predominantly due to the substrate annealing of the sample. Further plasma treatment of the SiN film leads to a marginal improvement in surface passivation quality.

7.5 Technology roadmap for the process



(a) (b)

Fig. 7.12: (a) EQE of a PERC solar cell compared with a screen printed solar cell [153] (b) Schematic of the PERC solar cell fabricated.

As previously discussed, the plasma post treatment process is an effective method to minimise the background plating process. The process discussed in this chapter, had shown a significant improvement in the effective lifetime following the plasma post treatment. The treatment step was also seen to result in an improvement in τ_{eff}, both on n-type emitters, n-type and p-type wafers, opening up a lot of avenues for implementation. One such implementation of the process was in rear surface passivation of PERC solar cell as shown in Fig. 7.12(b). The fabrication process for the PERC solar cell followed a similar process reported by Tous et al. [4]. Electroplated Ni - Cu contact was used as front contact while laser fired Al was used as rear contact. No high temperature firing process was used during the cell fabrication process. A low temperature anneal at 375^{o}C was used for Ni - Cu contact sintering. Initial results from the PERC solar cells thus fabricated demonstrated an improvement in rear surface passivation as compared to Al - BSF solar cells. The EQE is shown in Fig. 7.12(a). The improvement in the front side of the solar cell is the result of using a plasma grown SiO_xN_y - SiN1 stack in comparison to the reference cell using silicon nitride. The rear side of the cell was passivated using a hydrogen rich silicon nitride film (SiN2), and was post treated in Ar + N_2O ambient to improve τ_{eff}. The improvement in passivation quality of the rear surface manifested as an improved quantum efficiency for the longer wavelength (900 - 1200 nm) as compared to the reference cell, thus clearly demonstrating the future potential of the process. The cell performance was limited by series resistance, as the contact formation using laser firing would need

further optimisation.

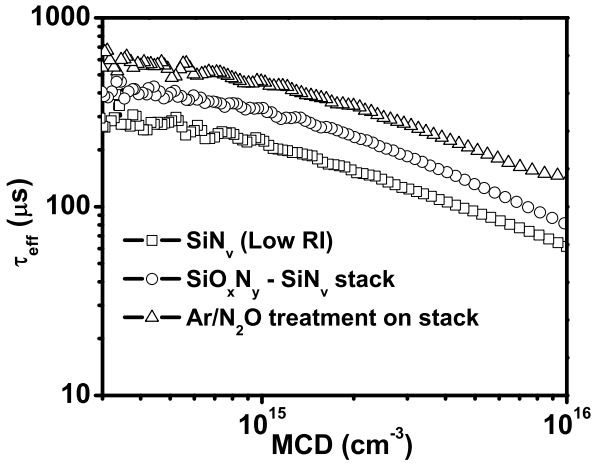


Fig. 7.13: τ_{eff} improvement as a result of plasma pre and post treatment; measured on n-type FZ wafer.

Another aspect that needs further investigation is the combined effect of a plasma oxidation step and the post treatment step on the Ni - Cu background plating. From initial results obtained, the lifetime enhancement is observed when the plasma oxidation step and the post treatment step are combined. The result of the same is shown in Fig. 7.13. The combined use of plasma oxidation and post treatment has the potential to significantly lower the back ground plating. In addition to this, the plasma oxidation step (pre-treatment) can result in an improvement in emitter surface passivation leading to an improvement in open circuit voltage and current. Therefore the true potential of this process combination needs to be investigated in detail. The result in shown in Fig. 7.13 also confirms that the plasma post treatment can be used for stacks of SiO_x/SiN films. The impact of plasma post treatment on a stack of Al_2O_3 - SiN can also be an interesting study, as it is the most widely used rear surface passivation stack in PERC solar cells.

7.6 Conclusions

In this chapter the impact of a post deposition plasma treatment process on the surface passivation quality of SiN was discussed. A significant improvement in τ_{eff} was observed for samples treated in different plasma ambient. The improvement in τ_{eff} was seen to be stable for temperatures typically used in PERC/PERL architectures and Ni - Cu contact sintering. Improvement

in τ_{eff} was observed not only on polished n-type FZ wafers but also on textured p-type Cz wafers, as well as n^+ emitter surfaces. The improvement in τ_{eff} was seen to be predominantly caused by the substrate annealing effect. Thus an Ar + N_2O plasma treatment on silicon nitride not only has the potential to reduce background plating but also improve the quality of surface passivation, making it a very promising process technology for low temperature c - Si solar cells based on electroplated Ni - Cu contacts.

Chapter 8

Inverted pyramidal texturing of silicon through blisters in silicon nitride

8.1 Motivation

The concept of inverted pyramidal texturing assumes further significance in light of decreasing wafer thickness. The current industry standard wafers are typically 180 μm thick, and can absorb all the light falling on it. Conventional random/inverted pyramidal texturing process results in pyramids of 3 - 10 μm in size [9]. The process consumes 10 - 20 μm of silicon absorber material and is hence not a viable process for thin wafers [93]. However, as the thickness of the wafer scales down, efficient light trapping mechanisms are required to ensure that a thin wafer can absorb as much light as a thick 180 μm silicon wafer. Fig. 8.1 shows the impact of starting wafer thickness on the short circuit current density in a solar cell assuming a 100% collection. The simulation was carried out using Wafer Ray Tracer in PV Lighthouse. No antireflective coating was used during the simulation. A pyramid height of 3 μm was assumed. As can be seen, the maximum current density that can be obtained for a given spectrum (J_{abs}), falls for decreasing wafer thickness. However, during conventional random pyramidal texturing of c - Si wafers, $\sim$ 10 - 20 μm thick silicon is removed from both sides of the wafer. Consider a silicon wafer of 100 μm, the minimum loss of silicon from both sides is $\sim$ 20 μm [6], resulting in a net wafer thickness of 80 μm. J_{abs} will fall by 0.7 mA/cm^2 as shown in Fig. 8.1. Inverted pyramidal texturing on the other hand etches $\sim$ 0.7 * Width of etch pattern. By tailoring the width of the etch pattern, the amount of silicon lost can be lowered. For example, an etch pattern with a width of 1 μm can result in etching of $\sim$700 nm of silicon, resulting in significant saving of

silicon substrate as compared to random pyramidal texturing. This coupled with higher J_{abs}, lower defect densities and lower stress on dielectrics makes inverted pyramidal texturing an interesting option for lower wafer thickness [8].

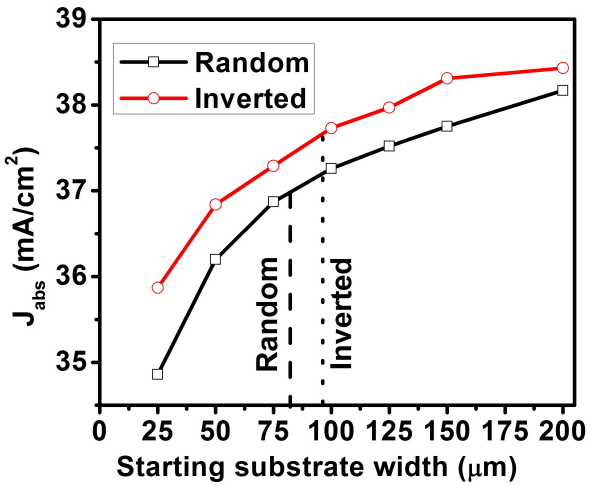


Fig. 8.1: J_{abs} versus starting wafer thickness for random and inverted pyramidal texturing. Also indicated (dotted lines) are J_{abs} after random and inverted texturing for a 100 μm thick wafer.

The chapter begins with a proposal for a novel process for the fabrication of micrometer scale inverted pyramids on crystalline silicon. The key to the process are the blisters formed upon annealing of silicon nitride films. Inverted pyramids are formed by etching the sample in Tetra Methyl Ammonium Hydroxide (TMAH) solution. The silicon nitride film remaining on the wafer surface serves as an etch mask during the etching process. A detailed discussion on both the mechanism behind the formation of blisters in silicon nitride films as well as the impact of various process conditions on the blister size, shape and density is also included in this chapter. The chapter concludes with a brief discussion on some of the approaches that maybe utilised for fabricating inverted pyramids of sub micron dimensions.

8.2 Inverted pyramidal texturing through blisters in silicon nitride

The proposed novel approach for fabricating inverted pyramids on silicon is shown in Fig. 8.2. RCA cleaned, single side polished, <100> Si wafers with a resistivity of 4 - 7 Ω cm was chosen as the substrate. A thin film of silicon nitride was deposited using an ICP - CVD plasma reactor, using silane and nitrogen as the process gases. After depositing the silicon nitride film,

the sample is annealed in a rapid thermal annealing (RTA) chamber to create blisters. Fully open blisters would expose the silicon underneath the silicon nitride film, and thus it serves as a template for fabrication of inverted pyramids. Before the texturing process, blistered samples were treated in 2% HF solution to remove any native oxide that may have grown on the exposed silicon surface. The sample was subsequently rinsed in de-ionised water and transferred to the etching solution. Texturization process was carried out in TMAH solution at 85 - 90^{o}C. After etching, the samples were observed under a scanning electron microscope. The weighted average reflectance was measured using a UV - VIS - NIR spectrophotometer after etching the silicon nitride film in 5:1 Buffered HF (BHF) solution.

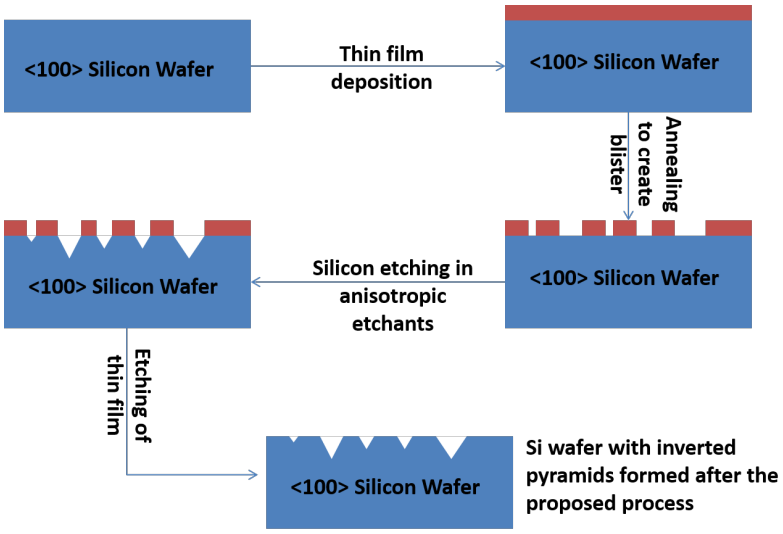


Fig. 8.2: Process flow for fabrication of inverted pyramids on silicon.

In order to validate the viability of the proposed process, two different silicon nitride films were chosen. The films were deposited at 320^{o}C with an ICP power of 200 W, and RF power of 40 W. SiH_4 to N_2 ratio was 0.8 and 1.0 respectively for the two films. The chamber pressure was kept at 4 mT and 20 mT respectively during the deposition of these films. The blisters were generated by annealing the silicon nitride film at 800^{o}C in N_2 ambient. One of the films had a large density of closed blisters, while the other film had a large density of fully opened blisters (SiH_4 to N_2 ratio = 1). The surface coverage of the blisters for both the samples were found to be about 30%. The inverted pyramidal texturing process was carried out in 2.5% TMAH solution at 85^{o}C. In order to understand the robustness of the blistered region to the etching solution, the etch process was carried out in two steps. The samples were first etched in TMAH solution for 1 min and was subsequently observed in a scanning electron microscope. This was followed by another etch for 4 min followed by electron microscopy imaging. The images

were taken prior to the removal of silicon nitride. No etching of silicon was observed under the blisters that had not cracked open after etching for 1 min as shown in Fig. 8.3 (a) and after etching for 5 min as shown in 8.3 (b). Hence it maybe advisable from a process stand point to look at films in which the blisters have completely cracked open for the purpose of inverted pyramidal texturing. However, for the sample with opened blisters, as can be seen in Fig. 8.3 (c), after 1 min of TMAH etching, the etch planes for anisotropic etching of Si can be seen to form along the circular outlines of the blisters formed. Upon etching it for another 4 min, fully formed inverted pyramids could be seen. This indicates that the circular blistered regions formed during annealing can be effectively etched in anisotropic etch solutions, resulting in inverted pyramids. The surface coverage of the pyramids formed is still low in comparison to conventional photolithography based inverted pyramid texturing process, and can be improved by optimising the blister formation process. It can also be seen that the inverted pyramids formed are not of uniform size. The size of the pyramids vary in accordance with the size of the blisters formed. However, as can be seen in Fig. 8.4, there was a decrease in broadband

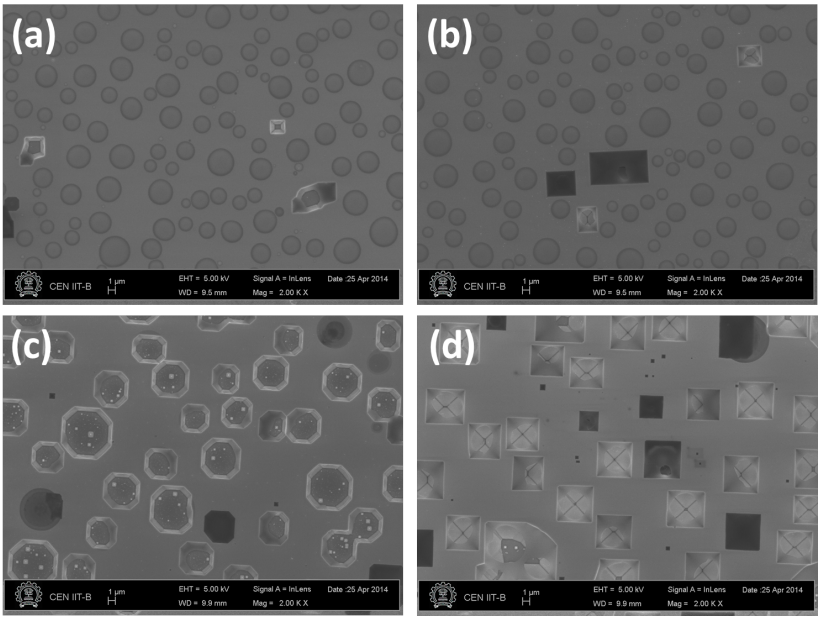


Fig. 8.3: (a), (b) SEM images of a sample with large density of unopened blisters after etching in TMAH solution for 1 min and 5 min respectively. No etching was observed under the unopened blister. (c), (d) SEM images of a sample with a large density of open blisters after etching in TMAH solution for 1 min and 5 min respectively. Etching can be seen to commence along the blister edges after 1 min and fully formed inverted pyramids can be seen after 5 min of etching.

reflectance of the sample as compared to polished silicon surface. W_{av} reflectance value of 28.4% was obtained for the sample with the open blisters. The weighted average reflectance value is high as compared to random pyramidal texturing process. This maybe the result of a

low surface coverage of blisters which resulted in a low density of pyramids. For the sample with unopened blisters, the reflectance value was comparable to that obtained for polished Si wafer. The reflectance was measured after removing the silicon nitride film in buffered HF (5:1) solution. It maybe concluded that a higher surface coverage of opened blisters is necessary for lowering the reflectance value. A better understanding of the blistering process and the influence of various process parameters on the blistering process can pave the way forward for improving the coverage of open blisters. As shown in the inset of Fig. 8.4, during the etching of silicon through the blister, a small undercut into the silicon can also be seen. The under etch can play a major role, in case of samples with a large surface coverage of blisters, in determining the final outcome of the etch process. From the above set of experiments, it maybe concluded that, the

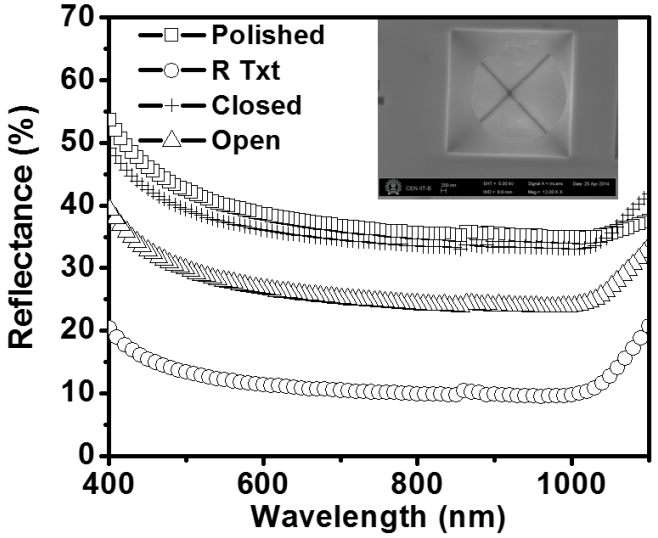


Fig. 8.4: Reflectance curves for textured samples showing a decrease in reflectance in comparison to polished silicon. No anti-reflective coating was used on the samples. Also shown is the reflectance curve for a commercial random texturization(R Txt) process for reference. Inset shows the undercut observed during etching through a blister.

silicon nitride film remaining on the wafer surface after blistering, can serve as an etch mask for the fabrication of inverted pyramids. Fully open blisters contributed to formation of inverted pyramids, whereas the closed blisters did not contribute to the inverted pyramid formation. However, as mentioned above, W_{av} reflectance was seen to be high at 28.4%. In order to design and develop processes for obtaining lower weighted average reflectance, the blister formation process needs detailed investigation.

8.3 Understanding the blistering problem in silicon nitride

Blistering in silicon nitride is a widely known problem in the solar cell industry. Localised removal of silicon nitride film upon annealing results in a higher reflectance and degrades the quality of surface passivation in case of crystalline silicon solar cells. The role of hydrogen in the formation of blisters in silicon nitride and aluminium oxide was previously reported [10, 155]. Silicon nitride film cracks open to form bubbles exposing the silicon underneath. The bubble formation is attributed to localised pile up of hydrogen upon annealing. Some of the blisters do not crack open, while some others do not, as shown in Fig. 8.5. As previously mentioned, a fundamental understanding on the nature of blister formation as well as its impact on various process conditions can pave way for designing and developing blistering processes for lowering the W_{av} reflectance. In the following section, the physical nature of blisters is looked at. The impact of various process parameters (annealing and deposition) on the blistering process in silicon nitride is also investigated.

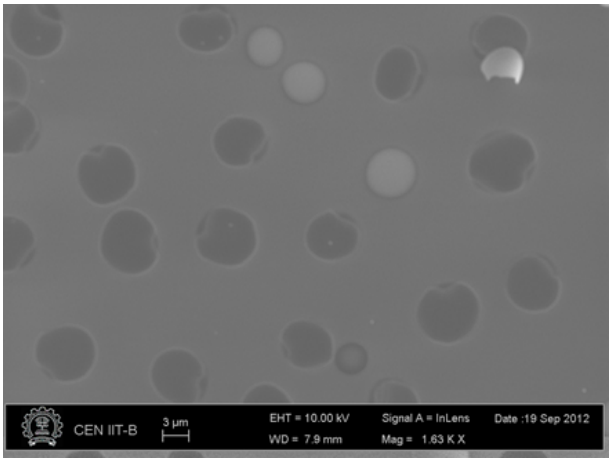
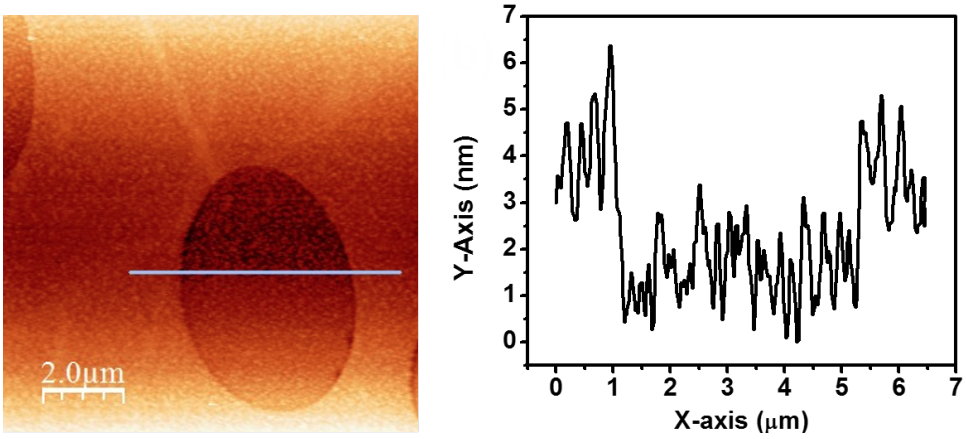


Fig. 8.5: Electron microscopy image showing the blister formed in silicon nitride film after annealing at 800^{o}C for 2 s. Some of the blisters had fully cracked open, while some did not.

8.3.1 Physical nature of blisters

A localised removal of silicon nitride through blister formation can result in exposing the silicon underneath. In order to understand what happens to silicon surface below the blister, AFM was carried out on the blistered areas. AFM was carried out in non contact mode on a silicon wafer after removing the silicon nitride film completely in buffered HF (5:1) solution. Fig. 8.6 shows the profile along the line drawn on the AFM image. It was observed that during blister

formation, not only was the silicon nitride film damaged, but it also lead to formation of a small pit on the silicon wafer surface. Similar pit formation on silicon surface after blistering was previously reported [155]. The trench depth observed in our experiments was about 2 - 3 nm. Similar crater formation on silicon surface as a result of silicon nitride blistering was reported by Hauser et al., who suggested that it can lead to a possible loss of active emitter area [162]. It was reported by Dekkers et al. that the blister formation in silicon nitride film has a very striking resemblance to the out-diffusion of hydrogen observed, during the hydrogen induced exfoliation of silicon, used for the SMART CUT process [155]. Similar circular shaped blisters were observed in hydrogen implanted silicon upon annealing at 350^{o}C [160]. Verma et al. reported that the blistering in hydrogen implanted silicon is a function of temperature and initial concentration of hydrogen [164]. The concentration of hydrogen during blister formation will depend on the annealing history of the sample. The increase in annealing time can result in substantial build up and coalescence of hydrogen within silicon which can lead to blister formation.



(a) (b)

Fig. 8.6: (a) AFM image on silicon surface after removing silicon nitride film (b) Surface profile along the line shown in (a) indicates pit formation in silicon under the blisters.

8.3.2 Impact of silicon nitride deposition conditions on blister formation in silicon nitride

Experiment details

Hydrogenated silicon nitride (SiN_x:H) films were deposited on RCA cleaned Si wafers using an ICP - CVD plasma reactor (plasmalab system 100) from Oxford instruments. The deposition

temperature was kept constant at 320^{o}C for all depositions. SiN_x:H films were deposited using SiH_4 and N_2 as the process gases. The films were deposited at a RF power of 200 W. Two different chamber pressures, 4 mTorr and 20 mTorr were used for the study. Film thickness and RI of the films were measured using a spectroscopic ellipsometer. The samples were subjected to a contact firing process in an RTA chamber, in N_2 ambient. The films were fired at 800^{o}C for 10 s. The chemical composition of the films were studied using FTIR, before and after firing to understand the impact of high temperature on the film composition.

Results and discussion

By varying the silane flow rate, films with different refractive indices were deposited. The thickness of the films was $\sim$15 nm. As expected, the refractive index increased for larger silane flow rates. The films were subsequently fired in a RTP chamber. As indicated in Fig. 8.7, films deposited at a lower silane flow rate did not show a blistering. Thus by regulating the silane flow rate, the blister formation in silicon nitride films can be controlled. Silane being the source of hydrogen in the silicon nitride films discussed in this chapter controls the amount of hydrogen trapped in the film. An increase in silane flow rate results in higher RI and larger hydrogen content in the silicon nitride film. The correlation between silane flow rates and the hydrogen content within the silicon nitride film is also reported by Lanford et al. [163]. Hence it is not surprising that the blistering threshold is purely determined by the silane flow. However, for silicon nitride films deposited at a higher plasma power ($>$ 200 W), blistering was observed irrespective of the silane flow rate. The higher degree of ionisation of the silane may have resulted in a significant increase in the hydrogen content within the film, contributing to the blister formation, after firing.

The variation in film composition with firing was investigated by means of FTIR measurements. From FTIR measurements it was observed that the Si-H and N-H bond peaks decreased upon annealing. Fig. 8.8(a) shows FTIR spectrum for a film deposited using a silane flow of 11 sccm, before and after anneal. The Si-H and N-H peak intensity came down upon firing and a corresponding increase in the Si-N peak was seen. This increase can be attributed to the reaction of the liberated N radicals with the free Si bonds. FTIR spectrum also shows a small Si - O peak due to possible trapping of atmospheric oxygen within the film. Fig. 8.8(b) shows the FTIR spectrum for a thermally stable film deposited using SiH_4 flow rate of 3.5 sccm. Despite a decrease in the Si - H and N - H bond density upon anneal as seen in Fig. 8.8(b), the film did

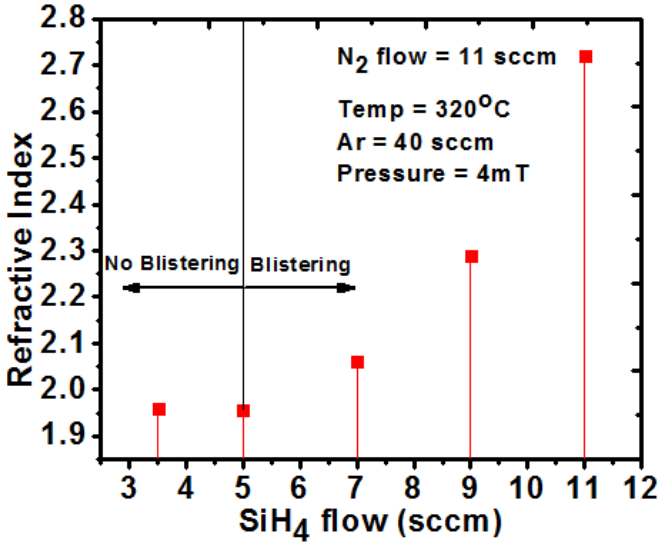
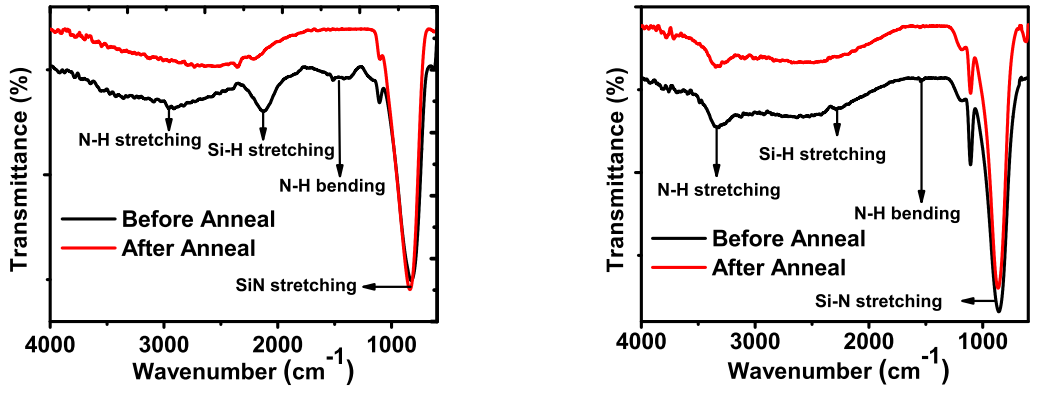


Fig. 8.7: Variation in RI with changing silane flow. The threshold silane flow rate beyond which blistering commences is also shown in figure.

not exhibit blistering. From the above set of experiments, Si - H and N - H bonds were seen to break as a result of firing, releasing hydrogen. This free hydrogen may get accumulated and form bubbles which may expand upon annealing, resulting in the formation of blisters. If the hydrogen concentration under a blister is large enough, the blisters would crack open exposing the silicon underneath.



(a) (b) .

Fig. 8.8: FTIR spectrum before and after firing for (a) SiN_x:H film deposited using a silane flow of 11 sccm. The film blistered upon firing at 800^{o}C (b) SiN_x:H film deposited using a silane flow of 3.5 sccm. The film did not exhibit any blistering upon firing at 800^{o}C.

As shown in Fig. 8.8(a) and 8.8(b), the film deposited with a higher silane flow rate (higher RI) was seen to blister upon firing at 800^{o}C. The film with higher RI also showed a sharp decrease in Si - H bond intensity upon firing. Hong et al. had previously reported that low RI

films are more thermally stable as compared to the higher RI silicon nitride films [159]. The weak thermal stability of Si - rich silicon nitride film was also previously reported [10]. In order to investigate the out-diffusion of hydrogen and the weak nature of Si - H bonds in rich silicon nitride film during firing, an experiment was designed using a trilayer stack of silicon nitride. The film was prepared by sandwiching a thin layer ($\sim$ 14 nm) of high RI (2.3) silicon nitride between two low RI (1.8 - 1.9) silicon nitride films. The bottom layer was deposited with a silane flow rate of 2.5 sccm while the top layer was deposited using a silane flow of 3.5 sccm. The middle layer was deposited at a higher silane flow of 13.5 sccm. All other process parameters were kept constant. The schematic of the stack can be seen in inset of Fig. 8.9. The film was fired at 800^{o}C for 2 seconds in N_2 ambient and the hydrogen concentration before and after annealing was studied using TOF-SIMS.

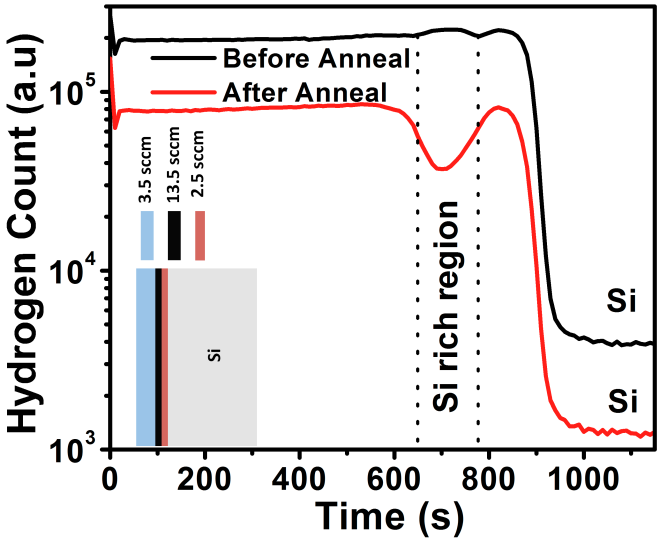


Fig. 8.9: TOF - SIMS data for a trilayer silicon nitride stack deposited by varying the silane flow rate (inset) showing a decrease in hydrogen count upon annealing. The decrease in H count was drastic in the Si rich SiN region, indicating the weak nature of Si - H bonds.

It was observed, as shown in Fig. 8.9, that the hydrogen count within the silicon came down upon firing, indicating an out-diffusion of hydrogen. Before firing, a small gradient in the hydrogen concentration could be seen for the Si-rich layer as compared to surrounding layers. However, upon firing, a sharp fall in hydrogen content could be observed at the region corresponding to the Si-rich nitride layer. This may indicate the lower thermal stability of the Si-H bonds in Si-rich nitride films as was previously reported [10, 159]. The variation in the refractive index across the stack may also have played a role in the sharp fall in hydrogen count. From this experiment it may be concluded that upon firing a hydrogenated silicon nitride

film, bulk out-diffusion of hydrogen happens, which maybe playing a key role in the formation of blisters upon annealing. Additionally, no blistering was observed upon annealing a silicon nitride film deposited on top of a thermally grown SiO_2 film (∼180 nm). This behaviour of SiO_2 maybe attributed to the various defects within the SiO_2 film, which can trap the hydrogen, thus impeding the blistering process [161]. The SiO_2 film can also serve as a buffer layer releasing the thermal stress on the silicon nitride upon annealing.

It may thus be concluded that blistering in silicon nitride film was strongly correlated to the hydrogen content within the silicon nitride film. For silane flow rate above 5 sccm, blistering was seen to commence for low ICP powers (200 W). However, since the texturing experiments warranted blister formation, silicon nitride films deposited with a silane flow rate of 13.5 sccm, at an ICP power of 1000 W, temperature of 250^{o}C were chosen. The higher deposition temperature was chosen to ensure that the film was robust to the anisotropic etch solutions used during the texturing process.

8.3.3 Impact of annealing conditions on blister formation in silicon nitride

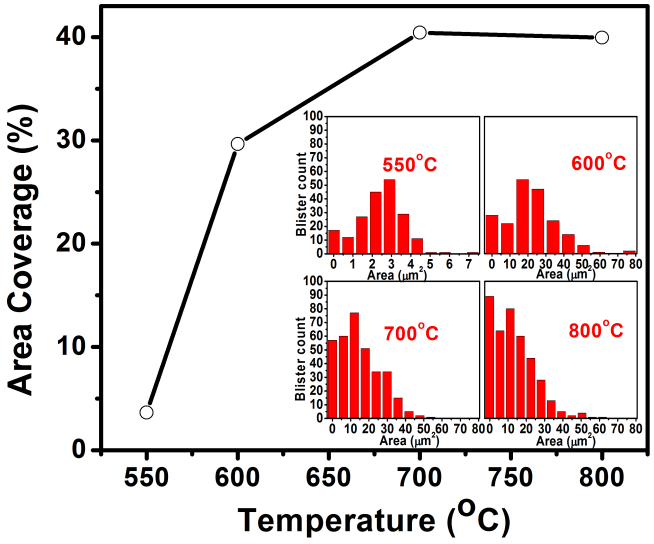
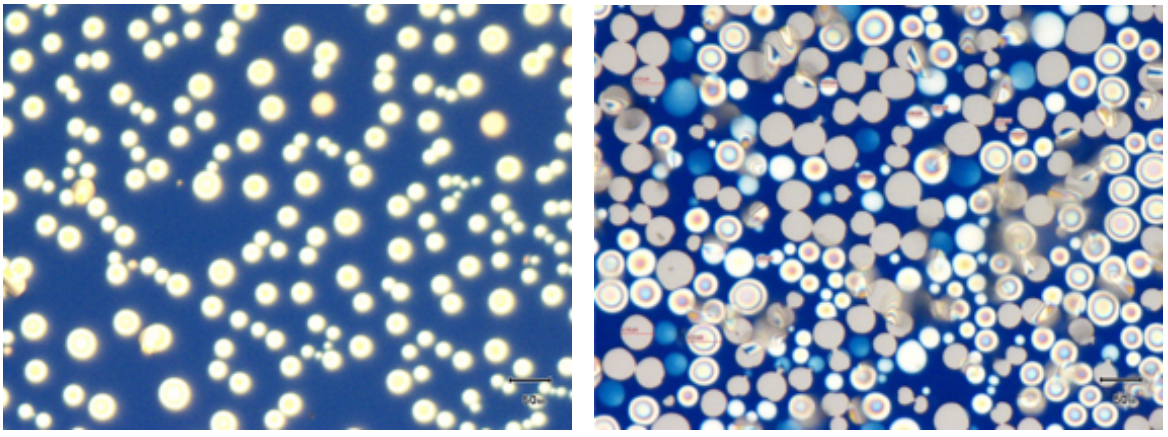


Fig. 8.10: Variation in blister coverage with increasing anneal temperature. Inset shows the distribution of blisters of different areas for varying anneal temperatures. Blister count is given as a percentage of the total number of blisters. The area used for the analysis was 140 μm x 105 μm.

From previous discussions, it was concluded that the blistering in silicon nitride films was found to be strongly correlated to the hydrogen content within the silicon nitride film. Gatz et

al. had previously reported that H - effusion from silicon nitride films commences beyond a temperature of 500^{o}C [165]. Thus it maybe interesting to study the impact of the annealing on the blister formation process. In this section, the influence of anneal conditions (temperature, time) on blister formation in silicon nitride films is investigated. The silicon nitride films were deposited on polished p-type Cz wafers, and was annealed in a RTA chamber for 2 s. As the annealing temperature was increased from 550^{o}C to 800^{o}C, it was observed that the size as well as the density of blisters increased. It was observed that the areal density of the blisters increased from 3.5% at 550^{o}C to 40.0% at 800^{o}C, as shown in Fig. 8.10. At or beyond this temperature, the Si - H and N - H bonds are reported to dissociate resulting in the formation of atomic hydrogen. A saturation in the hydrogen concentration taking part in the blistering process, may have happened for temperatures beyond 700^{o}C resulting in a saturation of blister density. It was also observed that though a large number of blisters were formed, they did not crack open exposing the silicon underneath the silicon nitride film.

By keeping the temperature constant at 800^{o}C, the impact of anneal time on blister size and shape was studied. It was observed that the shape and size of the blisters evolved with an increase in annealing time. As the annealing time was increased from 2 s to 10 s the size and density of blisters increased as shown in Fig. 8.11. The areal coverage was found to improve from 23% to 58%. However, here again, not all blisters had cracked open to expose the silicon underneath.



(a) (b)

Fig. 8.11: Increase in blister coverage for increasing anneal duration (a) 2 s (b) 10 s. The samples were annealed at 800^{o}C in N_2 ambient in a RTP chamber.

From the above set of experiments, it may be concluded that the blister formation process is strongly dependent on the annealing temperatures as well as annealing time. By varying

the annealing time and temperature, the size, shape and areal coverage of the blisters can be modified. In the next section, the impact of deposition conditions on the formation of blisters in silicon nitride is investigated.

8.4 Role of inert gas plasma treatment on the blister formation in silicon nitride

From the above set of experiments, though a surface coverage of 58% was obtained, the samples were not chosen for the texturing experiments owing to the following reasons: (1) the films obtained had a large fraction of unopened blisters which would hinder any texturing process (2) the films were deposited at room temperature, resulting in a low density silicon nitride film which was not robust against the TMAH etch solution. In order to improve the robustness of the film against the etching solution, silicon nitride was deposited at a higher temperature of 250^{o}C, and to improve the fraction of open blisters, an inert gas plasma pretreatment prior to silicon nitride deposition is proposed. It was previously reported by Duo et al. that by co-implanting helium and hydrogen into silicon, the smart cut process can be carried out more efficiently [166]. A reduction in implant dose, implant time and lower crystal damage were reported as the benefits of helium - hydrogen co-implant [166]. Helium being an inert gas would not result in bond breakage through chemical means. However, along with hydrogen, it can take part in the physical processes resulting in an enhancement of the layer splitting process [166]. The use of inert gas for optimising blister formation in silicon nitride films for texturization is investigated in this section. Silicon wafers were pretreated in an Ar plasma in the same process tool at 250^{o}C for 5 min. It may be noted that this do not add any significant complexity to the process except for a 5 min time penalty. The ion flux towards the silicon surface was controlled by varying the substrate power. In our experiment, two different bias powers of 40 W and 100 W were chosen. This corresponded to a negative bias of -107 V and -203 V respectively at the substrate. The plasma was struck at 1000 W ICP power at 4 mTorr chamber pressure. The samples were capped with silicon nitride film deposited at 250^{o}C. The samples were further annealed at 550^{o}C, and 800^{o}C for 10 s. The areal density, shape and size of the blisters thus formed were investigated.

It was observed that for the samples prepared with an argon plasma pre-treatment, the results were much in the lines of what was reported by Duo et al. [166] for helium - hydrogen co-

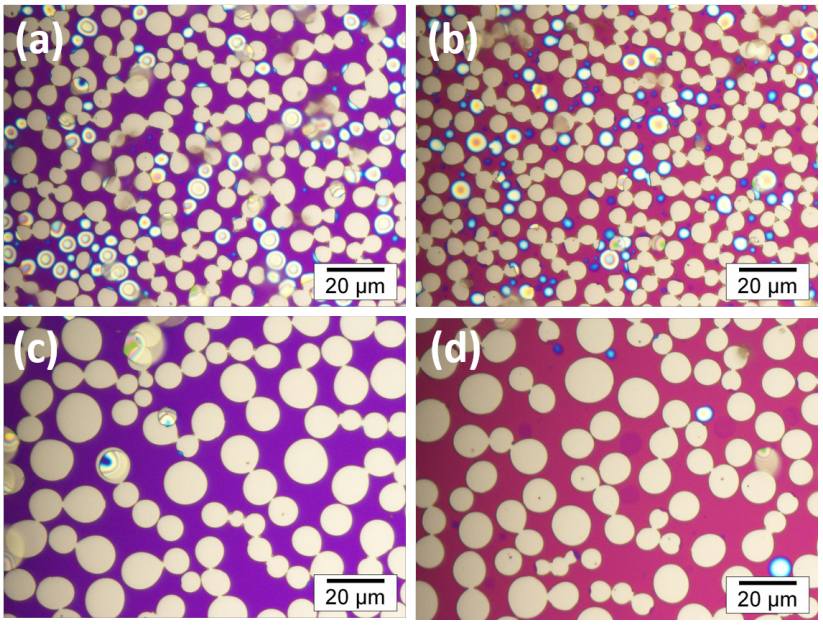
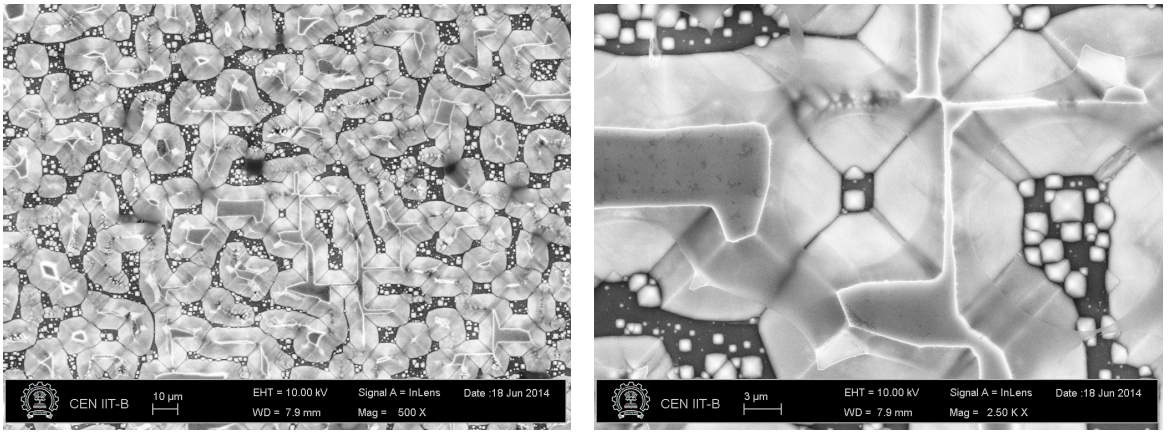


Fig. 8.12: Optical micrographs(100X magnification) of samples after 40 W argon pretreatment followed by anneal at (a) 550^{o}C (b) 800^{o}C and 100 W argon pretreatment after anneal at (c) 550^{o}C (d) 800^{o}C.

implant. As can be seen in Fig. 8.12 (a) and (b), circular shaped blisters were formed upon annealing, exposing the silicon underneath. However few unopened blisters could also be seen in Fig. 8.12 (a) and (b) as bright spots on the wafer surface. The surface coverage of the blisters were calculated to be around 55%. However, as the substrate power was increased from 40 W to 100 W, the average size of the blisters increased from 8 μm to 16 μm, as can be seen in Fig. 8.12 (c) and (d). The blister coverage was found to be about 51%. It could also be seen that, as the anneal temperature was raised from 550^{o}C to 800^{o}C, no improvement in blister coverage was observed. Hence, by incorporating an argon plasma pretreatment, the coverage of opened blisters improved and the the annealing temperature for the blister formation was reduced.

Analogous to what was reported for co-implanted helium and hydrogen, argon too may have played a role in enhancing the physical processes associated with blistering [166, 167]. Being chemically inert, argon maybe able to segregate easily within the silicon close to the surface. Upon annealing, smaller bubbles of argon can coalesce (similar to helium) along with the hydrogen and generate the required pressure for creating the blisters on silicon surface. An increase in the substrate power would correspond to an increase in the ion flux towards silicon surface, which can result in a higher argon concentration within silicon. This increased argon concentration, coupled with Ostwald ripening process during annealing may have resulted in the increase in the blister size[167]. It maybe conclude from Fig. 8.12 that Ostwald ripening



(a) (b)

Fig. 8.13: SEM images (a) showing the formation of inverted pyramids after etching the sample in TMAH solution for 5 min (b) Magnified image showing an inverted pyramid, the undercut as a result of etching through the blister can also be seen. The sample prepared with 100 W Ar plasma pretreatment and annealed at 550^{o}C was used for the experiment.

process may be playing a key role in determining the shape of the blisters formed. Like He and H, Ar and H may also have worked in synergy to enhance the blistering process. There have been reports of argon induced bubbling of silicon at higher implantation energies ($\sim$ 100 KeV) at room temperature [168]. The low mobility of argon in silicon and its low sputter yield is reported as the reasons for the blister formation in that case. However, in our experiments, the energy and dose of implant is much lower than what was previously reported. Hence the exact role of Ar implantation at low energy into silicon needs further investigation.

The sample prepared with 100 W Ar plasma pretreatment and annealed at 550^{o}C was chosen for the texturing experiment. The sample was etched in 2.5% TMAH solution at 85^{o}C for 5 min. The silicon nitride film was etched out in 5:1 BHF and reflectance measurements were carried out. As can be seen in Fig. 8.14, the weighted average reflectance came down to 17.3%. Reflectance curve for a randomly textured process is also shown for reference. No anti-reflective coating was used on the samples. The fall in reflectance can be attributed to an increase in the surface coverage of the fully open blisters, as was seen in Fig. 8.12 (c). The etching of silicon through the blister resulted in the formation of an undercut into the silicon nitride which further contributed to an increase in the surface coverage. As can be seen in Fig. 8.13 (b), the front side of the wafer had fully formed $<111>$ planes on the silicon surface, while very small random pyramids is seen to be form in regions where there was no blister. This may have been the result of a possible seepage of the etch solution into these regions, as the etching progresses.

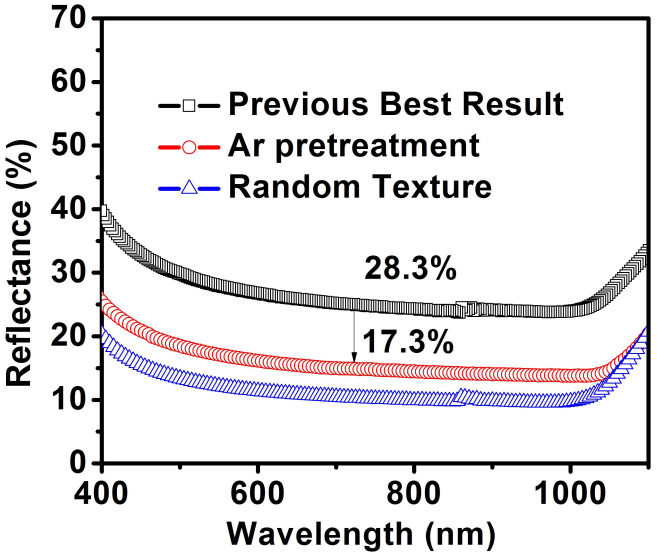


Fig. 8.14: Reflectance values showing a decrease in weighted average reflectance from 28.3% to 17.3%, owing to an increased surface coverage of open blisters as result of Ar pretreatment. W_{av} reflectance of 17.3% was obtained for the sample prepared with 100 W Ar plasma pretreatment and annealed at 550^{o}C was used for the experiment. Previous best results refers to the results presented in Fig. 8.4.

8.5 Roadmap for fabrication of inverted nano pyramids

8.5.1 Reduction of blister size for nano texturing applications

From the discussion in the previous sections, it was seen that the size of the blisters formed as a result of annealing the silicon nitride film was in excess of 5 μm. These larger size blisters were seen to result in the formation of pyramids which are of the similar size. However, the true potential of the process discussed in above section can be exploited, if the dimension of the blister sizes can be brought down to sub micron levels. One of the approach was to reduce the thickness of the silicon nitride film. Fig. 8.15, shows the blister formation in $\sim$ 8 nm thick silicon nitride film. The size of the blisters formed were very small than what was clearly resolvable using an optical microscope. However, as can be seen the blisters formed were not fully opened rendering them unsuitable for texturing applications. In order to address the problem of unopened blisters for lower thickness, the process was modified. The blister process was seen to be directly correlated to the concentration of hydrogen trapped within the silicon nitride film and silicon. Keeping this fact in mind, an experiment was designed by depositing a thick layer of silicon nitride, which was etched in BHF(5:1) for varying time durations (30s, 60s, 90s). This etch back scheme ensured that the amount of hydrogen trapped within the silicon

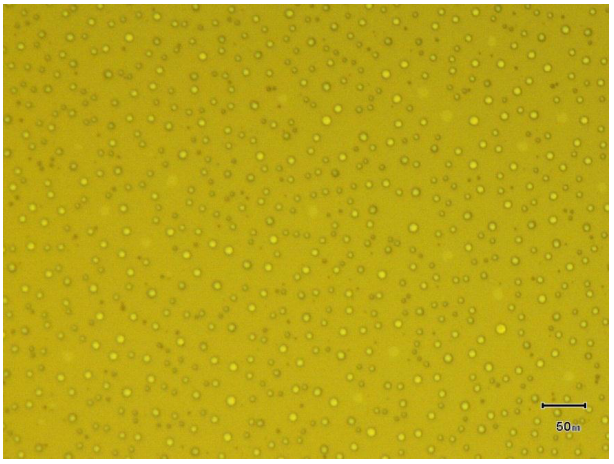


Fig. 8.15: Optical image showing small blisters in a thin silicon nitride film of thickness 18 nm.

remained the same for all samples. The samples were then annealed in RTA at 800^{o}C for 10 s. The result of the experiment can be seen in Fig. 8.16.

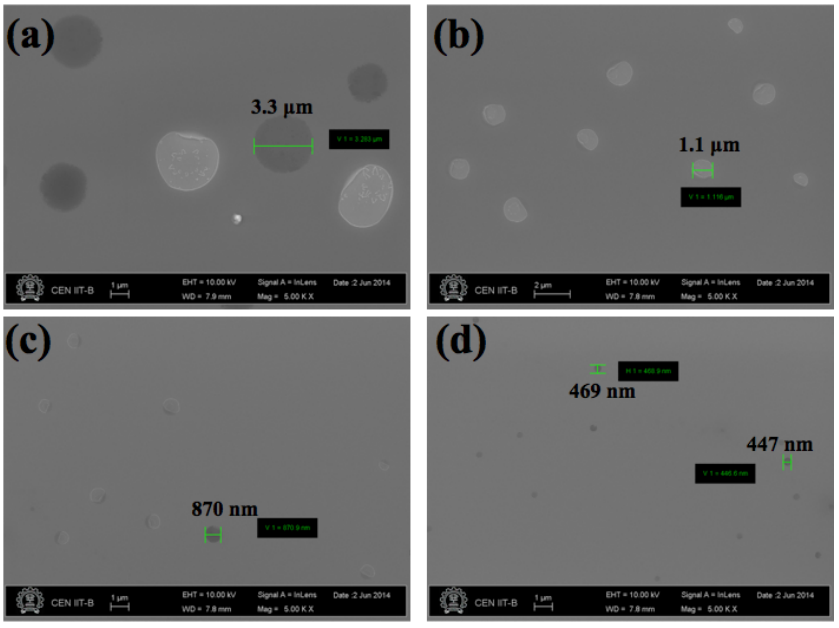


Fig. 8.16: SEM images showing the blister formation in a silicon nitride film as its thickness was reduced by etching it in BHF solution. For increasing etch durations (a) 0 s (b) 30 s (c) 60 s (d) 90 s, the size of the blisters came down from 3 μm to 450 - 470 nm.

As can be seen, the size of the blister formed was found to decrease with increasing BHF etch time. The size of the blister decreased from 3 μm for the as deposited sample to 446 nm after 90 s of BHF etching. There was no major change in density of the blisters formed as can be seen in Fig. 8.16. Therefore by varying the thickness of the silicon nitride film, the size of the blisters can be tuned and thus be used for nano texturing. In order to improve the surface coverage of the process, one needs to start with a sample which has a large density of

blisters. The combination of a thinner film, along with an inert gas treatment prior to silicon nitride deposition can improve the blister density, and pave way for fabrication of inverted nano pyramids.

8.5.2 Boron etch stop for fabrication of inverted nano pyramids in silicon

Experiment details

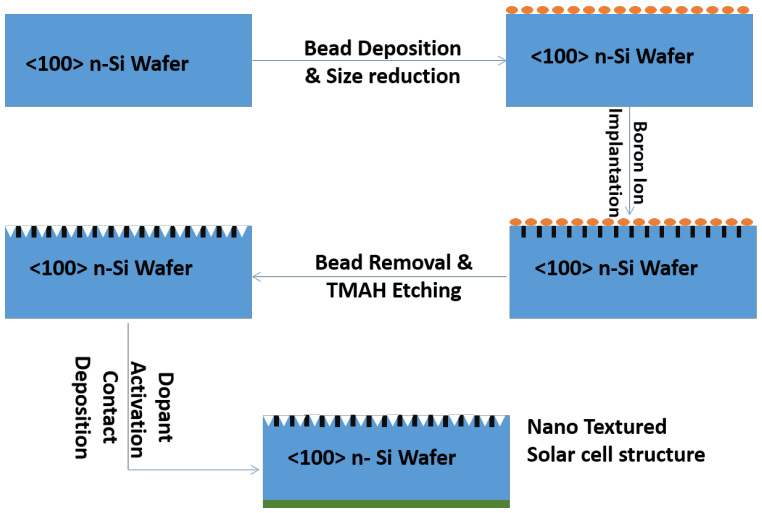


Fig. 8.17: Process flow for nano texturing of silicon using boron etch stop layer.

In this section, a novel process for the fabrication of nano texture in silicon is proposed. The process utilises colloidal lithography [103] and a boron etch stop layer for the same. The schematic of the proposed process is shown in Fig. 8.17. As was previously reported, a boron implant can result in the formation of an etch stop layer in case of etchants like KOH and TMAH [169]. Polystyrene beads are spin coated onto a silicon wafer, and the size of the beads are reduced using an O_2 plasma. By varying the O_2 plasma exposure time, the spacing between the beads can be varied. After the bead size reduction, the sample is subjected to a low boron energy implant in a plasma immersion ion implanter. The implantation process is carried out for a short duration (30 s) at 1 KV DC bias. The beads are then removed in toluene, and the samples are annealed in RTA chamber in O_2 ambient at 1050^oC to activate the dopants. Upon dopant activation, the borosilicate glass is removed and the samples are etched in TMAH, resulting in the formation of the pyramids. The proposed process is shown in Fig. 8.17.

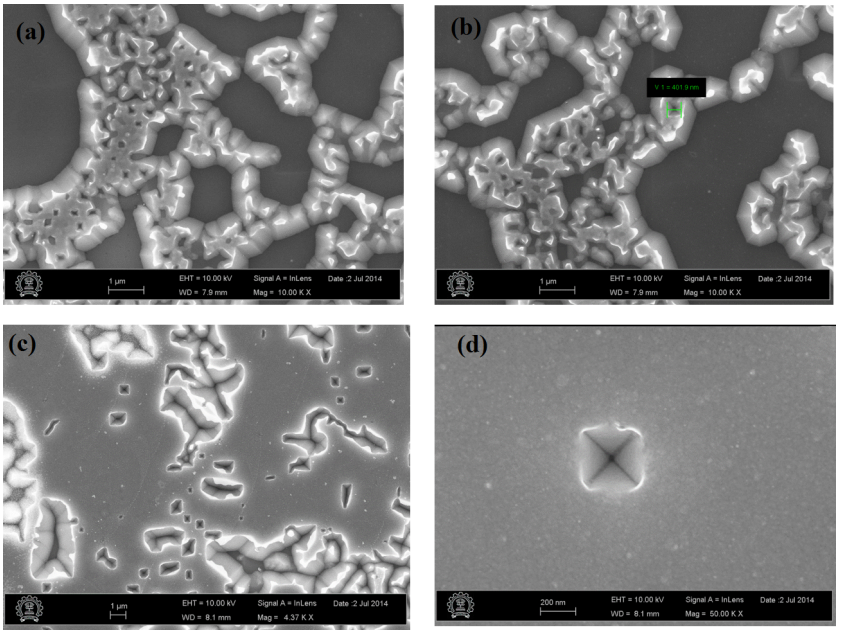


Fig. 8.18: SEM images after etching in TMAH showing the nano pyramids at different regions on the wafer.

Results and discussion

In the experiment, after the ion implantation process, it was observed that all the PS beads were removed. Hence the implant may have happened on almost all areas on the wafer. However, it was observed that few beads were scattered around the wafer surface.The samples were then etched in TMAH solution, and the SEM imaging was carried out to check for formation of inverted pyramids. As can be seen in Fig. 8.18, few nano pyramids were formed, the base width of which varied from 350 nm to 400 nm. The size of the PS beads before size reduction was 500 nm. As can be seen in Fig. 8.18(a), there were regions which had no etching at all, which maybe be the boron implanted region. The shape of the regions with pyramids seen in Fig. 8.18(a) and (b) resembled the shape of a region with multiple layers of beads. Fig. 8.18(d) shows a perfectly formed inverted pyramid, with a size of 356 nm. The experiment was the first experiment for testing of the concept, and it seemed to work. However, by varying the implant conditions, and the firing conditions, a better control on the pyramid formation process maybe possible.

8.6 Conclusions

Two novel processes for fabrication of inverted pyramids on silicon surface were presented in this chapter. The blistering process in silicon nitride was found to be strongly correlated to the

hydrogen implantation process used in SMART cut process. A pre deposition plasma treatment in an argon ambient resulted in an improvement in the size of the blisters formed. By reducing the thickness of the silicon nitride film, the size of the blisters could be lowered to sub micron levels. Further optimisation would focus on improving the blister density further, which can result in a decrease in reflectance. The impact of inert gas plasma pretreatment on the silicon surface may also be looked into.

The feasibility study of another novel process for fabrication of nano pyramids in silicon was reported here. The process involves the usage of colloidal lithography and a boron etch stop layer for the fabrication of the nano pyramids. From the initial results of the experiment, it maybe concluded that the process is feasible and periodically spaced inverted nano pyramids maybe achieved by further optimisation of the implant and anneal conditions.

Chapter 9

Conclusions and Future work

In this thesis, three novel plasma processes for application in crystalline silicon solar cell fabrication were discussed. In Chapter 5, the potential of a novel plasma oxidation process based on nitrous oxide plasma for growing thin oxy-nitride films was presented. The surface passivation potential of the film was investigated by depositing hydrogenated amorphous silicon nitride film. The stack of plasma grown silicon oxy-nitride - hydrogenated silicon nitride was seen to result in better thermal stability as compared to a single layer hydrogenated silicon nitride film. The plasma ambient used for the growth of the silicon oxy-nitride film was also found to have a bearing on the surface passivation quality. It was also seen that, the stack of plasma grown silicon oxy-nitride - silicon nitride was seen to result in an improved emitter surface passivation. This was seen to result in an improvement in short wavelength quantum efficiency of the corresponding silicon solar cells. The performance of the solar cell with a plasma grown silicon oxy-nitride - silicon nitride stack as the front surface passivation layer was found to be significantly better than what was observed for cells with silicon nitride layer as the surface passivation layer. V_{oc} for cells with the stack based passivation was seen to be $\sim$ 5mV higher than their counterpart with silicon nitride layer as the surface passivation layer. The performance the plasma grown silicon oxy-nitride - silicon nitride stack as a front surface passivation layer was compared with that of a stack of thermally grown silicon oxide film - silicon nitride. Comparable solar cell performance was obtained indicating the true potential of the proposed plasma oxidation process as a front surface passivation layer.

An inert gas + nitrous oxide plasma treatment of silicon nitride film was seen to make the film more robust to Ni - Cu electroplating baths. The improved robustness, translated into a decrease in residual plating of Ni - Cu on the pin holes in silicon nitride film. The plasma treat-

ment process was seen to alter the surface chemistry of the silicon nitride film by incorporating more oxygen on the surface. However, FTIR measurements revealed no significant changes in N - H, Si - H or Si - N bond intensity of the silicon nitride film following plasma treatment. Investigations into the impact of the plasma treatment process on the surface passivation quality of silicon nitride film threw up very interesting results. A significant improvement in minority carrier lifetime (260 μs to 864 μs) was obtained following an Ar + N_2O plasma treatment of silicon nitride film. The improvement in lifetime was seen for various plasma ambient, and was seen to dependent on the duration of plasma exposure. The improvement in lifetime was also observed on both p-type and n-type wafers. Further investigations to understand the mechanism behind the lifetime enhancements were carried out. It was concluded from these experiments that the improvement in minority carrier lifetime was predominantly brought about by the substrate annealing during the plasma treatment process.

In the final part of the thesis, novel processes for the fabrication of inverted pyramids on silicon is discussed. The process described relies on using a blistered silicon nitride film as the etch mask. The chapter also discussed in detail about the underlying mechanism behind blister formation in silicon nitride films. The impact of various process conditions, surface treatments, and anneal conditions on the blister formation in silicon nitride was also discussed. The chapter also discussed about a plasma pre treatment step which not only improved the surface coverage of blisters formed but also lowered the temperature of blister formation. The process was found to result in inverted pyramidal structures which showed a higher value of reflectance as compared to what have been reported previously for random pyramidal texturing. The chapter concludes with a discussion on the potential of the proposed process for the fabrication of sub micron inverted pyramids on silicon, which may pave the way for further reduction in weighted average reflectance. Another novel approach involving colloidal lithography and boron etch stop was also discussed as a potential candidate for fabricating nano pyramids on silicon surface.

9.1 Future directions and process improvements

- Plasma grown films for surface passivation of silicon surfaces

  Efficacy of the plasma oxidation process for emitter surface passivation needs to be verified for baseline silicon solar cells with higher efficiency. The presence of a dead layer

in the emitter plays a significant role in degrading the quantum efficiency of the solar cell close to the emitter surface. Dead layer removal through etch back or high sheet resistance emitter based processes are potential route towards performance improvements. Further reduction in the front contact dimension is also proposed for further performance improvement.

Ultra thin silicon oxide films have developed lot of interest in the area of passivated contacts. The potential of growing ultra thin films in plasma ambient maybe investigated and its application in passivated contacts is an area that maybe pursued in future. A comparison between ultra thin oxides grown in HNO_3, UV/O_3 and plasma ambient maybe interesting from a technology perspective as well.

- Post treatment of PECVD silicon nitride films

  The combined potential of a Ar + N_2O plasma pre treatment and post treatment step towards reducing background plating in Ni - Cu metallisation needs to be investigated further. Impact of plasma post treatment of silicon nitride based dielectric stacks like SiO_x - SiN and Al_2O_3 - SiN can also be further investigated for application in rear surface passivation. With further development in low temperature Ni - Cu based PERC solar cell process, the post treatment process maybe integrated for background plating reduction as well as for improving the surface passivation at the rear and front surface of the solar cell.

- Inverted pyramidal texturing through blisters in silicon nitride

  Fabrication of inverted pyramids using sub micron sized blisters need to be investigated. This would require thinner films as was indicated in chapter 8. However, using thinner films as an etch mask can be challenging, as the plasma CVD silicon nitrides are not etch resistant to the anisotropic etchants like KOH/TMAH. One potential way to address the etching of silicon nitride films would be to use a plasma post treatment step like the one described in chapter 7, on the blistered silicon nitride films. Higher plasma power and substrate power can result in significant increase in film density, which can reduce the etch rate [149]. Another aspect, that can be investigated would be the impact of inert gas plasma treatment step on the coverage of blisters for lower silicon nitride film thickness. The use of the blisters as a template for fabrication of other nanostructures like nanowires or nano dots can also be a subject of further investigation.

For fabricating inverted nano pyramids in silicon, colloidal lithography needs to be investigated further as a potential candidate. One such example was described in chapter 8. However, the process outlined in chapter 8, involved an ion implantation process and a high temperature activation step, which might increase the cost of production. However, other approaches to replace the implantation process would involve metal deposition like the one described by Sun et al. [103]. Replacing the vacuum evaporation system with a chemical process based on electroless Ni plating can significantly lower the cost of production.

Appendices

Appendix A

Simulation and MATLAB codes

A.1 Simulation of surface passivation

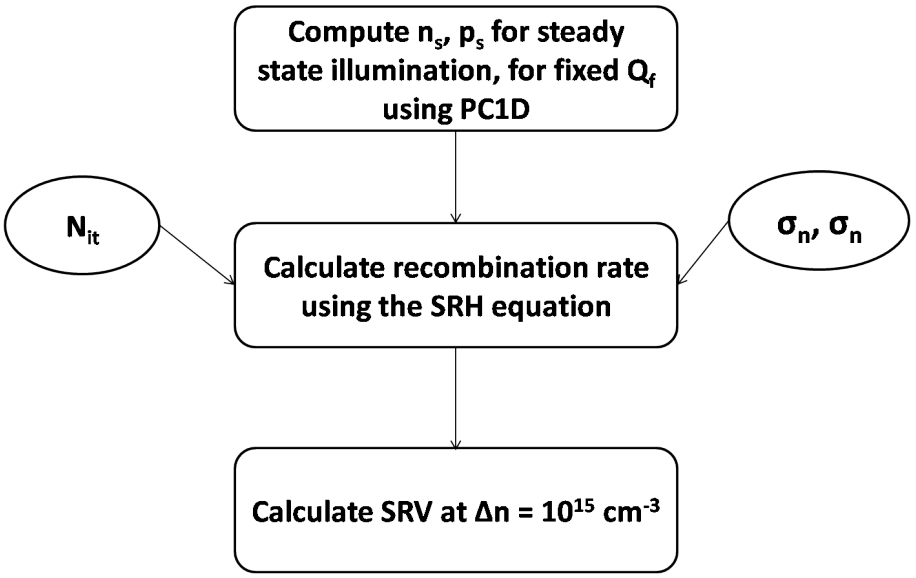


Fig. A.1: Flow chart for simulating impact of N_{it} and Q_f on S_{eff}.

Relevant equations

$$U_s = \frac{pn - n_i^2}{\frac{n+n_1}{S_p} + \frac{p+p_1}{S_n}} \tag{A.1}$$

where $S_n = \sigma_n N_{it} v_{th}$ and $S_p = \sigma_p N_{it} v_{th}$, where N_{it} represents the trap density at the surface in cm^{-2}. S_n, S_p are the surface recombination velocity for electrons and holes respectively. p and

n represent the excess carrier density [23]. Ignoring the $n_i{}^2$, Eqn modifies to

$$U_s = \frac{pn}{\frac{n+n_1}{S_p} + \frac{p+p_1}{S_n}} \tag{A.2}$$

The effective surface recombination velocity (S_{eff}) is calculated from U_s using the relation:

$$S_{eff} = \frac{U_s}{\Delta n} \tag{A.3}$$

Δn is the injection level. In the simulations described in the thesis, Δn = 10^{15} cm^{-3} was used.

Table A.1: Parameters used for calculating excess carrier density

Parameter	Value
Wafer thickness	1 μm
Front surface texture	5 μm
Anti-reflective coating	75 nm, RI - 2.0
Emitter contact resistance	1 $\mu\Omega$
Base contact resistance	1 $\mu\Omega$
Shunt resistance	∞
N - type substrate doping	2.382x10^{15} cm^{-3}
Bulk lifetime	1 ms
Excitation mode	Steady state
Temperature	300 K
Steady state intensity	0.1 W/cm^2
Steady state wavelength	300 nm
Fixed charge density	10^{10} - 10^{12} cm^{-2} (varied)

MATLAB Code

```
breaklines
%computation for a n-type wafer
clc
clear all
x=xlsread('doping.xlsx','1e20') %input file with ns, ps for Qf
Charge_density = x(:,1);
Ns = x(:,2);
Ps = x(:,3);

len = length (Ns);
Vth = 2.0*10^7; %in cm/s
Dit = input('Enter Nit in cm-2      ');
sigma_n = 10^-16;
sigma_p = 10^-16;
```

```
Sn = Dit*Vth*sigma_n;
Sp = Dit*Vth*sigma_p;

Us = zeros(1,len);
for i = 1:len
denom(i) = (Ns(i)/Sp+Ps(i)/Sn); %computation of Us
num(i) = Ns(i)*Ps(i);
Us(i) = num(i)/denom(i);
end

Seff = Us/(1*10^15);
Seff1 = Seff';
loglog(Charge_density, Seff);
```

A.2 Extraction of interface state density and fixed charge in the dielectric from high frequency capacitance - voltage curves

The relevant equations and methodology used for the extraction of interface state density and fixed charge density was discussed in detail in section. 4.6 of the thesis. The MATLAB code shown below is just an implementation of the same.

```
    breaklines
% CV Extract
clc

%Constants
Esi = 11.7*8.85*10^-14;
B = 0.026;
ni = 1.5*10^10;
q = 1.6*10^-19;

% Computation of Substrate Doping Concentration
C1 = input ('Enter Cmax ');
C2 = input ('Enter Cmin ');
Area = input ('Enter Area of the capacitor ');
Cmax = C1/Area;
Cmin = C2/Area;
Cshf = (Cmax*Cmin)/(Cmax-Cmin);
Xd = Esi/Cshf;
Na = 10^14;
for i = 1:0.5:10^4
ind = length(i);
```

```
LHS(1:ind) = log(ni)+((Xd^2*i*Na*q)/(4*Esi*B));
RHS(1:ind) = log(Na*i);
if(abs(LHS(ind)-RHS(ind))<0.5)
    Na=Na*i;
    break
else
    continue
end
 end
phiB = B*log (Na/ni);
debyelength = ((B*Esi)/(q*Na))^0.5;
CsFB = Esi/debyelength;
CFB = (Cmax*CsFB)/(Cmax+CsFB);
XMG = ((2*Esi*phiB)/(q*Na))^0.5;
CsMG = Esi/XMG;
CMG = (CsMG*Cmax)/(CsMG+Cmax);
uCMG = Area*CMG;
disp (uCMG);
VMG = input ('Enter the mid gap voltage ');
phiMS = -(0.55+phiB);
VMGideal = phiMS + phiB + (q*Na*XMG/Cmax);
deltaV = VMGideal - VMG;
Qox = 6.25*10^18*Cmax*deltaV; %Computation of fixed charge density
disp (Qox);

% Computation of interface trap density
Gm = input ('Enter the maximum value of conductance ');
Cm = input ('Enter the value of capacitance Cm ');
f = input ('Enter the frequency of operation in Hz ');
w = 2*pi*f;
Cm1 = Cm/Area;
denom = (Gm/(w*C1))^2 + (1-Cm/C1)^2;
num = Gm/w;
Dit = (2/(q*Area))*(num/denom);
disp (Dit);
```

Appendix B

Process recipes for solar cell fabrication

Saw damage removal

Tool: Wet chemical bench

- 2% HF dip - 240 ml of HF (49% HF), DI water - 5760 ml, 30 s.
- DI water rinse
- KOH - 1200 gm in 6000 ml of DI water, process temperature = 80^{o}C, time = 3 min.
- DI water rinse following the process.

Texturization

Tool: Wet chemical bench

- 2% HF dip - 240 ml of HF (49% HF), DI water - 5760 ml, 30 s.
- DI water rinse.
- KOH - 150 gm in 6000 ml of DI water, IPA - 480 ml of IPA, process temperature = 80^{o}C, time = 40 min.
- DI water rinse following the process.

RCA cleaning

Tool: Wet chemical bench

- 2% HF dip - 240 ml of HF (49% HF), DI water - 5760 ml, 30 s.
- RCA1 - NH_4OH:H_2O_2:DI water in the ratio 600ml:1200 ml:4200 ml, 80^{o}C, 20 min on heater and 20 min off heater.
- DI water rinse and 2%HF dip followed by DI water rinse.
- RCA 2 - HCl:H_2O_2:DI water in the ratio 600ml:1200ml:4200ml, 80^{o}C, 20 min on heater and 20 min off heater.
- DI water rinse and 2%HF dip followed by DI water rinse.

Diffusion

Tool: Diffusion furnace, Protemp

- Load in: 450^{o}C, 2 min, N_2 = 1 SLPM.
- Ramp up: 875^{o}C, 12 min, N_2 = 8.15 SLPM.
- Idle: 875^{o}C, 5 min, N_2 = 8.15 SLPM.
- Oxide: 875^{o}C, 5 min, N_2 = 8.15 SLPM ,O_2 = 0.45 SLPM.
- Ramp down: 840^{o}C, 10 min, N_2 = 8.15 SLPM.
- Stabilise: 840^{o}C, 5 min, N_2 = 8.15 SLPM.
- $POCl_3$ deposition: 840^{o}C, 20 min, N_2 = 8.15 SLPM, O_2 = 0.45 SLPM, $POCl_3$ = 0.45 SLPM.
- Purge: 840^{o}C, 5 min, N_2 = 8.15 SLPM.
- Drive in: 840^{o}C, 36 min, N_2 = 8.15 SLPM, O_2 = 0.45 SLPM.
- Ramp down: 750^{o}C, 12 min, N_2 = 8.15 SLPM.
- Load out: 750^{o}C, 5 min, N_2 = 8.15 SLPM.

- Ramp down: 450^{o}C, 20 min, N_2 = 8.15 SLPM.
- Idle: 450^{o}C, N_2 = 1 SLPM.

Edge isolation

Tool: NT2 plasma etcher, BSET EQ

- SF_6 - 27 sccm, 45 min, 200 mTorr, RF - 450 W, 0.5 rpm.

PSG removal

Tool: Wet chemical bench

- 2% HF dip - 240 ml of HF (49% HF), DI water - 5760 ml, 5 min.
- DI water rinse

Silicon nitride deposition

Tool: PECVD 100, Oxford instruments

- SiH_4: N_2 :: 25 sccm : 980 sccm, NH_3 = 20 sccm, 6 min, 380^{o}C, 650 mTorr, 20 W.

Screen printing

Tool: Screen printer, Haikutech

- Front contact printing: Finger width - 80 μm, bus bar width - 1.5 mm, Squeegee pressure - 0.14 MPa, Snap off - 1.5 mm.
- Back contact printing: Squeegee pressure - 0.14 MPa, Snap off - 1.0 mm.
- Drying: 250^{o}C, 7 min.

Contact firing

Tool: RTP, Allwin systems

- Delay: 0^oC, N_2 = 10 SLPM, 30 s.
- Ramp up: 300^oC, N_2 = 2 SLPM, O_2 = 3 SLPM, 7 s.
- Steady: 300^oC, N_2 = 2 SLPM, O_2 = 3 SLPM, 2 s.
- Ramp up: 400^oC, N_2 = 2 SLPM, O_2 = 3 SLPM, 20 s.
- Steady: 400^oC, N_2 = 2 SLPM, O_2 = 3 SLPM, 1 s.
- Ramp up: 850^oC, N_2 = 2 SLPM, O_2 = 3 SLPM, 8 s.
- Steady: 850^oC, N_2 = 2 SLPM, O_2 = 3 SLPM, 1 s.
- Delay: 0^oC, N_2 = 2 SLPM, O_2 = 3 SLPM, 240 s.

Other silicon nitride and silicon oxy-nitride recipes

Recipe for plasma oxidation described in section. 6.1

Tool: PECVD 100, Oxford instruments

- N_2O = 200 sccm, time = 5 - 40 min, 380^oC, 1000 mTorr, 10 W.

Recipe for plasma oxidation described in section. 6.2

Tool: PECVD 100, Oxford instruments

- N_2O = 20 sccm, Ar = 180 sccm time = 5 - 40 min, 380^oC, 1000 mTorr, 10 W.

Silicon nitride film labelled SiN described in chapter 7

Tool: PECVD 100, Oxford instruments

- Bottom layer: SiH_4: N_2 :: 50 sccm : 50 sccm, NH_3 = 50 sccm, Ar = 40 sccm, 1 min, 380^oC, 650 mTorr, 20 W.
- Capping layer: SiH_4: N_2 :: 25 sccm : 980 sccm, NH_3 = 20 sccm, 5:30 min, 380^oC, 650 mTorr, 20 W.

Single layer silicon nitride flim labelled SiN_y:H, described in chapter 7

Tool: PECVD 100, Oxford instruments

- SiH_4: N_2 :: 25 sccm : 980 sccm, NH_3 = 20 sccm, 6:00 min, 380^{o}C, 650 mTorr, 20 W.

Recipe for post deposition plasma treatment of silicon nitride described in chapter 7

Tool: PECVD 100, Oxford instruments

- N_2O = 20 sccm, Ar = 180 sccm, time = 10 min, 380^{o}C, 1000 mTorr, 10 W.

Bibliography

[1] http://en.wikipedia.org/wiki/Photovoltaics

[2] S. W. Glunz, R. Preu, D. Biro, and E. Systems, "Crystalline Silicon Solar Cells: State-of-the-Art and Future Developments," in *Comprehensive Renewable Energy*, A. Sayigh Ed., Elsevier, 2012. DOI: 10.1016/B978-0-08-087872-0.00117-7.

[3] http://www.itrpv.net/Reports/Downloads/2015/

[4] L. Tous, M. Aleman, R. Russell, E. Cornagliotti, P. Choulat, A. Uruena, S. Singh, J. John, F. Duerinckx, J. Poortmans, and R. Mertens, "Evaluation of advanced p-PERL and n-PERT large area silicon solar cells with 20.5% energy conversion efficiencies," *Prog. Photovoltaics Res. Appl.*, 2014. DOI: 10.1002/pip.2478.

[5] M. C. Raval and C. S. Solanki, "Review of Ni-Cu Based Front Side Metallization for c - Si Solar Cells," *J. Sol. Energy*, 2013. DOI: 10.1155/2013/183812.

[6] S. Wang, T. Puzzer, B. Vogl, B. Tjahjono, B. Hallam, M. Eadie, N. Borojevic, Z. Hameiri, S. Wenham, "Overcoming Over-Plating Problems on Acid Textured Multicrystalline Wafers with Silicon Nitride Coated Surfaces," *proc. of the 24th European Photovoltaic Solar Energy Conference*, 2009. DOI: 10.4229/24thEUPVSEC2009-2CV.2.12.

[7] M. Green, "The path to 25% silicon solar cell efficiency: history of silicon cell evolution," *Prog. Photovoltaics Res. Appl.*, 2009. DOI: 10.1002/pip.892.

[8] N. Borojevic, A. Lennon, and S. Wenham, "Light trapping structures for silicon solar cells via inkjet printing," *Phys. Status Solidi*, 2014. DOI: 10.1002/pssa.201330654.

[9] A. Goetzberger, J. Knolbolch, B. Voss, "Crystalline Silicon Solar Cells," *John Wiley and Sons*, 1998. ISBN: 978-0-471-97144-3.

[10] Dingemans G., Kessels W.M.M. "Status and prospects of Al2O3-based surface passivation schemes for silicon solar cells", *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 2012. DOI: 10.1116/1.4728205.

[11] A. Goodrich, P. Hacke, Q. Wang, B. Sopori, R. Margolis, T. L. James, and M. Woodhouse, "A wafer-based monocrystalline silicon photovoltaics road map: Utilizing known technology improvement opportunities for further reductions in manufacturing costs," *Sol. Energy Mater. Sol. Cells*, 2013. DOI: 10.1016/j.solmat.2013.01.030.

[12] N. E. Grant and K. R. McIntosh,"Passivation of a (100) Silicon Surface by Silicon Dioxide Grown in Nitric Acid," *IEEE Electron Device Letters*, 2009. DOI: 10.1109/LED.2009.2025898.

[13] O. Schultz, A. Mette, M. Hermle, and S. W. Glunz, "Thermal oxidation for crystalline silicon solar cells exceeding 19% efficiency applying industrially feasible process technology," *Prog. Photovoltaics Res. Appl.*, 2008 DOI: 10.1002/pip.814.

[14] K. Sekine, Y. Saito, M. Hirayama, and T.Ohmi "Highly reliable ultrathin silicon oxide film formation at low temperature by oxygen radical generated in high-density krypton plasma," *IEEE Trans. Electron. Dev.*, 2001. DOI: 10.1109/16.936559.

[15] A. Uzum, A. Hamdi, S. Nagashima, S. Suzuki, H. Suzuki, S. Yoshiba, M. Dhamrin, K. Kamisako, H. Sato, K. Katsuma, and K. Kato, "Selective emitter formation process using single screen-printed phosphorus diffusion source," *Sol. Energy Mater. Sol. Cells*, 2013. DOI: 10.1016/j.solmat.2012.11.013.

[16] S. Wang, A. Lennon, B. Tjahjono, L. Mai, B. Vogl, and S. Wenham, "Overcoming over-plating problems for PECVD SiN_x passivated laser doped p-type multi-crystalline silicon solar cells," *Sol. Energy Mater. Sol. Cells*, 2012. DOI: 10.1016/j.solmat.2011.12.003.

[17] G. Hamm, D.L Jacques, C.J. Colangelo "Method of inhibiting background plating," U.S. patent 7,939,438 B2, May 10, 2011. Weblink.

[18] M. Bose, D. K. Basa, and D. N. Bose, "Study of nitrous oxide plasma oxidation of silicon nitride thin films," *Appl. Surf. Sci.*, 2000. DOI: 10.1016/S0169-4332(00)00023-4.

[19] M.C.Raval, S.Saseendran, S.Suckow, S.Saravanan, C.S.Solanki, A. Kottantharayil, "N_2O plasma treatment for minimization of background plating in silicon solar cells with Ni-Cu front side metallization," under review, *Sol. Energy Mater. Sol. Cells*

[20] J. D. Murphy, R. E. McGuire, K. Bothe, V. V. Voronkov, and R. J. Falster, "Competitive gettering of iron in silicon photovoltaics: Oxide precipitates versus phosphorus diffusion," *J. Appl. Phys.*, 2014. DOI: 10.1063/1.4892015.

[21] S. M. Sze, Kwok K. Ng, "Physics of semiconductor devices", 3^{rd} edition, *John Wiley & Sons*, 2007. ISBN: 978-0-471-14323-9.

[22] S. Rein "Lifetime Spectroscopy - A method of defect characterization in silicon for photovoltaic applications", *Springer*, 2005. ISBN: 978-3-540-27922-8.

[23] A. G. Aberle, S. Glunz, W. Warta, "Impact of illumination level and oxide parameters on Shockley-Read-Hall recombination at the Si-SiO_2 interface," *J. Appl. Phys*, 1992. DOI: 10.1063/1.350782.

[24] R. Har-Lavan, R. Schreiber, O. Yaffe, and D. Cahen, "Molecular field effect passivation: Quinhydrone/methanol treatment of n-Si(100)," *J. Appl. Phys.*, 2013. DOI: 10.1063/1.4793497.

[25] A. Aberle, S. Glunz, and W. Warta, "Field effect passivation of high efficiency silicon solar cells," *Sol. Energy Mater. Sol. Cells*, 1993. DOI: 10.1016/0927-0248(93)90075-E.

[26] R. A. Sinton and A. Cuevas, "Contactless determination of current- voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data", *Appl. Phys. Lett.*, 1996. DOI: 10.1063/1.117723.

[27] S. W. Glunz, D. Biro, S. Rein, and W. Warta, "Field-effect passivation of the SiO_2-Si interface," *J. Appl. Phys.*, 1999. DOI: 10.1063/1.370784.

[28] A. Stephens, M, Green, "Effectiveness of 0.08 molar iodine in ethanol solution as a means of chemical surface passivation for photoconductance decay measurements," *Sol. Energy Mater. Sol. Cells*, 1997. DOI: 10.1016/S0927-0248(96)00061-X.

[29] H. Takato , I. Sakata , R. Shimokawa , "Surface passivation of silicon subtrates using Quinhydrone/Methanol treatment," *proc. of 3rd IEEE World Conference on Photovoltaic Energy Conversion*, 2003. DOI: not available. Weblink.

[30] W. Soppe, H. Rieffe, and A. Weeber, "Bulk and surface passivation of silicon solar cells accomplished by silicon nitride deposited on industrial scale by microwave PECVD," *Prog. Photovoltaics Res. Appl.*, 2005. DOI: 10.1002/pip.611.

[31] T. Lauinger, J. Moschner, A. G. Aberle, and R. Hezel, "UV stability of highest-quality plasma silicon nitride passivation of silicon solar cells,"*proc. of 25th IEEE Photovoltaic Specialists Conference*, 1996. DOI: 10.1109/PVSC.1996.564032.

[32] S. Dauwe, L. Mittelstadt, A. Metz, and R. Hezel, "Experimental evidence of parasitic shunting in silicon nitride rear surface passivated solar cells," *Prog. Photovoltaics Res. Appl.*, 2002. DOI: 10.1002/pip.420.

[33] G. Dingemans, P. Engelhart, R. Seguin, F. Einsele, B. Hoex, M. C. M. van de Sanden, and W. M. M. Kessels, "Stability of Al_2O_3 and Al_2O_3/a-SiN_x:H stacks for surface passivation of crystalline silicon," *J. Appl. Phys.*, 2009. DOI: 10.1063/1.3264572.

[34] M. Schaper, J. Schmidt, H. Plagwitz, and R. Brendel, "20.1%-Efficient Crystalline Silicon Solar Cell With Amorphous Silicon Rear-Surface Passivation," *Prog. Photovoltaics Res. Appl.*, 2005. DOI: 10.1002/pip.641.

[35] T. Matsumoto, R. Hirose, F. Shibata, D. Ishibashi, S. Ogawara, and H. Kobayashi, "Nitric acid oxidation of Si method for improvement of crystalline Si solar cell characteristics by surface passivation effect," *Sol. Energy Mater. Sol. Cells*, 2015. DOI: 10.1016/j.solmat.2014.11.040.

[36] S. Mack, C. Wufka, a. Wolf, U. Belledin, D. Scheffler, and D. Biro, "Surface passivation of phosphorus-diffused emitters by inline thermal oxidation," *Energy Procedia*, 2011. DOI: 10.1016/j.egypro.2011.06.147.

[37] A. Rohatgi, S. Narasimha, U. Ebong, and P. Doshi, "Understanding and implementation of rapid thermal technologies for high-efficiency silicon solar cells," *IEEE Trans. Electron Devices*, 1999. DOI: 10.1109/16.791984.

[38] A. Das, K. Ryu, and A. Rohatgi, "20% efficient screen-printed n-type solar cells using a spin-on source and thermal oxide/silicon nitride passivation," *IEEE J. Photovoltaics*, 2011. DOI: 10.1109/JPHOTOV.2011.2172189.

[39] D. L. Meier, V. Chandrasekaran, H. P. Davis, A. M. Payne, X. Wang, V. Yelundur, J. E. Oneill, Y. W. Ok, F. Zimbardi, and A. Rohatgi, "N-type, ion-implanted silicon solar cells and modules," *IEEE J. Photovoltaics*, 2011. DOI: 10.1109/JPHOTOV.2011.2169944.

[40] C. Schmiga, H. Nagel, and J. Schmidt, "19% efficient n-type czochralski silicon solar cells with screen-printed aluminium-alloyed rear emitter," *Prog. Photovoltaics Res. Appl.*, 2006. DOI: 10.1002/pip.725.

[41] J. Zhao, a. Wang, P. Altermatt, and M. A. Green, "Twenty-four percent efficient silicon solar cells with double layer antireflection coatings and reduced resistance loss," *Appl. Phys. Lett.*, 1995. DOI: 10.1063/1.114124.

[42] J. Benick and K. Zimmermann, "Rear side passivation of PERC - type solar cells by wet oxides grown from purified steam," *Prog. Photovoltaics Res. Appl.*, 2011. DOI: 10.1002/pip.1020.

[43] M. Hofmann, S. Janz, C. Schmidt, S. Kambor, D. Suwito, N. Kohn, J. Rentsch, R. Preu, and S. W. Glunz, "Recent developments in rear-surface passivation at Fraunhofer ISE," *Sol. Energy Mater. Sol. Cells*, 2009. DOI: 10.1016/j.solmat.2008.11.056.

[44] S.Gatz et al."Firing Stability of SiN_y / SiN_x surface passivation stacks for crystalline silicon solar cells".*proc. of the 26th European Photovoltaic Solar Energy Conference and Exhibition*, 2011. DOI: 10.4229/26thEUPVSEC2011-2DO.1.5.

[45] D. Zielke, D. Sylla, T. Neubert, R. Brendel, and J. Schmidt, "Direct Laser Texturing for High-Efficiency Silicon Solar Cells," *IEEE J. Photovoltaics*, 2012. DOI: 10.1109/JPHOTOV.2012.2228302.

[46] X. Wang, V. Allen, V. Vais, Y. Zhao, B. Tjahjono, Y. Yao, S. Wenham, and A. Lennon, "Laser-doped metal-plated bifacial silicon solar cells," *Sol. Energy Mater. Solar Cells*, 2014. DOI: 10.1016/j.solmat.2014.06.020.

[47] T. Dullweber, S. Gatz, H. Hannebauer, T. Falcon, R. Hesse, J. Schmidt, and R. Brendel, "Towards 20% efficient large-area screen-printed rear-passivated silicon solar cells," *Prog. Photovoltaics Res. Appl.*, 2011. DOI: 10.1002/pip.1198.

[48] Y. Tao, A. Payne, V. D. Upadhyaya, and A. Rohatgi, "20.7% Efficient ion-implanted large area n-type front junction silicon solar cells with rear point contacts formed by laser opening and physical vapor deposition," *Prog. Photovoltaics Res. Appl.*, 2014. DOI: 10.1002/pip.2545.

[49] Meenakshi Bhaisare, Abhishek Misra and Anil Kottantharayil, "Aluminum Oxide Deposited by Pulsed-DC Reactive Sputtering for Crystalline Silicon Surface Passivation," *IEEE J. Photovoltaics*, 2013. DOI: 10.1109/JPHOTOV.2013.2251057.

[50] Kalaivani S., Anil Kottantharayil, "Spray Coated Aluminum Oxide Thin Film For P-type Crystalline Silicon Surface Passivation," *presented at the 42nd IEEE Photovoltaic Specialist Conference*, 2015.

[51] J. Schmidt and M. Kerr, "Surface passivation of silicon solar cells using plasma-enhanced chemical-vapour-deposited SiN films and thin thermal SiO_2 / plasma SiN stacks," *Semicond. Sci. Technol.*, 2001. DOI: 10.1088/0268-1242/16/3/308.

[52] T. Lauinger, J. Schmidt, A. G. Aberle, and R. Hezel, "Record low surface recombination velocities on 1 Ω - cm p-silicon using remote plasma silicon nitride passivation," *Appl. Phys. Lett.*,1996. DOI: 10.1063/1.115936.

[53] T. Lauinger, J. Moschner, A. G. Aberle, and R. Hezel, "Optimization and characterization of remote plasma-enhanced chemical vapor deposition silicon nitride for the passivation of p-type crystalline silicon surfaces," *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, 1998. DOI: 10.1116/1.581095.

[54] S. Duttagupta, F. Lin, M. Wilson, M. B. Boreland, B. Hoex, and A. G. Aberle, "Extremely low surface recombination velocities on low-resistivity n-type and p-type crystalline silicon using dynamically deposited remote plasma silicon nitride films," *Prog. Photovoltaics Res. Appl.*, 2012. DOI: 10.1002/pip.2320.

[55] B. Lenkeit, S. Steckemetz, F. Artuso, and R. Hezel , "Excellent thermal stability of remote plasma-enhanced chemical vapour deposited silicon nitride films for the rear of

screen-printed bifacial silicon solar cells", *Sol. Energy Mater. Sol. Cells*, 2001. DOI: 10.1016/S0927-0248(00)00108-2.

[56] H. Mackel and R. Ludemann, "Detailed study of the composition of hydrogenated SiNx layers for high-quality silicon surface passivation," *J. Appl. Phys.*, 2002. DOI: 10.1063/1.1495529.

[57] M. Mccann, K. Weber, and A. Blakers, "Surface Passivation by rehydrogenation of silicon nitride coated silicon wafers," *Prog. Photovoltaics Res. Appl.*, 2005. DOI: 10.1002/pip.580.

[58] M. W. P. E. Lamers, K. T. Butler, J. H. Harding, and A. Weeber, "Interface properties of a-SiNx:H/Si to improve surface passivation," *Sol. Energy Mater. Sol. Cells*, 2012. DOI: 10.1016/j.solmat.2012.06.025.

[59] M. Lamers, L. E. Hintzsche, K. T. Butler, P. E. Vullum, C. M. Fang, M. Marsman, G. Jordan, J. H. Harding, G. Kresse, and A. Weeber," The interface of a-SiNx:H and Si: Linking the nano-scale structure to passivation quality," *Sol. Energy Mater. Sol. Cells*, 2014. DOI: 10.1016/j.solmat.2013.04.026.

[60] H. Jin, K. J. Weber, P. N. K. Deenapanray, and A. W. Blakers, "Hydrogen Reintroduction by Forming Gas Annealing to LPCVD Silicon Nitride Coated Structures," *Journal of The Electrochemical Society*, 2006. DOI: 10.1149/1.2207058.

[61] K. J. Weber and H. Jin, "Improved silicon surface passivation achieved by negatively charged silicon nitride films," *Appl. Phys. Lett.*, 2009. DOI: 10.1063/1.3077157.

[62] Y. Wan, K. R. McIntosh, A. F. Thomson, and A. Cuevas, "Recombination and thin film properties of silicon nitride and amorphous silicon passivated c-Si following ammonia plasma exposure," *Appl. Phys. Lett.*, 2015. DOI: 10.1063/1.4907377.

[63] G. Dingemans, M. M. Mandoc, S. Bordihn, M. C. M. van de Sanden, and W. M. M. Kessels, "Effective passivation of Si surfaces by plasma deposited SiO_x/a-SiN_x:H stacks," *Appl. Phys. Lett.*, 2011. DOI: 10.1063/1.3595940.

[64] S. Mack, A. Wolf, C. Brosinsky, S. Schmeisser, A. Kimmerle, P. Saint-Cast, M. Hofmann, and D. Biro, "Silicon Surface Passivation by Thin Thermal Oxide/PECVD Layer Stack Systems," *IEEE J. Photovoltaics*, 2011. DOI: 10.1109/JPHOTOV.2011.2173299.

[65] Y. Larionova, V. Mertens, N.-P. Harder, and R. Brendel, "Surface passivation of n-type Czochralski silicon substrates by thermal-SiO_2/plasma-enhanced chemical vapor deposition SiN stacks," *Appl. Phys. Lett.*, 2010. DOI: 10.1063/1.3291681.

[66] S. Narasimha and A. Rohatgi, "Effective passivation of the low resistivity silicon surface by a rapid thermal oxide / plasma silicon nitride stack," *Appl. Phys. Lett.*, 1998. DOI: 10.1063/1.121211.

[67] S. MacK, A. Wolf, A. Walczak, B. Thaidigsmann, E. Allan Wotke, J. J. Spiegelman, R. Preu, and D. Biro, "Properties of purified direct steam grown silicon thermal oxides," *Sol. Energy Mater. Sol. Cells*, 2011. DOI: 10.1016/j.solmat.2011.03.002.

[68] A. Moldovan, F. Feldmann, G. Krugel, M. Zimmer, J. Rentsch, M. Hermle, A. Roth-Folsch, K. Kaufmann, and C. Hagendorf, "Simple Cleaning and Conditioning of Silicon Surfaces with UV/Ozone Sources," *Energy Procedia*, 2014. DOI: 10.1016/j.egypro.2014.08.067.

[69] K. Wolke, C. Gottschalk, J. Rentsch, and H. Angermann, "Ozone Based Chemical Oxide Growth for Crystalline Solar Cell Production," *Solid State Phenom.*, 2012. DOI: 10.4028/www.scientific.net/SSP.187.321.

[70] N. E. Grant and K. R. McIntosh, "Low Surface Recombination Velocity on (100) Silicon by Electrochemically Grown Silicon Dioxide Annealed at Low Temperature," *IEEE Electron Device Lett.*, 2010. DOI: 10.1109/led.2010.2052780.

[71] J. Cui, X. Wang, R. Opila, and A. Lennon "Light-induced anodisation of silicon for solar cell passivation," *J. Appl. Phys.*, 2013. DOI: 10.1063/1.4829701.

[72] Z. R. Chowdhury, K. Cho, and N. P. Kherani, "High-quality surface passivation of silicon using native oxide and silicon nitride layers High-quality surface passivation of silicon using native oxide and silicon nitride layers," *Appl. Phys. Lett.*, 2012. DOI: 10.1063/1.4733336.

[73] V. D. Mihailetchi, Y. Komatsu, and L. J. Geerligs, "Nitric acid pretreatment for the passivation of boron emitters for n-type base silicon solar cells," *Appl. Phys. Lett.*, 2008. DOI: 10.1063/1.2870202.

[74] F. Shibata, D. Ishibashi, S. Ogawara, T. Matsumoto, C.-H. Kim, and H. Kobayashi, "Improvement of Minority Carrier Lifetime and Si Solar Cell Characteristics by Nitric Acid Oxidation Method," *ECS J. Solid State Sci. Technol.*, 2014. DOI: 10.1149/2.024406jss.

[75] A. A. Bright, J. Batey, and E. Tierney, "Low-rate plasma oxidation of Si in a dilute oxygen/helium plasma for low-temperature gate quality Si/SiO_2 interfaces," *Appl. Phys. Lett.*, 1991. DOI:10.1063/1.104547 .

[76] I. Garduno, P. Saint-Cast, J. C. Tinoco, and M. Estrada, "Dependence With Pressure And Temperature Of The Plasma Oxidation Mechanism Applied To Ultrathin Oxides," *proc. of the 6th International Caribbean Conference on Devices, Circuits and Systems*, 2006. DOI: 10.1109/ICCDCS.2006.250851.

[77] J. A. Diniz and P. J. Tatsch, "Oxynitride films formed by low energy NO^+ implantation into silicon," *Appl. Phys. Lett.*,1996. DOI: 10.1063/1.117169.

[78] A. Masuda, A. Morimoto, M. Kumeda, T. Shimizu, Y. Yonezawa, and T. Minamikawa, "Novel oxidation process of hydrogenated amorphous silicon utilizing nitrous oxide plasma," *Appl. Phys. Lett.*, 1992. DOI: 10.1063/1.107754.

[79] Y. W. Choi and B. T. Ahn, "A study on the oxidation kinetics of silicon in inductively coupled oxygen plasma," *J. Appl. Phys.*, 1999. DOI: 10.1063/1.371320.

[80] S. R. Kaluri and D. W. Hess, "Constant Current N_2O Plasma Anodization of Silicon," *J. Electrochem. Soc.*, 1997. DOI: 10.1149/1.1837765.

[81] T. Kaspar, A. Tuan, R. Tonkyn, W. P. Hess, J. W. Rogers, and Y. Ono, "Role of O1D in the oxidation of Si(100)," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 2003. DOI: 10.1116/1.1563254.

[82] H. Kakiuchi, H. Ohmi, M. Harada, H. Watanabe, and K. Yasutake, "Significant enhancement of Si oxidation rate at low temperatures by atmospheric pressure Ar/O_2 plasma," *Appl. Phys. Lett.*, 2007. DOI: 10.1063/1.2721366.

[83] A. K. Antonenko, V. a. Volodin, M. D. Efremov, P. S. Zazulya, G. N. Kamaev, and D. V. Marin, "Oxidation kinetics of a silicon surface in a plasma of oxygen with inert gases," *Optoelectron. Instrum. Data Process.*, 2011. DOI: 10.3103/S8756699011050268.

[84] Y. C. Liu, L. T. Ho, Y. B. Bai, T. J. Li, K. Furakawa, D. W. Gao, H. Nakashima, and K. Muroaka, "Growth of ultrathin SiO 2 on Si by surface irradiation with an O2/Ar electron cyclotron resonance microwave plasma at low temperatures," *J. Appl. Phys.*, 1999. DOI: 10.1063/1.369183.

[85] B. H. Kim, J. H. Ahn, and B. T. Ahn, "Finding interstitial oxygen in an Si substrate during low-temperature plasma oxidation," *Appl. Phys. Lett.*, 2003. DOI: 10.1063/1.369183.

[86] M. Stavola, "Infrared spectrum of interstitial oxygen in silicon," *Appl. Phys. Lett.*, 1984. DOI: 10.1063/1.94816.

[87] G. D. K. Mahanama and H. S. Reehal, "A comparison of nitrous oxide and hydrogen ECR plasma discharges for silicon solar cell passivation," *Vaccum*, 2011. DOI: 10.1016/j.vacuum.2011.06.001.

[88] P. K. Basu, A. Khanna, and Z. Hameiri, "The effect of front pyramid heights on the efficiency of homogeneously textured inline-diffused screen-printed monocrystalline silicon wafer solar cells," *Renew. Energy*, 2015. DOI: 10.1016/j.renene.2015.01.058.

[89] U. Gangopadhyay, S. K. Dhungel, P. K. Basu, S. K. Dutta, H. Saha, and J. Yi, "Comparative study of different approaches of multicrystalline silicon texturing for solar cell fabrication," *Sol. Energy Mater. Sol. Cells*, 2007. DOI: 10.1016/j.solmat.2006.08.011.

[90] D. H. Macdonald, a. Cuevas, M. J. Kerr, C. Samundsett, D. Ruby, S. Winderbaum, and a. Leo, "Texturing industrial multicrystalline silicon solar cells," *J. Sol. Energy*, 2004. DOI: 10.1016/j.solener.2003.08.019.

[91] J. Dong and S. H. Huang, "Low-reflective surface texturing for large area multicrystalline silicon using NaOH-NaClO solution," *Surf. Eng. Appl. Electrochem.*, 2014. DOI: 10.3103/S1068375514010050.

[92] C. Trompoukis, O. El Daif, P. P. Sharma, H. S. Radhakrishnan, M. Debucquoy, V. Depauw, K. Van Nieuwenhuysen, I. Gordon, R. Mertens, and J. Poortmans, "Passivation of photonic nanostructures for crystalline silicon solar cells," *Prog. Photovolt: Res. Appl.*, 2014. DOI: 10.1002/pip.2489.

[93] V. Prajapathi, "Advanced Front-Side Technology in Crystalline Silicon Solar Cells," Ph.D thesis, KU Leuven, Belgium, 2013. Weblink.

[94] M. A. Green, C. M. Chong, F. Zhang, A. Sproul, J. Zolper, and S. R. Wenham, "20% efficient laser grooved buried contact silicon solar cells," *proc.of 20th IEEE Photovoltaic Specialists Conference*, Las Vegas, USA, 1988. DOI: 10.1109/PVSC.1988.105733.

[95] B. M. Kayes, H. a. Atwater, and N. S. Lewis, "Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells," *J. Appl. Phys.*, 2005. DOI: 10.1063/1.1901835.

[96] J. Zhu, C. Hsu, Z. Yu, S. Fan, and Y. Cui, "Nanodome solar cells with efficient light management and self-cleaning.," *Nano Lett.*, 2010. DOI: 10.1021/nl9034237.

[97] K.-Q. Peng, X. Wang, L. Li, X. Wu, and S.-T. Lee, "High-performance silicon nanohole solar cells.," *J. Am. Chem. Soc.*, 2010. DOI: 10.1021/ja910082y.

[98] A. Mavrokefalos, S. E. Han, S. Yerci, M. S. Branham, and G. Chen, "Efficient light trapping in inverted nanopyramid thin crystalline silicon membranes for solar cell applications," *Nano Lett.*, 2012. DOI: 10.1021/nl2045777.

[99] H. Hauser, B. Michl, S. Schwarzkopf, V. Kubler, C. Muller, M. Hermle, B. Blasi, "Honeycomb Texturing of Silicon Via Nanoimprint Lithography for Solar Cell Applications," *IEEE J. Photovoltaics*, 2012. DOI: 10.1109/JPHOTOV.2012.2184265.

[100] M. Moreno, D. Daineka, and P. R. Cabarrocas, "Plasma texturing for silicon solar cells : From pyramids to inverted pyramids-like structures," *Sol. Energy Mater. Sol. Cells*, 2010. DOI: 10.1016/j.solmat.2009.12.015.

[101] N. S. Zin, A. Blakers, and K. Weber, "RIE-induced carrier lifetime degradation," *Prog. Photovolt: Res. Appl.*, 2010. DOI: 10.1002/pip.935.

[102] K. Kumar, K. K. C. Lee, J. Nogami, P. R. Herman, and N. P. Kherani, "Ultrafast laser direct hard-mask writing for high efficiency c - Si texture designs," *EPJ Photovoltaics*, 2013. DOI: 10.1051/epjpv/2013015.

[103] C.H. Sun, W.L. Min, N. C. Linn, P. Jiang, and B. Jiang, "Templated fabrication of large area subwavelength antireflection gratings on silicon," *Appl. Phys. Lett.*, 2007. DOI: 10.1063/1.2821833.

[104] K. J. Weber and a. W. Blakers, "A novel silicon texturization method based on etching through a silicon nitride mask," *Prog. Photovolt: Res. Appl.*, 2005. DOI: 10.1002/pip.632.

[105] N. Chaturvedi, E. Hsiao, D. Velegol, and S. H. Kim, "Maskless fabrication of nanowells using chemically reactive colloids," *Nano Lett.*, 2011. DOI: 10.1021/nl1037984.

[106] J. Kim, D. Inns, K. Fogel, and D. K. Sadana, "Surface texturing of single-crystalline silicon solar cells using low density SiO_2 films as an anisotropic etch mask," *Sol. Energy Mater. Sol. Cells*, 2010. DOI: 10.1016/j.solmat.2010.06.026.

[107] J. Liu, X. Zhang, G. Sun, B. Wang, T. Zhang, F. Yi, and P. Liu, "Fabrication of inverted pyramid structure by Cesium Chloride self-assembly lithography for silicon solar cell," *Mater. Sci. Semicond. Process.,* 2015. DOI: 10.1016/j.mssp.2015.05.048.

[108] Y. Wang, L. Yang, Y. Liu, Z. Mei, W. Chen, J. Li, H. Liang, A. Kuznetsov, and D. Xiaolong, "Maskless inverted pyramid texturization of silicon," *Sci. Rep.*, 2015. DOI: 10.1038/srep10843.

[109] F. Giorgis, F. Giulani, C.F. Pirri, E. Tresso, C. Summonte, R. Rizzolli, R. Galloni, A. Desalvo, and E. Rava, "Optical, structural and electrical properties of device-quality hydrogenated amorphous silicon-nitrogen films deposited by plasma-enhanced chemical vapour deposition", *Philosophical Magazine B*, 1998. DOI: 10.1080/13642819808206395.

[110] M. Lattemann, E. Nold, S. Ulrich, H. Leiste, and H. Holleck, "Investigation and characterisation of silicon nitride and silicon carbide thin films," *Surf. Coatings Technol.*, 2003. DOI: 10.1016/S0257-8972(03)00695-9.

[111] D. Hiller, R. Zierold, J. Bachmann, M. Alexe, Y. Yang, J. W. Gerlach, A. Stesmans, M. Jivanescu, U. Muller, J. Vogt, H. Hilmer, P. Loper, M. Kunle, F. Munnik, K. Nielsch, and M. Zacharias, "Low temperature silicon dioxide by thermal atomic layer deposition: Investigation of material properties," *J. Appl. Phys.*, 2010. DOI: 10.1063/1.3327430.

[112] E. Bustarret, M. Bensouda, M. C. Habrard, J. C. Bruyere, S. Poulin, and S. C. Gujrathi, "Configurational statistics in a-SixNyHz alloys: A quantitative bonding analysis," *Phys. Rev. B*, 1988. DOI: 10.1103/PhysRevB.38.8171.

[113] D. K. Schroder, "Semiconductor Material and Device Characterization", 3^{rd} edition, *John Wiley & Sons*, 2006. ISBN: 978-0-471-73906-7.

[114] S. Q. Xiao, S. Xu, and K. Ostrikov, "Low-temperature plasma processing for Si photovoltaics," *Mater. Sci. Eng. R Reports*, 2014. DOI: 10.1016/j.mser.2014.01.002.

[115] J. W. Coburn and M. Chen, "Optical emission spectroscopy of reactive plasmas: A method for correlating emission intensities to reactive particle density," *J. Appl. Phys.*, 1980. DOI: 10.1063/1.328060.

[116] Helmut Mackel and Kenneth Varner, "On the determination of the emitter saturation current density from lifetime measurements of silicon devices," *Prog. Photovolt: Res. Appl.*, 2013. DOI: 10.1002/pip.2167.

[117] E. H. Nicollian and J. R. Brews, "MOS (Metal Oxide Semiconductor)Physics and Technology", *Wiley*, 2002. ISBN: 978-0-471-43079-7.

[118] W. A. Hill and C.C. Coleman, "A single-frequency approximation for interface-state density determination," *Solid-State Electronics*, 1980. DOI: 10.1016/0038-1101(80)90064-7.

[119] Photovoltaic devices - part 3: Measurement principles for terrestrial photovoltaic solar devices with reference spectral irradiance data, IEC Std. 60904-3, Geneva, Switzerland, 2015. Weblink

[120] S. Bowden, A. Rohatgi, "Rapid and Accurate Determination of Series Resistance and Fill Factor Losses in Industrial Silicon Solar Cells", *proc. of the 17th European Photovoltaic Solar Energy Conference*, 2001. DOI: not available. Weblink.

[121] "Measuring Photovoltaic Cell I - V Characteristics with the Model 2420 SourceMeter Instrument", Application notes, Keithley Instruments. Weblink

[122] A. Rohatgi, P. Doshi, J. Moschner, T. Lauinger, A. G. Aberle, and D. S. Ruby, "Comprehensive Study of Rapid , Low-Cost Silicon Surface Passivation Technologies," *IEEE Trans. Electron. Dev.*, 2000. DOI: 10.1109/16.841230.

[123] Sandeep, S.S., K. Warikoo, A. Kottantharayil, "Optimization of ICP - CVD silicon nitride for Si solar cell passivation," *proc. of 38th IEEE Photovoltaic Specialists Conference* 2012. DOI: 10.1109/PVSC.2012.6317795.

[124] C. K. Wong, H. Wong, V. Filip, and P. S. Chung, "Bonding Structure of Silicon Oxynitride Grown by Plasma-Enhanced Chemical Vapor Deposition," *Jpn J. Appl. Phys.*, 2007. DOI: 10.1143/JJAP.46.3202.

[125] S. Hajati, S. Tougaard, J. Walton, N. Fairley, "Noise reduction procedures applied to XPS imaging of depth distribution of atoms on the nanoscale," *Surface Science*, 2008. DOI: 10.1016/j.susc.2008.08.005.

[126] S. Bordihn, P. Engelhart, V. Mertens, and G. Kesser, "High surface passivation quality and thermal stability of ALD Al_2O_3 on wet chemical grown ultra-thin SiO_2 on silicon," *Energy Procedia*, 2011. DOI: 10.1016/j.egypro.2011.06.197.

[127] H. Chen, D. Landheer, T. Chao, J. E. Hulse, T. Huang, "X-Ray Photoelectron Spectroscopy of Gate-Quality Silicon Oxynitride Films Produced by Annealing Plasma-Nitrided Si (100) in Nitrous Oxide," *J. Electrochem. Soc.*, 2001. DOI: 10.1149/1.1374219.

[128] U. Cvelbar, N. Krstulovic, S. Milosevic, and M. Mozetic, "Inductively coupled RF oxygen plasma characterization by optical emission spectroscopy," *Vacuum*, 2007. DOI: 10.1016/j.vacuum.2007.07.016.

[129] G. Recio-Sanchez, K. Namura, M. Suzuki, and R. J. Martin-Palma, "Nanostructured copper/porous silicon hybrid systems as efficient sound-emitting devices," *Nanoscale Res. Lett.*, 2014. DOI: 10.1186/1556-276X-9-487.

[130] H. Jin, K. J. Weber, and P. J. Smith, "Characterization of the Si - SiO_2 Interface Following Room Temperature Ammonia Plasma Exposure," *J. Electrochem. Soc.*, 2007. DOI: 10.1149/1.2716554.

[131] H. Arai, K. Tanaka, S. Kohda, and H. Arai, "Effect of ammonia plasma treatment on plasma deposited silicon nitride films/silicon interface characteristics," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, 1988. DOI: 10.1116/1.584349.

[132] E. Cartier, D. A. Buchanan, and G. J. Dunn, "Atomic hydrogen-induced interface degradation of reoxidized-nitrided silicon dioxide on silicon," *Appl. Phys. Lett.*, 1994. DOI: 10.1063/1.110990.

[133] Y. Yamashita, N. Ikeno, T. Tachibana, Y. Ohshita, and A. Ogura, "X-ray evaluation of electronic and chemical properties and film structures in SiN passivation layer on crystalline Si solar cells," *Jpn. J. Appl. Phys.*, 2015. DOI: 10.7567/JJAP.54.08KD14.

[134] A. Moldovan, F. Feldmann, M. Zimmer, J. Rentsch, J. Benick, and M. Hermle, "Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO2 layers," *Sol. Energy Mater. Sol. Cells*, 2015. DOI: 10.1016/j.solmat.2015.06.048.

[135] B. Hoex, M. C. M. van de Sanden, J. Schmidt, R. Brendel, and W. M. M. Kessels, "Surface passivation of phosphorus - diffused n+ - type emitters by plasma-assisted atomic-layer deposited Al_2O_3," *Phys. status solidi - Rapid Res. Lett.*, 2012. DOI: 10.1002/pssr.201105445.

[136] L. Chen, X. Yu, P. Chen, P. Wang, X. Gu, J. Lu, and D. Yang, "Effect of oxygen precipitation on the performance of Czochralski silicon solar cells," *Sol. Energy Mater. Sol. Cells*, 2011. DOI: 10.1016/j.solmat.2011.06.044.

[137] N. Khelifati, D. Bouhafs, S.E.H. Abaidia, A. E.G. Boucheham, and B. Palahouane, "Impact of Phosphorus Diffusion Gettering on HEM Multicrystalline Silicon Wafers Taken from Different Ingot Regions," *proc. of the International Congress on Energy Efficiency and Energy Related Materials (ENEFM2013)*, pp. 295 - 300, 2013. DOI: 10.1007/978-3-319-05521-3_38.

[138] A. G. Aberle, W. Zhang, and B. Hoex, "Advanced loss analysis method for silicon wafer solar cells," *Energy Procedia*, 2011. DOI: 10.1016/j.egypro.2011.06.131.

[139] Karthick Murukesan, "Doping module optimization and process integration for the fabrication of c-Si solar cells," Masters thesis, Dept. Elec. Eng., IIT Bombay, Mumbai, India, 2014.

[140] O. Breitenstein, J. P. Rakotoniaina, M. H. Al Rifai, and M. Werner, "Shunt types in crystalline silicon solar cells," *Prog. Photovoltaics Res. Appl.*, 2004. DOI: 10.1002/pip.544.

[141] O. Breitenstein, J. Bauer, a. Lotnyk, and J.-M. Wagner, "Defect induced non-ideal dark - characteristics of solar cells," *Superlattices Microstruct.*, 2009. DOI: 10.1016/j.spmi.2008.10.025.

[142] S. Cho, K. Hong, J. Huh, H. Jung, and J. Jeong, "Role of the ambient oxygen on the silver thick-film contact formation for crystalline silicon solar cells," *Curr. Appl. Phys.*, 2010. DOI: 10.1016/j.cap.2009.11.054.

[143] D. Pysch, A. Mette, A. Filipovic, and S. W. Glunz, "Comprehensive analysis of advanced solar cell contacts consisting of printed fine-line seed layers thickened by silver plating," *Prog. Photovoltaics Res. Appl.*, 2009. DOI: 10.1002/pip.855.

[144] Y. H. Su, W. Y. Ma, T. N. Yang, C. Y. Hou, and C.D. Lee, "The brand-new metallization patterning processes for plated solar cells," *Int. J. Energy Res.*, 2015. DOI: 10.1002/er.3353.

[145] E. Lee, H. Lee, J. Choi, D. Oh, J. Shim, K. Cho, J. Kim, S. Lee, B. Hallam, S. R. Wenham, and H. Lee, "Improved LDSE processing for the avoidance of overplating yielding 19.2% efficiency on commercial grade crystalline Si solar cell," *Sol. Energy Mater. Sol. Cells*, 2011. DOI: 10.1016/j.solmat.2011.07.030.

[146] C. Zhou, T. Li, Y. Song, S. Zhou, W. Wang, L. Zhao, H. Li, Y. Tang, H. Diao, Z. Gao, Y. Duan, and Y. Li, "SiO_x(C)/SiN_x dual-layer anti-reflectance film coating for improved cell efficiency," *J. Sol. Energy*, 2011. DOI: 10.1016/j.solener.2011.09.007.

[147] Y. L. Tu, S.P. Cheng, K.J. Tsai, L.G.Yao, "Plasma treatment method for PECVD silicon nitride films for improved passivation layers on semiconductor metal interconnections," US patent 5,962,344, Oct, 5, 1999. Weblink.

[148] S. Majee, M. F. Cerqueira, D. Tondelier, B. Geffroy, Y. Bonnassieux, P. Alpuim, and J. E. Bouree, "The effect of argon plasma treatment on the permeation barrier properties of silicon nitride layers," *Surf. Coatings Technol.*, 2013. DOI: 10.1016/j.surfcoat.2013.07.067.

[149] R. Vernhes, A. Amassian, J. E. Klemberg-Sapieha, and L. Martinu, "Plasma treatment of porous SiN_x: H films for the fabrication of porous-dense multilayer optical filters with tailored interfaces," *J. Appl. Phys.*, 2006. DOI: 10.1063/1.2202692.

[150] M. S. Rogers, "Plasma treatment of silicon nitride and silicon oxynitride," US patent, US2012/0190185 A1, Jan 26, 2012. Weblink

[151] Y. Wan, K. R. McIntosh, and A. F. Thomson, "Characterisation and optimisation of PECVD SiN_x as an antireflection coating and passivation layer for silicon solar cells," *AIP Adv.*, 2013. DOI: 10.1063/1.4795108.

[152] L. Cai and A. Rohatgi, "Effect of post-PECVD photo-assisted anneal on multicrystalline silicon solar cells," *IEEE Trans. Electron Devices*, 1997. DOI: 10.1109/16.554799.

[153] Mehul C. Raval, Sandeep S. Saseendran, Som Mondal, Balraj Arunachalam, Sandeep Kumbhar, Aldrin Antony, Chetan S. Solanki, Anil Kottantharayil, "Low temperature fabrication process for silicon solar cells based on front- side Ni-Cu metallization and rear-side silicon-nitride based passivation," submitted to *18^{th} International workshop on physics of semiconductor devices (IWPSD)*, 2015.

[154] E. Fourmond, J. Dupuis, F. Marcq, C. Dubois, M. Lemiti, "Impact of ammonia pretreatment of the silicon surface prior to deposition of silicon nitride layer by PECVD," *23^{rd} European Photovoltaic Specialist Conference*, 2008. DOI: 10.4229/23rdEUPVSEC2008-2CV.5.13.

[155] Dekkers, H. F W, Duerinckx, F., De Wolf, S., Agostinelli, G., Szlufcik, J., "The influence of surface preparation on rear surface passivation of mc - Si by thermally treated direct PECVD silicon nitride," *proc. of the 3^{rd} World Conference on Photovoltaic Energy Conversion*, 2003. DOI: not available. Weblink.

[156] Sandeep S. S., A. Kottantharayil, "Method of fabricating inverted pyramid on crystalline silicon using lithography free fabrication technique (2013)," *Indian patent*, application no. 132/MUM/2013.

[157] Sandeep, S.S., A. Kottantharayil, "Photolithography Free Inverted Pyramidal Texturing for Solar Cell Applications," *proc. of the 40^{th} IEEE Photovoltaic Specialists Conference (PVSC)*, 2014. DOI: 10.1109/PVSC.2014.6925140.

[158] Lenoble, D., Anil, K.G., De Keersgieter, A., Eybens, P., Collaert, N., Rooyackers, R., Brus, S., Zimmerman, P., Goodwin, M., Vanhaeren, D., Vandervorst, W., Radovanov, S., Godet, L., Cardinaud, C., Biesemans, S., Skotnicki, T., Jurczak, M., "Enhanced performance of PMOS MUGFET via integration of conformal plasma-doped source/drain extensions," *Digest of Technical Papers - Symposium on VLSI Technology*, 2006. DOI: 10.1109/VLSIT.2006.1705270.

[159] J. Hong, W. M. M. Kessels, W. J. Soppe, A. W. Weeber, W. M. Arnoldbik, and M. C. M. van de Sanden, "Influence of the high-temperature 'firing' step on high-rate plasma

deposited silicon nitride films used as bulk passivating antireflection coatings on silicon solar cells," *J. Vac. Sci. Technol. B*, 2003. DOI: 10.1116/1.1609481.

[160] L.J. Huang, Q.Y. Tong, Y.L. Chao, T.H. Lee, T. Martini, and U. Gosele, "Onset of blistering in hydrogen-implanted silicon," *Appl. Phys. Lett.*, 1999. DOI: 10.1063/1.123430.

[161] P. K. Chu and X. Zeng, "Hydrogen-induced surface blistering of sample chuck materials in hydrogen plasma immersion ion implantation," *J. Vac. Sci. Technol. A Vacuum, Surfaces, and Films*, 2001. DOI: 10.1116/1.1384557.

[162] A. Hauser, M. Spiegel, P. Fath, and E. Bucher, "Influence of an ammonia activation prior to the PECVD SiN deposition on the solar cell performance," *Sol. Energy Mater. Sol. Cells*, 2003. DOI: 10.1016/S0927-0248(02)00180-0.

[163] W. A. Lanford and M. J. Rand, "The hydrogen content of plasma-deposited silicon nitride," *J. Appl. Phys.*, 1978. DOI: 10.1063/1.325095.

[164] C. M. Varma, "Hydrogen-implant induced exfoliation of silicon and other crystals," *Appl. Phys. Lett.*, 1997. DOI: 10.1063/1.120378.

[165] S. Gatz, T. Dullweber, V. Mertens, F. Einsele, and R. Brendel, "Firing stability of SiN_y/SiN_x stacks for the surface passivation of crystalline silicon solar cells," *Sol. Energy Mater. Sol. Cells*, 2012. DOI: 10.1016/j.solmat.2011.09.051.

[166] X. Duo, W. Liu, M. Zhang, L. Wang, C. Lin, M. Okuyama, M. Noda, W. Y. Cheung, S. P. Wong, P. K. Chu, P. Hu, S. X. Wang, and L. M. Wang, "Evolution of hydrogen and helium co-implanted single-crystal silicon during annealing," *J. Appl. Phys.*, 2001. DOI: 10.1063/1.1389478.

[167] A. Agarwal, T. E. Haynes, V. C. Venezia, O. W. Holland, and D. J. Eaglesham, "Efficient production of silicon-on-insulator films by co-implantation of He^+ with H^+," *Appl. Phys. Lett.*, 1998. DOI: 10.1063/1.120945.

[168] K. Wittmaack and W. Wach, "Blistering effects in argon-bombarded silicon," *Appl. Phys. Lett.*, 1978. DOI: 10.1063/1.90118.

[169] A. Merlos, M. Acero, M. H. Bao, J. Bausells, and J. Esteve, "TMAH/IPA anisotropic etching characteristics," *Sensors Actuators A*, 1993. DOI: 10.1016/0924-4247(93)80125-Z.

Publications, Patents and Awards

Publications

Journal publications

1. **Sandeep S. Saseendran**, Mehul C. Raval, Anil Kottantharayil, "Impact of post-deposition plasma treatment on surface passivation quality of silicon nitride films," IEEE Journal of Photovoltaics, 2016. DOI: 10.1109/JPHOTOV.2015.2493369.

2. **Sandeep S. Saseendran**, Anil Kottantharayil, "Inverted pyramidal texturing through blisters in silicon nitride," IEEE Journal of Photovoltaics, 2015. DOI: 10.1109/JPHOTOV.2015.2412463.

3. **Sandeep S. Saseendran**, Anil Kottantharayil, "Plasma grown oxy-nitride films for silicon surface passivation," IEEE Electron Device Letters, 2013. DOI: 10.1109/LED.2013.2263331.

4. Mehul C. Raval, **Sandeep S. Saseendran**, Stephan Suckow, S. Saravanan, Chetan S. Solanki, Anil Kottantharayil, "N_2O plasma treatment for minimization of background plating in silicon solar cells with Ni-Cu front side metallization," Solar Energy Materials and Solar Cells, 2016. DOI:10.1016/j.solmat.2015.10.002.

5. Mehul C. Raval, Amruta Joshi, **Sandeep S. Saseendran**, Stephan Suckow, S. Saravanan, Chetan S. Solanki, Anil Kottantharayil, "Study of nickel silicide formation and associated fill-factor loss analysis for silicon solar cells with plated Ni-Cu based metallization," IEEE Journal of Photovoltaics, 2015. DOI:10.1109/JPHOTOV.2015.2463741.

Manuscripts under review

1. **Sandeep S. Saseendran**, Mehul C. Raval, S. Saravanan, Anil Kottantharayil, "Impact of interstitial oxygen trapped in silicon during plasma growth of silicon oxy-nitride films on silicon solar cell passivation," under review, Journal of applied physics.

Conference publications

1. **Sandeep S. Saseendran**, Tarun S. Yadav, Mehul C. Raval, Balraj Arunachalam, Sandeep Kumbhar, Anzar Gani, S. Saravanan, and Anil Kottantharayil, "Low temperature oxidation of silicon for emitter surface passivation," presented at the *18th International Workshop on Physics of Semiconductor Devices (IWPSD)*, Bangalore, India, Dec. 2015.

2. **Sandeep, S.S.**, Kottantharayil, A., "Photolithography free inverted pyramidal texturing for solar cell applications," *proceedings of the 40th IEEE Photovoltaic Specialists Conference (PVSC)*, Denver, USA, 2014. DOI: 10.1109/PVSC.2014.6925140.

3. **Sandeep S. S.**, Anil Kottantharayil, "Potential of plasma grown oxide films for surface passivation of silicon solar cells," *proceedings of the 28th European PV Solar Energy Conference,* Paris, France, 2013. DOI:10.4229/28thEUPVSEC2013-2DV.3.23.

4. **Sandeep S. S.**, Ketan Warikoo, Anil Kottantharayil "Optimization of ICP-CVD silicon nitride for Si solar cell passivation," *proceedings of the 38th IEEE Photovoltaic Specialists Conference,* Austin, USA, 2012. DOI:10.1109/PVSC.2012.6317795.

5. A. K. Sharma, **Sandeep S. Saseendran**, K. L. Narasimhan, B. M. Arora, and Anil Kottantharayil, "Investigation of carrier lifetime improvements with SiO_2/SiN_x stacking layer during c-Si solar cell fabrication," presented at the *18th International Workshop on Physics of Semiconductor Devices (IWPSD)*, Bangalore, India, Dec. 2015.

6. Mehul C. Raval **Sandeep S. Saseendran**, Som Mondal, Balraj Arunachalam, Sandeep Kumbhar, Aldrin Antony, Chetan S. Solanki and Anil Kottantharayil, "Low temperature fabrication process for silicon solar cells based on front- side Ni-Cu metallization and rear-side silicon-nitride based passivation," presented at the *18th International Workshop on Physics of Semiconductor Devices (IWPSD)*, Bangalore, India, Dec. 2015.

7. S. Saravanan, A. Balraj, Sandeep. K, Mehul C. Raval, **Sandeep S. S.**, Anzar. G, H. K. Singh, A. K. Sharma, K. L. Narasimhan, B M Arora, C.S. Solanki, and A. Kottantharayil,"Development of Baseline Fabrication Process for Large Area Silicon Solar Cells and Associated Novel Structures," presented at the *18^{th} International Workshop on Physics of Semiconductor Devices (IWPSD)*, Bangalore, India, Dec. 2015.

8. Meenakshi Bhaisare, **Sandeep S. Saseendran**, Anil Kottantharayil, "Thermal stability of single layer pulsed - DC reactive sputtered AlO_x film and stack of ICP - CVD SiN_x on AlO_x for p - type c - Si surface passivation," *proceedings of the International Conference on Emerging Electronics*, Bangalore, India, 2014. DOI: 10.1109/ICEmElec.2014.7151212.

9. Som Mondal, Hemant K. Singh, Vishnu K. Bajpai, Mehul Raval, Bandana Singha, **Sandeep S. S.**, Meenakshi Bhaisare, Anil. K, Chetan S. Solanki, "Advances in c-Si Cell Processes Suitable for Near Future Commercialization," *proceedings of the International Conference on Energy Efficient LED Lighting and Solar Photovoltaic Systems*, Kanpur, India, 2014.

10. Anil Kottantharayil, Meenakshi Bhaisare and **Sandeep S. S.**, "Advanced thin films for surface passivation of crystalline silicon solar cells," *proceedings of the International Workshop on Physics of Semiconductor Devices (IWPSD)*, Gurgaon, India, 2013. (invited)

Patents

1. Post-treatment of silicon nitride used in a solar cell (2015), Sandeep S. S., Mehul Raval, Anil Kottantharayil, Indian patent filed, Application number 636/MUM/2015.

2. Method of fabricating inverted pyramid on crystalline silicon using lithography free fabrication technique (2013), Sandeep S. S., Anil Kottantharayil, Indian patent filed, Application number 132/MUM/2013.

3. A Method for Etching Silicon Substrates (2012), Sandeep S. S., Anil Kottantharayil, Indian patent filed, Application number 2063/MUM/2012

Awards

1. Certificate of appreciation for capturing 'Best Image' in JEOL FEG - TEM for the year 2014, SAIF, IIT Bombay.