Investigation of Advanced MOS device Technology

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Technology

by

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This thesis is dedicated to my parents and brother for their love and endless support.

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Special thanks to Naveen Kumar N.V. for supporting me morally, guiding and driving me during the three years of my M.Tech through all the encouraging and thought provoking discussions both on career and personal front.

Declaration of Academic Ethics

I declare that this written submission represents my ideas in my own words and where others ideas or words have been included, I have adequately cited and referenced the original sources. I declare that I have properly and accurately acknowledged all sources used in the production of this thesis.

I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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Abstract

Lithography process is one of the critical process in MOSFET fabrication process flow. Optical lithography has been the preferred process for patterning due to it's high throughput but the minimum feature size attainable is limited by the wavelength of optical source. Electron Beam lithography(EBL) is an alternative for patterning high resolution features but takes long durations for writing. Mix and Match lithography process is developed which takes advantage of both optical throughput and electron beam lithography resolution. This process is implimented for patterning of gate for short-channel MOSFET fabrication. Process plan for fabricating RF oscillator circuit using Mix and Match lithography is made with process results reported till gate level lithography.

Focused electron beam induced deposition(FEBID) is the process of depositing materials at nano-meter scale by using electron beam and a gas precursor flow. Initial experiments are done to study the composition of Pt deposited using $Me_3PtCpMe$ precursor and fabrication of Pt nano-deposition for electrical and compositional characterisation.

Chapter 1

Lithography

1.1 What is Lithography

Lithography is the process of printing patterns of features ranging from micron to sub-micron on a resist (typically comprised of organic polymers) coated on the wafer. These patterns are transferred later onto the wafer either by etching or lift-off.

General Process steps for Lithography

1. Substrate cleaning
2. Resist coat
3. Pre-exposure bake
4. Exposure
5. Post-exposure bake
6. Development of resist
7. Post-development bake

1.2 Types of Lithography

Different types of lithography methods for transferring patterns onto a wafer are Optical lithography, X-ray lithography, electron beam lithography, projection e-beam lithography and Extreme ultraviolet lithography. Optical lithography is the primary method for all ICs manufacturing. As technology scales, to attain the minimum feature sizes other technologies are also being explored.

In this report, we will mainly be focusing on optical and electron beam lithography.

1.3 Optical lithography

1.3.1 What is Optical lithography

In optical lithography, a light sensitive photoresist is spun on the wafer which is selectively exposed using optical source passed through a mask containing the desired patterns.

Basic setup of optical lithography is shown in fig:1.1.

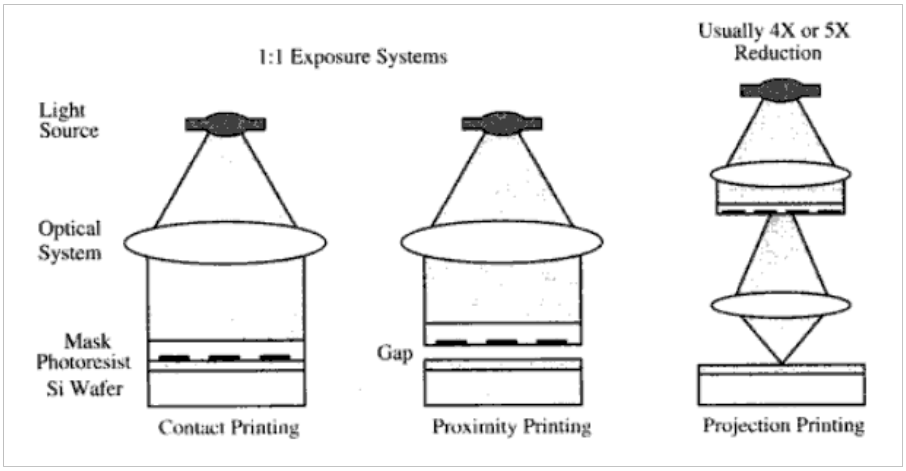


Figure 1.1: Different types of optical lithography printing[1]

These different printing methods differ in the manner of forming aerial image on the photoresist surface.

1.3.2 Contact Printing Lithography

In contact printing lithography the mask is in direct contact with the resist surface thus leading to less diffraction effects as shown in fig:1.2 and are therefore capable of high resolution lithography(limited by the wavelength range of the UV light source).

Typical light sources contain Hg vapor inside a sealed glass envelope. Gas inside the glass is ionised by applying a high enough voltage. The free electrons in the plasma collides with Hg atoms resulting in energy transition of electrons in the Hg atoms. These electrons radiate photons at a number of UV wavelengths during their transition from higher to lower energy states. The resolution of the lithography system depends on the wavelength of these photons.

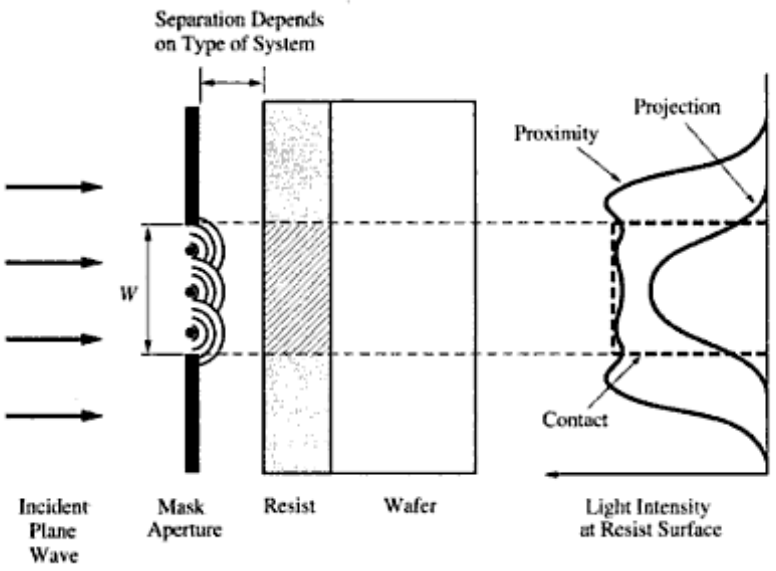


Figure 1.2: Aerial image formed by different types of optical lithography printing tools[2]

Contact printing tool used for our process has 500W Hg lamp with a wavelength range of 350-450 nm.

The UV light from the light source passes through the mask plate which is in contact with the resist layer on the wafer. The chrome side of the mask plate is placed in contact with the resist to minimize diffraction effects.

The mask plate contains patterns of bright(transparent) and dark region as shown in fig:1.3. The light passes through the bright regions and forms an aerial image on the resist surface changing the properties of the resist in the exposed regions. Contact printers use multiple wavelength range to minimize the ringing effects but diffraction effects remain.

After exposure, depending on the type of resist it is followed by a Post-exposure/Post-development bake and resist development. During development, for positive resists the exposed regions dissolves in the developer solution and leaves behind the required mask patterns, it's the reverse for negative resists, the exposed regions getting retained on the wafer.

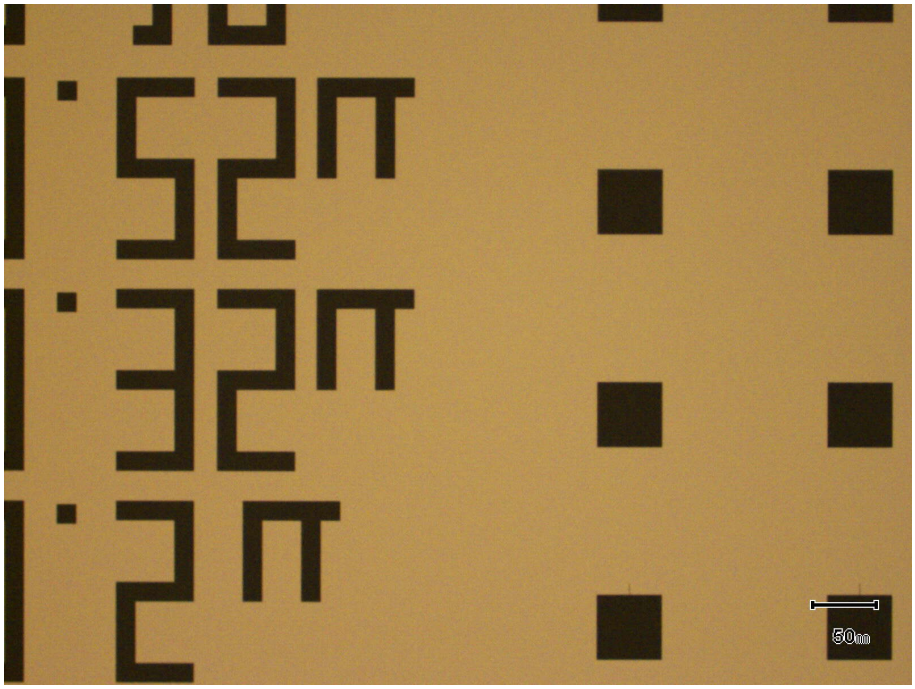


Figure 1.3: Olympus image of the mask plate used for our process

1.4 Electron Beam Lithography

1.4.1 What is Electron Beam Lithography

Electron Beam Lithography is a maskless lithography process in which patterns are directly written by exposing the resist with an electron beam and using a deflection mechanism to focus the beam at different regions on the wafer.

Electron beam lithography has the advantage of going beyond the resolution limit of optical lithography which is limited by the radiation source. The wavelength of electron beam is given by

$$\lambda = \frac{h}{p} = \frac{h}{m_0 v} = \frac{h}{\sqrt{2 m_0 e U}} \tag{1.1}$$

where,

λ = wavelength of the electron, h = Planck's constant, p = momentum of the electron, m_o = mass of the electron, v = electron velocity, e = electron charge, U = electric potential

Depending on the accelerating voltage of the beam, wavelength of the electron beam can be changed. At $10kV$, the electron beam has a wavelength of $12.3pm$. This makes it possible to pattern features well smaller than those possible with optical. However, electron beam

lithography writes patterns pixel by pixel thus taking a very long time for exposure.

1.4.2 Process of Electron Beam Lithography

The electron beam lithography setup consists of an electron gun, electromagnetic lenses for focusing the beam and controlling it's diameter, beam deflector for focusing the beam at different points on the wafer and a detector mechanism which gives an image from the reflected electrons.

The tool used for our process is RAITH 150two EBL. Typical modern EBL tool columg is shown in fig:1.4.

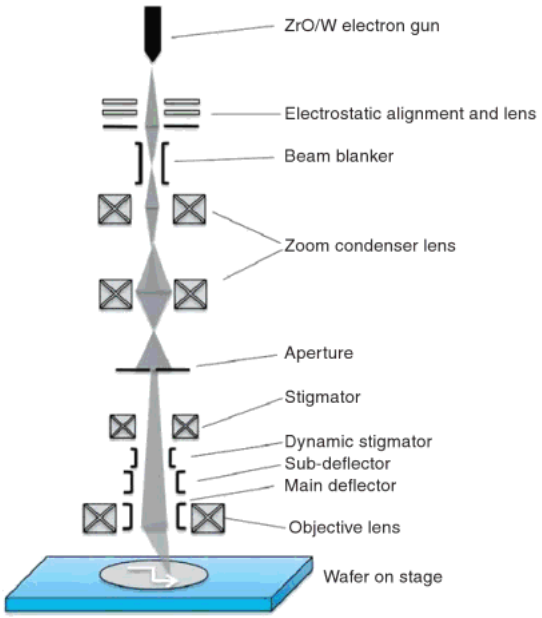


Figure 1.4: Modern Electron Lithography Tool column[3]

The electron source consists of a sharp pointed tungsten filament coated with Zirconium oxide which helps in reducing the work function barrier of tungsten. A strong electric field is applied at high temperature resulting in emission of electrons from the tungsten tip. The tip radius is $0.5\mu m$. To minimize current fluctuations, the electron gun is operated in a high vacuum environment of the order of $1E^{-9}$ torr.

Electrostatic and magnetic lenses are used to focus the electron beam. They have a relatively poorer quality compared to optical lens in terms of abberations. Electrostatic lenses are used in the gun regions as condensor lens and magnetic lens are used as objective

lens at the bottom of the column.

Stigmator lens are used to correct for the asymmetry(non-rounded feature) in the electron beam. This asymmetry could arise due to non-symmetric strength of the electron lenses or aperture charging.

Apertures are used at different levels in the column. A blanking aperture is used to turn the beam on and off. Beam limiting apertures of size ranging from standard $30\mu m$ to $7.5\mu m$ are used. Smaller apertures give better resolution but limits the beam current from the gun.

1.4.3 Electron-Solid Interaction

The resolution attainable with EBL doesn't just depend on the probe diameter attainable by varying magnification(strength of electron lenses) and apertures. This is because when the electron beam hits the surface of the resist many scattering events take place.

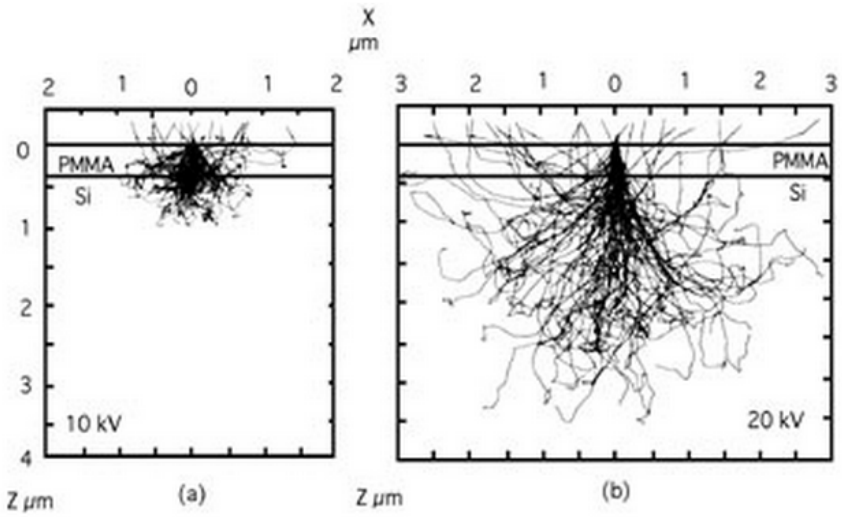


Figure 1.5: Monte carlo simulation of electron scattering at a) $10KV$ and b) $20KV$ accelerating voltage[4]

Forward scattering

As the electrons from the beam penetrate through the resist small angle scattering occurs. This leads to an increased beam diameter at the bottom of the resist than top. This scattering mechanism is the reason for angled side-wall profile of resist. The forward scattering can be minimized by using a thinner resist and higher accelerating voltage.

Back Scattered Electrons(BSE) scattering

As electrons penetrate further into the substrate they interact with the atoms and get scattered back into the resist retaining most of their energy. The width of BSE scattering distrubution is far greater than the forward scattering width. These back scattered electrons cause proximity effects i.e., dense features get higher dose due to BSE electrons from nearby patterns. BSE are used by the detector for forming the scanning electron microscope image.

Secondary electrons

The primary electrons from the electron beam collide with the atoms as they penetrate through the resist. These collisions lead to expulsion of electrons from these atoms. They are called secondary electrons having energy less than $50eV$ and are responsible for majority of resist exposure process.

1.5 Summary

The process and different types of lithography was explained. In chapter 2, the process developed for Mix and Match lithography using Su8 2000.5 resist is explained. Chapter 3 and 4 show the implimentation of Mix and Match lithography for fabrication of short-channel devices and RF oscillator circuit respectively. Chapter 5 focuses on the technology of Focused Electron Beam Induced Deposition(FEBID) which uses electron beam in the presence of precursor gas flow for selective nano-scale deposition.

Chapter 2

Mix and Match Lithography

Optical lithography and electron beam lithography have their own advantages and disadvantages. Optical lithography has high throughput but is limited in resolution attainable whereas in EBL very high resolution can be attained but the process takes a very long time.

Mix and Match lithography aims at taking advantage of both optical and EBL for resist patterning. The bigger features in the pattern are printed using optical lithography and high resolution features are patterned using EBL. Thus, this process helps in printing patterns having high resolution features at a reasonable process duration.

2.1 Process of Mix and Match Lithography

The following flow shows the generic process of Mix and Match Lithography.

1. Si wafer RCA cleaning
2. Resist coat
3. Pre-exposure bake
4. Optical exposure for bigger patterns
5. Electron beam exposure for smaller features
6. Post-exposure bake
7. Development of resist
8. Post-development bake

2.2 Mix and Match Lithography process developed for Sub-100nm MOSFET fabrication

2.2.1 Resist used

Su8 2000.5 resist is used. It's a epoxy based negative photo-resist (NPR) from Micro-chem Co[5].Negative resist become polymerised and difficult to dissolve in developer after exposure, thus the region exposed is retained and the un-exposed region is dissolved during development. Su8 resist has the advantage of being sensitive to both optical and electron beam.It also has high sensitivity to electron beam,thus requiring very less dose and hence time for electron beam exposure.

For patterning high resolution sub-100nm features using Su8 resist we require very high accelerating voltage of 100kV [6].The process developed in this report is at accelerating voltage of 20kV and high resolution features of 100nm are obtained but without concern about the critical dose required. The resist was also not thinned for the process reported.Thus,after development the total thickness of resist is not retained.

2.2.2 Design of Gate Mask

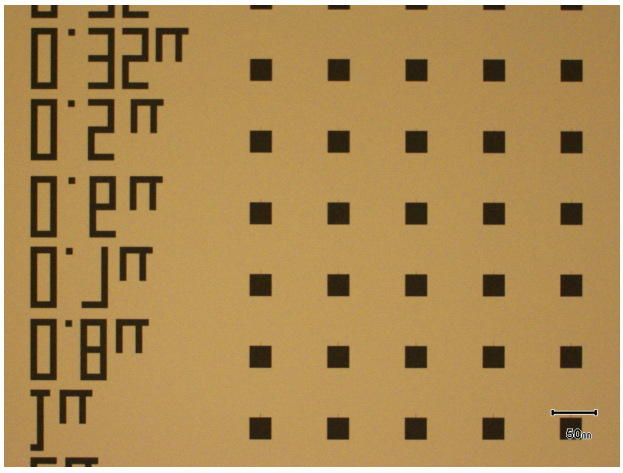


Figure 2.1: Gate Area Dark Field Olympus microscope image

As the resist used is negative resist, the mask plate used for gate patterning is dark field i.e., the field region is opaque and the light passes through the gate region.The mask plate design

is shown in fig 2.2 and mask in fig 2.1.

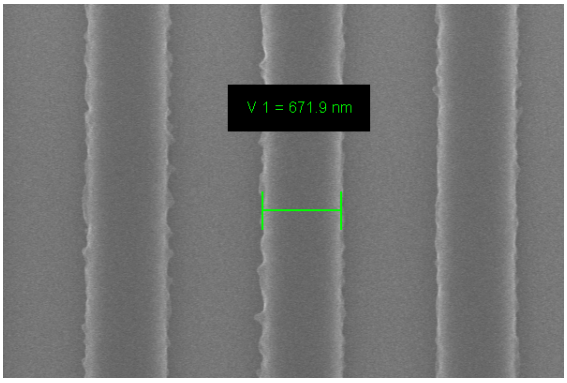
Figure 2.2: Gate mask design

2.2.3 Optical lithography Dose Experiment

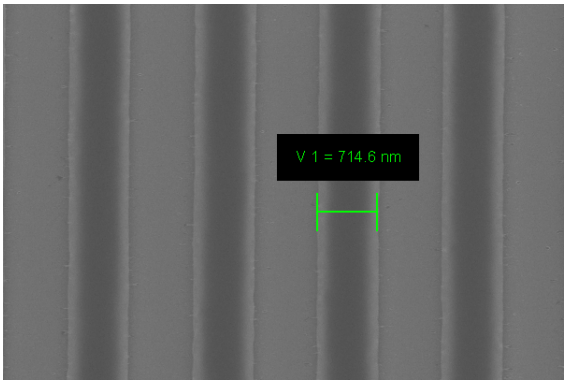
Dose variation experiment for optical exposure of Su8 2000.5 was done. Taking Micro-chem dose range of $60 - 80 mJ/cm^2$[5] as reference dose was varied from 60 to $100 mJ/cm^2$.

Resist	Spin schedule	Pre-bake/PEB	Exposure
Su8 2000.5	5 sec – 500 rpm 45 sec – 6000 rpm 5 sec – 0 rpm	65°C – 1 min 95°C – 1 min Wafer should be on the hot-plate during ramp up/down	70 – 100 mJ/cm^2
Development- Su8 developer 1min followed by IPA rinse			

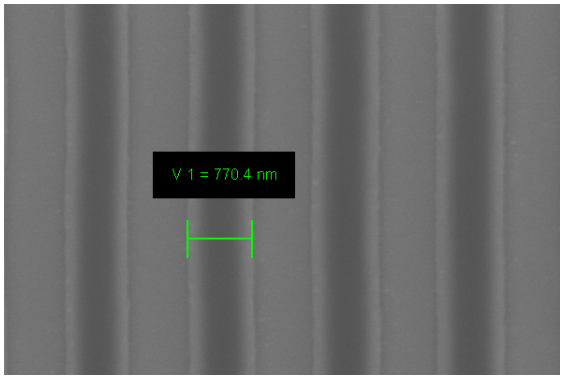
Table 2.1: Optical lithography dose variation Experiment



(a) Dose $80mJ/cm^2$



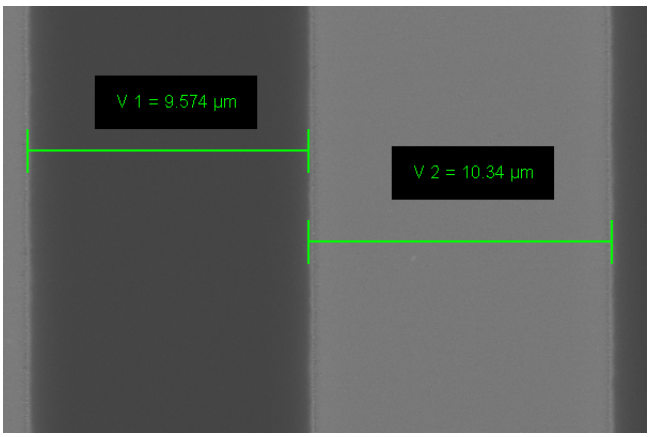
(b) Dose $90mJ/cm^2$



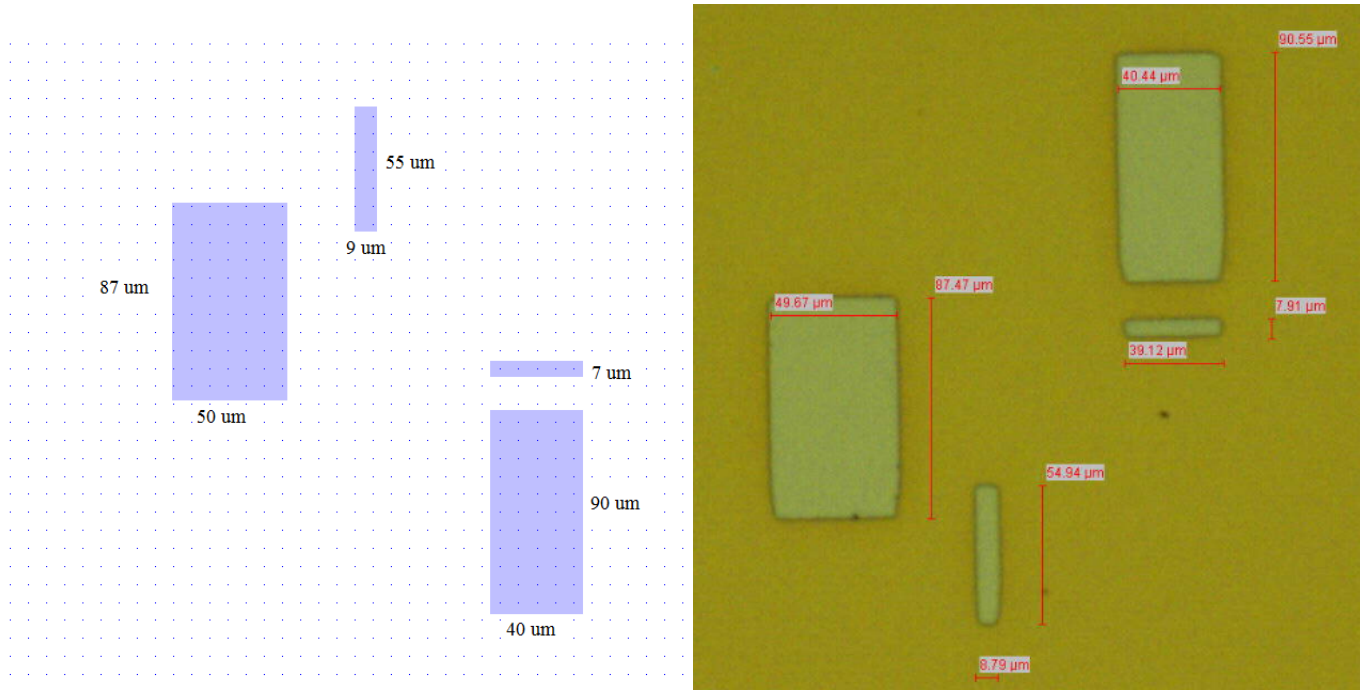
(c) Dose$100mJ/cm^2$

Figure 2.3: Dose variation Experiment 500nm SEM surface

From the Scanning Electron Microscope(SEM) inspection of the exposed samples it shows the dose is less than $80mJ/cm^2$. Critical dose for exposure of the resist at $70mJ/cm^2$ gave proper pattern transfer from mask onto the resist as shown in fig:2.4.



(a) SEM surface $10um$



(b) Active area design and pattern transfer

Figure 2.4: Optical exposure at dose $70mJ/cm^2$

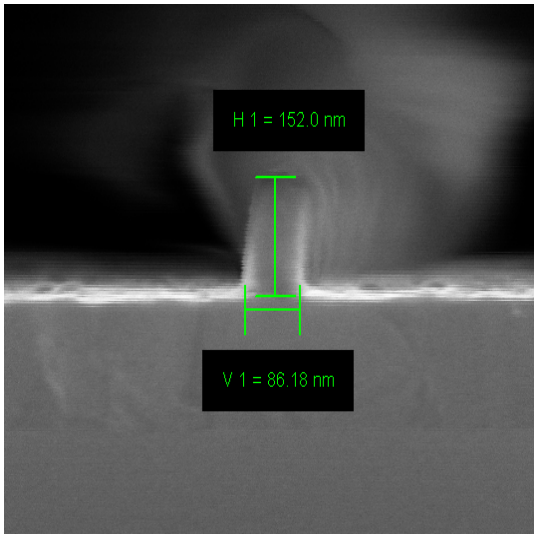
2.2.4 Electron Beam Lithography Dose Experiment

Dose variation experiment for electron beam exposure of Su8 2000.5 was done.As the resist is highly sensitive dose was varied from $1\mu C/cm^2$ to $6\mu C/cm2$[6].SEM lines of feature size $800nm$, $400nm$, $200nm$, $100nm$ were written and optimized for line width and side-wall profile.

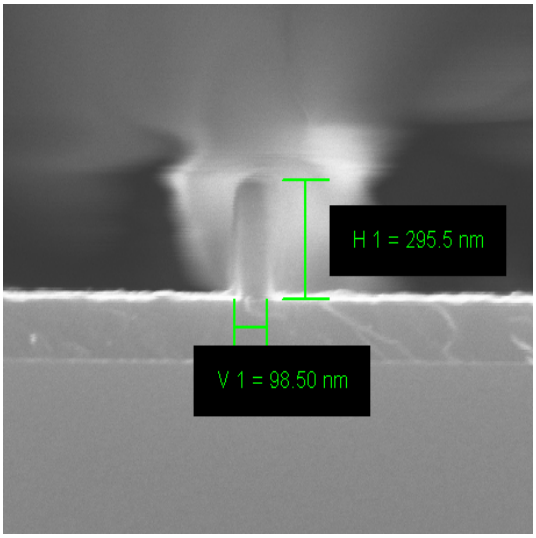
Resist	Spin schedule	Pre-bake/PEB	Exposure
Su8 2000.5	5 sec – 500 rpm 45 sec – 6000 rpm 5 sec – 0 rpm	65°C – 1 min 95°C – 1 min Wafer should be on the hot-plate during ramp up/down	1 – 6 uC/cm^2
Development- Su8 developer 30 sec followed by IPA rinse			

Table 2.2: EBL dose variation Experiment

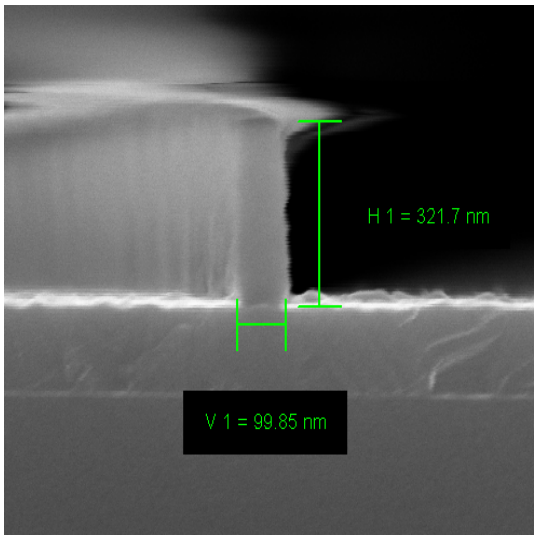
As seen in fig:2.5, dose of $4\mu C/cm^2$ was optimum for line-width and good aspect-ratio.



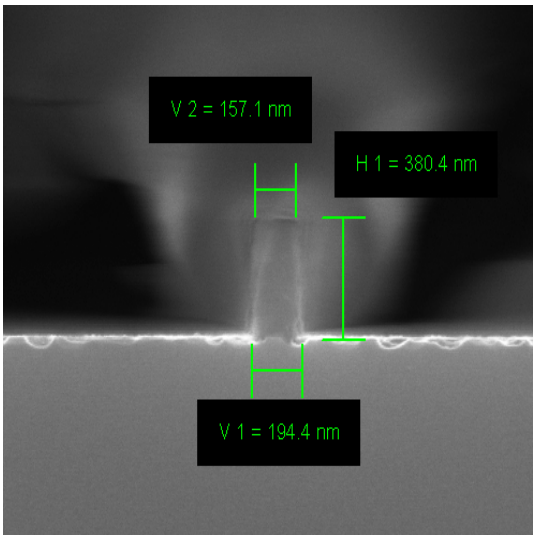
(a) Dose $1\mu C/cm^2$



(b) Dose $3.5\mu C/cm^2$



(c) Dose$4\mu C/cm^2$



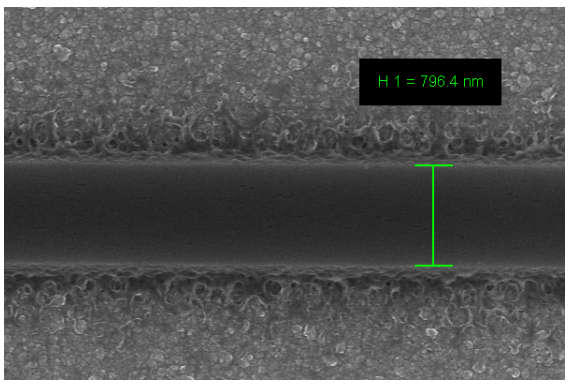
(d) Dose$6\mu C/cm^2$

Figure 2.5: Dose variation Experiment 100nm SEM cross-section

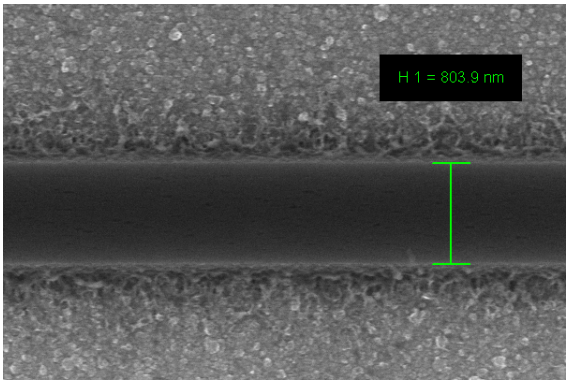
As seen in fig:2.6, development time of $60sec$ was optimum for good side-wall profile.

Resist	Spin schedule	Pre-bake/PEB	Exposure
Su8 2000.5	5 sec – 500 rpm 45 sec – 6000 rpm 5 sec – 0 rpm	65°C – 1 min 95°C – 1 min Wafer should be on the hot-plate during ramp up/down	4 uC/cm^2
Development- Su8 developer 20 sec – 90 sec followed by IPA rinse			

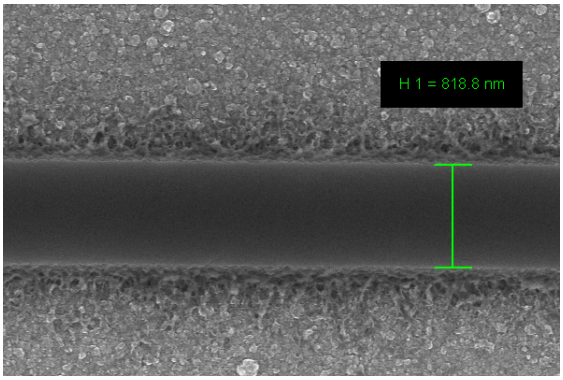
Table 2.3: EBL resist development time variation Experiment



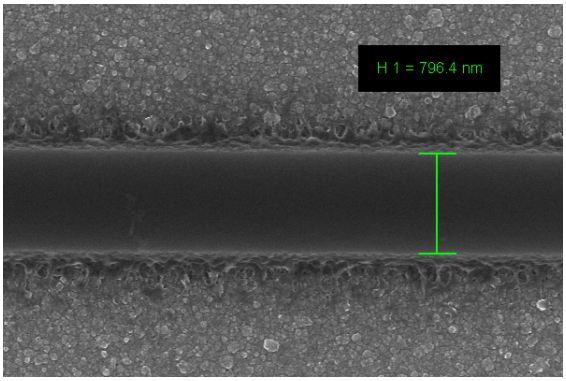
(a) 20sec



(b) 30sec



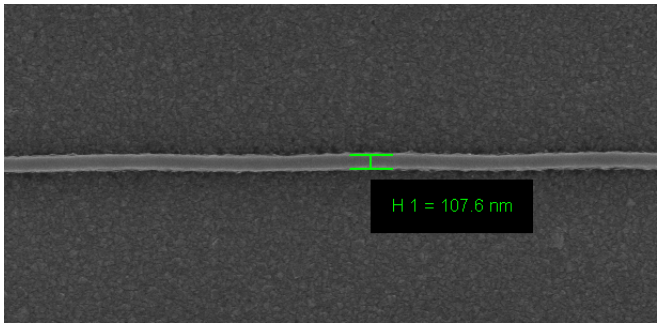
(c) 60sec



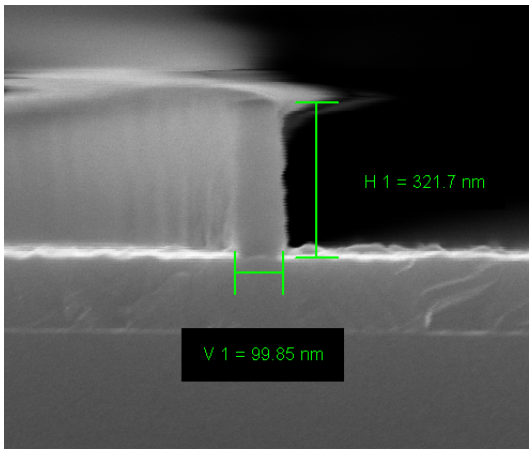
(d) 90sec

Figure 2.6: Development time variation Experiment 800nm SEM surface

Dose of $4\mu C/cm^2$ and development time of 60sec gave good line widht and side-wall profile as shown in fig:2.7.



(a) 100nm SEM surface

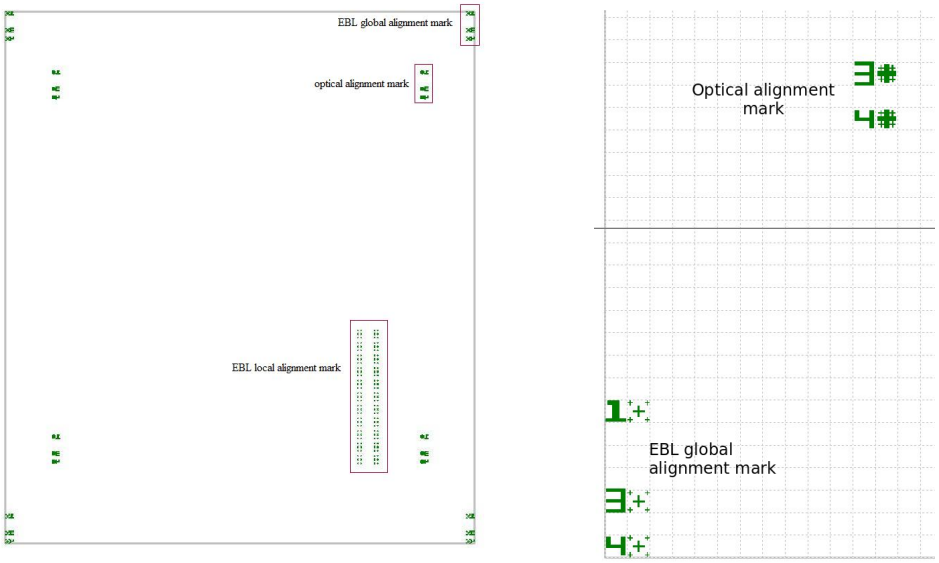


(b) 100nm SEM cross-section

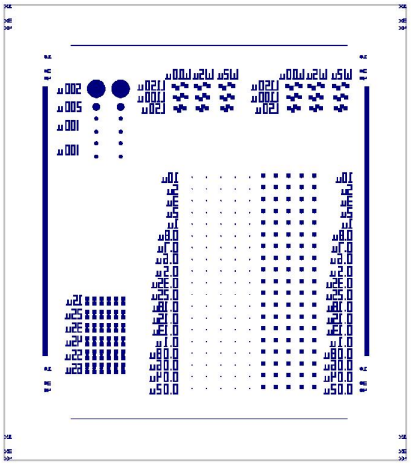
Figure 2.7: EBL exposure at dose of $4\mu C/cm^2$

2.2.5 Process Steps for Sub-100nm MOSFET Gate patterning

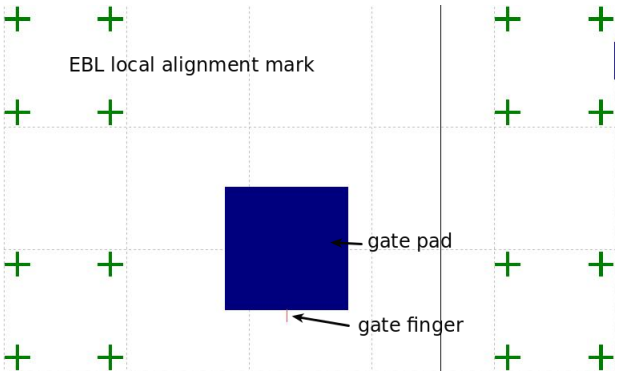
For Mix and Match lithography first we need to define alignment marks which will be used as reference for optical and electron beam exposure,thus ensuring alignment of optical exposed patterns with electron beam exposed patterns.



(a) 0^{th} level EBL



(b) Optical pattern design



(c) Gate fingers EBL

Figure 2.8: Design for Mix and Match

The above figure shows the design for the three levels of lithography i.e., 0^{th} level EBL, Gate pads and other structures using optical lithography and gate fingers using EBL. As seen in the design, the optical alignment marks are used for aligning gate mask with 0^{th} level patterns on wafer. The EBL global and local alignment marks are used for aligning gate

fingers with gate pads.

In the design, considering separate exposure for gate pad (Optical) and gate finger (EBL), overlapping of $2um$ between gate pads and gate fingers is kept. This ensures proper connectivity between gate pad and finger.

The process steps developed for Mix and Match lithography are listed below.The recipe for the process is given in Table 2.4.

1. Si wafer 4 inch 100 p-type
2. RCA clean
3. pyrogenic oxide growth
4. EBL 0^{th}level for alignment marks
5. wet etch of oxide
6. resist strip
7. Reactive Ion etching(RIE) of Si for trench formation in the wafer
8. blanket wet etch of oxide
9. SEM inspection of alignment marks
10. optical lithography using Gate area dark field mask for gate pads
11. Electron beam lithography for gate fingers

Initially,a thick pyrogenic oxide is patterned for alignment marks in EBL.This oxide acts as a hard mask for trenching of alignment marks in Si substrate, more than $2\mu m$ deep trench is formed.The trenches are made deep enough so that the trench doesn't get filled at further layers.This alignment mark trench is used as a reference for aligning the gate pads in optical lithography and alignment of gate fingers in electron beam lithography.

SU8 resist is used for gate patterning.When baking Su8 resist the wafer needs to be placed on the hot plate at 65^0C and after time specified (table 2.4, process step no.10) the hot plate should be ramped up to 95^0C keeping the wafer on the hot plate.After baking for the specified time the hot plate needs to be ramped down back to 65^0C and only after this the wafer should be taken off the hot plate. This process is required to avoid cracks in the Su8 resist.

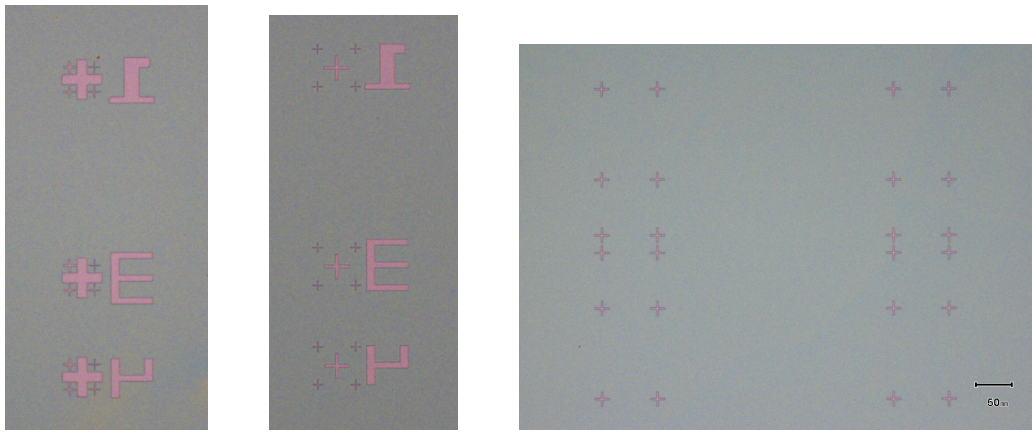
Process Step no.	Process	Receipe
3	Pyrogenic Oxide – 200 nm	H2-8000 sccm, O2-6000 sccm, Temp-1000°C, Torch temp-835°C, Duration-20 min
5,8	Oxide wet etch	BHF : 2 ~ 3 min followed by DI water rinse
6	PMMA resist strip	Acetone :5 min + IPA :5min
7	Si RIE dry etch	SF6-40 sccm, 400 W, 100 mtorr, 2 min (etch rate > 2um/min)

Process Step no.	Process	Resist	Spin schedule	Pre-bake	Exposure	PEB/PDB
4	0^{th} level EBL (align marks)	PMMA 950K 4%	5 sec – 500 rpm 45sec - 3500 rpm 10 sec- 0 rpm	180°C - 90 sec	EBL 10 KV , 30 um aperture Dose – 73 uc/cm2	PDB- 100°C-2 min
10	1^{st} level optical litho (gate pads)	Su8 2000.5	5 Sec – 500 rpm 45 sec – 6000 rpm 5 sec – 0 rpm	65°C - 1 min 95°C – 1 min Wafer should be on the hot plate during ramp up/down	Optical Dose – 70 mJ/cm2 ⇩	-
11	1^{st} level EBL (gate fingers)	-	-	-	EBL 20 Kv , 7.5 um aperture Dose – 4 uc/cm2	PEB 65°C - 1min 95°C - 4 min

Resist	Development Receipe
PMMA 950k 4%	MIBK:IPA (1:3) – 30 sec followed by IPA – 15 sec
Su8 2000.5	Su8 developer – 1 min followed by IPA rinse

Table 2.4: Process recipe developed for Mix and Match using Su8 2000.5 resist

In process step no.4, the design shown in fig:2.8(a) is used for patterning the alignment marks on the wafer.

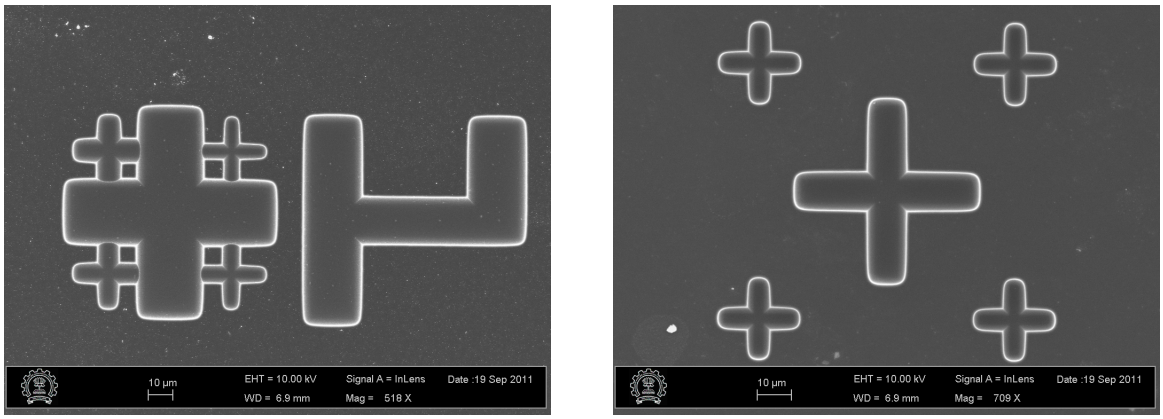


(a) Optical mark (b) EBL global mark (c) EBL local alignment mark(design shown in fig:2.8(c)

Figure 2.9: Microscope images after 0^{th} level EBL(Process step no.4)

After alignment mark patterning the oxide beneath the resist is exposed in the regions of marks.In process step no.5, when the wafer is wet processed in BHF the exposed oxide is etched revealing the silicon beneath.Due to wet process the patterns on the wafer come out bigger than the EBL pattern design.

After resist strip(process step no.6) oxide will act as a hard mask(high selectivity between Si and SiO2) for etching(process step no.7).During Reactive Ion Etching(RIE) trenches are formed in the exposed silicon region,thus successfully transferring the alignment mark patterns onto the wafer.This is followed by blanket wet etch of oxide(process step no.8).



(a) Optical alignment mark

(b) EBL global alignment mark

Figure 2.10: SEM image after RIE(Process step no.7) and Oxide wet etch(process step no.8)

The alignment marks on wafer shown in fig:2.10 will be used as reference point for aligning further layers(gate pads and gate fingers).As seen in SEM image trenching helps to get better contrast to identify the marks clearly.

For process step no.10 i.e., patterning of gate pads using optical lithography the optical alignment mark shown in fig:2.10(a) will be used for alignment.These marks will be aligned with the Gate area dark field mask whose design is shown in fig:2.8(b) and microscope image shown in fig:2.11.

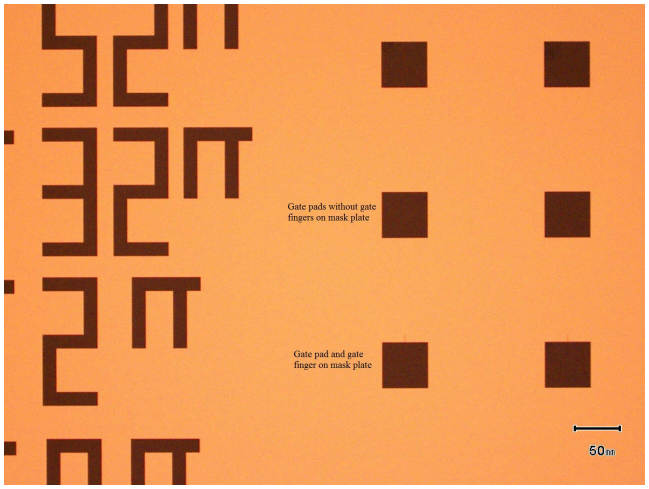
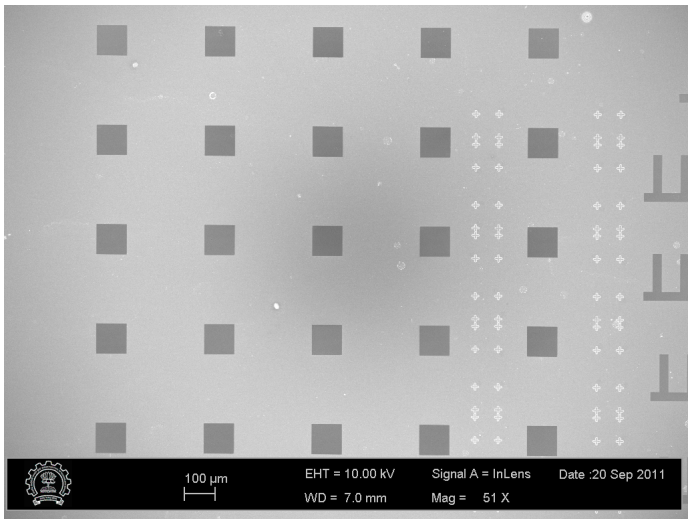
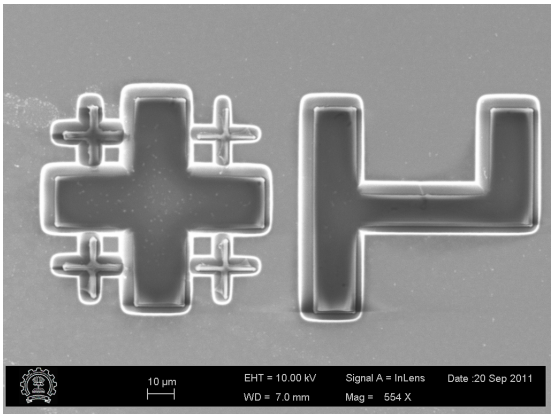


Figure 2.11: Microscope image of Gate area dark field mask

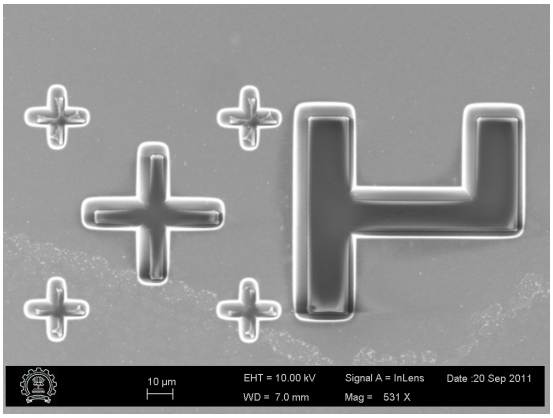
For Mix and Match process, the Gate pads without gate fingers on mask plate will be used.SEM image of fig:2.12 after process step no.10(the image was taken after completing Mix and Match process as the patterns are visible only after resist is developed after process step no.11), shows the gate pads(this was the dye where gate fingers were not patterned) aligned with the EBL local alignment marks as shown in design in fig:2.8(c). This alignment was achieved by aligning the alignment marks on mask plate with the marks on wafer.



(a) optical patterned pads aligned with 0^{th} level EBL local alignment marks



(b) Optical alignment mark*



(c) EBL global alignment mark*

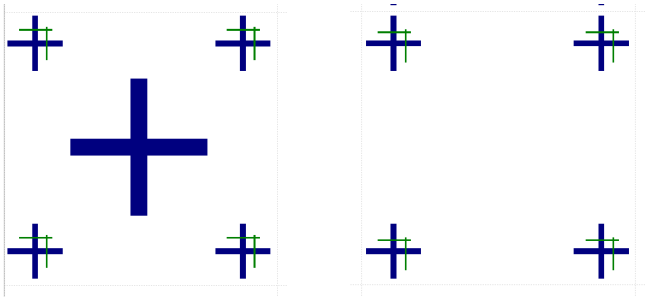
Figure 2.12: SEM image of optical pattern alignment of process step no.10

*Misalignment between EBL 0^{th} trench marks and Optical alignment mark is seen in order of $1um$. This was due to difference in dimensions of marks (due to wet etch process during trench process) and also the visibility of trench edges after resist spin during Optical lithography is not sharp.

Now for final process step no.11, the gate fingers need to be aligned with the gate pads patterned using optical lithography.The EBL global(fig:2.9(b)) and local(fig:2.9(c)) alignment marks on the wafer need to be aligned with similar marks in design(fig:2.8(c))

Unlike in optical lithography, in EBL the pattern is formed by exposing the resist to the electron beam by scanning the whole region pixel by pixel.In EBL there is the concept of WriteField(WF), the design is divided into multiple WFs(for example here we have chosen 100um*100um WF).Each WF is patterned by deflecting the beam along the WF area without moving the stage(on which the wafer is placed).

Fig:2.13 shows the WFs of global and local alignment mark.Aligning these WFs with the help of alignment marks,effectively aligns the whole design to be patterned onto the wafer.Auto mark scan are used for specifying the region to be scanned on wafer for locating the alignment marks.



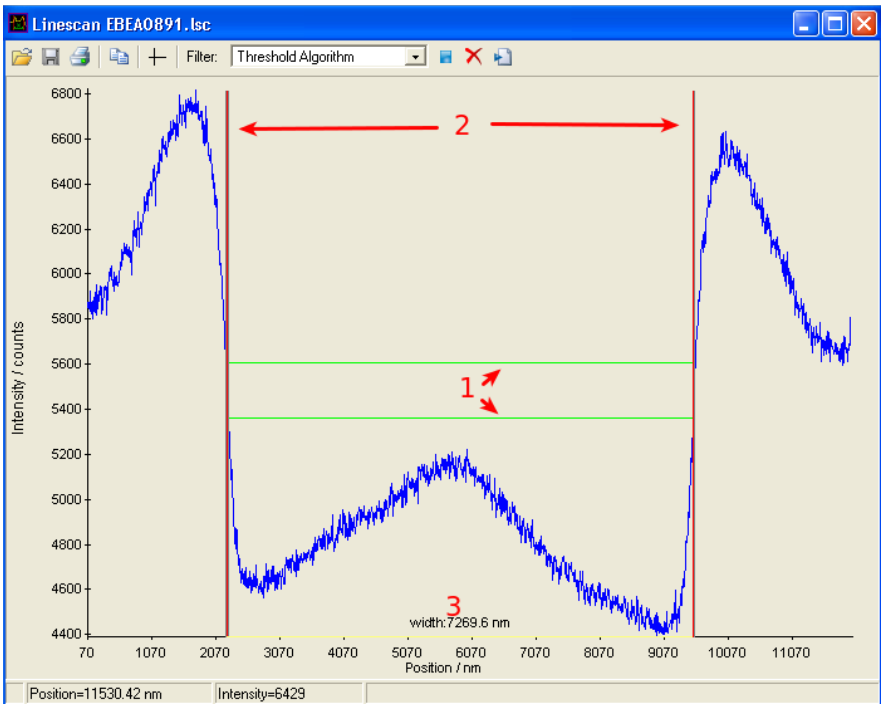
(a) EBL global alignment mark

(b) EBL local alignment mark

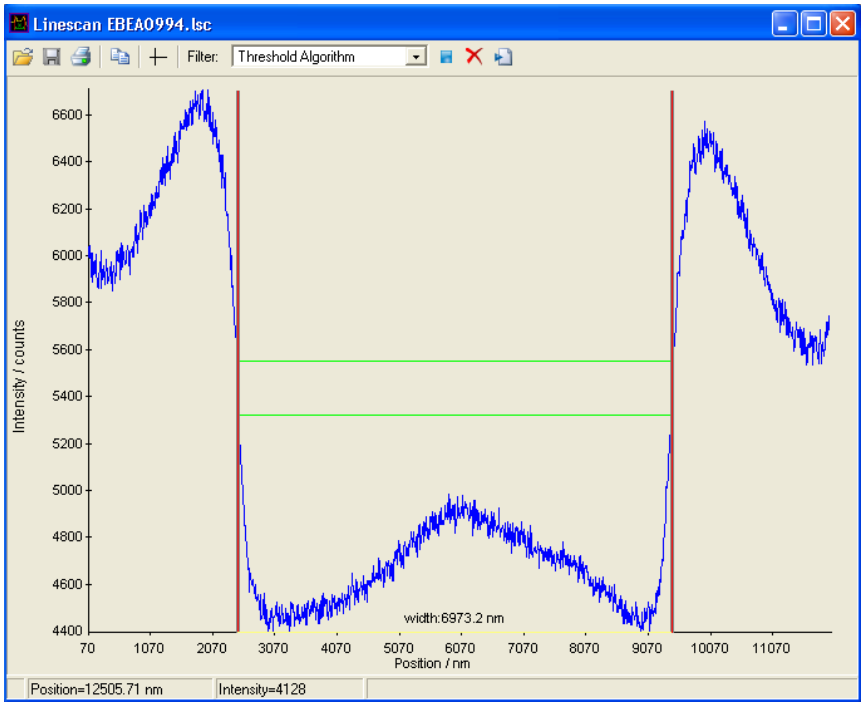
Figure 2.13: Design showing marks with auto mark scan in green colour

The trench marks on the wafer are scanned (using auto mark scan) which gives an intensity profile as shown in fig:2.14.

Threshold algorithm shown in fig:2.15 is used for finding the edges of the alignment marks from the intensity profile scan.



(a) EBL global alignment mark



(b) EBL local alignment mark

Figure 2.14: Intensity profile along the auto mark scan region

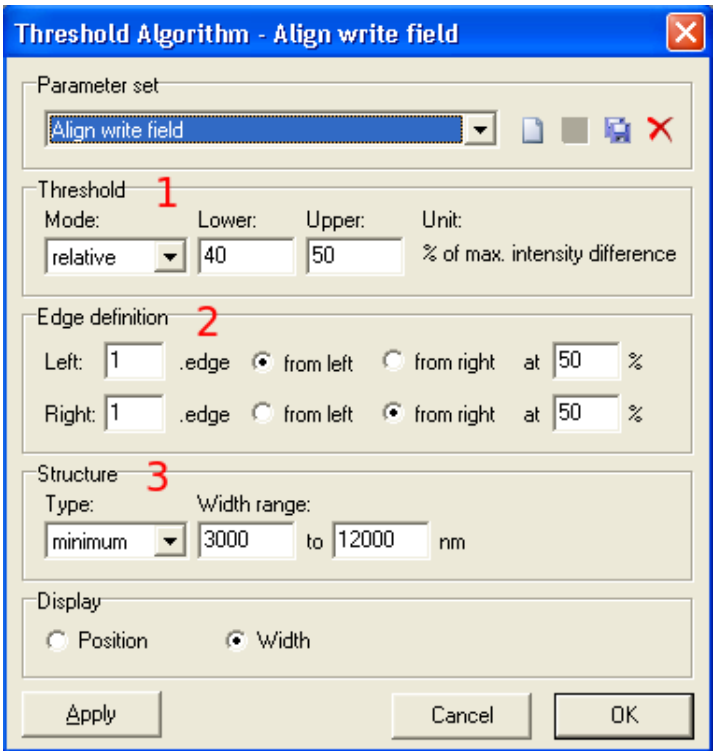


Figure 2.15: Threshold algorithm used to define edges of alignment marks from the intensity profile

1.Threshold

The lower and upper values define the threshold levels shown as horizontal green lines in the intensity profile. These percentage values are relative. As seen in fig 2.14:(a), 4400 is the minimum and 6800 is the maximum intensity, the difference between these two values is 2400. Now for calculating lower threshold of 40%, 40% of 2400 is added to minimum intensity resulting in lower threshold at 5360. Similarly for upper threshold, it is at 5600.

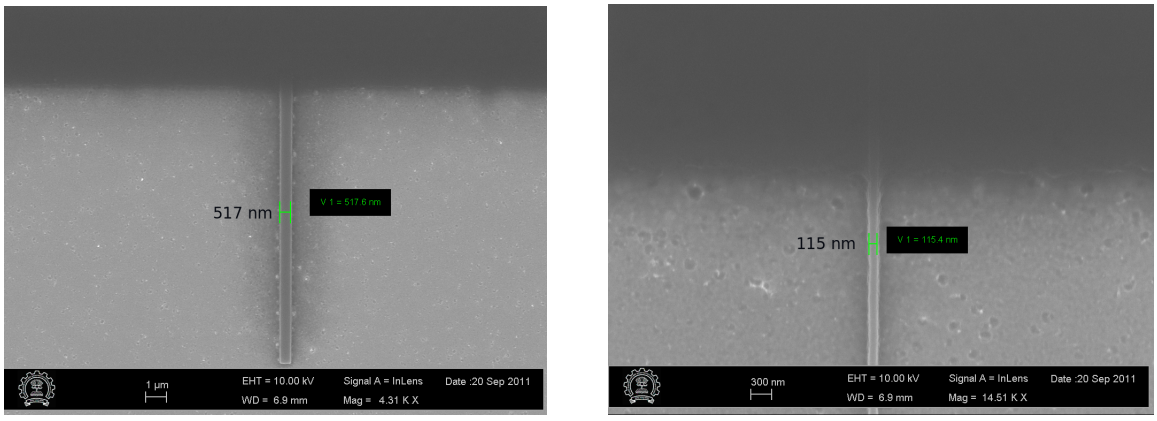
2.Edge definition

It is used for defining the edges of the structure scanned. This is useful other peaks (excluding the structure peaks) are present within the scan.50% means the edge is in the centre of the range defined by the threshold values.

3.Structure

The width range limits the range the algorithm is searching for the second edge after finding the first edge.

If the algorithm fails to find the edges the parameters in the algorithm should be tuned(vary the threshold values,structure width range) such that the edges are detected by the algorithm.Thus, the design for patterning gate fingers is aligned with the already existing pattern on the wafer. The final gate(pads with optical lithography and fingers with EBL) with different gate lengths are shown below.



(a) 500nm Gate pattern (b) 100nm Gate pattern

Figure 2.16: Final Gate patterns after Mix and Match lithography

2.3 Summary

The process flow and recipe for Mix and Match lithography is developed using Su8 resist which is sensitive to both optical source and electron beam.It gives advantage of fabricating patterns having big features as well as small nano-scale features by dividing the patterning process between Optical and electron beam exposure.The other major advantage is the ability to pattern design with varied dimensions without compromising on throughput.

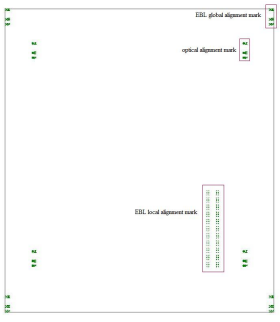
Chapter 3

Implimentation of Mix and Match lithography for fabrication of short-channel devices

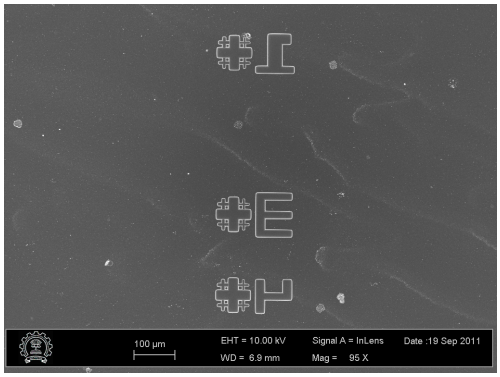
The process of Mix and Match explained in the previous chapter was used for the fabrication of short channel devices. for these devices, the gate pads are patterned using optical lithography and gate fingers using EBL.The steps below only explain the lithography steps in transistor fabrication(example:field oxide growth, gate deposition are not shown).

3.1 Alignment marks

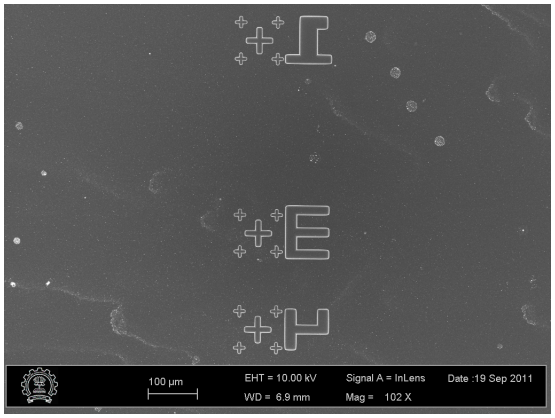
Alignment marks were defined using electron beam lithography. The process steps and recipe are same as explained in section 2.2.5.



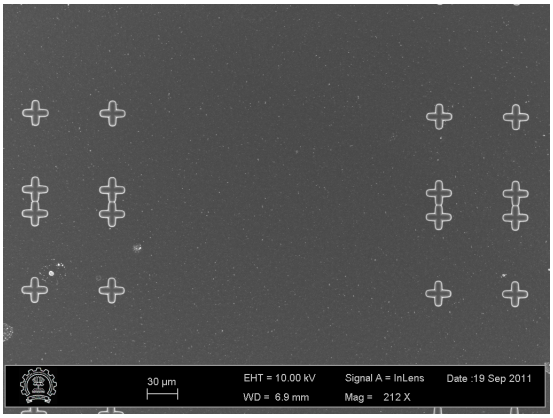
(a) 0^{th} level design



(b) DSA alignment mark



(c) EBL global alignment mark

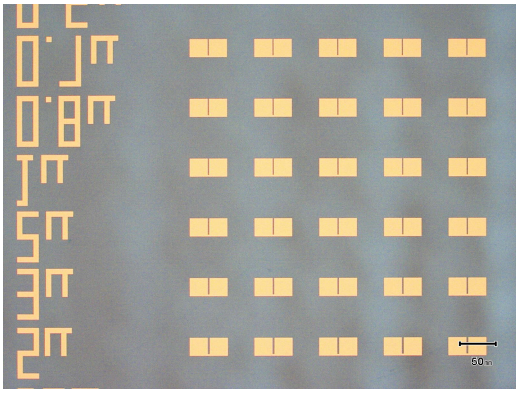


(d) EBL local alignment mark

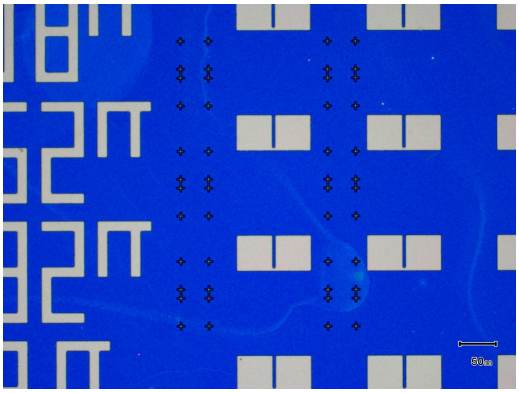
Figure 3.1: 0^{th} level electron-beam lithography

3.2 Active area

After alignment marks trenching comes active area definition.Active area was patterned using optical lithography. This is second level lithography which will be aligned with the alignment marks(DSA marks and EBL global marks).



(a) Active area mask

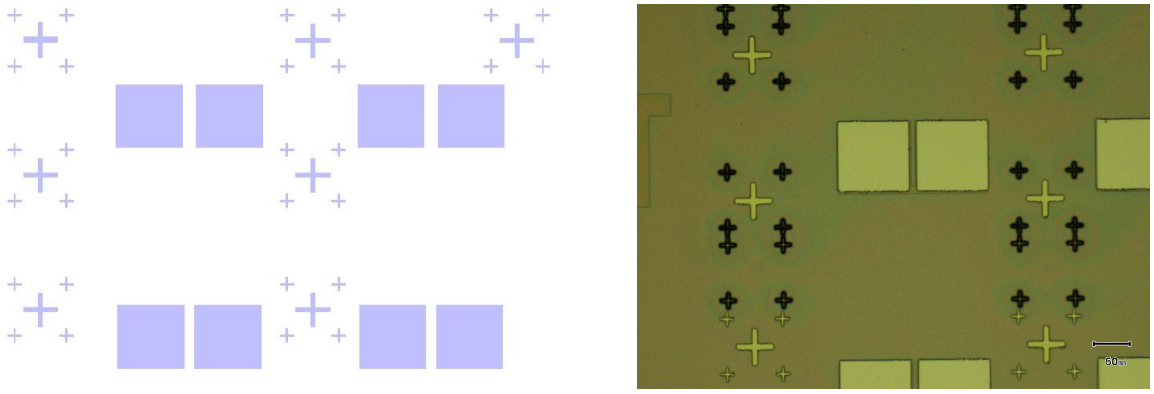


(b) Pattern defined on wafer

Figure 3.2: Active area defintion using Optical lithography

3.3 Probe area

The next lithography step was probe area lithography,for deep implants in source/drain regions(this would help in probing source/drain during characterisation).



(a) Probe area mask

(b) Box opened in source/drain region for deep source/drain implant

Figure 3.3: Probe area defintion using Optical lithography

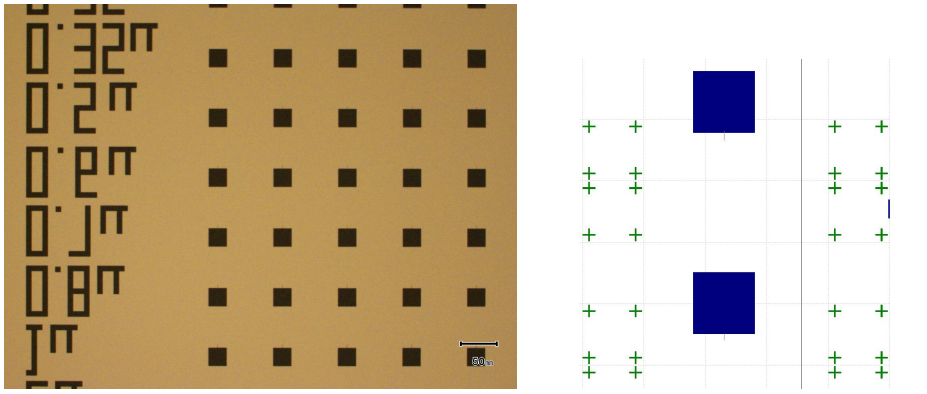
The recipe for both active area and probe area lithography is shown below.

	Resist	Spin schedule	Pre-bake	Exposure	PDB
Active area /Probe area	HMDS	10 sec – 500 rpm 45sec - 7000 rpm 10 sec- 500 rpm	120°C – 6 min	Optical Dose – 64 mJ/cm2	90°C – 2 min
	S1813	5 Sec – 500 rpm 30 sec – 6000 rpm 5 sec – 0 rpm	90°C – 2 min		
Development- MF319 developer for 25 sec followed by D.I water rinse					

Table 3.1: Recipe for active and probe area lithography

3.4 Gate area Mix and Match

The last lithography step was the mix and match lithography for gate patterning.The recipe for this is in Table 1.1:process steps 10(gate pads) and 11(gate fingers).



(a) Gate area mask

(b) gate fingers(to be patterned) overlapping gate pads

Figure 3.4: Gate area lithography

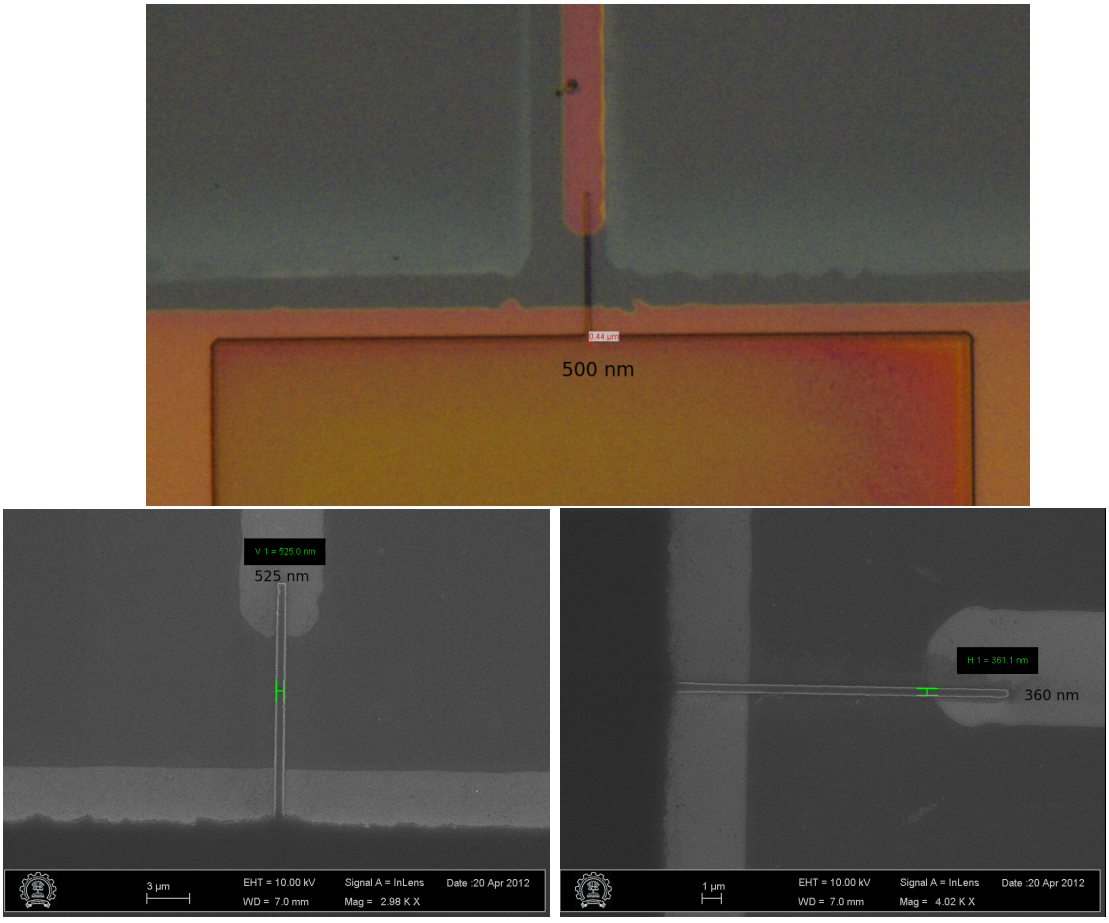


Figure 3.5: Microscope(400nm) and SEM image(525nm and 360nm) after gate level lithography(Mix and Match)

3.5 Summary

The ability to fabricate short-channel devices using Mix and Match lithography is demonstrated. Mix and match lithography was used for patterning gate region, where the gate pads were exposed using optical source and gate fingers using electron beam.

Chapter 4

Fabrication of RF oscillator circuit using Mix and Match lithography

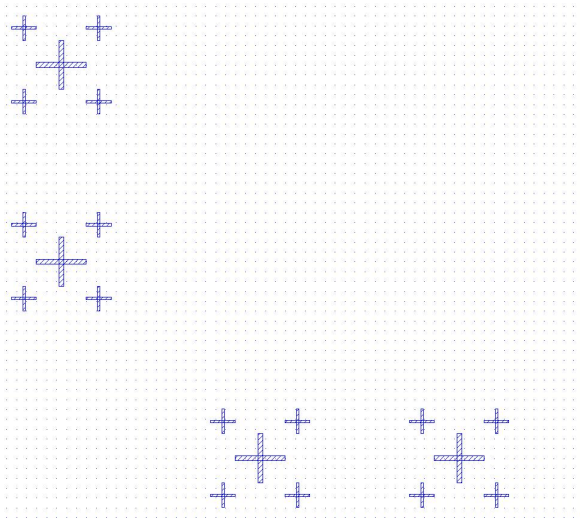
In this chapter, circuit level implimentation of Mix and Match lithography is shown. This work was done in collaboration with Indian Institute of Science (IISc). The mask designs and mask plates were provided by IISc. The process flow for fabrication of RF oscillator circuit and results of different unit processes are explained.

4.1 Alignment marks definition

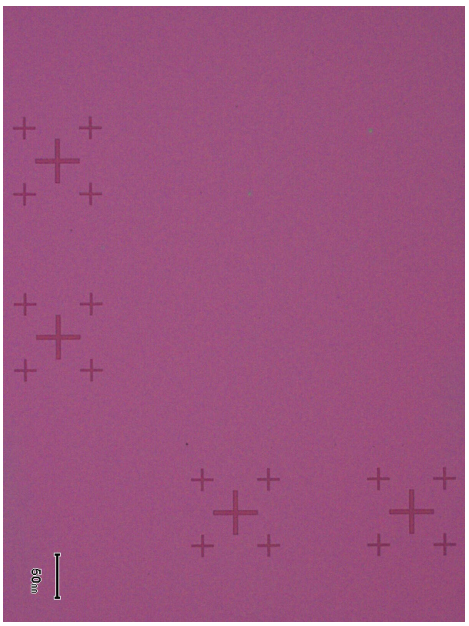
Firstly, the alignment marks need to be defined because in gate level,the gate fingers need to be patterned using EBL and gate pads/resistor using optical lithography requiring use of Mix and Match lithography.

1. Si wafer 4 inch 100 p-type
2. RCA clean
3. pyrogenic oxide growth
4. EBL 0^{th}level for alignment marks
5. wet etch of oxide
6. resist strip
7. Reactive Ion etching(RIE) of Si for trench formation in the wafer
8. blanket wet etch of oxide
9. Inspection of alignment marks

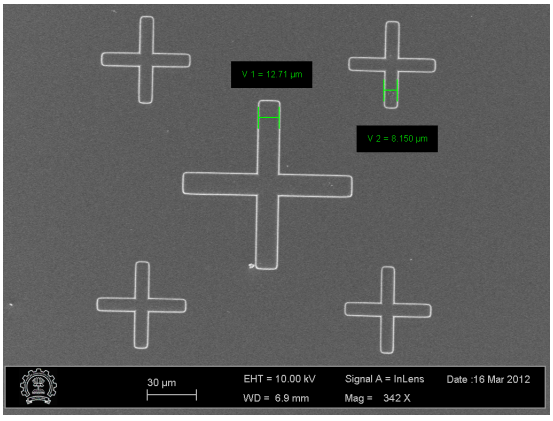
The recipe for alignment mark definition is same as shown in Table 1.1 (process steps 1-9). The pyrogenic oxide is patterned using EBL design shown in fig 4.1:(a). After patterning(fig 4.1:(b)), the oxide in the alignment marks region is wet etched to expose the silicon beneath for dry etch. During RIE, the pyrogenic oxide will act as a hard mask for silicon trenching (high selective recipe between Si and Silicon dioxide is used). These trenched alignment marks give a good contrast image in SEM as shown in fig 4.1:(c) which will be used for aligning gate fingers in EBL.



(a) EBL design



(b) Pattern on wafer after EBL



(c) alignment mark trench

Figure 4.1: Alignment mark definition

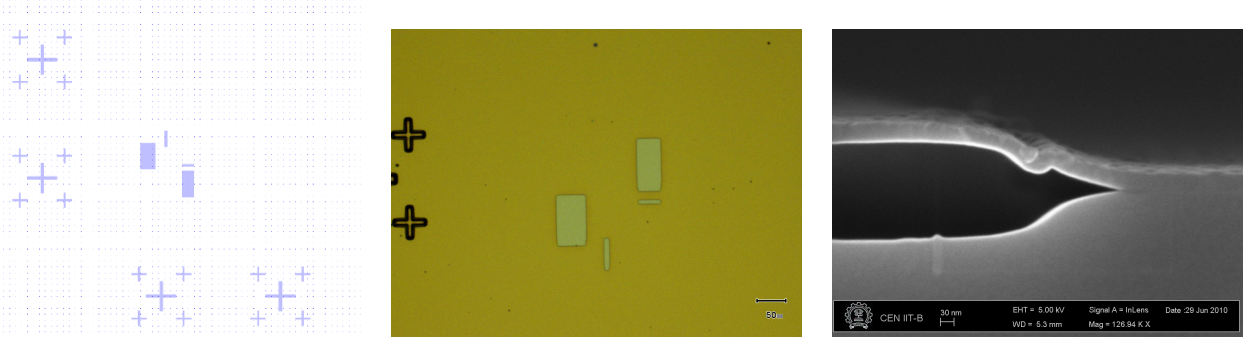
4.2 Active area definition

After alignment mark trenching, the active area is patterned on the wafer.The design shown in fig 4.2:(a) defines the active region .This design is aligned with the alignment marks on the wafer during lithography.After patterning the active region, silicon dioxide is grown isolating the active regions.

The process steps for active area definition are:

1. RCA clean
2. pad oxide growth
3. silicon nitride deposition
4. Active area optical lithography
5. silicon nitride dry etch
6. Piranha clean
7. HF dip
8. Field Oxide growth
9. Nitride wet etch

The active area region and field oxide can be seen in fig 4.2(b).The devices will be patterned over these acive regions.



(a) Design (b) pattern on wafer (c) Field oxide SEM image

Figure 4.2: Active area definition

	Process	Receipe			
1	RCA clean	2% HF dip – 30 sec RCA 1 – NH_4OH:H_2O_2:DIwater::125 ml:250 ml:875 ml Hot plate – 75°C 2% HF dip – 30 sec RCA 2 – HCL:H_2O_2:DIwater::125 ml:250 ml:875 ml 2% HF dip – 30 sec			
2	Pad oxide growth(6nm)	Pre-growth step: temp-800°C,O_2-50 sccm,N_2-on,duration-120 sec Growth step: temp-800°C,O_2-5000 sccm,duration-1800 sec Anneal: temp-900°C,N_2-on,duration-600 sec			
3	Silicon Nitride deposition(60nm)	SiH_4-45 sccm, NH_3-40 sccm,N_2-1000 sccm,temp-780°C Pressure-0.3torr,duration-4200sec			
4	Active area Optical lithography	Resist	Spin schedule	Pre-bake/PEB	Exposure
		Su8 2002	5 sec – 500 rpm 45 sec – 4000 rpm 5 sec – 0 rpm	65°C – 1 min 95°C – 1 min Wafer should be on the hot plate during ramp up/down	50 mJ/cm^2
		Development- Su8 developer 1min followed by IPA rinse			
5	Silicon Nitride dry etch	CF_4-40 sccm,O_2-4 sccm,RF-50 W,pressure-110 mtorr Selectivity Si_3N_4/SiO_2- 3.5			
6	Piranha clean	H_2SO_4:H_2O_2 – 910 ml:390 ml, 1 hr dip			
7	HF dip	2% HF – 30 sec			
8	Field oxide growth(280 nm)	H_2 – 8000 sccm,O_2 – 6000 sccm, temp – 1000°C, torch temp –835°C duration – 35 min			
9	Silicon Nitride wet etch	BHF(5:1) – 10 sec, H_3PO_4- 87%, temp – 160°C, time – 50 min Si_3N_4 etch rate – 2 nm/min			

Table 4.1: Recipe for active area definition

4.3 Gate area definition

The gate area of devices and resistor are defined in this module. Poly-silicon is used as gate/resistor material.Mix and match lithography will be used for patterning the design(fig 4.4(a)),the patterns in red colour will be patterned using optical lithography and patterns in black(gate fingers) will be patterned using EBL.

The process steps for gate area definition are:

1. RCA clean
2. gate oxide growth
3. n-poly deposition

4. Thermal activation of n-poly
5. oxide wet etch(front/back)
6. gate pads and resistor photo-lithography
7. gate fingers patterning using EBl
8. Poly dry etch
9. resist ashing
10. piranha clean
11. APM clean

	Process	Receipe			
1	RCA clean	2% HF dip – 30 sec RCA 1 – NH_4OH:H_2O_2:DIwater::125 ml:250 ml:875 ml Hot plate – 75°C 2% HF dip – 30 sec RCA 2 – HCL:H_2O_2:DIwater::125 ml:250 ml:875 ml,2% HF dip – 30 sec			
2	Gate oxide growth(3nm)	Pre-growth step: temp-850°C,O_2-50 sccm,N_2-on,duration-30 sec Growth step: temp-850°C,O_2-500 sccm,duration-120 sec Anneal: temp-850°C,N_2-on,duration-600 sec			
3	N-poly deposition	SiH_4 – 85 sccm, PH_3 – 120 sccm,temp – 700°C Pressure – 275 torr,duration – 1 min			
4	N-poly thermal activation	O_2 – 900 sccm, temp – 1000°C, duration – 30 sec			
5	Oxide etch front/back	2% HF – 2 min followed by DI water rinse			
6, 7	Gate/resistor patterning (Mix and Match lithography)	Resist	Spin schedule	Pre-bake/PEB	Exposure
		Su8 2000.5	5 sec – 500 rpm 45 sec – 6000 rpm 5 sec – 0 rpm	65°C – 1 min 95°C – 1 min Wafer should be on the hot plate during ramp up/down	Optical – 70mJ/cm^2 + EBL – 4 uc/cm^2
		Development- Su8 developer 1min followed by IPA rinse			
8	Poly dry etch	CF_4:O_2 – 40 sccm:5 sccm, RF:350 W, pressure – 20 mtorr, time – 45 sec CF_4:O_2 – 40 sccm:5 sccm, RF:20 W, pressure – 500 mtorr, time – 30 sec			
9	Resist ashing	N_2- 200 sccm, O_2 – 3500 sccm, H_2O – 300 sccm Pressure – 2 mtorr, source power – 1400 W, time - 2 min			
10	Piranha clean	H_2SO_4:H_2O_2 – 910 ml:390 ml, 1 hr dip			
11	APM (RCA-I)	NH_4OH:H_2O_2:DIwater::125 ml:250 ml:875 ml Hot plate – 75°C, 10 min 2% HF dip – 30 sec			

Table 4.2: Recipe for Gate area definition

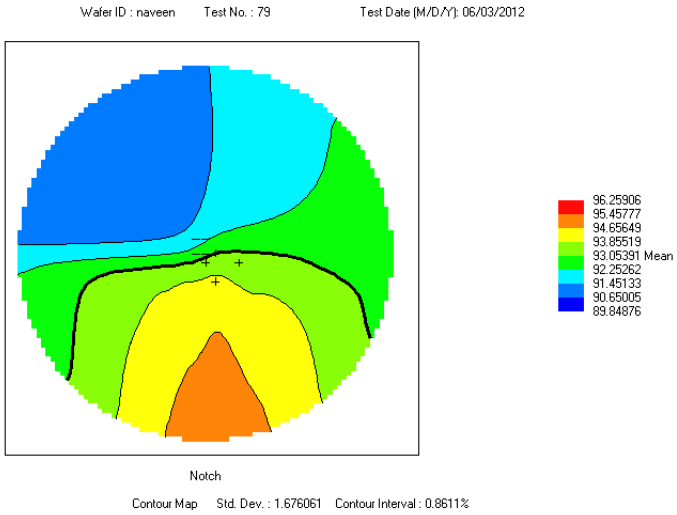
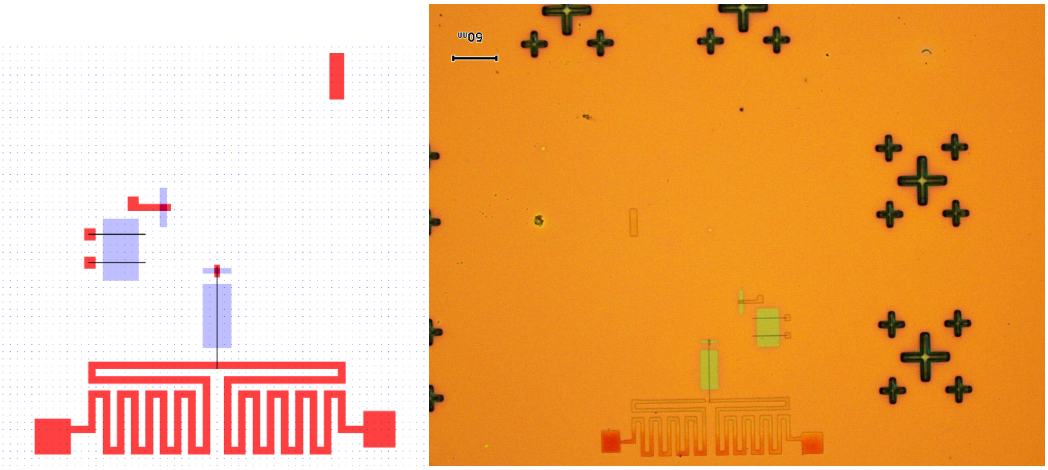


Figure 4.3: Poly sheet resistance data



(a) Design (b) pattern on wafer

Figure 4.4: Gate area definition

The pattern after gate Mix and Match lithography is shown in fig 4.4:(b). There were discontinuities seen in the resistor and as well in gate pads after lithography. This was due to mask plate defects as shown in fig 4.5. The process should be repeated with new mask plates (where defects are corrected).

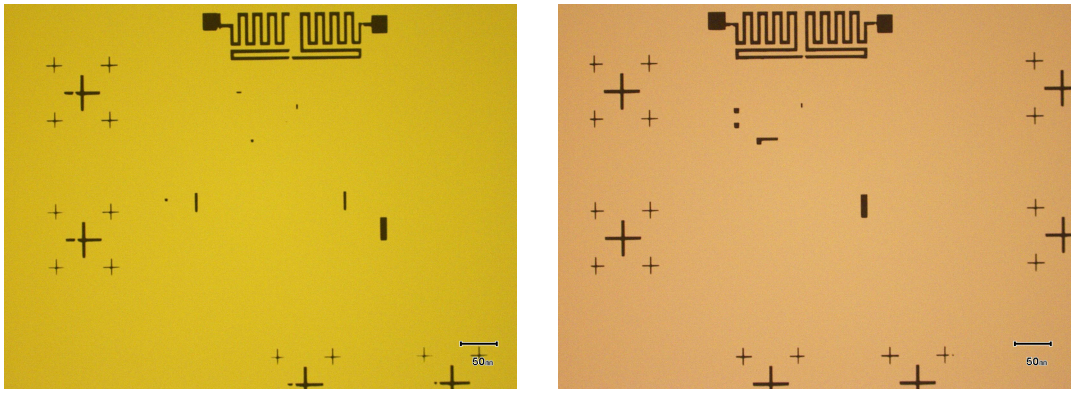


Figure 4.5: Gate area mask

4.4 Further process plan

After re-patterning of gate area definition, the following process is planned for completing the fabrication process.

1. Source/Drain implant and activation.
2. Source/Drain, Gate pads and resistor pads via definition on deposited oxide.

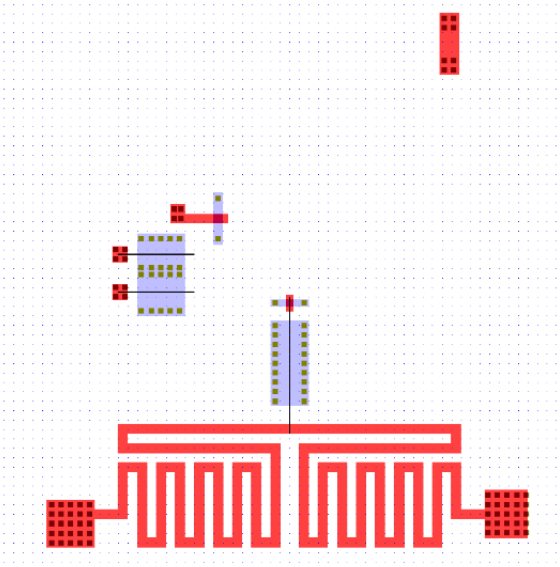


Figure 4.6: Via design showings openings in Source/Drain, Gate pads and resistor pads

3. Titanium and Titanium nitride deposition followed by silicidation.
4. Interconnect definition

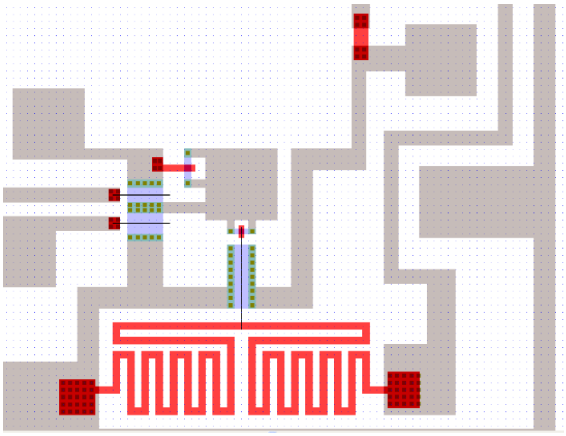


Figure 4.7: Interconnect design for circuit definition

4.5 Summary and Future scope

The initial process plan for fabricating RF oscillator is shown. The fabrication process is done till gate level lithography using Mix and Match.As shown in the results, the gate patterns had discontinuities due to defects in mask plate. The wafers need to be re-processed with new mask plates (defect free) and the integration of further process as planned should be done.

Chapter 5

Focused Electron Beam Induced deposition(FEBID)

5.1 Process of FEBID

Focused electron beam induced deposition(FEBID) is the process by which patterns can be defined on a solid substrate using electron beams with the help of a precursor gas.By focusing an electron beam over the sample in the presence of a precursor gas, pattern is defined directly.As shown in fig:5.1, the precursor gas molecules are adsorbed on a substrate. When the electron beam is focused on the adsorbed precursor molecules , the precursor molecules are dissociated into volatile and nonvolatile components .The nonvolatile components adhere to the substrate and form a deposit.Since e-beams can be focused into spots with diameters varying from micrometers down to the subangstrom level, this direct-write process is suitable for the micro and nanometer regimes.

5.2 Types of interactions

There are mainly three kind of interactions taking place in the FEBID process.

1. substrate – precursor molecule interaction
2. electron – substrate interaction
3. electron – precursor molecule interaction

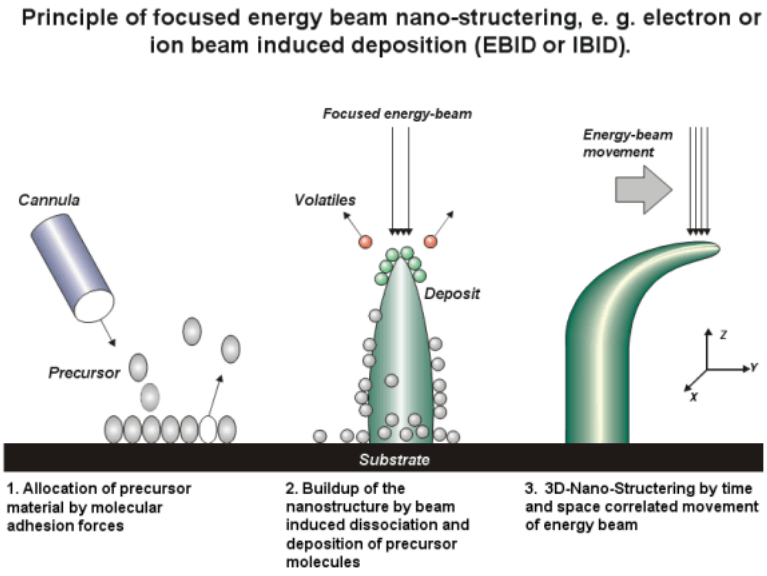


Figure 5.1: Process of FEBID[7]

5.2.1 substrate – precursor molecule interaction

Interactions between the substrate and precursor molecules such as diffusion, adsorption and desorption take place. Adsorption of the precursor molecule may occur as chemisorption or physisorption depending on the combination of precursor, substrate and temperature. The residence time of the precursor molecule on the substrate also can affect beam induced deposition . Longer residence time increases the probability of dissociation by electrons.Desorption of by-products is also an important phenomena , which when inadequately desorbed can lead to contamination of deposited material.

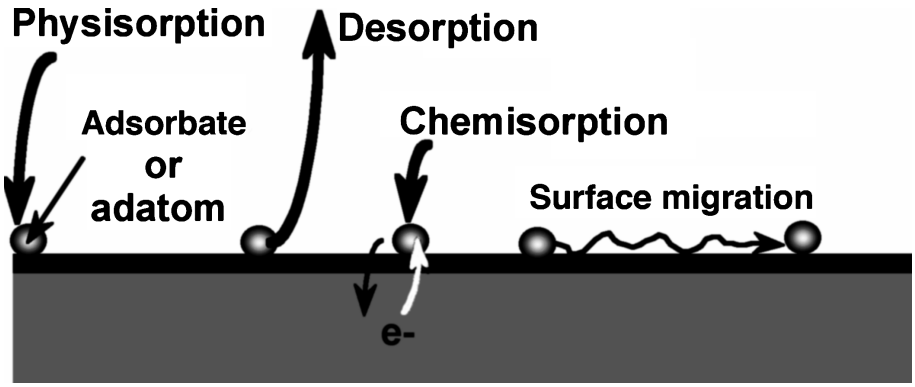


Figure 5.2: substrate – precursor molecule interaction[8]

5.2.2 electron – substrate interaction

The e-beam is focused on the substrate for the initiation of deposition.These electrons are called primary electrons (PEs) . When these PEs collide with the substrate surface, they are deflected from their original trajectory . Inelastic collisions take place and part of its initial energy is transfered from the PE to other electrons in the solid which in turn lead to further scattering . The newly generated electrons are called secondary electrons (SEs) if their energy upon leaving substrate is smaller than 50eV and backscattered electrons (BSEs) if their energy is larger than 50eV. These generated electrons lead to dissociation of precursor molecules around the irradiated spot (e-beam focused region) and play an important role in deposition of material.

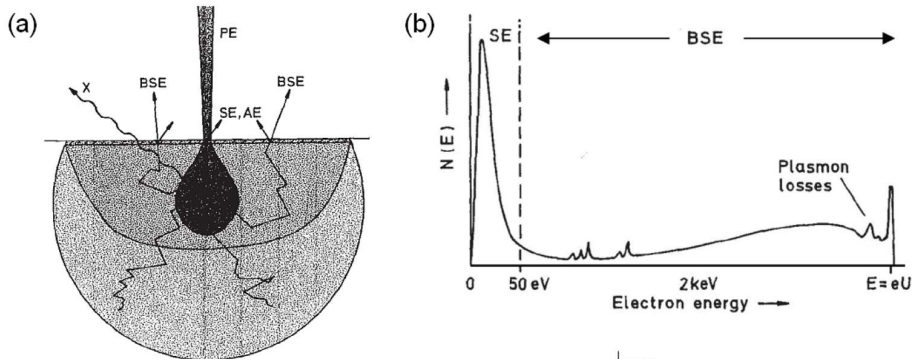


Figure 5.3: (a)schematic of the electron scattering and (b) energy spectrum of electrons emitted[9]

5.2.3 electron – precursor molecule interaction

Apart from dissociation , e-beam can stimulate the desorption process. Probability that an electron induces the scission of a bond in a precursor molecule depends on electron energy and is expressed as a cross section $\sigma_E(cm^2)$.Larger the cross section, larger the probability that the dissociation will take place. The cross section for dissociation of adsorbed molecules depends on many parameters such as energy of bonds within molecule and also the environment . The dissociation process has been studied for both low energy (SEs) and high energy electrons. These studies show that SEs are relevant for the dissociation process. Dissociation processes not only influence the growth rates but can also determine the composition of the deposit.

5.3 Pt deposition using FEBID

Initial experiments were carried out for optimization of FEBID deposited Pt.Precursor used for Pt deposition is $Me_3PtCpMe$.This deposition was done using the Gas Injection System(GIS) of RAITH 150 two.The process was similar to EBL with the addition of precursor gas flow during writing.Literature shows the increase of the deposition rate at lower beam energies as shown in fig:5.4 and showed a correlation with the secondary electron yield as reported.The experiments reported here were done at $3KV$.

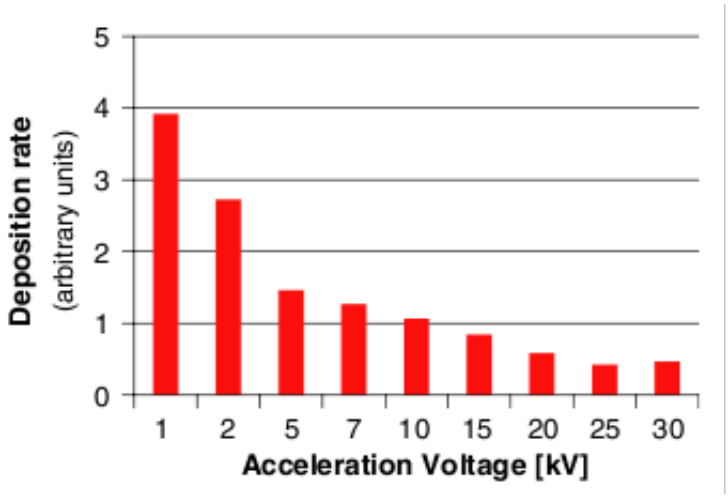


Figure 5.4: Deposition rate correlated to primary electron energy[10]

5.3.1 Thickness estimation of GIS deposited platinum

For determining the thickness of GIS deposited platinum,line depositions were done.Depositing lines of $5-7mm$ required for cross-section sample preparation takes a very long time and lot of precursor is consumed.Therefore,lines of $1\mu m$ length were deposited and tilted imaging was done to estimate the thickness of deposited Pt.

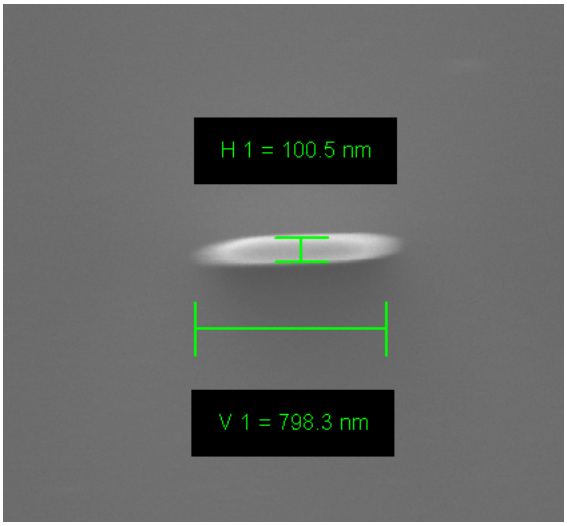
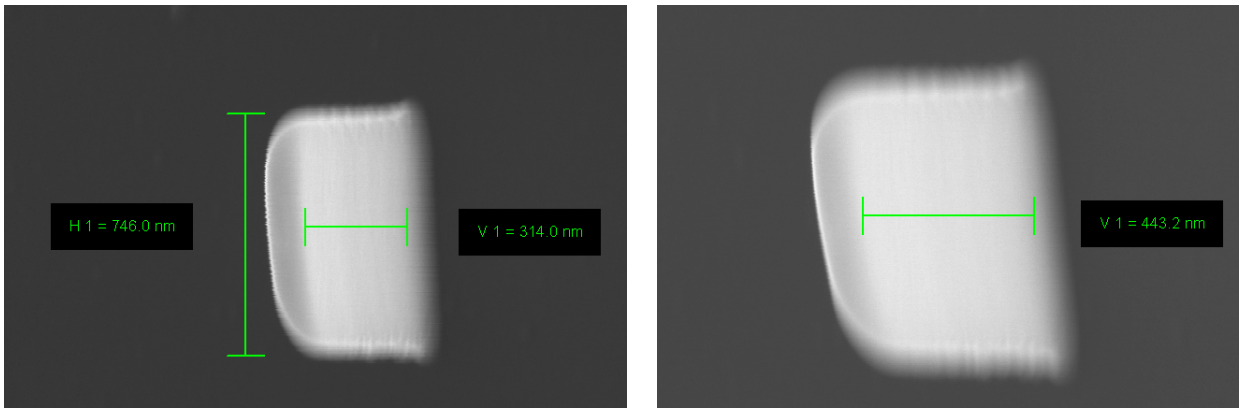


Figure 5.5: SEM image after deposition



(a) SEM image 20 tilt

(b) SEM image 45 tilt

Figure 5.6: SEM images of deposited Pt at different tilts

SEM image at 45^o tilt shows dimensions in $400nm$ range. Thus, thick Pt deposition is possible with FEBID.

5.3.2 Electrical characterisation of FEBID Pt

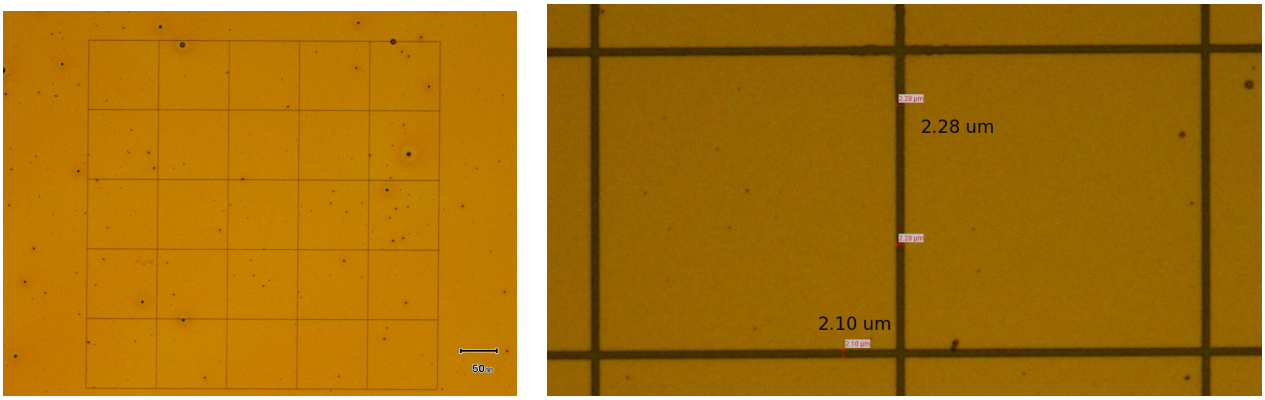
I-V characterisation of deposited Pt was done to estimate the current driven through the nano-deposition.Isolated pads of metal were fabricated.These pads were probed to characterise the Pt nano-depostion connecting the pads.

The process steps for the fabrication and characterisation of FEBID Pt.

1. Si wafer 4 inch 100 p-type

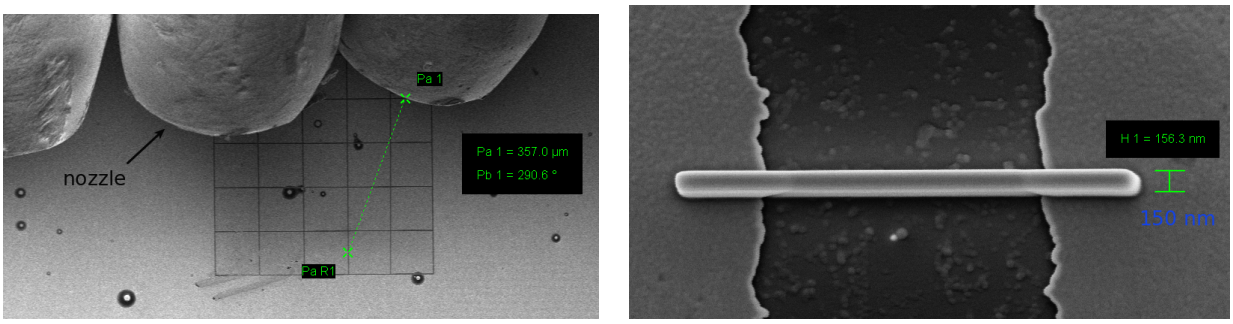
2. RCA clean
3. thin dry oxide growth(5nm)
4. chrome deposition(10nm)
5. gold deposition(100nm)
6. EBL for patterning isolated pads
7. gold wet etch
8. chrome wet etch
9. resist strip
10. SEM inspection of pads
11. Pt deposition using GIS
12. I-V characterisation

The following images are taken at different process steps during the fabrication.



(a) After EBL patterning (b) After gold,chrome etch(2um gap between pads)

Figure 5.7: Olympus images of probe pads patterning



(a) SEM image showing GIS nozzle (b) GIS deposited Pt

Figure 5.8: FEBID of Platinum

The precursor gas flows through the nozzle shown in fig 5.8:(a). The deposition parameters for Pt shown in fig 5.8:(b) are Accelerating voltage of 3 KV, number of loops - 1000, dwell time-100 us, step size-10 nm, magnification - 20K, WF - 5 um.

Electrical characterisation was done by probing the gold pads connected to the deposition. The non-linear behavior is attributed to the semiconducting carbonaceous composition in the deposited Pt[11] verified from the Energy dispersive X-ray analysis(EDAX) results.

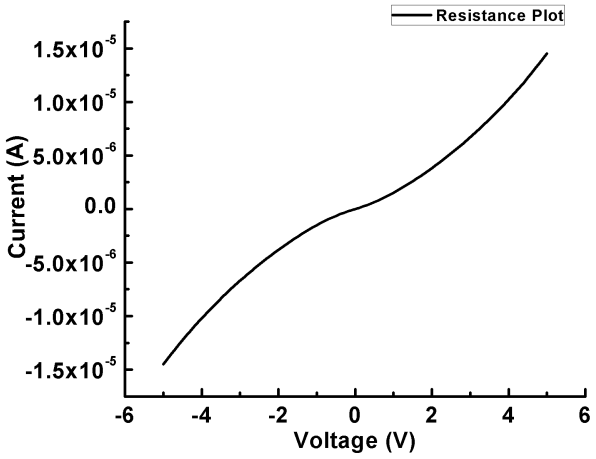


Figure 5.9: I-V charateristics of FEBID Pt

5.3.3 EDAX experiment for determining the composition of Pt

EDAX is used for determining the elemental composition of a specimen.In this technique,the area of interest is exposed to electron beam in a SEM setup and the emitted X-rays are analyzed to determine the elemental composition.

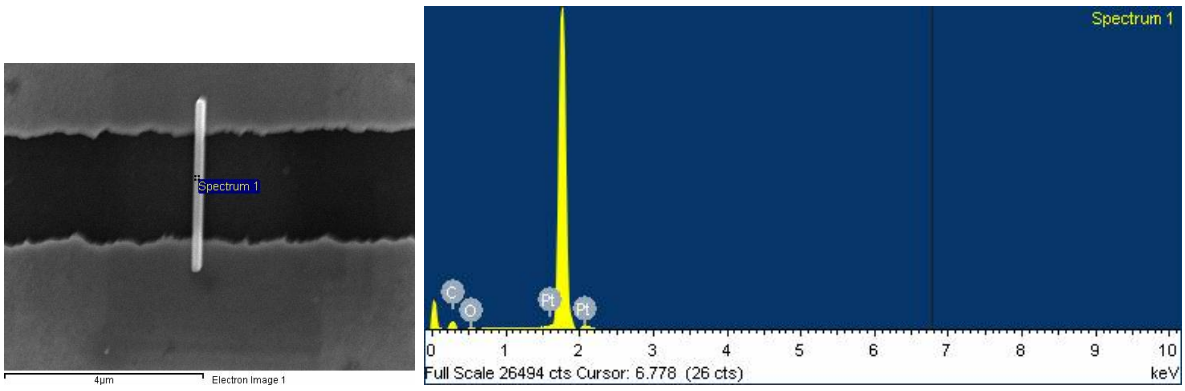


Figure 5.10: EDAX spectrum analysis

Element	Weight%	Atomic %
Carbon	34.68	76.53
Oxygen	9.60	15.91
Platinum	55.71	7.57

Table 5.1: Composition of GIS deposited Pt

5.4 Summary and Future Scope

FEBID technology gives the advantage of selective nano-scale deposition. Using this technology, Pt nanowire were deposited using $Me_3PtCpMe$ precursor. The depositions had nearly 50% carbon composition. The carbon content could be further reduced by parallel introduction of water precursor.

Chapter 6

Summary and Future Work

The Mix and Match lithography process which takes advantage of both optical and electron-beam lithography for patterning design with both nano features and features of micron dimensions is developed. It has better throughput in comparison to using only electron beam lithography for patterning designs having nano-features. This developed process is implimented for patterning gate in the fabrication of short-channel transistor. The process plan for fabricating RF oscillator circuit is reported and the fabrication results till gate level lithography are shown.The wafers need to be further processed for completing the circuit fabrication.

FEBID technology for nano-scale selective deposition is reviewed. Initial experiments for elctrical and compositional characterisation of Pt deposited using $Me_3PtCpMe$ precursor are done.Further experiments to reduce the carbon content in the deposited Pt by parallel introduction of water precursor, annealing the deposited Pt nanowire can be done.

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