Advanced Texturization Processes for Industrial Crystalline Silicon Solar Cells

A thesis submitted in partial fulfillment of
the requirements for the degree of

Doctor of Philosophy

by

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“To my family, teachers, colleagues and friends”

Approval Sheet

The thesis entitled **"Advanced Texturization Processes for Industrial Crystalline Silicon Solar Cells"** submitted by **Sreejith K. P.** (Roll No. 133076005) is approved for the degree of **Doctor of Philosophy**.

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Part of thesis are already published or under review in journals and presented at conferences as listed below.

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and

K. P. Sreejith, A. K. Sharma, S. Behera, S. Kumbhar, P. K. Basu and A. Kottantharayil, "Optimization of MACE Black Silicon Surface Morphology in Multi-crystalline wafers for Excellent Opto-electronic Properties", *IEEE 47th Photovoltaic Specialists Conference (PVSC)*, 2020, Calgary, Canada.

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Abstract

Implementation of diamond wire sawing (DWS) technique over multi-wire slurry sawing (MWSS) for cutting wafers from ingots was one of the significant steps that industry adopted for reducing the overall cost of PV technology in the last decade. DWS technique allows to produce wafers at a much cheaper rate due to its increased cutting rate, reduced kerf-loss and lower wire wear and breakage. DWS wafer surface is relatively polished, consist of thinner damage layer compared to multi-wire slurry sawn (MWSS) wafers. Also, 10-20 nm thin amorphous silicon (a-Si) layer is present on the DWS wafer surface, which hinders the wet texturing processes. Hence, the adoption of DWS wafers has resulted in urgent requirement of an industrial texturing process for both mono-crystalline silicon (c-Si) and multi-crystalline silicon (mc-Si) wafers.

Alkaline texturing process used in industry consists of two process steps; (i) a saw damage removal (SDR) step that removes the unwanted damages present on the as-cut wafer surface followed by (ii) uniform random pyramid texture generation utilizing the preferential etching properties of KOH solution. The uniformity and quality of pyramid formation heavily depends on the morphology and quality of wafers used. Hence, development of an SDR process that effectively removes the unwanted saw mark impressions and a-Si layer was the major challenge in processing DWS c-Si wafers. The previously reported SDR processes were either inefficient or expensive for industrial implementation. In this context, we proposed and demonstrated a novel alkaline texturing process; potassium hydroxide (KOH)-sodium hypochlorite (NaOCl) solution based SDR process followed by a high throughput KOH-isopropyl alcohol-potassium silicate solution based etching process for pyramid texturing of DWS c-Si wafers. The texturing process generates 2-5 μm sized textures and the weighted average reflectance (WAR) of textured samples were 13.1% and 2.3%, respectively before and after silicon nitride anti-reflection coating (ARC). The proposed texturing process is

cost-effective and can be easily integrated to any of the existing alkaline texturing tools. The chemicals used in our process are PV grade chemicals, which also eliminates additional safety and waste disposal concerns.

In contrast, a single step acid etching process was employed for both saw damage etching and texturing of mc-Si wafers in industry. Acid texturing requires thicker and uniform saw damage layer for uniform texture generation. This limited its applicability for DWS mc-Si wafers. Almost all of the methods reported as an alternative to acid texturing, either use expensive texture-additives or demand additional process steps that necessitate monetary investment. In this regard, we demonstrated an additive-free, energy-efficient acid texturing process and named it as NCPRE acid texturing process. The proposed texturing process uses hydrofluoric acid (HF)-rich acid solution for generating porous silicon structures, followed by a dilute KOH rinse to produce inverted scalloped textures. The surface reflectance and recombination properties of additive-free acid textured samples were comparable to conventional acid textured MWSS mc-Si samples. The additive-free acid texturing process developed using small footprint tools, was later demonstrated in three of the leading PV manufacturing units in India. When the demonstrations were conducted, PV manufacturing units were using expensive additive-based acid texturing process for solar cell production. Our additive-free process was performed efficiently in the production lines without compromising in process performance parameters such as material loss, process time and temperature. Comparable batch average efficiency values were achieved for the NCPRE additive-free and additive-based acid textured mc-Si cells. Most importantly, through a detailed cost analysis, we illustrated that ~60% of the chemical cost involved in preparing the acid bath can be cut down by choosing additive-free process over additive-based acid texturing.

Over the years, especially after the arrival of DWS wafers, metal assisted chemical etching (MACE) process gained significant attention for texturing industrial wafers; initially for mc-Si wafers and later as a universal process applicable for both mc-Si and c-Si wafers. MACE process allows to produce fine anti-reflective nano-structures called black silicon (b-Si) uniformly across the mc-Si wafer surface. However, b-Si textured wafers can not be directly used for solar cell fabrication because of the presence of high density surface defects. Hence, b-Si features are modified further prior to solar cell

processing and acid etching based processes are reported for generating nano-textures from b-Si features. However, the potential of such nano-textured surface over acid textured (iso-textured) surface is not completely investigated yet. Through a comprehensive analysis, we demonstrated that implementation of MACE nano-textures over iso-textures produce higher short circuit current by substantially lowering the surface reflection and ensures remarkable enhancement in fill factor due to lower series resistance. The contact formation mechanism in screen printed mc-Si solar cells, investigated using scanning electron microscopy, revealed that the elevated portions at the boundaries of the textures act as favorable sites for silver crystallite precipitation. A larger areal density of such sites is observed on the MACE nano-textured surface than in case of acid textured solar cells, which was responsible for much lower series resistance. The results suggest the potential for the application of MACE in the more popular mono-crystalline silicon cell technology for further reduction of contact resistance. Alternatively, MACE may be used to obtain similar contact resistance with lower amount of silver paste, compared to iso- and pyramid textured solar cells.

Recent studies demonstrated that anti-reflective (WAR in the range of 16%) inverted pyramidal nano-textures can be fabricated from MACE b-Si samples by advanced and expensive processes like RIE, which are not industrially viable in the present scenario. In this context, we developed a simple surface modification process by sequentially etching the MACE b-Si samples in HF-HNO_3 and dilute KOH solutions for the fabrication of random inverted nano-pyramid textures. Further, the optical losses in MACE inverted pyramid textured mc-Si solar cells and modules are estimated using SunSolve module ray-tracer simulator of PV Lighthouse. Our study established that adoption of MACE inverted pyramid texturing over acid texturing would enhance the total photo-generation in mc-Si modules by ~0.5% and the total photo-generation current density in mc-Si solar modules approaches 99.6% of that in random pyramid textured c-Si modules.

Advanced texturing methods like nano-wire and ordered inverted pyramid texturing promise better light harvesting efficiency than in conventional random pyramid and acid textures. However, fabrication of these textures require complex and expensive photo-lithography steps, which limits their application in industry. In this regard, we present preliminary experimental results on some of the lithography-free

process steps that are developed for the fabrication of nano-wires and regular inverted pyramids in the last part of the thesis. Relatively inexpensive processes compared to photo-lithography such as colloidal lithography, reactive ion etching and MACE are utilized for the fabrication of silicon nano-wires and inverted pyramid textures.

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Nomenclature

Al-BSF	Aluminum Back Surface Field
ALD	Atomic Layer Deposition
ARC	Anti Reflection Coating
a-Si	Amorphous Silicon
BPL	Biased Photoluminescence
BSRV	Back Surface Recombination Velocity
b-Si	Black Silicon
CCD	Charge Coupled Device
CL	Colloidal Lithography
CTM	Cell To Module
Cz	Czochralski
c-Si	Mono-crystalline Silicon
DRE	Damage Removal Etching
DWS	Diamond Wire Sawing
ECV	Electrochemical Capacitance Voltage
EMD	Electro-less Metal Deposition
EQE	External Quantum Efficiency
FF	Fill Factor
FOV	Field of View
FSRV	Front Surface Recombination Velocity
Fz	Float Zone
Ge	Germanium
G_P	Parallel Conductance
HP	High Performance
ICP	Inductive Coupled Plasma

IPA	Isopropyl Alcohol
IQE	Internal Quantum Efficiency
I_{SC}	Short Circuit Current
ITRPV	International Technology Roadmap for Photovoltaics
iV_{OC}	Implied Open Circuit Voltage
J_{MPP}	Current Density at Maximum Power Point
J_{SC}	Short Circuit Current Density
J_{0e}	Emitter Saturation Current Density
k	Extinction Coefficient
K	Boltzmann Constant
LBIC	Light Beam Induced Current
LED	Light Emitting Diode
LTO	Low Temperature Oxidation
MACE	Metal Assisted Chemical Etching
MCD	Minority Carrier Density
MWSS	Multi Wire Slurry Sawing
mc-Si	Multi-crystalline Silicon
n	Refractive Index
η	Power Conversion Efficiency
NSR	Nano Structure Rebuilding
PECVD	Plasma Enhanced Chemical Vapour Deposition
PEG	Polyethlene Glycol
PERC	Passivated Emitter Rear Contact
P_{MPP}	Power at Maximum Power Point
Por-Si	Porous Silicon
PL	Photoluminescence
PSG	Phosphosilicate Glass
PV	Photovoltaic
QSSPC	Quasi-steady State Photoconductance
QHM	Quine Hydrone in Methanol
R	Surface Reflectance
RIE	Reactive Ion Etching

R_S	Series Resistance
R_{Sh}	Shunt Resistance
R_{Sheet}	Sheet Resistance
SDR	Saw Damage Removal
SDE	Saw Damage Etching
SEM	Scanning Electron Microscopy
Si	Silicon
SR	Spectral Response
SRH	Shockley - Read - Hall
SRV	Surface Recombination Velocity
STC	Standard Testing Conditions
SWS	Slurry Wire Sawing
τ_{Aug}	Auger Lifetime
τ_{Bulk}	Bulk Lifetime
τ_{Eff}	Effective Carrier Lifetime
τ_{Rad}	Radiative Lifetime
TTV	Total Thickness Variation
V_{MPP}	Voltage at Maximum Power Point
V_{OC}	Open Circuit Voltage

Chapter 1

Introduction

Fossil fuels contribute to more than 70% of greenhouse gas emissions. Photovoltaic (PV) solar panels emerged as alternative to fossil fuel energy sources to bring off the increasing energy demand. The cumulative installed PV capacity was estimated to ~ 627 GW by the end of 2019, with new installations of ~ 115 GW in 2019 alone [1]. This corresponds to carbon dioxide (CO_2) emission saving of 720 million ton per year [1]. The current market share for crystalline silicon technology and thin film technology are about 95% and 5%, respectively and are expected to remain unchanged in near future as well [2]. In addition, the current annual production capacity of crystalline silicon cells and module panels was likely to have reached > 130 GW with the recent advances in process optimizations and with the implementation of passivated emitter rear contact (PERC) architecture over aluminum back surface field (Al-BSF) architecture in production lines [1]. Assuring continuous improvement in power conversion efficiency and reduction in production cost are the main challenges associated with crystalline silicon solar cells. The cost to performance factor is the key element, which decides the future of any new technology or process in PV industry. For instance, PERC architecture was opted over Al-BSF architecture because the anticipated gain in efficiency by sandwiching a thin passivation layer between back aluminum contact and silicon is significant compared to the cost involved in incorporating those process steps to the existing production lines.

Over the years, especially in the last decade, the performance of multi-crystalline silicon (mc-Si) and mono-crystalline silicon (c-Si) solar cells have improved significantly with the advancements in materials and process technology. As per the international

technology roadmap for photovoltaic (ITRPV-2020) results, average efficiency (η) of Al-BSF mc-Si and c-Si solar modules are in the range of 18.5% and 20%, respectively [2]. The η values are expected to reach 20% and 22.5%, respectively for mc-Si and c-Si modules in next 10 years due to the industrial adoption of PERC architecture and half cell interconnect etc. [2]. Use of thinner and large area wafers for solar cell fabrication and adoption of diamond wire sawing (DWS) technique for cutting thinner wafers from ingots were some of the major steps that industry have availed in the last decade for significantly reducing the cost for wafer production. DWS technique allows to produce thinner and better quality wafers at a much faster rate than conventional multi-wire slurry sawing (MWSS) (also known as slurry wire sawing (SWS)) technique [3, 4]. In addition, the kerf-loss and total thickness variation (TTV) for DWS wafers are significantly lower than SWS wafers.

Two different texturing schemes, commonly known as alkaline texturing and acid texturing, respectively are used for texturing c-Si and mc-Si wafers in industry. The former uses hot (80°C) dilute (nearly 2%) potassium hydroxide (KOH) or sodium hydroxide (NaOH) solution and the later uses a combination of hydrofluoric acid - nitric acid (HF - HNO_3) solution, respectively for generating random upright pyramid and inverted scalloped textures. Acid texturing is relatively cheaper and high throughput process compared to alkaline texturing. In addition, acid texturing process nucleates on surface defects and hence, does not require additional saw damage removal (SDR) process prior to texturing. Significantly lower amount of material (< 5 μm per side) is removed in acid texturing process, while alkaline texturing removes nearly 10-12 μm per side [5, 6, 7]. However, the anti-reflection properties of acid textured mc-Si wafers are significantly lower than alkaline textured c-Si wafers. The WAR values of alkaline textured c-Si and acid textured mc-Si wafers without and with anti-reflection coating (ARC) are in the range of 11-13%, 2-3% and 23-28%, 5-7%, respectively.

1.1 Thesis motivation

MWSS and DWS processes, respectively follow rolling - indenting model and ductile model for cutting the wafers from ingots [3, 4]. MWSS process introduces thicker and uniform saw damage layer across the wafer surface. In contrast, DWS wafers

posses relatively thinner and non-uniform damages, where surface defects are mainly distributed along the wire cutting direction. DWS wafer surface also contains non-uniform hard damage pits and crystal defects, which are difficult to remove by wet etching processes. Presence of thin 10-20 nm amorphous silicon (a-Si) layer is reported close to saw marks [8]. a-Si layers are reported to hinder the wet etching process. All these factors jointly make the texturing of DWS wafers extremely challenging compared to MWSS wafers.

For DWS c-Si wafers, an SDR process that removes the unwanted saw damages and wire impressions is essential to solve the wet texturing issues. Pre-etching in concentrated KOH or NaOH solutions, mixtures of HF-HNO_3 solutions, hydrochloric (HCl) acid - hydrogen peroxide (H_2O_2) solutions and HCl-HF solutions were some of the previously reported methods for DWS c-Si wafers [9, 10]. However, all of them were ineffective in completely removing the saw damages. In contrast, Chen *et al.* reported tetra-methyl-ammonium hydroxide (TMAH) solution based pre-etching process at relatively higher temperature (85-90 °C) for completely removing the saw damages [8]. However, the reported TMAH process had several disadvantages. It require an additional pre-cleaning processes prior to SDR. TMAH solution is expensive compared to other PV grade wet chemicals used in industry.

The wet texturing issues were more severe for DWS mc-Si wafers due to lack of thicker and uniform defect layer, which are essential for the nucleation of iso-texture formation [11]. Several alternative approaches such as sand blasting [12], vapor etching [13] and reactive ion etching (RIE) [14] were proposed for texturing DWS mc-Si wafers. However, all of them require additional equipment setting cost and cannot be directly implemented in existing production lines. Hence, PV manufacturing units continued to use acid texturing with the inclusion of texture additives for generating deeper and more uniform surface textures [2]. However, these expensive texture additives provide only a limited gain in performance. Hence, the cost advantage of using DWS is not fully utilized for mc-Si solar cell production.

The minimum reported WAR achieved by acid texturing is in the range of 22-24%, which is significantly higher compared to pyramid textured c-Si wafers. Most of the other efficient texturing schemes such as laser texturing and RIE, are expensive and low throughput processes compared to existing wet texturing schemes. Hence, de-

velopment of an industry viable, efficient, chemical texturing process for mc-Si wafers was essential for reducing the performance gap of c-Si and mc-Si solar cells. In addition, even though the alkaline texturing lower the surface reflectance to as low as 11-12% and 2-3% without and with ARC respectively, significant amount of material loss continued to be a concern. Hence, alkaline texturing may not be a viable option for next generation thinner wafers due to the mechanical stability and wafer handling challenges. In addition, use of an universal texturing process applicable to both c-Si and mc-Si wafers will eliminate the redundancy of using two different etch chemistry and texturing tools [15].

It is well known that the texture geometry influence all the three performance parameters; open circuit voltage (V_{OC}), short circuit current density (J_{SC}) and fill factor (FF) of solar cells. However, the influence of texture morphology and dimensions on optical properties after module encapsulation are not widely investigated yet. The optical losses in solar cells before and after encapsulation are significantly different mainly because of the parasitic absorption in glass and encapsulants. Hence, evaluation of texture morphology with respect to the optical losses after encapsulation is essential for deciding the potential of any new texturing process.

As discussed above, the wet chemical processes utilized in industry have several performance limitations. Hence there is a great interest to explore the other low-cost processes for the fabrication of advanced textures. Over the years, use of colloidal lithography as an alternate to expensive photo-lithography, RIE for directional etching and metal assisted chemical etching (MACE) for the fabrication of wide range surface features are reported. However, there is a requirement of investigating the potential application of such processes for the fabrication of advanced surface textures.

1.2 Organization of the thesis

This thesis contains 10 chapters. The introduction chapter begins by discussing the importance, current status and significance of cost to performance factor of PV panels. Further, a brief background on the emergence of DWS technique and its implications on existing wet texturing processes are presented. Subsequently motivation behind this work is elaborated. The other chapters are organized in the following manner.

In chapter 2, an introduction and road-map to different texturing methods used in industry for texturing c-Si and mc-Si wafers are presented. The chapter reviews some of the efficient texturing methods developed as an alternative to alkaline and acid texturing processes. The advantages, disadvantages and challenges in industrial adoption of these methods are detailed subsequently.

Chapter 3 begins with a review of DWS technique; its working mechanism, advantages, industrial road-map and finally, the wet texturing difficulty associated with DWS wafers. Alternative processes developed for addressing the texturing difficulties of DWS wafers are detailed subsequently. A separate section was dedicated for detailing the usefulness and advantages of MACE process and the chapter ends by summarizing the potential of MACE.

Chapter 4 details the process flow used for the fabrication of lifetime test structures and the theory behind some of the widely used measurement techniques for characterizing the lifetime structures and solar cells in this thesis.

Chapter 5 discuss about our novel texturing process developed for DWS c-Si wafers. The chapter provide an in-depth comparative analysis of the random pyramid textures obtained by novel texturing process in terms of opto-electronic properties. The performance parameters of novel textured c-Si solar cells are studied and benchmarked against the standard alkaline textured DWS and MWSS c-Si solar cells.

Chapter 6 presents our additive-free acid texturing process developed for DWS mc-Si wafers. The underlying reaction mechanism of HF-rich acid texturing is detailed in this chapter. The chapter provide detailed analysis of surface properties of different iso-textures obtained by varying the HF concentration in the acid texturing solution.

Chapter 7 provides the details about the industrial implementation of NCPRE additive-free texturing process. A detailed comparative analysis of performance parameters of additive-free and additive-based acid textured cells and the scope for efficiency enhancement is presented. In the end, chemical cost comparison of additive-free and additive-based acid texturing processes are presented to illustrate the potential of additive-free texturing in industrial environment.

Chapter 8 describes a low cost approach for the generation of black silicon (b-Si) surface features and inverted pit-like nano-textures, using the combination of MACE and acid etching. Detailed performance parameter analysis of nano-textured and iso-

textured mc-Si solar cells are conducted to demonstrate the potential of nano-texturing. The improved short circuit current due to lower surface reflection and enhanced fill factor values due to lower series resistance were measured for MACE nano-textured solar cells. Further, the contact formation in iso-textured and nano-textured surfaces are investigated to probe the cause in reduced series resistance.

Chapter 9 describes a low cost approach for inverted nano-pyramid texture fabrication by MACE process. The optical and electronic properties of inverted pyramids are studied against the MACE nano-textures (discussed in Chapter 8) and iso-textures. Further, the optical loss analysis of inverted pyramid textured cells before and after module encapsulation were estimated using SunSolve ray tracer simulator of PV Lighthouse and interesting observations are presented.

Chapter 10 summarizes some of the lithography-free and cost-effective methods for the fabrication of advanced textures such as nano-wires and inverted pyramid textures on c-Si wafers. The process details and initial characterization (mainly SEM images and in some case reflectance also) of such textures are presented.

Chapter 11 concludes and details an outlook on the future directions of this work.

Chapter 2

Literature Review on Texturing of Industrial Silicon Wafers

This chapter reviews different etching processes used for texturing both c-Si and mc-Si wafers. The chapter is divided in to three sections. In the first section, we present different alkaline texturing processes proposed for c-Si wafers. This includes a review of both SDR as well as random pyramid texturing processes. In the second section, the evolution of acid etching process as the most feasible process for texturing industrial mc-Si wafers is discussed. The light trapping properties of acid textured mc-Si wafers were significantly lower than the alkaline textured c-Si wafers. Hence, there were several efforts made towards developing efficient texturing processes that lowers the surface reflectance of mc-Si wafers to as low as that of alkaline textured c-Si wafers. The final section of this chapter briefly reviews those efforts.

2.1 Alkaline texturing of c-Si wafers

From the beginning of c-Si solar cell production, alkaline solution based etching process was the dominant method for texturing c-Si wafers. Hot dilute NaOH or KOH solution selectively etches the <100> planes over <111> planes, resulting in generation of random upright pyramids unformly across the <100> surface. The dimensions, uniformity and substrate coverage of pyramids heavily depends on as-cut wafer surface morphology. Solar grade c-Si wafers are produced by slicing the Czochralski (Cz) grown silicon ingots. The carbon contaminants from Cz crucible and organic con-

taminants from wafer grinding and slicing processes are present at the wafer surface. Inadequate removal of organic and inorganic contaminants adversely affect the texture formation and V_{OC} of solar cells. Hence, a pre-texturization process namely saw damage removal (SDR) or saw damage etching (SDE) is used for removing both organic and in-organic surface contaminants from as-cut wafers.

2.1.1 Saw damage etching (SDE) process for c-Si wafers

Concentrated KOH, NaOH or TMAH solutions are commonly used for saw damage etching. However, KOH or NaOH solutions are preferred over TMAH solution due to the cost and safety (chemical handling) advantages. The chemical reaction involved with all three etching solutions remain the same and is as follows,

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2 \tag{2.1}$$

As seen in equation 2.1, the concentration of $2OH^-$ and H_2O play vital role in the mechanism of Si etching. The etch rate of <100> Si wafers for varied KOH concentrations at 72°C is shown in Figure 2.1 [16]. Initially the etch rate increases with increase in OH^- in the KOH solution and then reduces with further increase in OH^- because of decrease in H_2O content in the etching solution. Both etch rate and anisotropy of Si etching depends on process temperature and KOH concentration. For instance, the anisotropy (etch rate ratio between (100):(111) planes) of Si etching in KOH solution are in the range of 100:1 and 30:1, respectively at room temperature and 100°C. Similarly, the etch rate is changed from 0.1 nm/sec to 200 nm/sec for the variation in temperature from room temperature to 100°C. Hot (72-80°C) concentrated (6-10%) KOH or NaOH solutions are reported to be best suited for SDE of wire-sawn wafers. Under these conditions, etching process is isotropic in nature and the etch rate is in the range up to 2-4 μ/minute (min) [6, 17]. This corresponds to only 2-3 min of processing in industry. However, SDE using concentrated alkaline solution has several disadvantages. Firstly, etching of Si in KOH or NaOH are highly non-uniform and rigorous. PV manufacturing units currently use thin (160-180 μm) and large area (6 inch) wafers for solar cell production and the thickness and size of wafers are expected to get thinner and larger, respectively. Hence, any additional loss of Si material apart from the damaged layer may lead to the wafer breakage [18]. In addition, non uniform etching or inadequate damage removal

often results in either no pyramid generation or in non-uniform pyramid generation at different locations of the wafer surface area [19, 20, 21]. Also, the traces of carbon contaminants and inorganic contaminants such as oil, grease and slurry may also inhibit the effective removal of saw damages and nucleation of pyramid generation, resulting poor texture quality. For removing the organic contaminants, standard cleaning 1 (SC-I) solution consisting of ammonium hydroxide (NH_4OH) and H_2O_2 is used [22]. However, this is method is prolonged, hazardous and require additional processing steps compared to alkaline based etching processes.

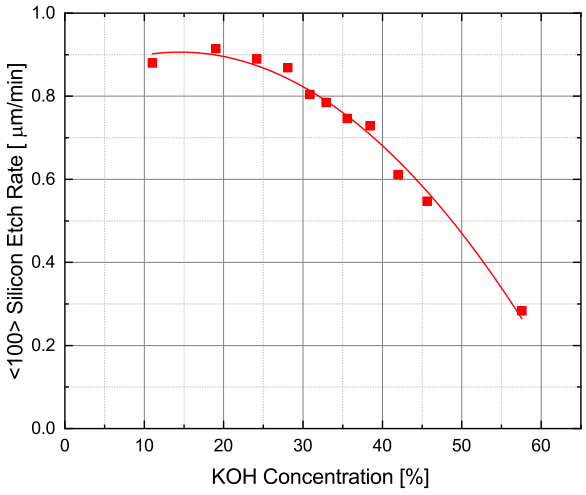

Figure 2.1: Variation in etch rate of <100> Si sample with KOH concentration. Data reproduced from [16].

In this regard, Gangopadhyay *et al.* proposed hot sodium hypochlorite (NaOCl) solution for removing organic contaminants present in the as-cut wire-sawn silicon wafers [19]. NaOCl based pre-treatment process was carried out for 15 min at 80°C and the wafers subsequently underwent a standard alkaline texturing (both SDE and pyramid texturing) process. The SEM images of alkaline textured c-Si wafers without and with NaOCl pre-treatment are shown in Figure 2.2. It can be clearly seen that, the absence of an effective etching method for removing the organic layer has significantly inhibited the nucleation of pyramid texturing process resulting in bad texture quality. The η difference of solar cells without and with NaOCl pre-treatment was nearly 6%. However, this approach does not solve the issue of higher etch rate and non-uniform etching as the proposed approach also use conventional NaOH based etching process

for SDE (after NaOCl pre-treatment). In addition, embedding an additional process is always a challenge in industry as it not only increase the cost of production, but also impacts the production throughput.

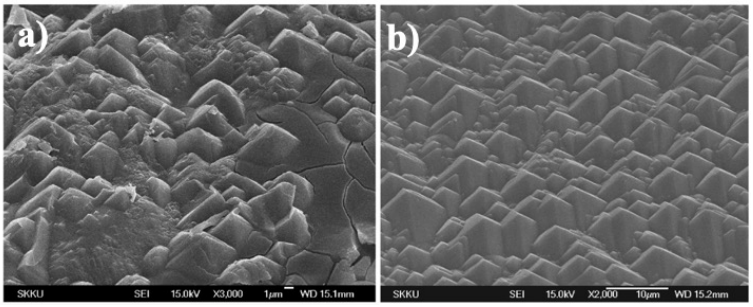

Figure 2.2: SEM images of pyramid textured c-Si surface (a) without and (b) with NaOCl pre-treatment [19].

The reaction chemistry of hot (80°C) NaOCl solution with Si is as follows,

$$NaOCl \leftrightarrow Na^{+} + OCl^{-} \tag{2.2}$$

$$2OCl^{-} + H_2O \leftrightarrow HOCl + OCl^{-} + OH^{-} \tag{2.3}$$

$$2OCl^{-} + Si \leftrightarrow SiO_2 + 2Cl^{-} \tag{2.4}$$

$$Na^{+} + OH^{-} \leftrightarrow NaOH \tag{2.5}$$

NaOCl at higher temperature dissociates to form hypo-clorous (OCl^{-}) ions (equation 2.2), and oxidize Si to form silicon dioxide (SiO_2) (equation 2.4). The oxidation properties of hot NaOCl was responsible for organic contaminant removal reported by Gangopadhyay *et al.* [19]. In addition, equation 2.5 indicate the formation of NaOH and this implies that hot NaOCl solution can be potentially used for SDE of Si wafers. On a related note, Basu *et al.* demonstrated the application of hot NaOCl solution for SDE by removing ~ 3 μm of saw damage layer per side in 10 min [23]. However, average etch rate of only 300 nm/min was observed for Si in NaOCl solution, which was significantly lower for industrial applications. The oxidation process (shown in equation 2.4) is responsible for the lower etch rate as SiO_2 layer act as a mask for Si etching.

Basu *et al.* improvised the above process further by using the combination of NaOCl and concentrated alkaline solution in the ratio of 1:3 for SDE. Moderate and

controlled silicon etch rate of ~ 900 nm/min was reported for NaOCl-NaOH solution , in comparison with higher (2-3 μm/min) and lower (300 nm/min) etch rates of NaOH and NaOCl solutions, respectively [20, 23]. The performance parameters of solar cells fabricated on modified SDE process with NaOCl-NaOH solutions were comparable to two step SDE (NaOCl pretreatment, followed by NaOH SDE) developed by Gangopadhyay *et al*. Importantly, the NaOCl - KOH SDE process can be transferred to industrial production lines, as inclusion of low-cost NaOCl overcomes the disadvantages of existing alkaline based SDE process (without disturbing the production throughput), and ensures the organic contaminant removal from the wafer surface.

2.1.2 Pyramidal texturing of c-Si wafers

The texturing of Si wafers in alkaline solutions is based on anisotropic or preferential etching of (100) planes over (111) planes. Dilute alkaline solution at lower temperatures exhibit very high etch anisotropy of >100 [16]. However, etch rate of Si in such solutions are as low as 10 nm/min [16]. Hence, dilute alkaline solution at higher process temperature (80°C) is used so that moderate etch rate and anisotropy is assured while texturing the c-Si wafers. Many studies co-related the variation in etch rate for (100) and (111) planes in low concentration alkaline solution to dangling bond density of each Si unit cells, where (111) and (100) planes, respectively have one and two dangling bonds each [24, 25]. This imply that two back bonds are only needed to break for (100) plane whereas three back bond breakage is essential for (111) plane for Si etching. Hence, controlled etching of (100) plane results in exposure of (111) and lower etch rate of this (111) plane, thus result in formation of up-right pyramid textures.

Dilute (~ 2%) KOH (NaOH) - isopropanol (IPA) solution is commonly used in industry for pyramidal texturing of c-Si wafers [6]. Even though the KOH - IPA based etching process is well established and used in industry for several years, it has several disadvantages especially in the choice of chemicals used. There were several attempts to replace both KOH (NaOH) and IPA in the texturing bath and based on this, the pyramidal texturing process can be classified in to three major groups. First group use the combination of KOH or NaOH and IPA as texturing solution, which is commonly followed in industry. In the second group, KOH or NaOH is replaced with other chemicals and IPA may or may not be used for solution preparation. Third group of

texturing process does not use IPA at all in solution preparation. The details of all three groups are separately discussed in the following subsections with their advantages and disadvantages.

KOH/NaOH-IPA based pyramidal texturing process

The chemical reaction of alkaline texturing can be summarized as follow,

$$Si + 2KOH + H_2O \rightarrow K_2SiO_3 + 2H_2 \tag{2.6}$$

One of the bi-product of the texturing process is the formation of hydrogen (H_2) bubbles, which act as localized mask against the alkaline etching process and results in non-uniform texture generation. IPA is added to improve the wettability of Si surface for preventing the adhesion of H_2 bubbles on the surface [6]. Constant removal of H_2 bubbles from Si surface maintain consistency in texturing process. Amount of IPA required in the texturing bath is proportional to the concentration of KOH and hence a fixed amount of KOH and IPA are regularly dosed to the texturing solution for maintaining the concentration of chemicals for texturing multiple batches. However, IPA usage has several disadvantages. IPA is expensive and the boiling point of IPA is less than 80°C, which leads to IPA evaporation [6]. Hence, larger consumption of IPA adds significantly to the cost per watt-peak value of solar cells.

As per equation 2.6, increase in concentration of reaction by-product potassium silicate (K_2SiO_3) reduces the active concentration of KOH in the texturing solution. This substantially reduces the etch rate and increases process bath stability [26]. Singh *et al.* reported that an established IPA - KOH alkaline texturing process was not repeatable for more than two or more batches due to lower etch rate [27]. Similarly, Basu *et al.* reported longer process time for pyramid generation for second batch of wafers and observed end of texture bath stability after only two consecutive KOH - IPA texturing process. Addition of crushed or broken pieces of Si wafers in to solution prior to texturization for pushing concentration of both reactants and products (equation 2.6) to much more stable process window is another method followed for processing multiple batches of wafers. Addition of Si pieces saturates the texturing solution by increasing the Si or silicate concentration [6]. However, this approach is challenging especially in industry due to the dynamic nature of chemical process shown in equation 2.6.

In this context, Basu *et al.* reported the use of K_2SiO_3 as an additive to the texturing bath for increasing the bath stability and controlling the chemical reaction [6]. In such a case, relatively lower concentration of KOH (1.4%), less H_2 bubbles formation and thereby lower consumption of IPA were achieved. The IPA consumption and bath lifetime, respectively were nearly three times lower and six times higher for K_2SiO_3 additive-based alkaline texturing process than standard alkaline texturing process.

IPA-free texturing process

IPA being expensive, there were attempts to develop IPA-free alkaline texturing process. Sun and Tang proposed a combination of NaOCl and ethanol instead of NaOH - IPA solution for generating smaller pyramid textures of 2 μm height [28]. Authors reported an excellent WAR of 10.8% for NaOCl - ethanol textured samples in comparison with 11.9% reflective standard NaOH textured samples for the wavelength range of 400 - 1000 nm. The process duration for generating uniform textures were also significantly lower (15 min) in that approach. However, cost, safety and handling aspect of hot ethanol solution is a challenge, which makes the process industrially inconvenient. On a similar note, Birman *et al.* proposed use of cyclohexanedial (CHX) instead of IPA as the boiling point of CHX (> 250°C) is significantly higher than the temperature at which texturing process is carried out [29]. Only 10 min of texturing using KOH - CHX solution at 90°C has produced uniform and smaller textures with size in the range of 2-4 μm. However, similar to ethanol, cost and chemical handling were the major drawbacks of this method as well. Addition of organic texture additive to the KOH solution is another common practice reported for eliminating the IPA usage [30]. Higher boiling point and lower flammability of texture additives over IPA offers better process window, allows higher temperature process and assures high etch rates (as high as 1.2 μm/min) [30]. Some of the texturing equipments suppliers like Stangal GmbH and Rena GmbH and chemical providers like GP solar and Dow chemical have also released IPA-free texture additives. However, the cost of these additives are significantly higher than silicate additives.

NaOH/KOH-free texturing process

Several efforts were made to replace NaOH/KOH based texturing solutions for avoiding contamination effects of sodium (Na) and potassium (K) on solar cell performance. However, most of them use IPA for improving the lateral uniformity, which provides no cost advantages over KOH/NaOH - IPA based processes. Merlose *et al.* utilized TMAH solution instead of KOH for pyramidal texturing [31]. However, TMAH has lower etch rate for Si etching and is expensive compared to KOH. Gangopadhyay *et al.* proposed use of tribasic sodium phosphate (Na_3PO_4, $12H_2O$) instead of NaOH that can lower the IPA consumption [11]. Authors reported that Na_3PO_4, $12H_2O$ readily hydrolyzes in water and act as active surface agent for the nucleation of pyramids requiring minimal consumption of IPA [11]. Similarly use of hydrazine monohydrate (N_2H_4, H_2O) and sodium carbonate/bicarbonate (Na_2CO_3/$NaHCO_3$) based texturing processes were also reported as an alternate to standard alkaline texturing process [32]. However, industrial adoption of these processes were limited due to the well established process window and cost-effectiveness of standard KOH/NaOH - IPA processes.

2.2 Acid texturing process for mc-Si wafers

2.2.1 History and basic mechanism

In the initial days, industrial mc-Si wafers were textured, basically saw damage etched in alkaline based (KOH or NaOH) solution. The chemical reaction of KOH with Si can be summarized as,

$$Si + 2KOH + H_2O \rightarrow K_2SiO_3 + 2H_2 \tag{2.7}$$

However, the reaction kinetics are highly anisotropic and selective with Si crystal plane orientations. The crystallographic planes close to <100> etches faster and crystallographic planes near to <111> etches very slowly in KOH solution. This leads to the formation of grain dependent irregular and shallow texture on mc-Si wafers as seen in Figure 2.3 (a) [17]. Non-uniform textures lead to non-uniform surface reflectance distribution across the wafer surface [17, 33]. Faster etch rates can be obtained by increasing the KOH concentration in the texture solution. As per equation (2.7), increase in KOH concentration leads to the increase in hydrogen (H_2) and potassium silicate

(K_2SiO_3) concentrations. Increased concentration of H_2 bubbles acts as localized masks during the etching process, which results in non-uniform etching and non-uniform texture generation. Drastic increase in K_2SiO_3 concentration saturates the texturing solution and suppresses the preferential anisotropic etch behavior of the chemical reaction. Hence, increased KOH concentration in the texturing solution pushes the process window of chemical reaction towards the isotropic etching, resulting in undesired surface undulations [6]. This condition does not contribute to texture generation even in <100> grains. Hence, concentrated alkaline treatment results in much higher surface reflectance distributions across the mc-Si wafer surface irrespective of grains, and grain boundaries and produce similar range of WAR values as that of polished Si wafers. There were also attempts to add additives to alkaline solution to improve the texture quality [17, 19, 34]. For instance, Gangopadhyay *et al*. demonstrated an enhancement in η of ~1.4% (absolute), for additive-based NaOH etching over conventional alkaline texturing. Sodium hypochlorite (NaOCl) solution was added as an additive in that case [19]. The addition of NaOCl significantly improved the surface smoothness of alkaline textured mc-Si surface as seen in Figure 2.3 (b), and thereby fill factor (FF) and open circuit voltage (V_{OC}) values. However, the WAR (after ARC) and I_{SC} values of the mc-Si cells were improved only by ~ 1% (absolute) and ~ 2% (relative), respectively and the reported WAR and I_{SC} values were still much higher than that of alkaline textured c-Si wafers and cells used in industry. As per literature, texturing of mc-Si wafers by alkaline texturing is limited by its anisotropic etching behavior.

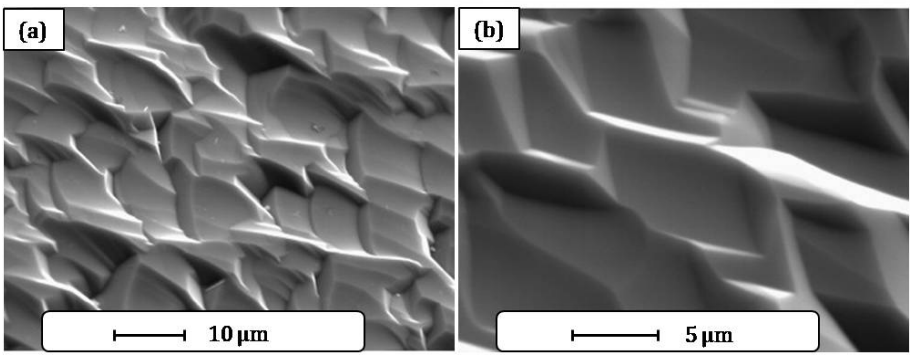

Figure 2.3: Top down SEM images of mc-Si wafers textured using (a) NaOH solution and (b) NaOCl-NaOH solution. Adapted from [34].

Hence, researchers started to explore industry viable isotropic Si etchants for tex-

turing mc-Si wafers to get the better of the strong material dependency observed in case of alkaline based etching. In 1997, Einhaus *et al*. [35] first reported a low-cost chemical texturing process using isotropic HF - HNO_3 acid solution for texturing mc-Si wafers. In their study, the morphological and optical properties of acid textured wafers were examined and the performance of the acid textured cells were compared with alkaline textured mc-Si cells. The acid texturing solution compositions were optimized to achieve uniform and deeper inverted pit-like textures with a diameter of about 10 μm across the wafer surface area irrespective of grains. The acid textured and alkaline textured mc-Si wafers had a WAR values of 24.5% and 30.1%, respectively. After titanium oxide (TiO_2) ARC deposition, the respective WAR values were reduced to 13.4% and 15.4% for acid textured and alkaline textured mc-Si wafers. An impressive enhancement in short circuit current density (J_{SC}) by 1.5 mA/cm^2 (5% relative) was achieved for acid textured mc-Si cells over conventional alkaline textured cells. The corresponding V_{OC} values of the cells were 600.9 mV and 597.6 mV for acid textured and alkaline textured cells, respectively. Additional 3% in increment (without considering the 2% gain in WAR after ARC) in J_{SC} and 3.2 mV enhancement in V_{OC} were attributed to the better passivation properties of acid textured surfaces over alkaline etched samples. Hence, the application of isotropic etching of Si in HF - HNO_3 solution for texturing mc-Si wafers gained immense industrial attention due to its simplicity, cost-effectiveness, and improved optical and electronic performance in comparison with alkaline texturing. The basic chemistry of Si etching in HF - HNO_3 solution, the optimization efforts carried out prior to industrial adoption and road-map of acid texturing process in industry are discussed in detail in the following subsections.

2.2.2 Reaction chemistry of acid texture process

Si etching in HF - HNO_3 solution can be explained by a hole-initiated mechanism [36, 37]. The oxidizing agent HNO_3 inject holes into the bulk of silicon. The mechanism of this process and the identity of the nitrogen intermediates involved are still uncertain. Different studies proposed various intermediates like nitrogen oxides, nitrous acid (HNO_2), nitrosonium ion (NO^+), dinitrogen trioxide (N_2O_3), trinitramide [$N_4O_6^{2+}$] etc., as the key intermediate formed during the oxidation of Si [38, 39, 40, 41]. The hole injected to the bulk diffuses to the Si surface. The presence of a hole in the valence band

of Si makes Si-Si bonds weaker. A nucleophilic addition of F^- occurs to the electron deficient Si which provides an electron to the conduction band. The newly formed Si-F bond polarizes the surrounding Si-Si bonds which facilitates further nucleophilic addition and breaking of Si-Si bonds as shown in steps 3 and 4 of Figure 2.4. Series of nucleophilic addition and Si-Si bond breaking furnishes the trifluorosilane ($SiHF_3$) intermediate which in turn converts to silicon hexafluoride (SiF_6^{2-}) in the solution as shown in Figure 2.4 [42].

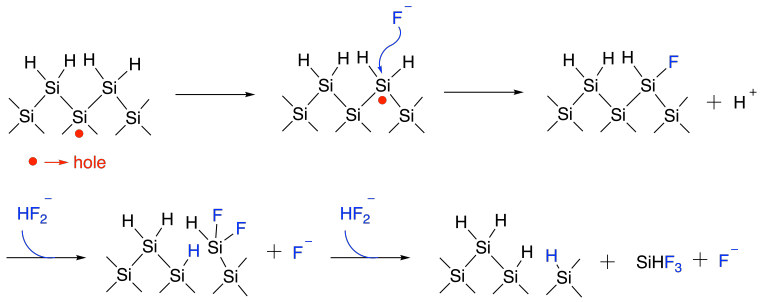

Figure 2.4: Mechanism of Si etching in HF-HNO_3 solution.

This etching process and removal of surface silicon continues until the surface features reach nanoscale. As the features reach nanoscale, the band gap increases. The electrons in the confined nanostructures possess higher kinetic energies. Hence higher energies are required to remove one electron and generate a hole. As a result of this quantum confinement, etching process stops when the surface features reach nanostructure level [43, 44, 45].

2.2.3 Application for low-cost mc-Si solar cells

The lower material cost of mc-Si wafers compared to c-Si wafers resulted in steady increase in the market share of mc-Si wafer based solar panel installation in the late 1990s and in early 2000 [46, 47]. As per the available literature, global installation of mc-Si based solar panels reached above 50% from less than 10% in a span of just 5-10 years during the above stated period [48, 49]. However, the performance of the mc-Si cells was limited in comparison with c-Si cells mainly due to the unavailability of an efficient texturing scheme for mass production. Though the acid etching process was reported to be an effective method for texturing mc-Si wafers, its industrial applicability was a major concern at that time because of several reasons. Very high etch rate up to 50 μm/min,

inconsistent etch rate in processing batch of wafers, lower throughput and lifetime of the acid bath, unavailability of an effective control mechanism for the excessive heat generated during the exothermic acid etching process, in-line system compatibility, difficulty in chemical disposal, low mechanical strength and higher breakage rate of wafers after texturing were some of the major concerns.

Chemical processes with higher etch rates are generally preferred for industrial scale manufacturing as large number of wafers can be textured in a short span of time. However, exceedingly high etch rates results in process control difficulties. Hence, it is important to achieve moderate and controllable etch rates consistently over a batch of wafers. Nishimato *et al.* achieved controlled reaction kinetics for acid texturing process without any compromise on the texture surface morphology and adverse impact on performance by using certain catalytic agents [50]. Low-ionizing acids such as phosphoric acid (H_3PO_4) and acetic acid (CH_3COOH) were tried as the catalytic agents for the controlled texturization process. mc-Si wafers were textured in HF:HNO_3 (12:1) solution without and with the additives and the surface morphologies were compared as shown in Figure 2.5. An etch rate of $\sim$ 50 μm/min was observed without any additive. The addition of a moderate amount of CH_3COOH (12:1:2) fairly controlled the etch rate and similar surface texture features as that of additive-free process were observed. However, a higher amount of CH_3COOH addition adversely influenced the morphology of surface textures, resulting in highly reflecting flatter textures (see Figure 2.5 (c)). Addition of H_3PO_4 as a catalytic agent also helped to control the etch rate with surface texture morphology and dimensions (Figure 2.5 (d-f)) similar to the additive-free processed one (Figure 2.5 (a)). The etch rate was effectively controlled in the range from 50 μm to 10 μm by altering only the H_3PO_4 concentration. H_3PO_4 based acid textured cells has resulted in 1 mA/cm^2 higher J_{SC} in comparison with alkaline textured mc-Si solar cells. However, no further studies were found on H_3PO_4 based acid texturing process. On the other hand, the role of CH_3COOH in acid etching of Si wafers has been widely investigated [51, 52, 53, 54]. In line with Nishimoto *et al.* [50], Kim *et al.* also observed the formation of smoother surface textures with higher reflectance with the addition of CH_3COOH to the HF-HNO_3 etch solution [51]. The WAR values were 5.62%, 6.84%, and 7.05%, respectively for acid textured, alkaline etched, and CH_3COOH based acid textured mc-Si samples after ARC deposition in their

case [51]. Hence, the use of CH_3COOH adversely affects the light trapping properties of acid textured wafers and hence, is not used for texturing applications.

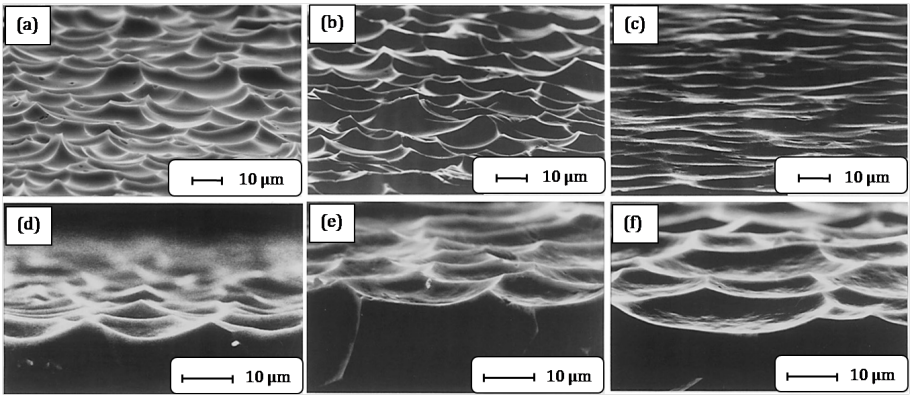

Figure 2.5: The cross-sectional SEM images of mc-Si wafers textured using an acid solution comprising of; (a) HF, HNO_3 (12:1) solution only, (b) and (c) HF, HNO_3 and CH_3COOH solution in the ratio of 12:1:2 and 12:1:12, respectively, and (d), (e) and (f) HF, HNO_3-H_3PO_4 solution in the ratio of 12:1:3, 12:1:9 and 12:1:12, respectively. Adapted from [50].

On a related note, Hauser *et al.* developed a low-temperature (8-10°C) acid etching process for texturing mc-Si wafers, which proceeds with controlled etch rates [55]. Along with lower and controlled etch rates [41, 56], low-temperature acid etching has several reported advantages such as lesser heat generation during the acid process [41], higher process bath stability, and horizontal etching (in-line system) compatibility [55, 57] compared to room temperature acid texturing processes [35, 50]. No additives (e.g. H_3PO_4 or CH_3COOH) were used in the HF-HNO_3 acid solution in this method. This reduces the chemical cost involved in preparing the texture bath, simplifies both chemical disposal and solution mixing processes. The acid texturing process conditions were optimized to achieve an etch depth of 4-5 μm for which the V_{OC}, J_{SC} and η values of acid textured cells were maximum as shown in Figure 2.6 (a). Lower etch depth (< 4 μm) has resulted in significant emitter recombination leading to poor V_{OC} and J_{SC} values whereas higher etch depth (> 5 μm) resulted in larger surface area textures having higher surface reflection (lower J_{SC}). An optimal etch depth of only 4-5 μm (per side) assures better mechanical strength and lower breakage rate for mc-Si wafers during further processes like high temperature emitter diffusion and metalization. Acid textured mc-Si cells and modules generated an additional J_{SC} of 2 mA/cm^2 (4.0%

relative) and I_{SC} of 0.21 A (4.2% relative), respectively in comparison with alkaline textured cells and modules. In similar studies, McDonald *et al.* and Gangopadhyay *et al.* also reported an improved J_{SC} of 1 mA/cm^2 (3.3% relative) and 2 mA/cm^2 (8.0% relative), respectively for acid textured samples over alkaline textured cells [5, 58]. Similarly, McDonald *et al.* reported ~ 1.5 mA/cm^2 (5.1% relative) improvement in J_{SC} after encapsulation for acid textured cells over alkaline textured mc-Si modules.

Non-uniform etching and formation of deep grooves in acid texturing can soften the mechanical stability of textured wafers [35, 59]. However, Geipel *et al.* reported that acid textured mc-Si solar panels have almost 35% (relative) lesser breakage rate than that of alkaline textured panels [60]. Fracture force test and twist displacement test (up to wafer breakage) conducted by Arumughan *et al.* later confirmed better mechanical stability of acid textured wafers over as-cut and alkaline textured wafers [61]. Arumughan *et al.* also reported that the wafer breakage rate of acid textured mc-Si samples remained almost unchanged even after the high temperature processes used for buried contact solar cell fabrication through fracture force and twist displacement tests [61]. Significant improvement in performance parameters at both cell level and module level (before and after module encapsulation) with adequate mechanical stability expedited the industrial adoption of acid texturing.

Together with RENA GmbH, Hauser *et al.* developed an in-line small foot print (8 m^2) acid etching system with a throughput of ~ 600 wafers per hour for texturing large area mc-Si wafers [57]. Authors conducted three sets of experiments by processing 7000, 10000 and 4000 wafers, respectively for simulating the production conditions of the newly designed acid texturing tool. Manual dosing was used to maintain the concentration of chemicals in the bath. In the first trial, the long term process stability of the acid solution was established by recording the WAR values of 7000 acid textured wafers and only a minor variation of ±1.5% as shown in Figure 2.6 (b) was noticed. In the second trial, the lifetime of acid bath was examined by continuously etching 10000 mc-Si wafers with an etch rate of ~ 3 μm/min. 10000 wafers were processed in 60 hours. In the final trial, manual dosage of chemicals was adjusted to maintain the overall concentration of chemicals constant in the texturing bath and nearly 4000 wafers were etched in 24 hours without major variation in process parameters as shown in Figure 2.6 (c). Through these three trial runs, the larger process window

of acid texturing process in industrial in-line tool was confirmed, favorable for large scale production. In addition, in-line acid textured mc-Si cells consistently recorded 6% (relative) higher I_{SC} values compared to alkaline textured cells in industry (refer Figure 2.6 (d)). Authors reported that acid texturing method using an in-line texturing system have been commercialized and two of the industrial acid etching tools with a throughput of 1800 wafers/hour have been sold to PV manufacturing units by then. As per the literatures/reports, acid texturing process was used for texturing mc-Si wafers in industry for the first time in 2003-2004. Currently, there are industrial in-line acid texturing tools available from RENA, Schimid and Singulus for texturing mc-Si wafers [62, 63, 64]. The minimum average throughput of these tools is around ~3500 wafers per hour. The average lifetime of acid texturing bath is now around 10 days with continuous dosage of chemicals.

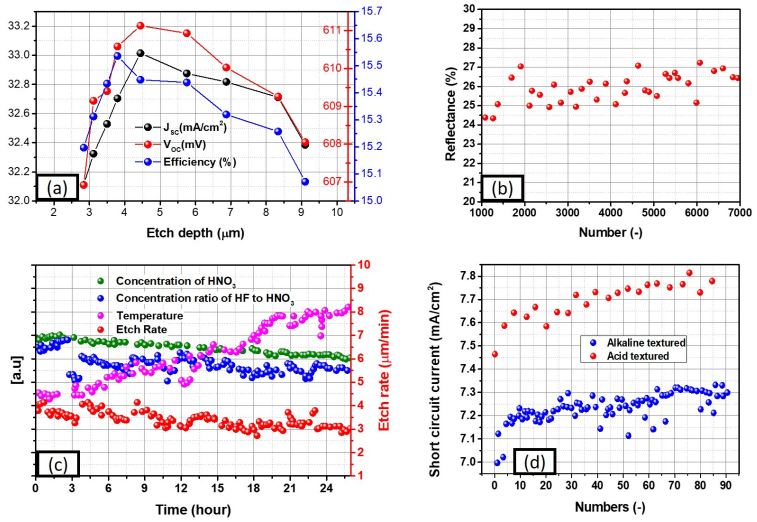

Figure 2.6: (a) Variation in V_{OC}, J_{SC} and η values of acid textured screen printed mc-Si cells with varied etch depth. (b) Reflectance variation of 70000 mc-Si wafers after continuous acid texturing, (c) recorded process parameter variation (etch rate, solution composition, and process temperature) in acid texturing process used for texturing 4000 wafers (d) I_{SC} value distribution of alkaline textured and acid textured neighboring solar cells fabricated in industry. Data reproduced from [55] and [57].

The size of the inverted pit-like texture formed after acid texturing was in the range of 10 μm in all previously reported articles [5, 55]. Smaller and uniform surface textures exhibit better light trapping properties than larger surface textures [33]. Chen *et al.* demonstrated that difference in acid solution composition can produce different

surface textures with varied dimensions on mc-Si wafers as depicted in Figure 2.7 [33]. Lower and moderate HF concentration in acid texturing solution produce larger inverted pit-like textures (~ 10 μm as reported in previous studies) as shown in Figure 2.7 (a) and (b) and very high HF concentration in acid etching solution resulted in small micro-crack like structures as shown in Figure 2.7 (d). Chen *et al.* reported that there exists a process window between the above conditions where the texture solution composition can be fine tuned to generate uniformly distributed inverted pit-like structures (see Figure 2.7 (c)) with diameter and height values in the range of 2 μm and 3.2 μm. The WAR associated with these surface textures were as low as 21.7% with adequate ARC surface passivation similar in the case of alkaline textured mc-Si cells. The light trapping properties of these textures were verified with theoretical simulations. Later, there were several attempts to improve the texture size uniformity further [65]. However, the average size of the textures (inverted pits) were still in the range of 2-4 μm in most of the cases [65, 66, 67].

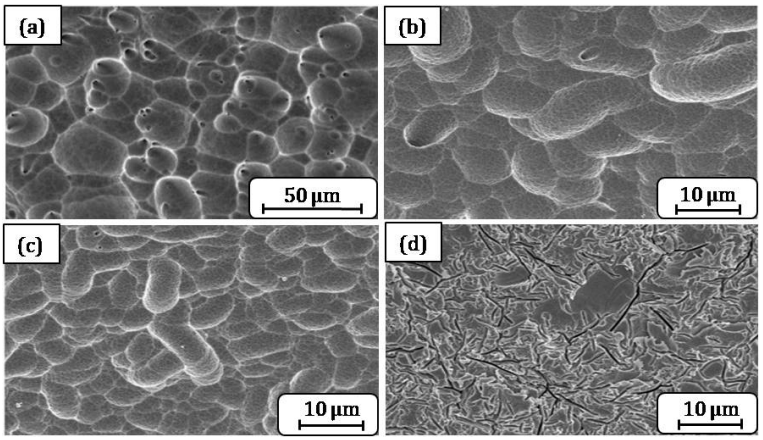

Figure 2.7: The SEM images of mc-Si wafers textured in acid solution comprising of HF:HNO_3:DI water in the ratio of; (a) 2.5:1:2.5, (b) 7:1:2.5, (c) 15:1:2.5, and (d) 36:1:2.5. Adapted from [33].

Addition of sulphuric acid (H_2SO_4) to acid texturing solution is another effective method reported for improving acid texturing process as it not only helps to stabilize the nitrogen-oxygen intermediates in the oxidation reaction, but also enhances the formation of fluorine capturing species [68, 69, 70]. Pseudo ternary system with concentrations of H_2SO_4, HF and HNO_3 as three input parameters was established to study the etch rate and surface texture morphology of H_2SO_4 based acid textured mc-Si

wafers [71]. Variation in etch rate from 2 μm/min to 700 μm/min was identified for different composition of H_2SO_4 - HF - HNO_3 mixture. Acid solution with moderate etch rate (< 5 μm/min) has resulted in uniform textures on the mc-Si wafer suitable for solar cell fabrication, which corresponds to H_2SO_4-rich region of pseudo ternary system. Few micrometer sized worm-eaten like random surface textures were obtained after H_2SO_4-rich acid etching in comparison with the inverted pit-like textures obtained after HF - HNO_3 acid texturing [70, 71]. H_2SO_4-rich acid textured MWSS mc-Si cells produced average 0.08% (absolute) higher η compared to conventional acid textured cells with an improvement of 0.12 mA/cm^2 in J_{SC} and 0.24% (absolute) in FF values [71]. A similar improvement in η of 0.12% were noticed in H_2SO_4-rich acid textured cells over conventional acid textured cells fabricated using DWS mc-Si wafers as well [71]. However, handling of large amount of sulphuric acid, stability and lifetime of texturing bath, throughput and waste disposal analysis of H_2SO_4-rich acid texturing process needs to be scrutinized for its industrial adoption. Interestingly, there are no reports on industrial implementation of the H_2SO_4 based acid texturing process as per our knowledge.

2.3 Other texturing schemes for mc-Si wafers

2.3.1 Reactive ion etching

Etching processes are broadly classified as chemical and physical etching. Chemical etching is based on the specific chemical interaction of the materials and physical etching (eg. plasma based etching) occurs due to the physical interaction of high energy ions with the substrate. Chemical etching process possess high selectivity and poor directionality whereas physical etching processes have better directionality and posses poor selectivity [72, 73]. RIE is a combination of both. This assures both selectivity (due to chemical species) as well as directionality (due to high energy species). Unlike acid texturing, RIE texturing does not depend on initial surface morphologies of as-cut wafers. Fluorine based plasma such as sulphur hexafluoride (SF_6) and carbon tetrafluoride (CF_4) are commonly used for the directional etching of Si wafers [74, 75, 76, 77].

Winderbaum *et al.* proposed a combination of photo-lithography and RIE processes for texturing mc-Si wafers [78]. Sputtered nichrome layer after photo-lithography was used as mask for RIE texturing of mc-Si wafers [78]. Regular pyramids with a base width of 5 μm was obtained after RIE as shown in Figure 2.8 (a). These RIE textured surface produced excellent WAR of 5.6% (without ARC) confirming the possibility of triple-bounce effect for incoming radiation, in contrast with alkaline textured c-Si (upright random pyramids) surface, which possess double-bounce effect [79, 80, 81]. Authors reported that the masked RIE textured mc-Si wafers in combination with conventional SiN_X ARC are capable of suppressing the surface reflectance to nearly 0% values for entire wavelength in the range of 500 nm to 1000 nm. Significant improvement in J_{SC} of 5.7 mA/cm^2 was reported for RIE textured cells over chemically polished mc-Si solar cells. However, the feasibility of masked RIE texturing method for industrial applications was limited by the use of photo-lithography, since the stated process is too complex and expensive for solar cell production.

Apparently, Inomata *et al.* developed photo-lithography-free (mask-less) chlorine (Cl_2) plasma based RIE texturing process for mc-Si wafers [82]. The varying aspect ratio pyramid-like nano-textures were generated on mc-Si wafers by altering the Cl_2 gas flow rate. Though higher aspect ratio textures produce extremely low surface reflection, they are very difficult to passivate using conventional SiN_X ARC layer. Optimal surface textures as shown in Figure 2.8 (b) having a balanced WAR and emitter saturation current density (J_{0e}) were generated for a Cl_2 gas flow rate of 4.5 sccm. The champion RIE textured cell recorded an impressive η of 17.1% with J_{SC}, V_{OC} and FF values of 36.13 mA/cm^2, 621 mV and 76.15%, respectively. This was the highest reported η value for large area mc-Si solar cells in that period. Authors reported that multiple wafers were textured using Cl_2 based RIE process, which makes it suitable for mass production. However, the corrosive and toxic nature of Cl_2 gas was the major bottleneck of this approach.

Later, Ruby *et al.* proposed metal catalyst assisted mask-less RIE texturing using SF_6/O_2 plasma instead of Cl_2 plasma for texturing industrial mc-Si wafers [83]. In addition, SF_6/O_2 plasma has a higher isotropic etch rate compared to Cl_2 plasma for RIE of Si. This corresponds to higher throughput in industry. Four different metal-assisted RIE texturing processes; namely Al-assisted, Cr-assisted, Ti-assisted, and chamber-

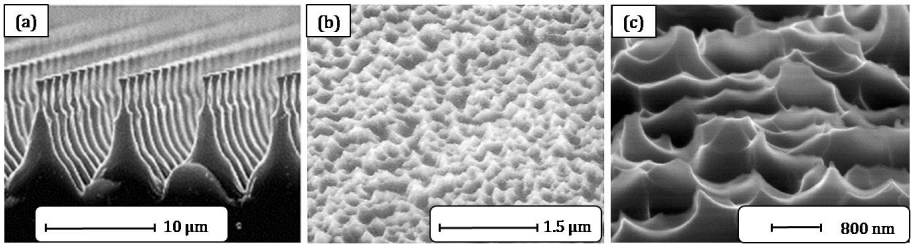

Figure 2.8: SEM images of mc-Si wafers textured by; (a) masked RIE, (b) mask-less RIE using Cl_2 plasma and (c) metal catalyst assisted mask-less RIE using SF_6/O_2 plasma. Adapted from [78], [82] and [83].

conditioned were developed [84]. However, RIE textured wafers underwent an additional damage removal etching (DRE) in dilute HF-HNO_3 solution for removing the shallow surface damages introduced on the wafer surface during the RIE process. RIE textured mc-Si cells with the DRE process performed better than both planar and RIE textured (without DRE process) cells, respectively because of increased light absorption and emitter spectral response, respectively. Authors stated that an additional DRE step is essential after RIE texturing for recovering the emitter spectral response.

Yoo *et al.* optimized SF_6/O_2 based mask-less RIE texturing process further for the fabrication of 16.1% efficient large area (156.75×156.75 cm^2) mc-Si solar cells [85]. In their experiments, RIE texturing for 5 min, 10 min and 15 min has resulted in dense pyramidal nano-textures. The width and the height of the textures were enlarged with an increase in RIE time as seen in the SEM images in Figure 2.9. The average material loss (in terms of thickness) and WAR value of RIE as-textured samples were only 0.43 μm, 1.01 μm and 1.56 μm and 17.6%, 13.7% and 13.3%, respectively for 5 min, 10 min and 15 min of RIE texturing. 10 min RIE textured cells produced the highest power conversion efficiency with maximum J_{SC}, V_{OC} and FF values. The blue response of 15 min RIE textured mc-Si cells were inferior compared to the other two batch of RIE textured cells. This suggests the possibility of RIE induced surface damage formation at the surface (for 15 min RIE textured samples) as previously reported by Ruby *et al.* [83]. In such a case, an additional cleaning process is essential to recover the blue spectral response. However, according to Yoo *et al.* [85], under optimized conditions, RIE process produce defect-free nano-textures on the mc-Si wafer surface with minimal material loss and excellent light absorption. Similar work was reported by Lee *et al.*

[86]. These investigations open up the potential applicability of RIE texturing method on the next generation kerf-less and thinner wafers.

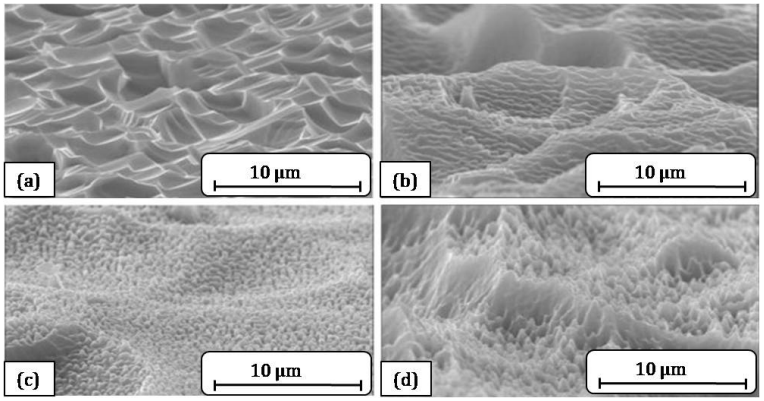

Figure 2.9: SEM images of mc-Si wafers textured by (a) only acid etching (no RIE) and RIE texturing for (b) 5 min, (c) 10 min, and 15 min. Adapted from [85].

Basu *et al.* proposed an improvised texturing scheme using the combination of acid texturing process and mask-less RIE for generating sub-micron surface features on mc-Si wafers [7]. Acid texturing process consisted of an isotropic etching in HF-HNO_3 solution followed by 5% KOH rinse. Micron-sized inverted pit-like textures (as discussed section in 2.2.3) with a WAR of 6.1% (after ARC) were obtained after acid texturing. Further, RIE texturing has produced sub-micron pyramidal textures on these micron-sized pits. The spikiness and roughness of the sub-micron pyramid-like textures were the key factors in deciding the balance between surface reflection and carrier recombination for RIE textured samples. The optimized RIE texturing on acid textured mc-Si wafers produced an overall enhancement in WAR by ~ 3.5% (after SiN_X ARC) and similar surface passivation properties in comparison with acid textured samples. This sets its suitability for high efficiency mc-Si solar cell fabrication. Similar approaches were reported for c-Si wafers as well, where a combination of alkaline etching and RIE was used to generate b-Si samples having extremely low surface reflection [87]. The major drawback of the RIE texturing method is the cost of the technology and poor production throughput compared to wet texturing methods. This makes industrial adoption of RIE texturing process extremely challenging irrespective of its improved performance.

2.3.2 Mechanical Grooving

Mechanical grooves on mc-Si wafers were first fabricated using a saw with bevelled blades used in the wafering process [25]. The tip angle and thickness of the blade were varied from 35° to 180° and 40 μm to 150 μm, respectively for the fabrication of V-shaped grooves on mc-Si wafers as shown in Figure 2.10 (a, b and c). These V-groove samples underwent HF - HNO_3 - CH_3COOH treatment for saw damage etching and surface smoothening as shown in Figure 2.10 (d, e and f). An impressive WAR of 6.6% (without ARC) was achieved for 35° blade angle and 120 μm pitch (Figure 2.10 (b)) sliced textured samples. This WAR value was as good as masked RIE textured mc-Si samples reported by Winderbaum *et al.* [78], indicating the possibility of triple-bounce effect in this case as well. The reflection coefficient of V-grove samples was dependent on the blade tip shape and quality of damage etching.

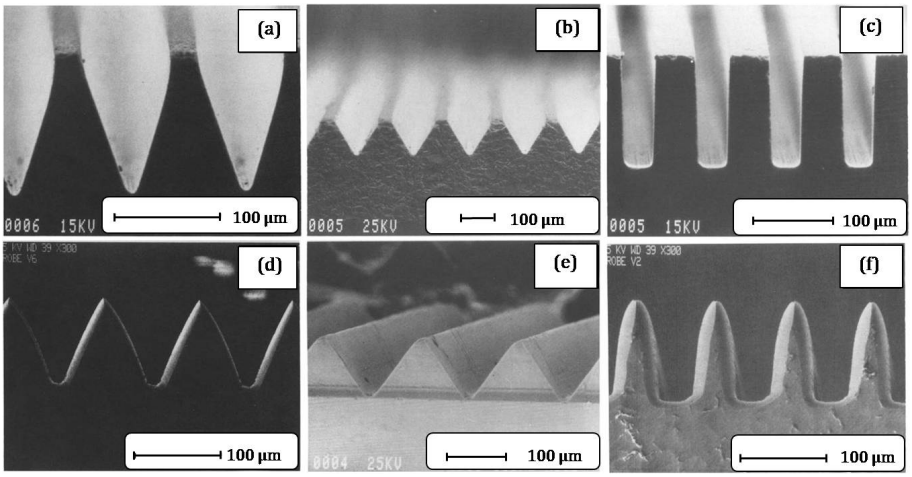

Figure 2.10: SEM images of mechanically textured mc-Si wafers using saw with bevelled blades. Adapted from [25].

Nakaya *et al.* studied the impact of blade tip angle on solar cell parameters by varying the blade tip angle from 40° to 70° [24]. 70 μm deep V-shaped grooves were fabricated on mc-Si wafer surface using a dicing machine consisting of bevelled blades. Unlike the previous study, the V-grooved samples were etched in 3% NaOH solution for surface smoothening and saw damage etching. Significant reduction in I_{SC} and η values were noticed for higher tip angle grooved samples in agreement with the previous study by Willeke *et al.* [25]. Authors also observed that V-groove textured samples have better light capturing and power conversion efficiency than that of U-

groove textured samples [24]. Later, Gerhards *et al.* developed a low-cost structuring wheel with V-grooved metal body coated with diamond abrasives for texturing mc-Si wafers and reported 8% enhancement in I_{SC} and η for V-groove textured mc-Si cells over the conventionally acid textured cells [88].

However, low speed (low throughput), higher tool wear, higher kerf-loss and the saw damage issues were some of the obvious drawbacks of V-groove texturing (mechanical texturing) compared to the wet chemical based texturization methods. A kerf-loss of ~140 μm was reported per wafer [25]. During that period, the thickness of wafers used for solar cell fabrication was in the range of 300-400 μm. However, currently industry use more thinner wafers (thickness of 160-180 μm) for cell fabrication. This limits the applicability of the proposed texturing process on thinner wafers. Also, the higher wafer breakage rate was another limiting factor for this method. Other mechanical ways of texturing such as inkjet texturing [89, 90] and sandblasting [91] were tried for texturing Si wafers. However, higher breakage rate and lower production throughput of mechanical ways of texturing always limited its usage in industry over wet texturing processes [61].

2.3.3 Laser etching

Fabrication of various arrays of textures such as conical spikes, inverted conical spikes, and parallel grooves were demonstrated on mc-Si wafers by laser etching [92, 93, 94, 95]. The laser texturing processes were carried out in SF_6, Cl_2, helium (He) or nitrogen (N_2) ambient using femto-second (fs) or nano-second (ns) lasers. The balance between the transverse mode order and laser power is reported to be the key for generating smaller and uniform textures suitable for solar cell applications [96]. Halbwox *et al.* demonstrated an impressive 30% enhancement in photo-current in laser textured areas of the solar cells in comparison with planar regions [97]. They have generated uniform 10 μm height 'penguin'-like structures using a fs laser on 1 mm^2 wafer area. Similar textures were generated in many of the previous studies too [93, 94, 98]. However, most of the studies were restricted to optical property analysis. The surface recombination velocity and solar cell performance studies were missing. In contrast, Abbott *et al.* performed a detailed investigation of morphological, optical, electronic and electrical performance comparison of laser textured mc-Si wafers and solar cells with alkaline

textured c-Si and planar wafers and solar cells [95]. Abbott *et al.* have generated interlock pit-like array of textures using Nd:YAG laser and used double sided buried contact cell architecture for solar cell fabrication. The SEM images of the interlock pits are shown in Figure 2.11 (a). An additional damage etching process was used for removing the amorphous ablation slag and damage layer introduced during the laser etching as shown in Figure 2.11 (a). A combination of alkaline (weak NaOH) and isotropic (HF - HNO_3 - CH_3COOH) solutions, respectively were used for ablation slag removal and surface smoothening. The SEM images of laser textured mc-Si wafers after alkaline and isotropic etching are shown in Figure 2.11 (b) and (c)-(d), respectively. The single-sided laser textured samples (shown in Figures. 2.11 (c) and (d)) exhibited lower surface reflectance than alkaline textured c-Si wafers, which resulted in an additional J_{SC} of 0.8 mA/cm^2 over an area of 7.3 cm^2 [97]. There were similar efforts for the fabrication of laser texture based solar cells on mc-Si wafers later as well [98, 99, 100]. However, mostly on smaller area mc-Si samples because of the lower speed of laser texturing.

Laser texturing process is expensive, complex, and time-consuming compared to existing chemical texturing processes. Also, the requirement of an additional chemical process step after laser etching limits its industrial adoption. However, with the emergence of passivated emitter rear contact (PERC) solar cells, femto second lasers are already used in industry for ablating the dielectric for rear side Al contact [101, 102, 103]. This may open up the possibilities for industrial adoption of laser etching for texturing.

2.3.4 Colloidal masking

As discussed in section 2.3.1, masked RIE textured wafers exhibited better light capturing properties than wet textured and mask-less RIE textured mc-Si samples because of triple-bounce effect [58, 78, 83]. The masked RIE textured samples were capable of suppressing the surface reflection to nearly zero in 500 nm to 900 nm wavelength range after SiN_X ARC deposition [78]. However, the masked RIE texturing approach did not gain significant industrial attention due to the involvement of complex and expensive photo-lithography steps. On a related note, there were attempts to develop photo-lithography-free masking techniques for the selective etching of Si wafers. Colloidal lithography (CL) was one of the leading candidate in those. The technique is often

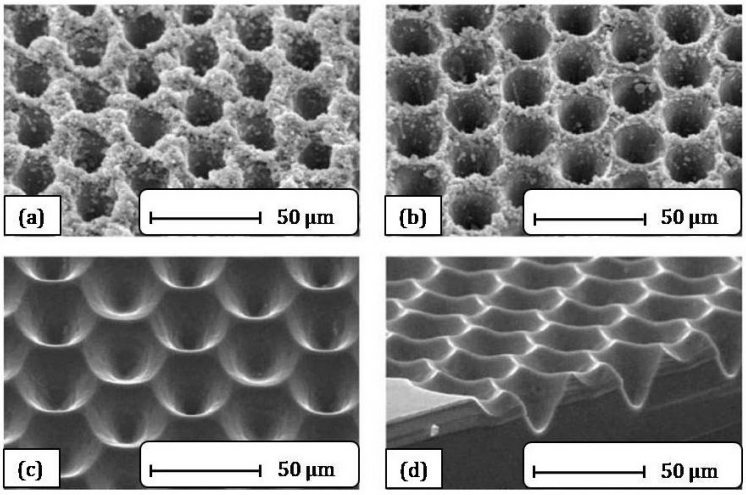

Figure 2.11: SEM images of laser textured mc-Si wafers at different processing stages; (a) after laser etching; (b) after alkaline (NaOH) etching; (c) and (d) after final isotropic (HF-HNO_3-CH_3COOH solution) etching. Adapted from [95].

called as natural lithography or nano-sphere lithography. In this approach, colloidal nano-particles such as polystyrene beads or silica beads are transferred on to Si wafer surface by low cost deposition techniques such as spin coating and dip coating. These beads act as the mask for Si etching [104, 105, 106]. The advantages of this method are good control on the periodicity, any standard Si dry etch recipes can be used, good mask selectivity for dry etching, and no need of additional processes for mask preparation and etching [107, 108, 109].

The CL based texturing process consists of four major steps; (i) transfer of single-layer colloidal masks on to Si substrate, (ii) organic residual etching and mask size reduction by O_2 plasma etching, (iii) Si etching by RIE and (iv) colloidal mask etching in HF solution [110, 111, 112, 113]. Nositschka *et al.* were the first to propose the combination of CL and RIE for texturing mc-Si wafers [110]. Authors have used spin coating method for transferring SiO_2 colloidal beads (silica beads) with a diameter in the range of 250 nm to 1000 nm on to saw damage etched mc-Si wafers. The top-down SEM images of beads spin coated on alkaline SDR mc-Si surface are shown in Figure 2.12 (a) and (b). The spin coating process parameters were optimized for achieving mono-layers of colloidal masks as shown in Figures 2.12 (a) and (b), and O_2 plasma etching was used effectively for reducing the size of beads and thereby opening the space for Si etching. $\sim$ 100-300 nm tall nano-pillars were fabricated by RIE etching.

The SEM images of surface textures are shown in Figures 2.12 (c) and (d). After the RIE process, the silica beads were etched in HF solution. The surface reflectance values of the colloidal RIE textured mc-Si samples were significantly lower than the reported wet chemical approaches and were in the range of V-groove textured and masked RIE textured mc-Si samples at both cell and module level. A relative increase in J_{SC} of nearly 3% was achieved for CL based RIE samples over mask-less RIE samples. Marginally improved V_{OC} and FF values were measured for CL based RIE textured cells over the other [114]. An overall 0.6% gain in η was reported for CL masked RIE textured cells over mask-less RIE textured mc-Si cells.

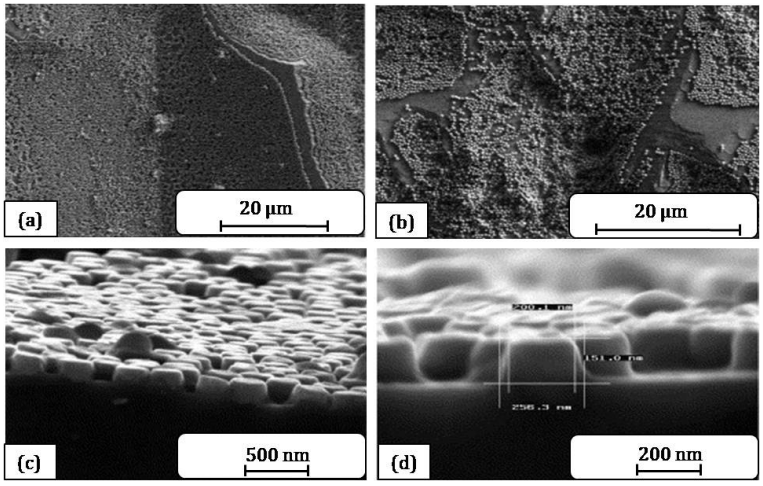

Figure 2.12: SEM images of (a) and (b) silica beads coated on mc-Si wafers. (c) and (d) represents the SEM images after RIE etching using silica beads as mask. Adapted from [110].

However, CL is best suited for polished planar Si wafers. Perfectly placed hexagonal close packing of beads was reported only on polished wafers. However, solar grade wafers undergo a SDR process in alkaline or acid solutions prior to any processing. Both acid and alkaline based processes result in surface undulations, which makes the uniform and mono-layer deposition of beads extremely difficult as seen in Figure 2.12 (a) and (b). Non-uniform distribution of beads results in non-uniform etching and texture formation after RIE. Cost analysis of the CL and RIE process would be the crucial parameters in deciding its industrial viability. At this point, we believe that the CL followed by RIE based texturing scheme may not be suitable for industrial production in near future since the process steps involved in the CL and RIE are still complex and

expensive compared to the existing wet texturing processes.

2.4 Conclusions

A comprehensive review of various etching processes used for texturing industrial c-Si and mc-Si wafers is presented in this chapter. History and evolution, basic reaction mechanisms involved, composition of chemicals and process sequence, advantages, disadvantages of each texturing schemes and, finally its influence on solar cell performance are discussed. The chapter can be summarized by stating that the alkaline etching (SDR in concentrated KOH solution followed pyramidal texturing in KOH-IPA solution) and acid (HF-HNO_3) etching, respectively dominated the texturing of MWSS c-Si and mc-Si wafers in industry.

Chapter 3

Literature Review on Texturing of Industrial DWS Wafers

This chapter starts with reviewing the diamond wire sawing technique and its implications on wet texturing methods. The basic cutting mechanism, advantages of DWS over MWSS and the methods proposed for addressing the texturing difficulty of DWS c-Si wafers are discussed in the first section of this chapter. Second section provides detailed reviews of different methods reported for texturing DWS mc-Si wafers. The advantages, disadvantages and challenges for industrial adoption of such methods are detailed in this section. The third section elaborately discusses the MACE process and its potential for solar cell fabrication.

3.1 Emergence of DWS wafers: a new challenge

Till the end of 2015, wafer manufacturing units were using MWSS (also known as loose abrasive slurry sawing in industry) technique for slicing wafers from ingots and casted blocks. In MWSS set up, multiple steel wires are rolled at a speed of 15-20 m/s and a specific tension in the range of 18 - 25 N in a roller like arrangement [3, 4]. The Si blocks (ingots) are continuously sprayed with a slurry containing SiC abrasive particles and polyethylene glycol (PEG) fluid and the material removal process happening between the steel-wire, SiC abrasive, and the casted block or Cz grown ingots is responsible for the wafering phenomenon [4, 115, 116, 117, 118, 119, 120]. The MWSS wafering processes are explained with respect to rolling and indenting model

[118]. The indenting process during wire sawing results in elastic deformation of Si material due to high contact stress and application of a critical load generates cracks near the indenter [121, 122, 123]. Further, with the release of the indenter, the wafers are separated from the ingots and the residual debris are collected along with the slurry [118, 122]. Multiple wafers are sawn simultaneously from a single ingot. However, the MWSS approach has several process limitations and disadvantages. In the rolling and indenting process, the speed of the SiC abrasives is always limited with respect to the wire moving speed and this sets the overall speed of the slicing process [4, 119]. In addition, MWSS technique requires huge amount of PEG based slurry, which makes waste management and recycling of Si debris extremely challenging [4, 120]. The wear of steel-wire is significant and almost all wires need to be replaced after each slice [119]. Importantly, the kerf-loss associated with the MWSS process is high. As per the industry reports, approximately 130 μm Si material is lost as kerf in the MWSS process for slicing 180 μm thick wafers [2, 119]. Also, considerable total thickness variation (TTV) is noticed for this approach due to the unavoidable size variation of SiC abrasives in the slurry fluid [4, 119]. All the above factors made the MWSS approach not favorable for the manufacturing of high quality, low-cost, and thinner wafers with a thinner saw damage, less kerf-loss, and smaller TTV.

The diamond plated wire sawing (DWS) approach, also known as fixed wire abrasive cutting emerged as an alternate technique for slicing thinner wafers from ingots and casted blocks. In DWS, the steel-wire used in the MWSS technique is replaced by thinner steel-wires with 10-20 μm sized diamond particles embedded on it. The diamond particles are attached to the wire by resin bonding or Ni electro-plating [4, 119]. Diamond scribing on Si surface usually follows a ductile behavior, which produces damage-free wafer surface after cutting [124]. Instead of PEG based slurry, the DWS approach uses chilled water as coolant. This reduces environmental pollution and makes the kerf material recycling easier [125]. The wire wearing with the DWS method is significantly lower than the MWSS approach and single roll of steel-wires are used for cutting multiple ingots. The kerf-loss and TTV are remarkably lower for DWS wafers [126]. The kerf-loss associated with DWS is now $\sim$ 75 μm and is expected to reduce to $\sim$ 50 μm by 2028 as per ITRPV 2020 predictions [2]. Since the diamond particles are attached on the steel wire itself, cutting speed of DWS technique

is not limited by a third body movement, and the cutting efficiency is influenced only by the wire speed. This results in 2-3 times enhancement in cutting efficiency (higher production throughput) for the DWS method than the MWSS approach [4]. The comparison of DWS and MWSS wafering approaches are summarized in Table 3.1

Table 3.1: Envormental and economical aspect comparison of DWS and MWSS approaches used for slicing mc-Si wafers from casted blocks.

	DWS	MWSS
Economical	• Higher productivity. • Good quality wafers. • Long life-cycle of steel wires. • Lower waste management cost. • Easy recycling of Si debris. • Affordable for large scale production.	• Lower productivity. • Poor quality wafers. • Higher breakage rate of steel wires. • Higher waste management cost. • Expensive recycling of debris. • Higher large scale manufacturing cost.
Environmental	• Reduced kerf-loss. • Water based based cooling and cutting. • Lower environmental pollution. • Thinner and fewer saw damage layer	• Higher kerf-loss. • PEG slurry cooling and cutting. • Higher environmental pollution. • Thicker and uniform saw damage layer.

The top-down SEM images of as-cut MWSS and DWS mc-Si wafers are shown in

Figure 3.2 (a) and (b), respectively. Both the types of wafers possess different surface morphologies because of the difference in their cutting mechanisms. Indentation process produce random defects and damages uniformly across the MWSS wafer surface [127]. The scratching process results in the formation of grooves and pits mainly along the diamond wire cutting direction. Several parallel saw marks are visible on the surface of DWS mc-Si wafers as seen in Figure 3.2 (b). Compared to MWSS wafers, DWS wafers possess smoother, thinner, and fewer saw damages due to the ductile behavior of Si while diamond wire sawing. Fewer surface damages are preferred for solar cell applications since these surface defects act as recombination centers at the emitter surface. However, the effectiveness of the texturing process also highly depends on the initial wafer surface topology and polished surfaces are relatively difficult to texture compared to defect-rich surfaces. Since the as-cut wafer topologies are significantly different for MWSS and DWS wafers, there exists a technical difficulty in using the same texturing process for both MWSS and DWS wafers, especially for mc-Si wafers [127].

For DWS c-Si wafers, a suitable SDR process for the removal of undesired parallel saw marks, a-Si layer and deeper grooves (shown in Figure 3.2 (b)), followed by an existing standard alkaline texturing process can effectively reduce the surface reflection to the same as that in the conventional alkaline textured MWSS c-Si wafers. In this regard, several pre-treatment processes such as etching in RCA1 and RCA2 solutions, NaOH - H_2O_2 solution and citric acid solution were previously tried [9, 10]. However, complete removal of saw marks were not achieved in any of the above cases. In most of the cases, the residual saw marks and traces of amorphous silicon layers were still present on the wafer surface as shown in Figure 3.1 (a) and (b) even after alkaline pyramid texturing. These saw mark impressions adversely impact the performance of solar cells and hence, the potential cost advantage of using DWS wafers are not completely utilized due to the lower performance of DWS alkaline textured cells in comparison with conventional alkaline textured MWSS c-Si solar cells.

On a related note, Chen *et al.* proposed TMAH solution based pre-polishing step for the SDE of DWS c-Si wafers prior to alkaline texturing [8]. The pre-polishing step was optimized by varying the etching time from 50 sec to 500 sec for a targeted removal of complete saw mark impressions and damages. All the saw marks were

nearly removed from the wafer surface for an etch time of 100 sec and with the further increase in TMAH etching time, the wafer surface started to become more polished and flat without any surface defects. However, these kind of surfaces are not suitable for the nucleation of pyramid texture formation. In addition, higher polishing time implies lower throughput and higher material loss, which makes it not suitable for industrial applications. Hence, authors considered 100 sec of TMAH treatment produce optimal surface quality, best suited for alkaline texturing. The SEM images of upright pyramids obtained after routine alkaline texturing for TMAH pre-treatment of 100 sec are shown in Figure 3.1 (c) and (d), respectively. No saw mark impressions were visible on 100 sec pre-polished alkaline textured samples and the texture distributions were similar to that of conventional alkaline textured c-Si samples. The solar cell performance parameters of 100 sec pre-polished alkaline textured DWS c-Si cells were also similar to that of the conventional saw damage etched and alkaline textured MWSS c-Si cells [8]. However, as discussed earlier, TMAH based Si etching process has several disadvantages and hence is not used in PV industry. In this regard, we proposed the NaOCl - KOH based etching for SDE of DWS c-Si wafers and optimized the process conditions for generating uniform and smaller pyramid textures on DWS c-Si wafers. The process details and performance of novel NaOCl - KOH solution based alkaline textured DWS wafers and cells are described in chapter 5 of this thesis.

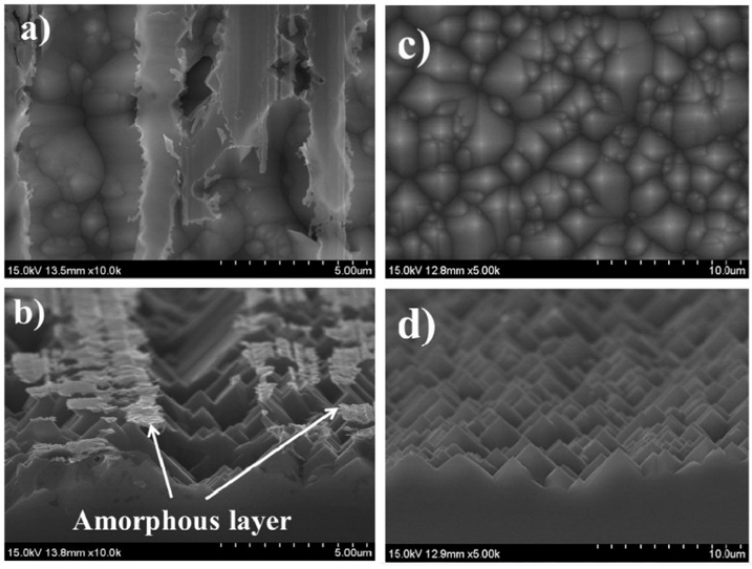

Figure 3.1: SEM images of pyramid textured DWS c-Si wafer (a), (b)without and with (c), (d) TMAH pre-polishing treatment [8].

Standard acid texturing process used in industry for MWSS mc-Si wafers was not effective in the case of DWS mc-Si wafers because of the absence of sufficient saw damage layer. The SEM images of acid textured MWSS and DWS wafers are shown in Figures 3.2 (c) and (d), respectively. In comparison with the acid textured MWSS mc-Si wafers, acid textured DWS mc-Si wafers have fewer surface textures and the textures are mainly located along the diamond wire saw marks and the regions where saw damages were initially present. The regions between the parallel saw marks, where there were no surface damages present initially were found to be relatively smoother even after acid etching as seen in Figure 3.2 (d). This leads to poor light trapping in acid textured DWS mc-Si wafers (WAR of >30%) compared to acid textured MWSS mc-Si wafers (WAR in the range of 23-26%). Wang *et al.* demonstrated that the acid texturing issue can cause 0.6% (absolute) reduction in η values for DWS mc-Si cells in comparison with MWSS mc-Si cells [12]. PV industries immediately adopted DWS technique over MWSS for slicing wafers and in two-three years of time the DWS wafers have completely replaced the MWSS mc-Si wafers in industry. This led to an urgent demand for developing an industrially viable texturing method for DWS mc-Si wafers.

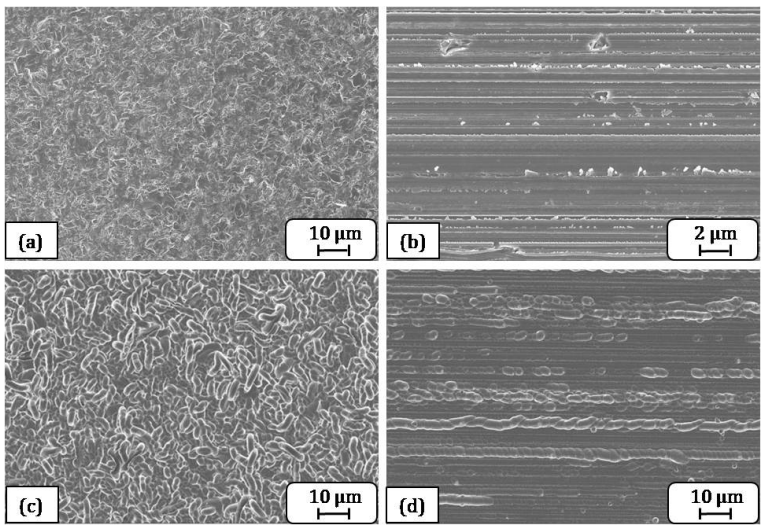

Figure 3.2: Top view SEM images of (a) as-cut MWSS, (b) as-cut DWS, (c) standard acid textured MWSS, and (d) standard acid textured DWS mc-Si wafers.

3.2 Texturing DWS mc-Si wafers

3.2.1 Additive-based acid texturing process

Researchers tried to address the wet texturing difficulties of DWS mc-Si wafers by examining alternate industrially feasible Si etching options. The first approach for the immediate industrial use was to dose texture additives to existing acid solution for improving the texture uniformity and thereby light absorption. In such a situation, the manufacturing process sequence and parameters are least disturbed. There are commercial texture additives developed by RENA and GP Solar available in the market for large scale texturing of DWS mc-Si wafers [62, 128]. As per the latest ITRPV reports [2], the majority of the industry ($\sim$ 60%) uses this method for texturing DWS mc-Si wafers in their production line. Deeper and denser textures (in comparison with the conventional acid textured DWS mc-Si samples) formed by additive-based acid texturing lowers the surface reflectivity of DWS mc-Si wafers in the range of acid textured MWSS mc-Si wafers. Significant improvement in J_{SC} and simultaneous enhancement in V_{OC} are guaranteed in the additive-based industrial texturing process [62, 128]. In addition, texture additives improve the stability and lifetime of acid texturing bath. However, only limited information is available in the literature regarding the composition of additives used and the process window of these additive-based acid texturing processes.

On a related note, Lippold *et al.* and Krieg *et al.* applied H_2SO_4-rich H_2SO_4 - HF - HNO_3 acid solution for texturing DWS mc-Si wafers [71, 129]. The SEM images of the surface texture formation at different stages of H_2SO_4-rich acid texturing are shown in Figure 3.3. Even for an etch depth up to 5 μm (the optimized process condition reported in the article), the uniformity of textures was not as good as in case of acid textured MWSS samples (see Figure 3.2 (c)). In addition, residual saw marks were still present on the DWS mc-Si wafer surface. H_2SO_4-rich acid textured cells recorded 0.12% gain in η, mainly due to 0.43 mA/cm^2 improvement in J_{SC} compared to conventionally HF - HNO_3 acid textured DWS mc-Si solar cells. However, the η, V_{OC}, and J_{SC} values of H_2SO_4-rich acid textured DWS mc-Si cells were 0.4%, 9 mV and 0.11 mA/cm^2 lower than H_2SO_4-rich acid textured MWSS mc-Si cells. This suggests that the surface quality of DWS wafers were significantly lower than MWSS wafers after H_2SO_4-rich acid texturing and

presence of residual saw marks (Figure 3.3 (d)) adversely affected the performance of DWS mc-Si solar cells.

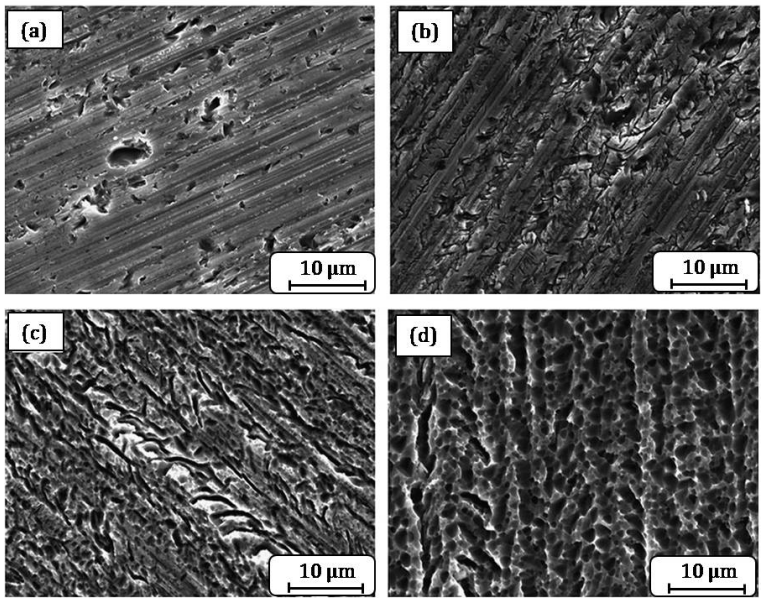

Figure 3.3: SEM images of DWS mc-Si wafers after etching in H_2SO_4 based acid solution for a saw damage etching of (a) 0 μm (as-cut), (b) 0.930 μm, (c) 2.970 μm, and (d) 5.53 μm [71].

3.2.2 Vapor etching

Liu *et al.* proposed vapor etching of HF - HNO_3 solution for producing saw mark-free corrosion pit-like textures on DWS mc-Si wafers [13]. The texturing process was carried out in a simple teflon container, which consists of an electric stove (placed at the bottom of teflon container) and a teflon based wafer holder (placed at the top of the container right above the stove). The HF - HNO_3 solution was heated up to 90°C for generating acid vapors. The evolution of corrosion pits with respect to etch time is shown in Figure 3.4. As seen in Figure 3.4 (b), at the initial stages, the elevated portions of saw marks were etched first to form bigger corrosion pits (for 2 min) and gradually the wafer surface becomes flatter after 5 min of vapor etching. The obvious saw marks gradually disappeared in this stage. As the etching time increased further (for 10 min) smaller corrosion pits started to form over the already formed larger pits and the saw marks completely vanished at this stage. After 15 min of etching, the larger corrosion pits were completely etched and replaced by smaller corrosion pits. Further, an increase in

etch time up to 20 min, forced the smaller pits to merge together to form larger corrosion pits. Excellent WAR value of ~10% was reported for 15 min of vapor etching. However, good anti-reflection properties alone does not guarantee high η in solar cells, especially for porous textures. Authors have not discussed about the passivation quality of the vapor etched surfaces. Also, there were no further relevant literature found describing the surface recombination properties or solar cell performance of acid vapor etched mc-Si cells. Authors report 15 min of etching as optimum for solar applications, which corresponds to 30 μm of material loss. This questions the applicability of vapor etching process on thinner mc-Si wafers.

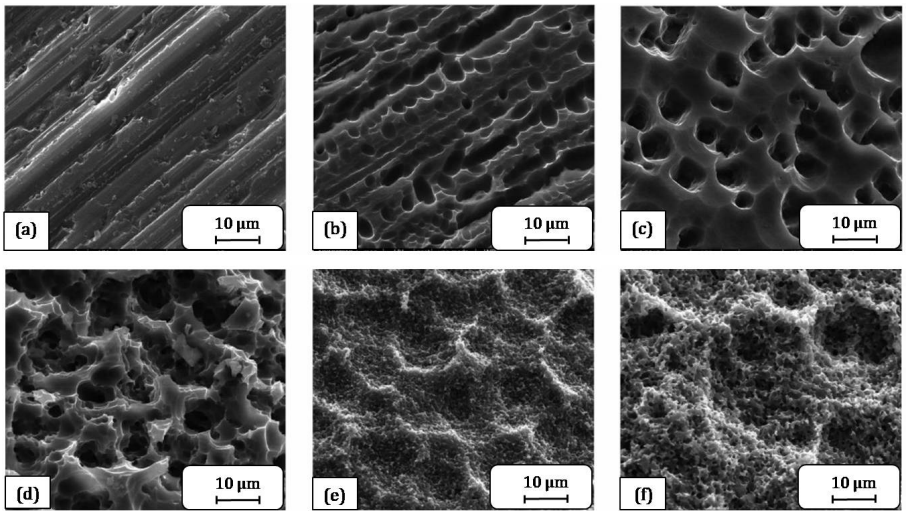

Figure 3.4: SEM images of DWS mc-Si wafers after vapor etching for (a) 0 min (as-cut), (b) 2 min, (c) 5 min, (d) 10 min, (e) 15 min, and (f) 20 min [13].

3.2.3 Sandblasting

Nishikota *et al.* [130] and Takato *et al.* [131] proposed a combination of traditional sandblasting and acid etching process for texturing mc-Si wafers in 2012 and 2013, respectively. However, difficulty in generating a uniform stream and higher breakage rate of wafers during sand blasting were two of the major bottlenecks of this approach. Later in 2018, Wang *et al.* introduced the X-Y micro-pressure sandblasting process particularly for addressing the texturing difficulty associated with DWS mc-Si wafers [12]. Unlike the traditional sandblaster system, the spray nozzle of the gun of X-Y micro-pressure sandblaster system moves in X-Y directions, and resolves the issue of

stream overlapping. In addition, one complete Si wafer can be sandblasted by using a single gun. The stabilized output stream significantly reduce the wafer breakage rate and marginally improve the uniformity of the blasting process in the X-Y micro-pressure sandblaster system. The wire saw mark impressions present on the DWS wafers were completely removed in the micro-pressure sandblasting process as seen in Figure 3.5 (c) in comparison with Figure 3.5 (b). The sandblasted DWS mc-Si surface topology was similar to that of as-cut MWSS wafers shown in Figure 3.5 (a). Hence, acid texturing of both sandblasted DWS and as-cut MWSS wafers resulted in uniformly distributed inverted pit-like structures (Figure 3.5 (d) and (f)) with similar WAR values in the range of 22% and η in the range of 17.95%. The η of acid textured DWS mc-Si cells (without sandblasting) was ~0.6% lower than the other two groups of mc-Si cells. The study demonstrated that the use of an additional process (X-Y sandblasting process in this case) for uniform defect generation across the wafer surface can assure similar η and I_{SC} values in DWS mc-Si cells as that of acid textured MWSS mc-Si cells. However, setting up an additional equipment to an existing line is always challenging in industry. Also, the wafer breakage rate with mechanical processes like sandblasting are always much higher than that of the existing solution based processes [61]. In addition, sandblasting contributes to an additional wastage of material, which lowers the strength of mc-Si wafers further. This additional material loss, higher breakage rate, and additional equipment setting cost associated with the sandblasting process limit the advantages of the proposed texturing process, especially for the fabrication of low-cost thin wafer based solar cells.

3.2.4 Laser texturing

Recently, Ding *et al.* demonstrated 19.26% efficiency for full area Al-BSF solar cell architecture on 6 inch laser textured DWS mc-Si wafers [132]. Similar to previous studies, laser texturing process consisted of two steps; laser ablation process for creating textures on mc-Si wafer surface and post acid etching processes for ablation slag removal and surface smoothening. DR-Al-Y100 industrial grade 532 nm wavelength laser with a repetition frequency of 500 KHz was used to fabricate two kinds of crater-like periodical textures by choosing two different laser power ratio of 50% and 100%. The SEM images of craters formed by laser texturing for laser power ratios of 50% and 100% are

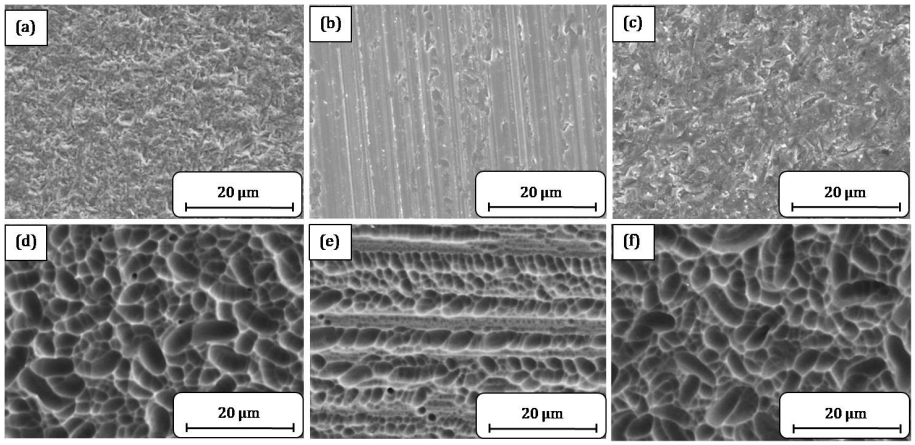

Figure 3.5: SEM images of (a) as-cut MWSS, (b) as-cut DWS, (c) sandblasted DWS, (d) acid textured MWSS, (e) acid textured DWS, and (f) sandblasted + acid textured DWS mc-Si wafers [12].

shown in Figure 3.6 (a) (before etching), (b) (post etching) and (c) (before etching), (d) (post etching), respectively. The average diameter and height of craters formed were 27.2 μm and 11.6 μm and 20.8 μm and 10.1 μm, respectively for 100% and 50% laser power ratio textured samples. Post etching process, the ablation slags were completely removed and surface became more smoother and less defective, more suitable for solar cell fabrication. However, post etching, the average diameter and depth of craters were changed to 35.5 μm and 10.4 μm and 23.6 μm and 8.6 μm, respectively for 100% and 50% laser power ratio textured samples. As a consequence, WAR value of laser textured samples changed from 15.39% to 25.12% and 16.65% to 25.61%, respectively for 100% and 50% laser power ratio textured samples after post etching, which only $\sim$ 2% lower than in case of acid textured DWS mc-Si wafers. In comparison to earlier reports [95], the WAR values of laser textured samples were significantly higher in this case before and after etching, relatively lower aspect ratio (height to diameter ratio) of the craters can be the reason for the same. Laser textured samples with 100% laser power ratio has produced 127 mA and 0.16% higher I_{SC} and η values compared to conventional acid textured solar cells. However, this enhancement in performance becomes insignificant considering the equipment setting cost of laser texturing tool. In addition, authors demonstrated that laser texturing process becomes less effective for higher defect concentration mc-Si wafers, as laser texturing produce recombination current density values compared to acid textured samples [132]. Even-though laser tex-

turing was demonstrated on full 6 inch wafers, relatively lower enhancement in WAR and performance parameters, additional equipment setting cost and ineffectiveness in producing good quality textures at defect-rich area questions its applicability for mc-Si wafers especially in industrial production lines.

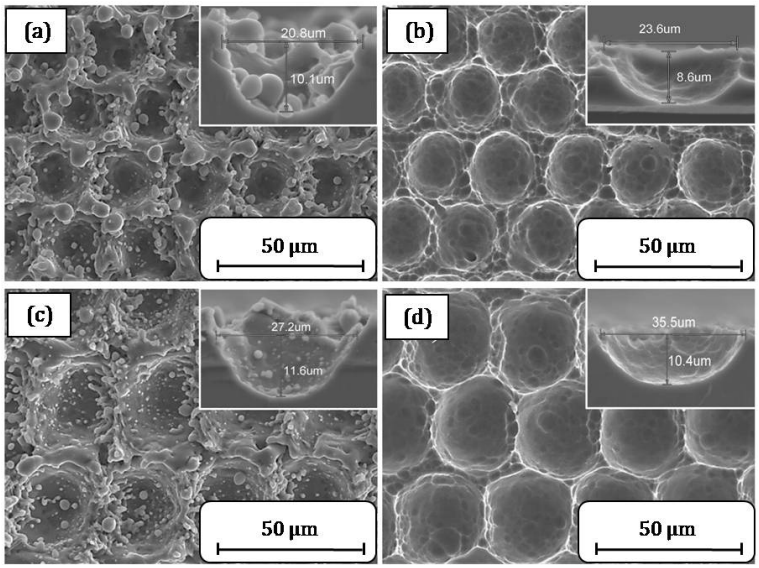

Figure 3.6: SEM images of craters formed by laser texturing for a laser power ratio of (a) 50% and (b)100%. SEM images in (c) and (d), respectively represent the crater like textures after post etching of laser textured samples with laser power ratio of 50% and 100% [132].

3.2.5 Reactive ion etching

Irrespective of high equipment setting cost, RIE has been always under investigation as a possible texturing method for mc-Si wafers [14, 133, 134]. This is because, RIE processes produce extremely good quality textures on Si wafers independent of wafer type and as-cut wafer morphology. This confirms its applicability on DWS mc-Si wafers too. Wang *et al.* recently used RIE for texturing DWS mc-Si wafers and demonstrated η of 19.05% for Al-BSF architecture on RIE textured wafers [135]. The SEM images of RIE textures are shown in Figure 3.7 (a). However, there were few drawbacks for the above RIE texturing process. Firstly, authors used corrosive Cl_2 plasma along with SF_6 and O_2 plasmas for Si etching. The WAR value of the RIE textured samples was in the range of 15%, significantly higher for RIE textured samples compared to earlier

discussed RIE textured mc-Si wafers [7, 82, 85]. Also, no significant improvement in τ_{eff} values were noticed for RIE textured samples over acid textured and MACE textured mc-Si samples. Beneck *et al.* recently reported a combination of SF_6-O_2 plasma based RIE texturing (without DRE process) and atomic layer deposition (ALD) aluminum oxide (Al_2O_3) + PECVD SiN_X stack for the fabrication of high efficiency solar cells using high performance (HP) n-type mc-Si wafers [14]. Inductively coupled plasma RIE (ICP-RIE) etching at lower voltage bias was used to produce high aspect ratio needle-like structures (Figure 3.7 (b)) with an excellent WAR of ~ 1% (after SiN_X ARC) and impressive J_{0e} of only 50 fA/cm^2. Interestingly, these values were better than alkaline textured float zone (Fz) n-type c-Si wafers. Record η of 21.9% was achieved for RIE textured TOPCon mc-Si solar cells with J_{SC}, V_{OC}, and FF values of 40.8 mA/cm^2, 673 mV and 79.7%, respectively. Hence, RIE texturing in combination with ALD Al_2O_3 + PECVD SiN_X dielectric stack is capable of producing higher power conversion efficiency than the alkaline textured ARC coated c-Si cells and the further enhancement in performance was limited only by bulk material quality in comparison with Fz c-Si wafers. This approach is expected to gain immense industrial attention considering the near zero surface reflection on mc-Si wafers with excellent J_{0e} as low as 50 fA/cm^2 as that of alkaline textured c-Si wafers.

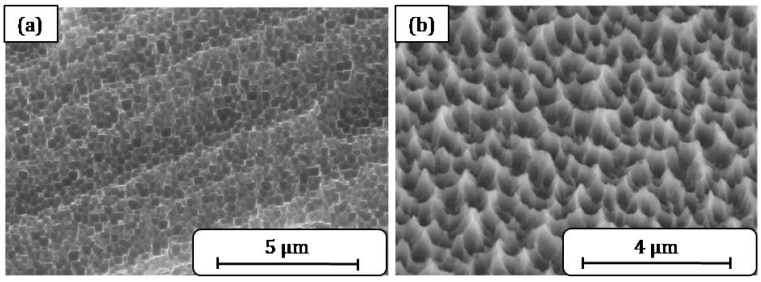

Figure 3.7: SEM image of RIE b-Si textured samples reported by; (a) Wang *et al.* [135] and (b) Beneck *et al.* [14] on p-type and n-type mc-Si wafers.

3.3 Metal Assisted Chemical Etching (MACE)

3.3.1 History and basic reaction mechanism

As the name indicates, the MACE process corresponds to enhanced etching of substrates such as Si and germanium (Ge) in the presence of metal particles or thin metal films. The MACE of Si consists of two steps; metal nano-particles (or film) deposition and etching in HF-oxidizing agent solution. Metal nano-particles can be deposited by various techniques [136, 137, 138, 139, 140]. MACE of Si was first demonstrated by Dimet *et al.* using an evaporated thin film of Al [141]. HF - HNO_3 solution was used for etching the Si beneath the Al layer for the fabrication of porous Si layer [141]. Later, Li and Bohn established the catalytic etching of Si in HF-hydrogen peroxide (H_2O_2) solution for noble metals such as Au, Ag, Pt, and Pd [136]. In the MACE process, the Si beneath the metal nano-particles etch at a much faster rate compared to uncovered Si surface. As a consequence, the metal nano-particles sink into the bulk of substrate, generating fine porous nano-structures. The morphology and dimensions of these nano-structures strictly depend on the pattern of metal deposition and the technique used for metal deposition [136, 139, 142, 143, 144, 145]. There were several models proposed for describing the mechanism of MACE of Si [136, 146, 147, 148]. A simple explanation is similar to that of electrochemical etching of Si in HF - HNO_3 acid solution as discussed in section 2.2.2. Instead of HF - HNO_3 acid solution, the MACE process widely uses HF - H_2O_2 acid solution for catalytic etching of Si samples. Hence, the electrochemical etching of Si beneath the metal nano-particles are explained with respect to HF - H_2O_2 solution. The red-ox reaction close to the metal particles can be summarized as,

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+ \tag{3.1}$$

$$2H^+ \rightarrow H_2 + 2h^+ \tag{3.2}$$

$$Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+ \tag{3.3}$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \tag{3.4}$$

The electrochemical potential of H_2O_2 solution is higher than the valence band of Si and more positive than other regularly used oxidizing agents like HNO_3 [36, 149, 150]. This implies that H_2O_2 can readily supply holes in to the valence band of Si irrespective of

wafer characteristics [136, 150, 151, 152], resulting in etching of Si in HF - H_2O_2 solution; however, at a much lower rate of only < 10 nm per hour [150]. The noble metals such as Ag [153], Au [154], Pt [155, 156] and Pd [157] are used widely to catalyze the oxidizing agents like H_2O_2 and O_2 bubbles [150]. These nano-particles act as cathode and the reductive reactions in equation 3.1 and 3.2 proceed on it at a faster rate. The generated holes are injected into the Si substrate in proximity of metal particle. This results in selective oxidation and dissolution of Si beneath the metalized areas. The presence of above mentioned metals results in faster Si etching with etch rate of > 1 μm per min. In contrast, the electrochemical etching process in HF - HNO_3 solution discussed in section 2.2.1 is auto-catalytic because of the presence of important intermediates like nitrous acid (HNO_2) [36]. This results in poor etch selectivity of MACE process in HF - HNO_3 solution. Hence, HF - H_2O_2 is the best suited oxidizing mixture for selective etching of Si.

3.3.2 Application in solar cell processing

The MACE Si wafers are often called as b-Si wafers, as it appears black because of its superior light harvesting properties. So, MACE b-Si wafers can be potentially used for solar cell applications. However, there are many challenges in incorporating any new technology to an existing solar cell production line such as (i) ensuring higher production throughput, (ii) managing the additional requirement of equipment setting, and (iii) balancing the cost of the technology, etc. Catalytic etching of Si in HF - H_2O_2 solution being a chemical process and using only PV grade chemicals fulfill the above conditions for its industrial adoption. Several techniques such as sputtering [136, 145, 158], focused ion beam [138], e-beam evaporation [144], spin coating [137], thermal evaporation [159, 160], and electroless deposition (EMD) [161] are reported for noble metal deposition step in the MACE b-Si process. Sputtering, e-beam and thermal evaporation methods are commonly used in MACE process for the fabrication of more specific and well controlled nano-structures and surface features. However, these methods are relatively expensive and low throughput processes for solar applications and hence, not suitable for industrial adoption. EMD is a simple, efficient, and inexpensive approach for metal nano-particle deposition if there aren't strict constraints on surface morphologies of the nano-structures after catalytic etching. Also, the cheapest metal,

Ag among the four frequently used metals (Au, Ag, Pt and Pd) for MACE processes can be easily deposited by the EMD method using silver nitrate ($AgNO_3$) solution at room temperature. Since it is a chemical solution based deposition, the process can be readily integrated to the existing industrial acid texturing tools without any additional equipment setting cost. As discussed earlier, after metal particle deposition, the wafers are etched in HF - H_2O_2 solution at room temperature. Both the metal deposition (Ag nano-particle deposition by EMD) and etching processes are done at room temperature and require only a few seconds (sec) for process completion. Hence, the MACE b-Si process fulfills all three criteria discussed above for its application in industrial production line. According to the latest industrial reports, MACE b-Si solar wafers have already started to replace the additive-based acid textured mc-Si wafers for low-cost high efficient solar cell fabrication in industry [2].

The MACE b-Si process used in the solar industry commonly consists of four steps. In the first step, the saw damages introduced during the sawing process are etched to form defect-free surfaces prior to metal deposition. Conventional acid etching in HF - HNO_3 solution [162] or concentrated alkaline etching [163, 164] can be applied for the same. Subsequently, the damage removed mc-Si wafers are soaked in $AgNO_3$ solution [164] or $AgNO_3$ - HF solution [165, 166] for a few sec at room temperature for Ag nano-particle deposition. Since the reduction potential of Ag/Ag^+ galvanic cell is more positive than valence band of Si, Ag^+ readily injects holes to the valence band of Si and the reduced Ag metal particles get deposited on the Si surface. During the EMD process, Ag^+/Ag acts as cathode, and Si in contact with metal particles acts as anode. The cathode reaction is summarized as follows,

$$Ag^+ \rightarrow Ag + h^+ \tag{3.5}$$

The injected holes in the valence band of Si facilitates the oxidation of Si to form SiO_2 at localized areas beneath the metal particles. The generalized anodic reaction can be summarized as follows,

$$Si + 2H_2O \rightarrow SiO_2 + 4h^+ + 4e^- \tag{3.6}$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{3.7}$$

If the metal nano-particles were deposited using $AgNO_3$ solution, then only the reaction given in equation 3.6 progresses, resulting in local oxidation of Si beneath the

metalized area. If $AgNO_3$ - HF solution was used for Ag nano-particle deposition, both the reactions listed in equation 3.6 and 3.7 progress simultaneously resulting in local oxidation of Si and etching of oxide layer beneath the metal particle. This leads to the sinkage of metal particles to the bulk of Si. However, the oxidation rate in such a case is too slow for deeper pores or nano-structure formation. Hence, strong oxidizing agents like H_2O_2 and H_3PO_4 are essential for the fabrication of deeper b-Si surface features. This corresponds to the third step of b-Si fabrication. As discussed earlier, a combination of HF - H_2O_2 solution is used for enhanced catalytic etching of Si. The red-ox reactions listed in equation 3.1 of section 3.3.1 confirms that addition of H_2O_2 in catalytic solution strongly oxidizes the Si beneath the metal particles and HF simultaneously etches the oxide layers, resulting in deeper sinkage of metal nano-particles and b-Si structure formation. Some of the literatures even describe about single step b-Si process where the reactions listed in equation 3.1, 3.5, 3.6, and 3.7 progress simultaneously to form b-Si features. For example, recently Kumagai *et al.* [167] and Kexun *et al.* [15] reported a single step b-Si fabrication process using the combination of $AgNO_3$, HF and H_2O_2 mixture. In the final step, the residual metal ion particles were removed from the wafer surface by etching the wafers in HNO_3 solution [15, 167] or NH_3 [168] or H_2O_2 - NH_3 solution [165]. The representative SEM images of DWS mc-Si wafers after Ag nano-particle deposition by EMD and Si etching in HF-H_2O_2 solution are shown in Figure 3.11. The shape, size and distribution of the Ag nano-particles are controlled by adjusting the HF and $AgNO_3$ solution composition and deposition time. The height/depth and size of b-Si nano-structure features can be controlled with respect to HF - H_2O_2 etching parameters.

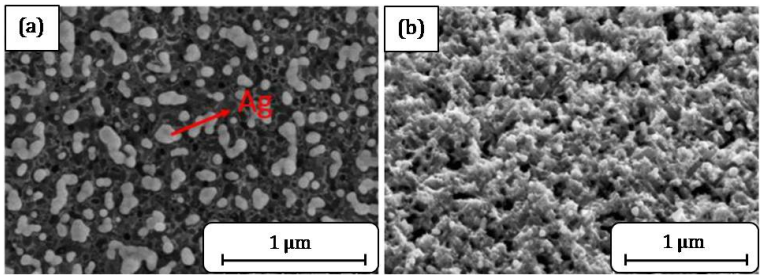

Figure 3.8: The SEM images of (a) Ag nano-particle deposited by EMD [166] and (b) nano-structures obtained after Si etching in HF - H_2O_2 solution on DWS mc-Si wafers [167].

3.3.3 Surface modification of b-Si samples

Requirement of surface modification

There were several attempts to fabricate high efficiency solar cells on both Ag catalyzed [169, 170] and Cu catalyzed [171] MACE b-Si textured samples, initially using c-Si wafers. MACE b-Si textured solar cells succeed to perform better than the planar reference cells in most of the cases as well [169, 170]. However, the blue wavelength spectral response of b-Si solar cell was extremely poor compared to planar cells due to poor passivation properties of b-Si surfaces [169, 170]. Hence, the advantages of superior light absorption in b-Si textured wafers were not completely translated to cell performance because of heavy surface recombinations at the emitter surface. Oh *et al.* modified the MACE b-Si surface for controlled surface recombination, using TMAH solution and demonstrated 18.2% efficient c-Si solar cells in 2012 [172]. The excess recombination losses associated with b-Si structures were suppressed by etching the b-Si samples (nano-pore textures) in TMAH solution to form wider surface features. The modified b-Si structures were well passivated using thermal SiO_X layer and 4 mV higher V_{OC} was reported for b-Si modified cells over conventional alkaline textured cells [172]. The study proved that b-Si samples after a suitable surface modification can perform better than other existing wet texturing methods used for low cost and high efficiency solar cells.

In 2014, Kumagai predicted the emergence of the DWS wafering technique and proposed the combination of MACE b-Si and conventional acid etching processes (HF-HNO_3 etching and followed by dilute KOH rinse) for texturing DWS mc-Si wafers [167]. 17.2% efficient Al-BSF solar cells were fabricated on acid textured b-Si DWS mc-Si wafers with 0.4% (absolute) gain in η compared to acid textured MWSS mc-Si cells. The optimized MACE b-Si processes were not only useful in addressing the texturing difficulty associated with DWS mc-Si wafers but also ensured better performance than acid textured MWSS mc-Si cells. Modification of the MACE b-Si surface for balanced optical and electronic properties is the key for achieving higher performance in b-Si mc-Si solar cells. The following subsections describe the advantages and disadvantages of various etching processes reported specifically for b-Si surface modification of MACE b-Si DWS mc-Si solar cells.

Alkaline etching

Fang Cao *et al.* proposed alkaline (NaOH) based etching for surface modification of MACE b-Si textured DWS mc-Si wafers [173]. Prior to alkaline etching, DWS wafers sequentially underwent an acid etching process in HF - HNO_3 solution and nano-texturing process in $AgNO_3$ - HF - H_2O_2, respectively for micron-sized inverted pit and nano-pore array (b-Si) fabrication. As seen in Figure 3.9 (a) and (b), 100 nm to 200 nm sized sub-micron pyramidal textures were formed after alkaline based b-Si surface modification. Alkaline etching of b-Si samples produced nano-pyramid like textures. Combination of micron-sized pits and sub-micron pyramids reduced the WAR value of DWS mc-Si wafers to below 16%. Reduced surface reflectance produced ~ 0.5% higher J_{SC} and η values compared to acid textured MWSS cells. However, relatively higher non-uniformity in both ARC thickness and emitter sheet resistance were noticed for the alkaline etched MACE b-Si samples in comparison with acid textured MWSS mc-Si samples. The anisotropic etch dependencies of NaOH solution towards different crystal orientations and non-uniform acid etching of DWS mc-Si wafers together contributed to non-uniform texture generation, and thereby resulting in non-uniform distribution of sheet resistance and ARC thickness across the wafer surface, making the proposed etching method not suitable for b-Si surface modification and large area high efficiency solar cell applications.

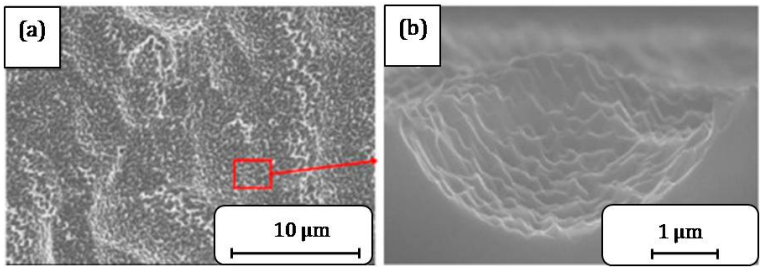

Figure 3.9: (a) Low and (b) high resolution SEM images of nano-pyramidal textures on acid textured DWS mc-Si wafers. Larger oval pits were formed by HF - HNO_3 acid etching and nano-pyramids were generated by MACE and NaOH surface modification [173].

Nanostructure rebuilding (NSR) process

Another useful approach reported was to treat the MACE b-Si DWS mc-Si wafers with sodium fluoride (NaF) and H_2O_2 solution for inverted pyramid fabrication [162, 165]. The process was named as nano-structure rebuilding (NSR) process. Zheng *et al.* [162] and Jiang *et al.* [165], respectively used the NSR process for modifying the Ag - Cu co-catalyzed and Ag catalyzed MACE b-Si textures. In the former case, NSR process was carried out for (90-360) sec at 55°C. NSR process turned the nano-pores (Figure 3.10 (a) and (c)) to smoother enlarged squares and the edge length of the squares increased with increase in NSR etching time. 360 sec of NSR process resulted in saw mark-free smoother and uniform inverted pyramid textures with a side length of ~ 600 nm as seen in Figure 3.10 (b) and (d). The WAR value of the b-Si samples changed from 6.23% to 16.5% after 360 sec of NSR process, however, ~ 13% lower than the acid textured DWS mc-Si wafers. NSR process modified b-Si cells outperformed the conventionally acid textured mc-Si cells and b-Si cells (without NSR) with a gain in η of 0.58% and 2.33%, respectively. Remarkably improved J_{SC} and V_{OC} value of NSR b-Si cells confirmed the excellent anti-reflection and passivation properties of the inverted pyramidal textures.

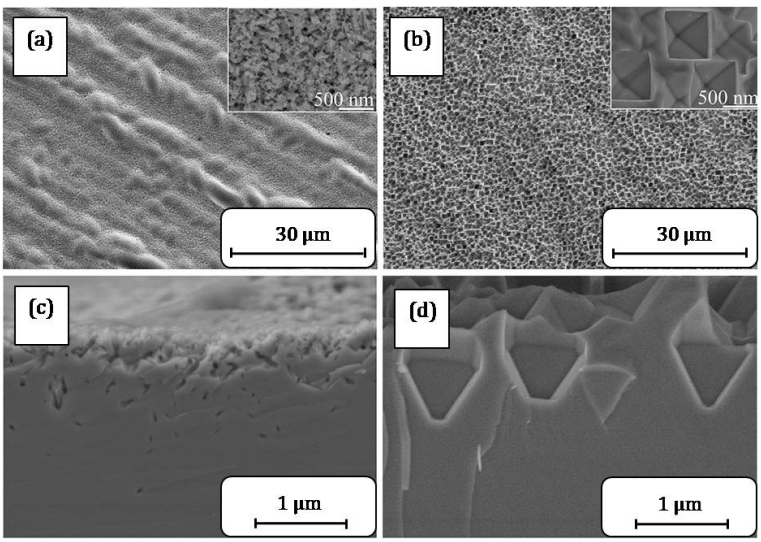

Figure 3.10: SEM images of DWS b-Si mc-Si wafers: (a) top view; (c) angular view before and (b) top view; (d) angular view after 360s of NSR etching [162].

A similar study was reported by Jiang *et al.* on inverted pyramidal texture formation from MACE b-Si by NSR process [165]. The evolution and change in WAR value trends of the inverted pyramid nano-textures with NSR etching time was similar to the

previous work reported by Zheng *et al.* [162]. An η gain of nearly 0.5% were reported for inverted pyramidal textured cells over acid textured DWS mc-Si cells. However, Jiang *et al.* studied the impact of NSR etching beyond 360 sec and observed saturation in inverted pyramid size enlargement in the range of 700 nm. In such a case, more flatter areas have formed between the larger inverted pyramids on the entire wafer surface area and the overall surface reflectance values of samples exceeded 20%. NSR process looked exceedingly promising for the fabrication of inverted pyramidal textures from MACE b-Si features on DWS mc-Si wafers as the obtained inverted pyramidal textures posses excellent light trapping as well as surface passivation properties. In addition, NSR process was applicable to both Ag and Cu catalyzed b-Si samples. However, the cost, stability and safety analysis of the chemicals, especially NaF (since the process is carried out at 55°C) need to be studied before its industrial use.

Reactive ion etching

Recently, Jin *et al.* proposed Cl_2, O_2 and SF_6 plasma mixture based RIE process for the fabrication of inverted pyramids on MACE b-Si textured wafers [133]. As seen in Figure 3.11 (c) and (d), the RIE process selectively etched the trenches formed by the MACE process (see Figure 3.11 (a)) to form inverted nano-pyramid like textures over the entire mc-Si wafer surface area irrespective of crystal orientations. MACE + RIE textured mc-Si wafers exhibited lower surface reflectance (in the short wavelength range) and lower recombination current densities ($J_{0-diffused}$ at front side and $J_{0-undiffused}$ at rear side) compared to both RIE textured (Figure 3.11 (b)) and MACE textured (Figure 3.11 (a)) mc-Si samples. 20.51% batch average η was achieved for MACE + RIE textured batch of PERC cells, absolutely 0.54% and 0.22% higher than that of MACE and RIE batch of PERC cells. Also, the earlier reported disadvantages of RIE texturing such as low Si etch rate and use of an additional DRE process for lattice damage etching were not critical in this case.

Acid etching

Acid etching being the most effective and commonly used method for texturing mc-Si wafers in industry, its usefulness on surface modification of MACE b-Si samples were investigated by many researchers and as of now, it has emerged as the best suited

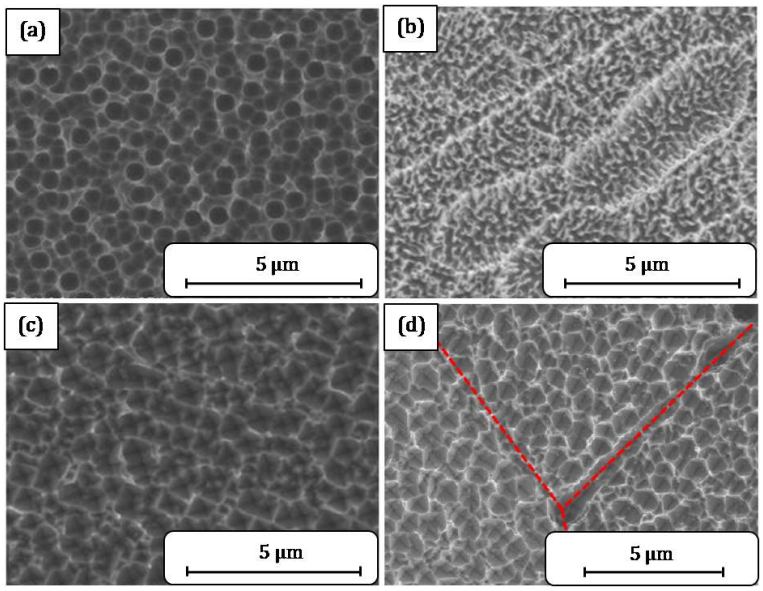

Figure 3.11: The SEM images of the (a) MACE textured, (b) RIE textured, and (c) MACE+RIE textured mc-Si wafers, respectively. (d) represents MACE+RIE textures in three crystal grains and the grain boundaries are separated by red lines [133].

method for the essential surface modification step in MACE b-Si solar cells. Guoy Su *et al.* used acid texturing process (HF - HNO_3 - H_2O_2 etching followed by 0.5% KOH dip) for the fabrication of inverted pyramidal textures on MACE b-Si DWS mc-Si wafers [166]. The MACE b-Si nano-structures were enlarged to form nano-sized inverted pyramids as shown in Figure 3.12 (a), (b) and (c) for acid etching time of 1 min, 3 min, and 6 min, respectively. The WAR values of b-Si samples were increased from 3.82% to 25.5% after 6 min of acid etching, still, ~11% lower than that of conventionally acid textured DWS mc-Si wafers. The τ_{eff} values of b-Si samples improved from 14.64 μs to 43.60 μs, 55.89 μs and 58.09 μs, respectively after 1 min, 3 min and 6 min of acid texturing, confirming the improvement in surface texture quality after b-Si surface modification. 3 min acid textured b-Si solar cells exhibited the highest η of 19.07% with a maximum J_{SC} of 37.55 mA/cm^2, which corresponds to 0.6% (absolute) gain in η compared to the acid textured DWS mc-Si cells. However, the WAR values of 3 min acid textured b-Si samples were 19.46% and 6.70%, respectively before and after ARC deposition and the WAR values are relatively higher compared to the WAR value of MACE inverted textures formed by NSR and RIE processes [133, 162, 165]. In addition, the τ_{eff} and V_{OC} values of 3 min acid textured (optimized process conditions in this case) MACE b-Si cells were ~ 6 μs and 2 mV lower than the acid textured DWS mc-Si

samples, suggesting the need for further optimization of acid texturing process window in achieving similar texture quality as that of the acid textured DWS wafers.

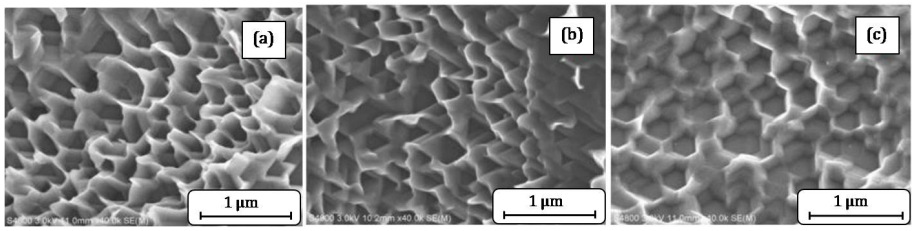

Figure 3.12: SEM images of MACE b-Si inverted pyramid textures after acid texturing for (a) 1 min (b) 3 min and (c) 6 min [166].

Apparently, Wang *et al.* also proposed HF - HNO_3 acid texturing process for MACE b-Si surface modification [135]. Unlike the previous work [166], final dilute KOH rinse was not done for MACE samples after acid etching in this case. Acid etching produced uniformly distributed 500-800 nm sized inverted pits on MACE b-Si DWS mc-Si wafers as shown in Figure 3.13 (d). The results of acid etched MACE b-Si wafers were compared with the acid textured MWSS (Figure 3.13 (a)), additive-based acid textured DWS (Figure 3.13 (b)) and RIE textured DWS (Figure 3.13 (c)) mc-Si wafers. The WAR and τ_{eff} values were 31.0% and 58.1 μs, 25.3% and 42.6 μs, 15.1% and 66.2 μs, and 23.2% and 101.3 μs, respectively for acid textured DWS, acid textured MWSS, RIE textured DWS and acid etched MACE b-Si DWS mc-Si samples. MACE acid etched solar cells exhibited better performance than the acid textured DWS and acid textured MWSS cells with an overall enhancement in V_{OC} and J_{SC} of 0.7 mV and 0.64 mA/cm^2 and 1.8 mV and 0.29 mA/cm^2, respectively. Significantly improved light absorption of RIE wafers and excellent surface passivation quality of MACE acid DWS mc-Si samples, respectively contributed to 0.59 mA/cm^2 enhancement in J_{SC} for RIE cells and 1.3 mV improvement in V_{OC} for MACE acid textured cells in comparison to each other, recording an excellent overall batch average η of 18.86% and 19.05%, respectively for the MACE acid etched and RIE textured solar cells. This difference in η become insignificant considering the cost-effectiveness of MACE technology over RIE. However, the reported WAR of 23.2% was higher for modified MACE b-Si samples compared to the approaches discussed earlier in this section. From our previous discussions it can be inferred that appropriate process optimization of acid etching process used for b-Si surface modification potentially can suppress the surface reflection loss further without compromising the

τ_{eff} values. In addition, examining the impact of KOH rinse after etching for MACE b-Si surface modification is essential for standardizing the process fully to its potential.

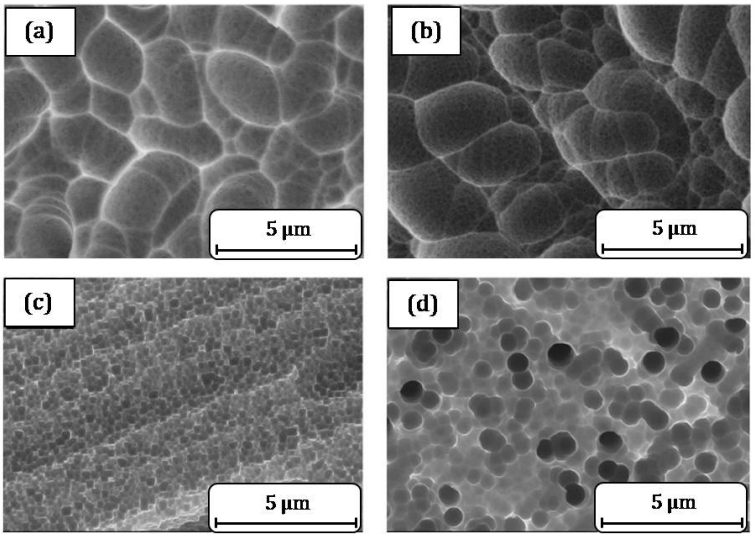

Figure 3.13: Top view SEM images of mc-Si wafers: (a) acid textured MWSS; (b) acid textured MWSS; (c) RIE textured DWS; and (d) MACE acid textured DWS [135].

3.4 Conclusions

In this chapter, we reviewed DWS technique and its implications on existing wet texturing techniques. The wet texturing issues were more severe for mc-Si wafers as the relatively thinner and fewer saw damage layer of DWS wafers renders the acid texturing process ineffective. Alternative texturing methods reported for overcoming the acid texturing issues of DWS c-Si wafers including MACE are reviewed further. The comprehensive literature review indicates that MACE b-Si approach has the potential to become the next generation texturing scheme for mc-Si wafers because of its cost-effectiveness, high throughput, and improved performance in comparison with acid texturing process.

Chapter 4

Experimental and Characterization Techniques

This chapter discuss the process flow used for the fabrication of lifetime test structures, and the theory behind some of the measurement techniques for characterizing the lifetime structures and solar cells used in this thesis.

4.1 Carrier lifetime measurements

In this thesis, the passivation properties of textured wafers are tested in two ways. The surface texture quality of the as-textured mc-Si wafers were evaluated by immersing the respective textured wafers in a passivating solution containing quinehydrone and methanol (QHM). Also, symmetrically diffused and passivated lifetime test structures are fabricated for extracting the emitter recombination current density (J_{0e}) values following the process flow given in Figure 4.1. The textured wafers are first subjected to phosphorous diffusion (on both the sides of the wafer) in a tube furnace (Protemp USA, Sirius PRO200) and 2% HF bath to etch out the PSG layer formed during emitter formation. Further an ultra thin silicon oxide (SiO_2) passivation layer is grown on diffused wafers by low temperature oxidation (LTO) process at 600 °C for 1 hour in the same tube furnace. Silicon nitride (SiN_X:H) ARC passivation layer is deposited on top of the ultra thin oxide layer on both sides by PECVD technique using Plasmalab 100 tool from Oxford Instruments. Finally, samples underwent firing at 770 °C (cell firing temperature used for baseline cell fabrication at NCPRE) in a RTP firing chamber

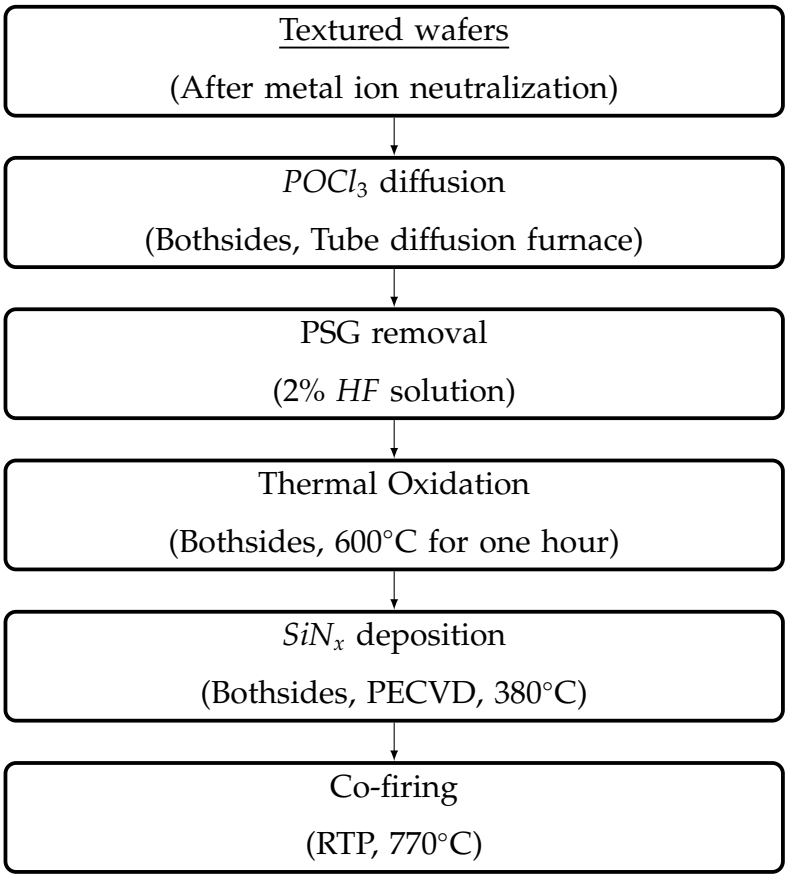

Figure 4.1: Process flow diagram of fabricating lifetime test structures.

(Allwin21 Corp.,AW 610) to complete the process flow. The passivation study in QHM solution and the fabricated symmetrically diffused and passivated lifetime test structures are referred to as chemical passivation and physical passivation, respectively in this thesis.

The minority carrier lifetime values were measured using quasi-steady state photoconductance (QSSPC) lifetime tester from Sinton Instruments (WCT 120). Sinton lifetime tester measures the effective minority carrier lifetime using the following formula,

$$\frac{1}{\tau_{Eff}} = \frac{1}{\tau_{Bulk}} + \frac{S_{Front}}{W} + \frac{S_{Back}}{W} \tag{4.1}$$

Where, τ_{Eff} and τ_{Bulk} are effective minority carrier lifetime and bulk lifetime, respectively in sec. S_{Front} and S_{Back} are the surface recombination rates at the front and rear surfaces, respectively in cm-sec^{-1} . W represents the wafer thickness in cm. The τ_{Bulk} factor consists of three components; radiative recombination, Auger recombination and Shockly-Read-Hall recombination, represented the corresponding lifetime of τ_{Rad},

τ_{Aug}, and τ_{SRH} in sec,

$$\frac{1}{\tau_{Bulk}} = \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}} \tag{4.2}$$

Since double side textured samples are used for chemical passivation studies and lifetime measurements are carried out by soaking the wafers in QHM solution, S_{Front} = S_{Back} = S_{Eff} and equation 4.1 reduces to,

$$\frac{1}{\tau_{Eff}} = \frac{1}{\tau_{Bulk}} + \frac{2S_{Eff}}{W} \tag{4.3}$$

Wafers with similar bulk lifetime are used for lifetime experiments, so that the τ_{Eff} value measured by chemical passivation is a direct indication of the surface passivation quality.

J_{0e} value is extracted from the inverse Auger corrected lifetime curves plotted against excess carrier concentration (Δn) following the method proposed by Kane and Swanson [174]. For the J_{0e} value extraction, lifetime measurements are carried out for symmetrically diffused and passivated test structures. The τ_{Eff} of lifetime test structures can be modeled and expressed as,

$$\frac{1}{\tau_{Eff}} - \frac{1}{\tau_{Aug}} = \frac{1}{\tau_{SRH}} + \frac{(J_{0e(front)} + J_{0e(back)})(N_{Dop} + \Delta n)}{qn_i^2 W} \tag{4.4}$$

where, $J_{0e(front)}$ and $J_{0e(back)}$ are the front and back emitter saturation current density values respectively, in A-cm^{-2}, N_{Dop} is the backround doping concentration of the substrate in cm^{-3}, q is the elementary charge value, n_i is the intrinsic carrier concentration in cm^{-3}. Since the lifetime test structure used are both side textured and diffused (n^+-p-n^+) with similar SiO_2-SiN_X:H passivation on both sides, then $J_{0e(front)}$ and $J_{0e(back)}$ values are identical, i.e. $J_{0e(front)}$ = $J_{0e(back)}$ = J_{0e}. Under this condition, the J_{0e} component is deducted by taking the differential of $\frac{1}{\tau_{Eff}}$ - $\frac{1}{\tau_{Aug}}$ curve with respect to Δn in high injection regimes ($\Delta n >> N_{Dop}$). The deduced expression used for the extraction of J_{0e} follow as,

$$J_{0e} = \frac{qn_i^2 W}{2} \frac{d(\frac{1}{\tau_{Eff}} - \frac{1}{\tau_{Aug}})}{d\Delta n} \tag{4.5}$$

J_{0e} is a direct measure of surface recombination at the emitter surface in solar cells.

4.2 Current - voltage measurements of solar cells

The performance of fabricated solar cell are tested by extracting the performance parameters from the lighted current-voltage (I-V) curves. The I-V measurements are carried out at unified testing conditions, commonly known as standard testing conditions (STC) defined by IEC standard 60904 [175]. The primary STC include; (i) illumination spectra of lamp should match with AM 1.5G spectra, (ii) measurement temperature should be 25 °C and the illumination intensity should be 1000 W-m^{-2}. The current density - voltage (J-V) and power - voltage (P-V) curves of a large area silicon solar cell fabricated at NCPRE is depicted in Figure 4.2. The V_{OC} and J_{SC} points marked in Figure 4.2, respectively represent the open circuit voltage and short circuit current density values. The maximum power point in the P-V curve is named as P_{MPP} and the corresponding voltage (V_{MPP}) and current density (J_{MPP}) values in the I-V curve are used for estimating efficiency (η) and fill factor (FF) values.

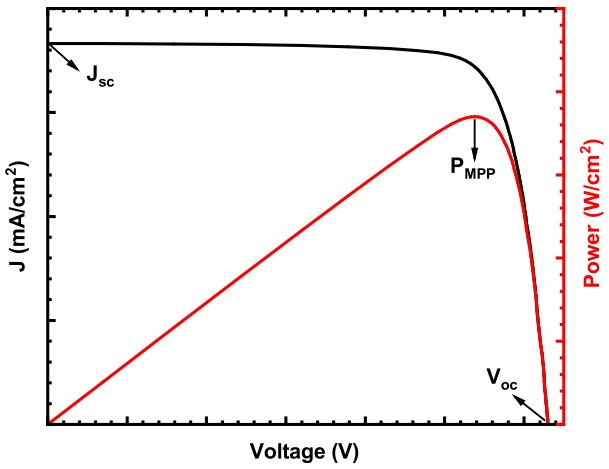

Figure 4.2: The I-V (black) and P-V (red) curves of a large area silicon solar cell measured using Abet Technologies AAA solar simulator.

$$\eta = \frac{P_{MPP}}{P_{In}} \tag{4.6}$$

Where, P_{In} is the irradiance incident on the solar cell, which is equal to 1000 W-m^{-2} under STC. Further FF is calculated from,

$$FF = \frac{P_{MPP}}{V_{OC} \times J_{SC}} = \frac{V_{MPP} \times J_{MPP}}{V_{OC} \times J_{SC}} \tag{4.7}$$

In this thesis, all the I-V measurements are conducted using a class AAA solar simulator from ABET technologies. Apart from the performance parameters (V_{OC}, J_{SC}, FF, and η), series resistance (R_S) and shunt resistance (R_{SH}) values of solar cells are also extracted, respectively from the I-V curves measured at two different illumination (1 sun and 0.1 sun) intensities following Bowden method [176] and from the slope of dark I-V curve in the range of -50 mV to 50 mV.

4.3 Quantum efficiency measurements

Quantum efficiency (QE) is defined as the ratio of number of electrons collected in the contact to number of photons incident on the sample. QE of a solar cell includes both optical and recombination losses. Ideally QE measurements are carried out close to the metal contact using a low intensity photon source so that resistive paths (series resistance) in solar cells do not influence the accuracy of measurement. In order to segregate the effect of optical and recombination losses, QE is classified as external QE (EQE) and internal QE (IQE). EQE refers to the ratio of electrons collected to the total number of photons incident on the sample area, which include both reflection from the sample surface and transmission through the sample as well. In contrast, IQE is defined as the ratio of total number of photons collected to the total number of electrons absorbed (excluding reflection and transmission losses) in the sample. It imply that IQE solely refers to recombination loss contribution in short circuit current. Further, IQE and EQE can be related as,

$$IQE = \frac{EQE}{1 - (R + T)} \tag{4.8}$$

Where R and T, represents the reflection and transmission losses in solar cells. For silicon solar cells with full area metal at the rear side, used in this study, the transmission loss through the samples is zero. Hence, equation 4.8 becomes,

$$IQE = \frac{EQE}{1 - R} \tag{4.9}$$

Following the equation 4.9, the wavelength dependent IQE values of solar cells are estimated from the measured EQE and reflectance values.

In this thesis, PVE-300 tool from Bentham instruments was used for QE measurements. The area of illumination was 1 mm × 5 mm and light with varied wavelength ranging from 300 nm to 1200 nm was used for generating QE curves. Representative QE (IQE and reflectance) curves of an industrial mc-Si solar cell is shown in Figure 4.3. Sharp falls in IQE values at blue wavelength (300 nm to 500 nm) and longer wavelength region (900 nm to 1200 nm), respectively are due to the surface recombination occurring at the front and rear sides of the solar cell. IQE values in the mid wavelength range is representative of the substrate bulk quality. Hence, IQE in combination with reflectance can be effectively used for comparing both optical and recombination properties of differently textured solar cells.

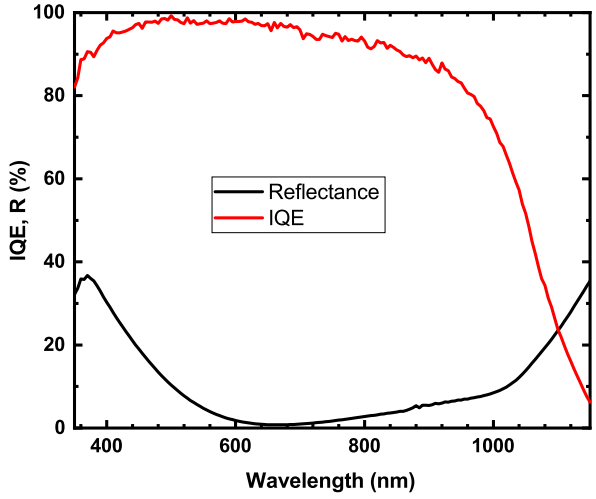

Figure 4.3: The line scan QE (black for reflectance, red for IQE) curves of industrial mc-Si silicon solar cell measured using PVE-300 tool from Bentham instruments.

However, the spot scan QE measurements may not be representative of the whole solar cell if there are non-uniformities, especially for mc-Si solar cells as different grains present in mc-Si wafer surface exhibit different surface reflection. Hence, light beam induced current (LBIC) IQE and reflectance maps are used comparing the optical and recombination properties of solar cells. We have used the four available wavelengths in our LBIC tool (Semilab WT-2000PVN); 407 nm, 658 nm, 877 nm, and 986 nm for the analysis in this work. In addition, the front surface recombination velocity (FSRV)

and back surface recombination velocity (BSRV) maps of solar cells are generated from the LBIC IQE and reflectance maps following the methods shown in [177] and [178], respectively.

4.4 Photoluminescence measurements

Optical absorption in semiconductor results in electron-hole pair generation inside the semiconductor. Further, these light generated carriers are recombined via radiative and non-radiative paths. Radiative recombination results in light emission with energy equivalent to the band gap and this phenomenon is known as photoluminescence (PL). The efficiency of luminescence (n) is given by,

$$n = \frac{R_{Rad}}{R_{Rad} + R_{nRad}} \tag{4.10}$$

where R_{Rad} and R_{nRad}, respectively represent radiative and non-radiative recombination rates. Further, the recombination rates are related to Δ n by,

$$R_{Rad} = \frac{\Delta n}{\tau_{Rad}}, \quad R_{nRad} = \frac{\Delta n}{\tau_{nRad}} \tag{4.11}$$

where, τ_{Rad} and τ_{nRad}, respectively represents the radiative carrier lifetime and non-radiative carrier lifetime values. Further, they are related to effective minority carrier lifetime (τ_{Eff}) by

$$\frac{1}{\tau_{Eff}} = \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{nRad}} \tag{4.12}$$

Since silicon is an indirect band gap material, most of the recombination occurs via non-radiative paths. However, the minimal amount of radiative recombination (PL) occurring in silicon can be effectively utilized for studying its electronic properties.

In thesis, PL images are captured using Lumisolar EL/PL system from Greateyes, which primarily use two arrays of 660 nm wavelength LEDs as an illumination source. For measurements, a silicon CCD camera is mounted above the sample placing chuck and the luminescence signal are filtered by 960 nm high pass filter to cut off the input LED signal and to recieve only the emission signal near the band gap. The maximum resolution of CCD camera and static thermal noise were 1024 $\times$ 1024 and 500-600 nm

pixel intensity, respectively. Further, the noise in the images are eliminated in the software itself by subtracting background images from the captured images.

The single diode circuit model used for PL image analysis is shown in Figure 4.4. Each pixel constitutes of current source ($J_{light,i}$) and an ideal diode current (J_i) as marked in the Figure. The other parameters used for the analysis are also marked in the Figure 4.4. Now, the pixel intensity of PL (Φ_i) is directly proportional to the diode voltage (V_i) following the exponential relation given below,

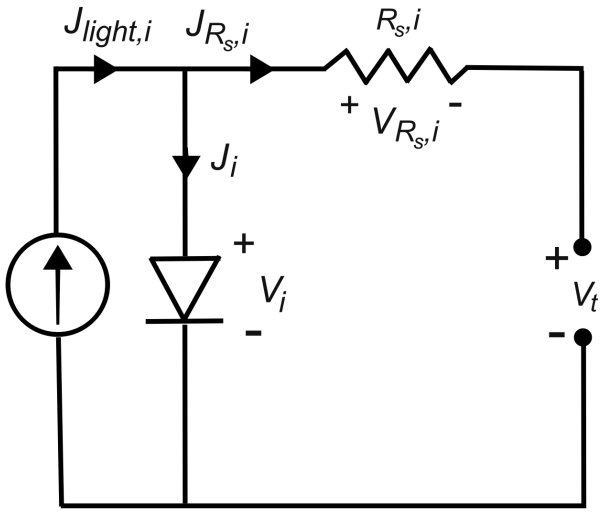

Figure 4.4: Equivalent circuit of a single node (pixel) of solar cell. Single diode model is used for explaining the working mode of PL images.

$$\Phi_i = C_i exp(\frac{qV_i}{KT}) \tag{4.13}$$

Where, C_i is the calibration constant. K, T and q, respectively represents the Boltzman constant, temperature and elementary charge. Now in accordance with the equation 4.13, under open circuit conditions, Φ_i is exponentially proportional to the quasi fermi-level separation or open circuit voltage of solar cells. This imply that, PL images at open circuit conditions can be used for comparing the passivation properties of solar cells under similar illumination conditions. In all measurements, identical illumination conditions are imposed on solar cells by normalizing the PL intensity with measured reflectance at 660 nm. PL images at open circuit conditions are extensively used in thesis for comparing the passivation properties of lifetime test structures and solar cells fabricated on different surface textures.

PL imaging technique can be applied to generate series resistance maps as well. PL images at different bias (BPL) are utilized for generating the series resistance maps. From the equivalent circuit shown in Figure 4.4, pixel series resistance $R_{S,i}$ can be extracted using the formula,

$$R_{S,i} = \frac{\Delta V_{R_{S,i}}}{\Delta J_{R_{S,i}}} = \frac{\Delta V_i - \Delta V_t}{\Delta J_{light,i} - \Delta J_i} \tag{4.14}$$

Now incorporating the relation between V_i and Φ_i (shown in equation 4.13) to equation 4.14 can be utilized for obtaining the series resistance maps. There are several methods available to simplify the equation 4.14 further and for eliminating the calibration constant in equation 4.13. We followed the Kampwerth method for generating series resistance maps in this work [179].

4.5 Summary of other characterization tools

Summary of the other characterization tools used in this thesis is given in Table 4.1.

Table 4.1: Summary of different characterization tools used in thesis.

Serial No.	Tool Name	Manufacturer and Make	Remarks
1	3D optical microscope	Zeta Instruments, ZETA-20	Size and height estimation of pyramid textures
2	Spectrophotometer with integrating sphere	Perkin Elmer, Lambda 950	Reflectance and transmission study
3	Four probe	Jandel,MHP-12 & Multi-PT8.	Diffusion uniformity analysis
4	SEM imaging	Zeiss Ultra 55	Morphology analysis
5	Electrochemical capacitance voltage	WEP CVP21	Diffusion profile measurement
6	Ellipsometer	Semilab SE 2000	Thickness, refractive index and extinction coefficient measurements
7	Dark lock in thermography	PV-LIT Infratec GmbH	Two diode model performance parameter mapping

Chapter 5

Novel Low-cost Alkaline Texturing Process for DWS c-Si Wafers

5.1 Motivation

As discussed earlier, the immediate adoption of DWS wafers has resulted in wet texturing challenges. An SDR process that completely etch out the unwanted saw damages, wire impressions and a-Si layer present on the DWS wafer surface was the need of the hour in c-Si solar cell industry. Pretreatment processes using HCl-H_2O_2 solution, KOH or NaOH based SDR solution, and HF-HNO_3 acid based SDR solution were tried for SDE of DWS wafers [9, 10]. However, all of the above processes were incapable of completely removing the saw marks impressions. In contrast, Chen *et al.* successfully reported a TMAH based SDR process for DWS c-Si wafers [8]. However, TMAH solution is a relatively expensive chemical (US $250/litre) and corrosive. Moreover, an additional pre-SDR wafer clean makes this method inappropriate for industrial applications.

In this chapter, we propose a novel low-cost and industrially viable approach for pyramidal texturing of DWS c-Si wafers. The proposed process combines a novel single step low-cost SDR solution with a new combination of KOH and NaOCl, followed by silicate pyramidal texturing process [6] for generating uniform and smaller pyramids of ~2-4 μm size. Unlike TMAH based SDR process, additional cleaning processes are not required, which makes our process industry-friendly and productive.

5.2 Experimental methods

5.2.1 Texturization

The texturing processes were performed on both MWSS and DWS as-cut industrial grade CZ c-Si wafers (6 inch pseudo-square, boron doped, p-type, <100> orientation, 2 Ω-cm resistivity, 160 - 180 μm thickness). For MWSS (Group 1) and one group of DWS (Group 2) wafers, our novel SDR process was applied. In this process, all these wafers underwent single step pre-cleaning and SDR process using a novel KOH (8% by weight) and NaOCl solution (laboratory grade, 6%) in a ratio of 1:1 (by volume). The SDR process time varied from 1 - 6 min to generate an optimized process time of 3 min at a temperature of 80°C for the DWS wafers (Group 2). However, for the MWSS wafers of Group 1, 10 min of SDR time was applied to etch 3-4 μm of Si from each side, which is similar to the earlier reported one [180]. For the pyramidal texturing of both the MWSS and DWS wafers, the silicate based low-IPA texturing process [6] was used. The other group of DWS wafers (Group 3), underwent pre-cleaning in HCl - H_2O_2- de-ionised (DI) water solution followed by SDR in 25% TMAH solution at 90°C for 90 sec as per an existing process report [8]. After SDR, the texturing was performed with 2% KOH solution mixed with commercial additive, GP Alkatex at 80°C [8]. Alkatex texture additive contains 2-5% sodium 2-ethylhexanoate. The Group 1, Group 2 and Group 3 wafers, respectively are termed as existing MWSS, novel DWS and existing DWS texturing processes. All three Groups of wafers underwent neutralization process in 50% (by volume) HCl acid solution mixed with 250 ml of H_2O_2 at 70°C for 10 min followed by a dip in 2% (by volume) HF solution. The complete texturing process flow of MWSS (Group 1) and Group 2 DWS wafers using new recipe of KOH - NaOCl SDR solution is shown in Figure 5.1. After texturing all the MWSS and DWS wafers were processed together as a single batch to fabricate cells.

5.2.2 Cell fabrication

After texturing of all the MWSS and DWS c-Si wafers, 25 wafers each from all the three Groups were taken for further studies. The diffusion was performed in a tube diffusion furnace (Protemp USA, Sirius PRO 200) using phosphorus oxychloride as the

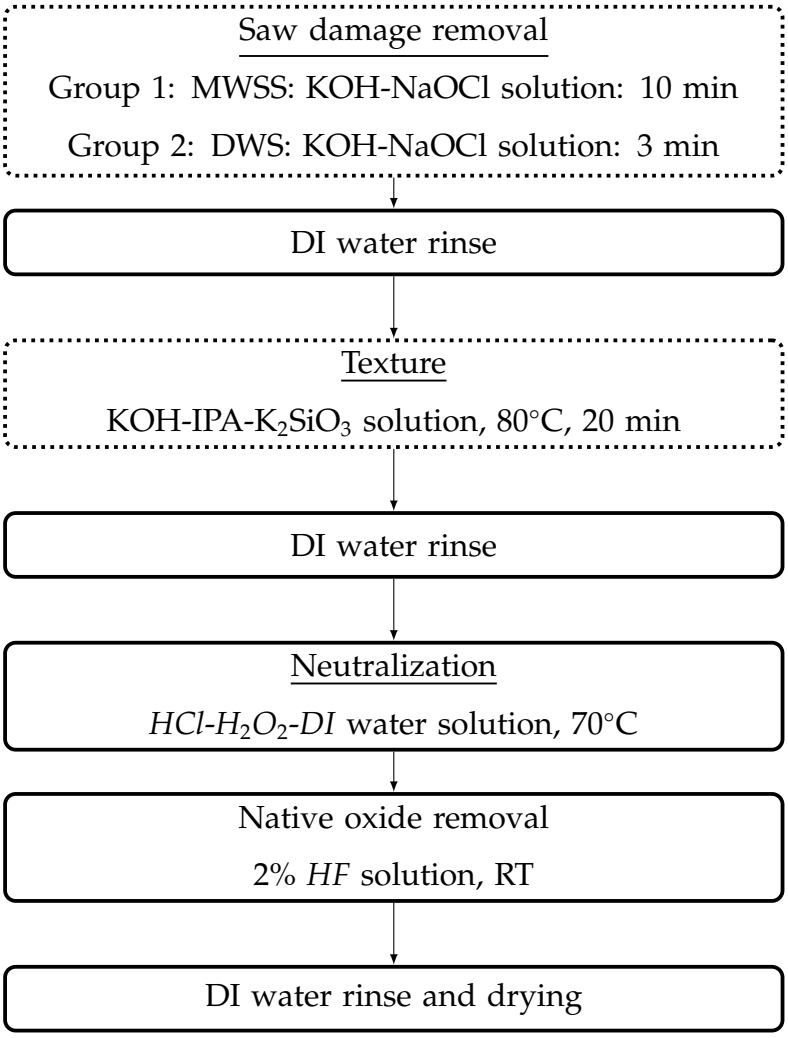

Figure 5.1: Process flow diagrams of the novel texturing processes. The modified process steps are shown as dashed boxes in the figure.

dopant source at 820°C peak diffusion temperature with a target R_{Sheet} of 80 Ω/sq. After the phosphosilicate glass (PSG) removal step in dilute HF solution, low temperature thermal oxidation (LTO, 1 hour 600°C) was carried out on the diffused wafers. SiN_X:H passivation and ARC layer was deposited by PECVD using Oxford Instruments, Plasmalab System 100 at 380°C. The deposited SiN_X:H film has refractive index of 2.00 (at 633 nm) and thickness of 90 nm as measured on our test sample of polished c-Si wafer. After dielectric deposition, 20 wafers from each Groups of the MWSS and DWS wafers (excluding representative lifetime samples) underwent plasma edge isolation using BSET EQ, NT-2. Lastly, front and rear contacts were formed by screen printing (Haiku Tech, P200S) and subsequently co-fired in a rapid thermal processing (RTP) unit (Allwin21 Corp., AW 610). The metallization pastes used were Monocrystal, PASE-1207

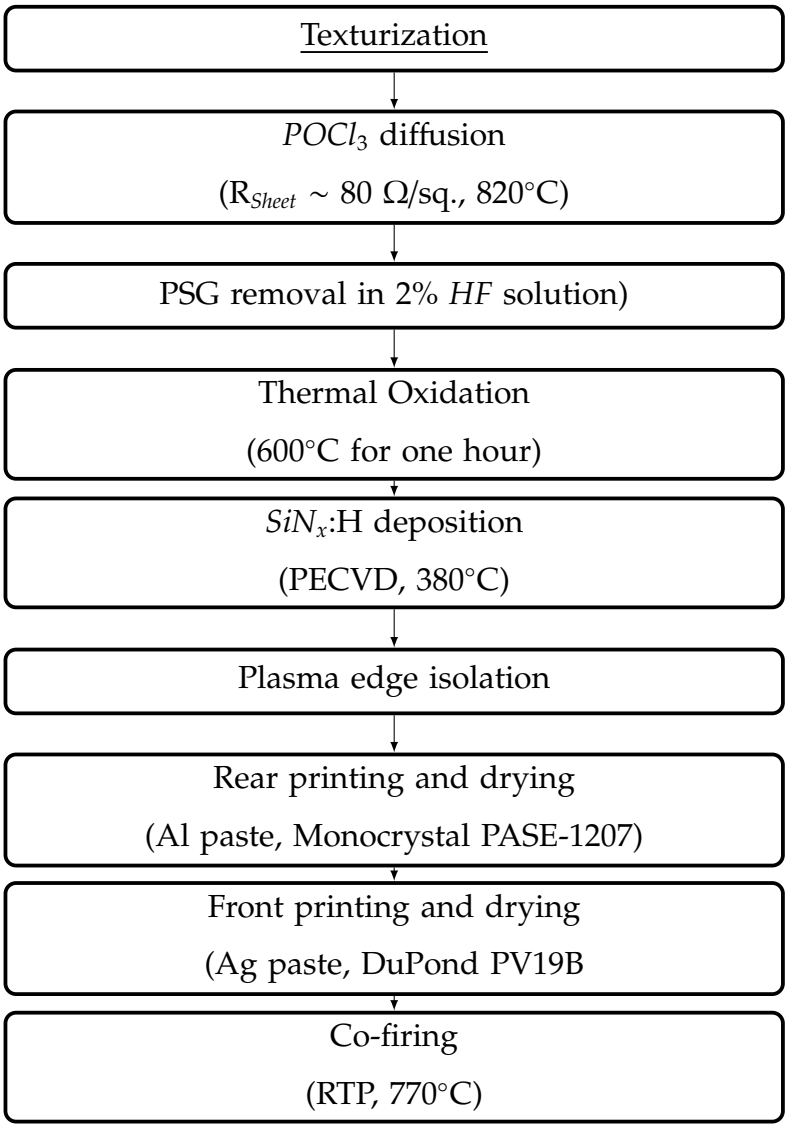

Figure 5.2: Schematic illustration of the solar cell processing flow used in this chapter.

and DuPont PV19B for the rear aluminium (Al) and front silver (Ag), respectively. A summary of the solar cell fabrication sequence is shown in Figure 5.2.

5.3 Noval SDR process

The chemical reaction of the NaOH - NaOCl process around 80°C is well understood [17, 20]. It was already used as an SDR solution for the MWSS c-Si pyramidal texturing [20] and for multicrystalline Si wafer polishing [17] processes. The final chemical reaction is given below [17]:

$$3NaOCl + 4NaOH + 2Si + H_2O \rightarrow 7Na^+ + 2Cl^- + OH^- + HOCl + SiO_2 + Si(OH)_2 \quad (5.1)$$

Thus the overall reaction (as shown in eqn.(5.1)) results in Si etching (by forming silicon hydroxide complex, $Si(OH)_2$), an oxidised Si surface (SiO_2) and hypochlorous acid (HOCl) formation. This way NaOCl oxidizes other surface contaminants present on the Si wafer. Simultaneously highly reactive chlorine ions (Cl^-) react with hazardous metallic impurities and dissolve them in the solution as soluble chlorides. In our process, NaOH is replaced by KOH. We initially tried to use the existing KOH - NaOCl process [20]. However, the process is fast because within two min at 80°C, it removed ~3 μm of Si per side for the DWS c-Si wafers. After alkaline texturing using these SDR wafers, uniform pyramid formation could not be achieved. The reason behind the non-uniform texturing of the DWS wafers with the existing process is that the DWS wafers have lesser damaged surface as compared to earlier used MWSS wafers [8]. So the existing recipe was thus needed to be modified to have slower Si etch rate. However, reduction of Si-etching time for this SDR solution generated non-uniformity on the SDR surface; thus became unsuitable for uniform pyramid formation over the entire DWS wafer.

In our novel SDR process, we have used a new composition (mentioned in section 5.2.1) of KOH and NaOCl solution. This solution has lower Si etch rate as compared to the existing SDR solution to generate smooth but damage free DWS Si surface. For the SDR duration optimization, the as-cut DWS wafers were etched for 1 - 6 mins. Figure 5.3 shows the variation of Si removal for each side for 1-6 min of SDR time. The Si-etch rate was found to be varying from 0.3-2.2 μm/side of the Si wafer. Besides, this graph (see Figure 5.3) also show a nearly linear etch depth with time over the entire duration and thus allows us to fix the required duration easily. The variation of WAR of the SDR surface after variable SDR durations is also shown in Figure 5.3. The values of WAR varies little (34.2 - 35.2%) within SDR time of 3-6 min.

The SEM micrographs of the as-cut DWS c-Si surfaces without and with SDR durations upto 6 min are shown in Figure 5.4. The wire-saw marks are clearly visible in the images from Figure 5.4(A) to Figure 5.4(C) for SDR time upto 2 min. However, these marks are not visible when the etching time extend from 3 min to 6 min (see Figure 5.4(C) - 5(G)). Hence a minimum SDR time of 3 min looks essential to etch the wire-saw marks.

For alkaline texturing, we thus need to select the appropriate and optimum SDR

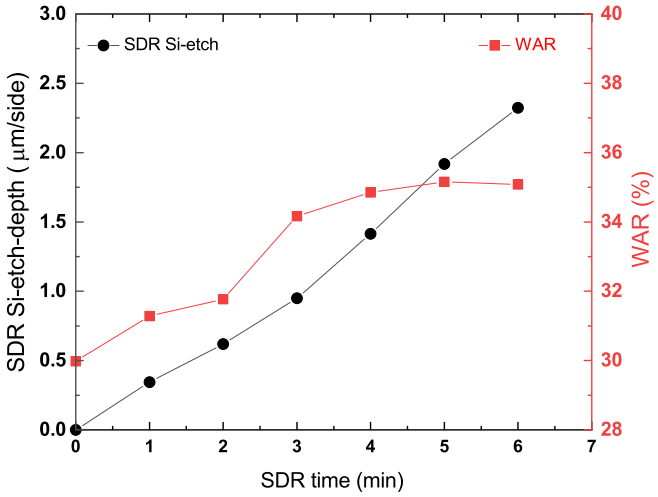

Figure 5.3: The variations of Si etch depth per side and the weighted average reflectance (WAR) with the SDR time upto 6 min in the novel SDR process are shown. WAR value is weighted using the AM 1.5G solar spectrum over the 300-1000 nm wavelength range.

time to secure the formation of uniform pyramids. We selected 3 min SDR time for three major reasons. Firstly, this time is enough to remove saw-marks on the DWS wafers; secondly, lower time generates higher SDR bath lifetime to minimize the process cost, and finally, low processing time ensures high throughput desirable from industrial point of view. However, for comparison, we have prepared the MWSS c-Si wafers with a SDR time of 10 min. This 10 min of SDR time etched nearly 3 μm/side for these wafers in the present SDR solution and was necessary to generate the required damage free SDR surface before final alkaline texturing step.

5.4 Silicate-based texturing process

The use of K_2SiO_3 additive in the KOH-IPA texture solution is already explained in section 2.1.2 of chapter 2. Formation of pyramids of this DWS wafer surfaces were studied after texturing times of 5, 10, 15 and 20 min. Figure 5.5 shows the variations of the amount of Si etched from each side and the variation of WAR during the complete texturing process of 20 min. Unlike Si-etch during SDR, Si-etch with time in texture is not linear (see Figure 5.5). The reason behind this is the surface area increase by the formation of more pyramids with increased texture duration. For the understanding

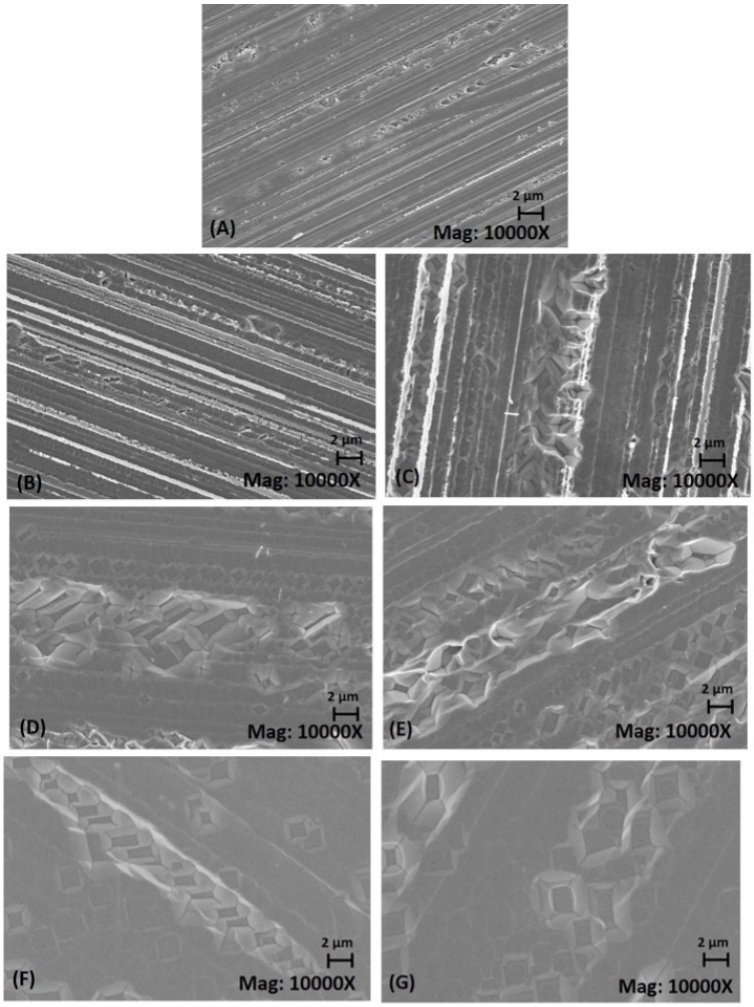

Figure 5.4: SEM micrographs (planar view, magnification = 10000X) of the c-Si wafer surfaces fabricated using the novel SDR process for durations: (A) No SDR (as-cut surface), (B) 1 min, (C) 2 min, (D) 3 min, (E) 4 min, (F) 5 min, and, (G) 6 min.

of the pyramid nucleation on our novel SDR wafer surface, we studied SEM images of the textured surfaces with the increase in texture time. Figure 5.6 shows the SEM images (both planar view and angular view of 45°) of the pyramidal structure formed on our SDR DWS Si wafer surface after different texturing times of 5, 10, 15 and 20 min. The lower magnified (1000X) images in the planar view of the surface (Figure 5.6 (N-1) - Figure 5.6(N-4)) depict the formation of uniform pyramidal surface over a large area of the textured surface. After final texturing time of 20 min, Figure 5.6(N-4) shows no existence of saw-marks or any non-pyramidal space on the textured wafer surface. High magnified (10000X) images of the same surface (Figure 5.6 (A-1) - Figure 5.6(A-4)) demonstrate the optical surface quality of the pyramids from the beginning

to the completion of the texture process in 20 min duration. The uniform pyramid formation over the entire Si wafer surface also establishes successful removal of the a-Si layer from the as-cut DWS c-Si wafer surface in our SDR process in 3 min.

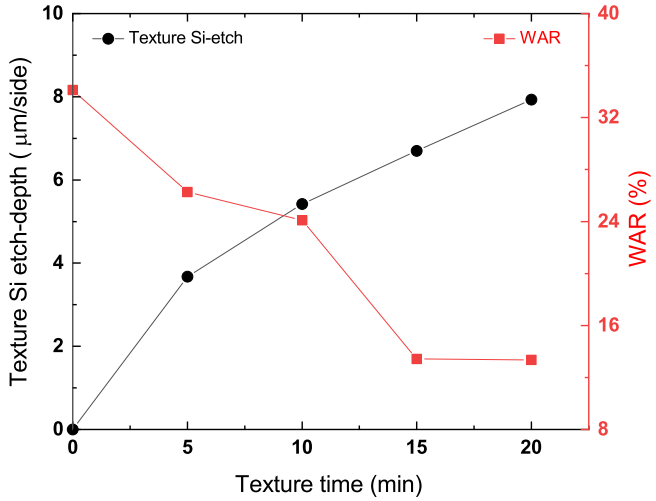

Figure 5.5: The variations of Si etch depth per side and WAR with the texturing time up to 20 min.

5.5 Quantitative analysis of pyramid formation

The uniformity of pyramid formation for the three Groups of textured wafers was analyzed by using Zeta 3D microscope and the pyramid statistics is shown in Table 5.1. It provides the quantitative idea about the pyramid sizes and heights of the representative textured wafers as shown in Figure 5.7. The average pyramid sizes are 2.6 μm (Face-1) and 2.5 μm (Face-2), 2.8 μm (Face-1) and 2.8 μm (Face-2), and 2.5 μm (Face-1) and 2.6 μm (Face-2) for Groups 1, 2, and 3, respectively. Average pyramid heights are 2.3 μm (Face-1) and 2.5 μm (Face-2), 2.5 μm (Face-1) and 2.5 μm (Face-2), and 2.2 μm (Face-1) and 2.3 μm (Face-2) for Groups 1, 2 and 3, respectively. These values are measured on both the faces over the field of view (FOV) of 95 μm x 71 μm for each measurement. The pyramid sizes over this area varies with a standard deviation of 0.6 μm, 0.7 μm and 0.6 μm for Groups 1, 2 and 3, respectively. Nearly similar values of average pyramid sizes, heights and their variations ensures the applicability of our proposed novel texturing process for the DWS c-Si wafers.

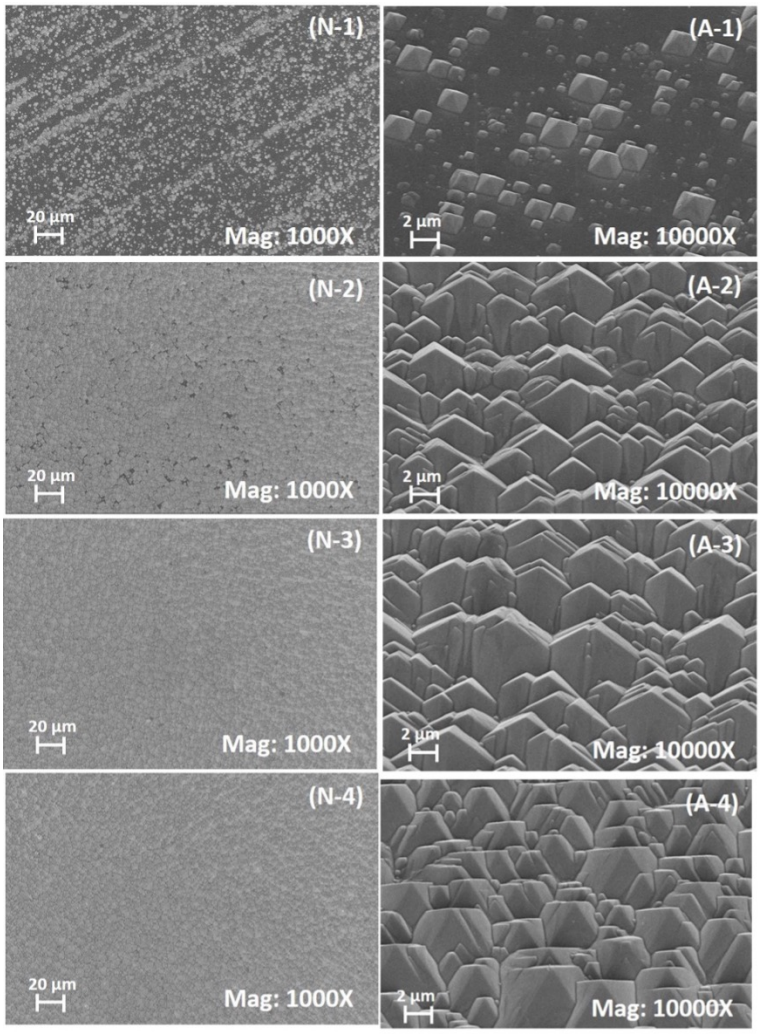

Figure 5.6: SEM micrographs of the final textured c-Si wafer surfaces fabricated using the novel SDR process after different times of texturing. N-1 to N-4 shows the planar view of wafers after 5, 10, 15 and 20 min, respectively with a magnification of 1000X. Similarly, A-1 to A-4 shows the angular view at 45° tilt of wafers after 5, 10, 15 and 20 min, respectively with a magnification of 10000X.

5.6 Surface reflectance analysis

The variation of WAR on both the faces of representative textured c-Si wafers from all the groups are shown in Figure 5.8. In-spite of different surface conditions of the starting c-Si wafers, the novel texturing process yields nearly similar WAR values on both the faces of the textured wafers before and after ARC. These spectral reflectance values certainly confirm excellent optical properties of textured wafers from different Groups.

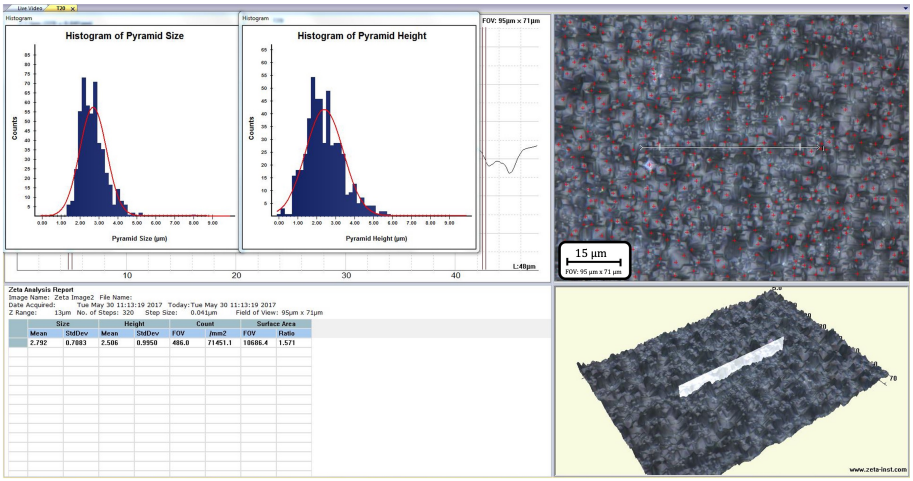

Figure 5.7: Zeta 3D optical microscope measurement data of pyramid size and height distribution for the novel textured DWS c-Si wafers.

Table 5.1: Zeta 3D measurement data for Group 1 (MWSS using existing texturing process), Group 2 (DWS using our novel texturing process), and, Group 3 (DWS using existing texturing process) c-Si wafers.

Wafer type	Texturing process	Wafer side	Pyramid size (μm)	Pyramid height (μm)
Group 1: MWSS	Existing	Face-1	2.6 ± 0.6	2.3 ± 0.8
		Face-2	2.5 ± 0.6	2.5 ± 0.8
Group 2: DWS	Novel	Face-1	2.8 ± 0.7	2.5 ± 1.0
		Face-2	2.8 ± 0.7	2.5 ± 1.0
Group 3: DWS	Existing	Face-1	2.5 ± 0.6	2.2 ± 0.8
		Face-2	2.6 ± 0.6	2.3 ± 0.8

5.7 Lifetime study

The passivation quality is dependent on texturing, diffusion and passivation layer uniformity. Since, similar diffusion and ARC deposition process conditions were used for all three Groups of textured wafers, PL images must reflect the texture uniformity. PL images were taken for the representative wafers (lifetime samples fabricated following the process flow in Figure 4.1) and the PL images were converted then into the carrier lifetime map using calibration of PL pixel intensity with measured QSSPC carrier lifetime values [181]. Nearly similar PL intensity images are observed for all the wafers

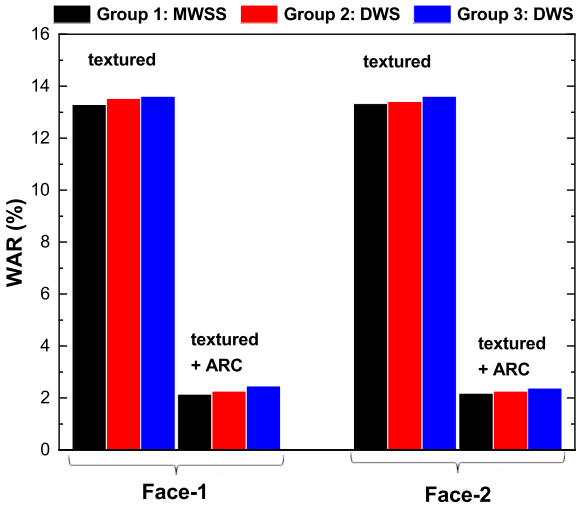

Figure 5.8: Variation of WAR on both the faces of c-Si wafers for the Group 1 (MWSS using existing texturing process), Group 2 (DWS using our novel texturing process) and Group 3 (DWS using existing texturing process) after texturing and after final ARC deposition.

with almost similar distribution of the lifetime values. Histograms are shown in the inset of Figure 5.9(A), 5.9(B) and 5.9(C) represent a narrow distribution of PL counts all over the sample area. This reflects that the uniformity of our novel texturing process on the DWS wafers is similar to the textured wafers from the other groups.

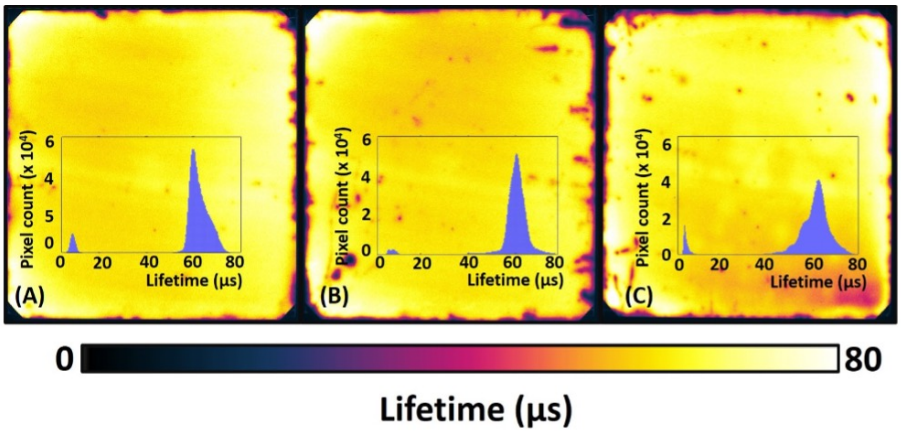

Figure 5.9: Spatially resolved PL images of lifetime samples of (A) Group 1 (MWSS using existing texturing process), (B) Group 2 (DWS using our novel texturing process), and, (C) Group 3 (DWS using existing texturing process).

5.8 Solar cell results

Figure 5.10 presents the distribution of the one sun I-V parameters of 60 cells (20 cell each) from Groups 1, 2 and 3 textured c-Si wafers. The average J_{SC} value is 36.5 mA-cm^{-2} for all the Groups of cells. The average V_{OC} values varies as 634.1 mV, 634.0 mV and 634.0 for the Group 1, 2 and 3 cells, respectively. However, there is a marginal difference in average FF values as 79.37%, 79.64% and 79.71% for the Group 1, 2 and 3 cells respectively. The Group 1, 2 and 3 cells have average η of 18.35%, 18.41% and 18.42%, respectively. Thus a minor improvement in average η are observed for the DWS cells (Groups 2 and 3), but this is within measurement error.

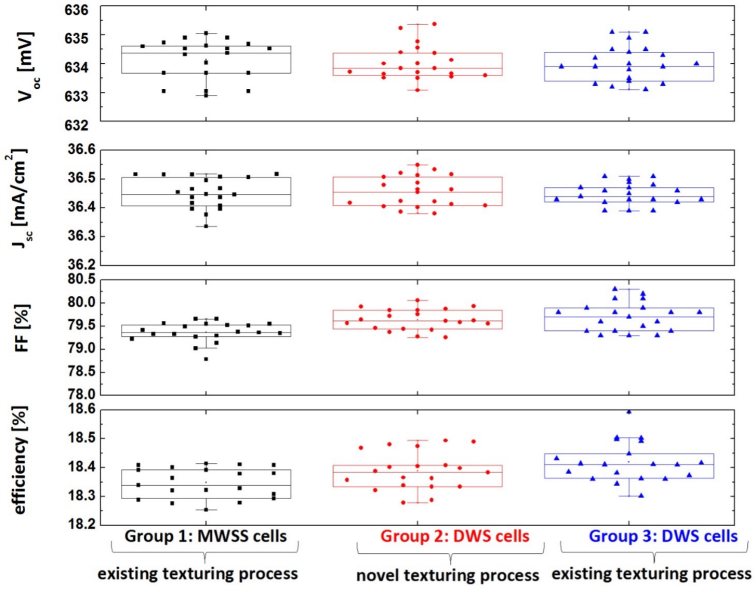

Figure 5.10: Distribution of electrical parameters and efficiency for solar cells using Group 1 (MWSS using existing texturing process), Group 2 (DWS using our novel texturing process), and, Group 3 (DWS using existing texturing process) c-Si wafers.

The IQE, EQE and surface reflectance (R) values are plotted in Figure 5.11. Figure 5.11 clearly indicates almost no variation of these parameters similar to that of one sun electrical parameters, confirming no adverse impact of proposed texturing on performance of solar cells.

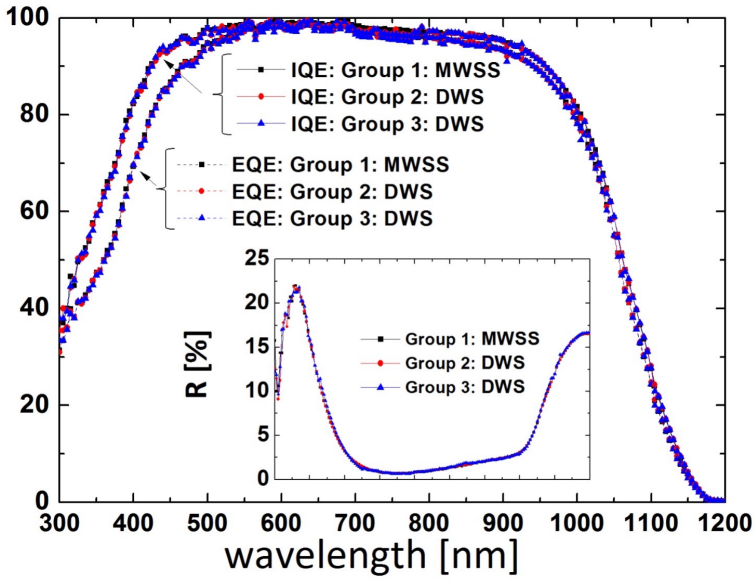

Figure 5.11: Measured IQE, EQE and R graphs of the representative solar cells using Group 1 (MWSS using existing texturing process), Group 2 (DWS using our novel texturing process), and, Group 3 (DWS using existing texturing process) c-Si wafers.

5.9 Conclusions

A cost effective alkaline texturing process for industrial DWS c-Si is demonstrated. The proposed texturing scheme is a two step process; SDR in NaOCl - NaOH solution followed by standard silicate pyramidal texturing. The cost of NaOCl is significantly lower compared to the existing TMAH based SDR process and the process can be immediately transferred to any of the alkaline texturing tool without any additional equipment setting cost. Through a detailed analysis, we demonstrated that our novel textured wafers and cells have similar optical, electronic and electrical properties as that of DWS and MWSS wafers and solar cells fabricated using existing texturing methods.

Chapter 6

An Additive-free Industrial Texturing Process for DWS mc-Si Wafers

6.1 Motivation

Conventional (HNO_3-rich HF - HNO_3 - DI water acid solution based) texturing of DWS mc-Si wafers results in non-uniform texture formation. The alternative processes developed for addressing the texturing challenges of DWS mc-Si wafers were either expensive, or use new chemicals or require additional processing tools and processing steps, which throws up challenges in industrial adoption. Hence, development of a texturing process that can be transferred to existing acid texturing tools was the immediate requirement in industry at the time of adoption of DWS mc-Si wafers.

In this context, we proposed a novel acid texturing process, in which an HF-rich acidic solution was used to fabricate porous silicon (Por-Si) surface first, followed by short KOH dip to dissolve the Por-Si to create a scalloped texture surface. The proposed texturing process does not require any additive, metal process or any additional tool and hence, can be readily integrated in any existing acid texturization tool. The morphological, optical and electronic properties of novel acid textured wafers and the performance parameters of solar cells were characterized and compared with conventional acid textured MWSS mc-Si wafers and solar cells to demonstrate the potential of the process. The developed process was named as "NCPRE additive-free acid texturing" process.

6.2 Texturization of DWS mc-Si wafers

The 6 inch full square, p-type, ~ 180 μm thick MWSS and DWS mc-Si wafers with resistivity of ~ 2 Ω-cm were used for the experiments. The bulk lifetime of the mc-Si wafers is in the range of 100-120 μs. In our novel acid texturing process, HF and HNO_3 solutions were used. The ratio of HF in our etching solution was varied from 40% to 60% (by volume) of the total volume of HF - HNO_3 texturing solution for Por-Si formation. All the processes were performed until minimum of 2 μm of Si was removed from each side of the wafer. Post-acid treatment, wafers were dipped in dilute KOH solution at room temperature. As a reference, MWSS mc-Si wafers were subjected to standard acid texturing process with HF - HNO_3 - DI water solution (1:3:2 ratio by volume) for 60 sec for Por-Si formation following the recipe presented in [173]. The residual metal-ion neutralization process (for both DWS and MWSS wafers) were similar as discussed in previous chapter and the process details are shown in Figure 6.1. Further, the textured (optimized NCPRE acid textured DWS and standard acid textured MWSS) mc-Si wafers underwent phosphorous tube diffusion, PSG and rear junction isolation, PECVD SiN_X ARC deposition, front silver (Ag) and back aluminium (Al)/Ag-Al metallization, and, co-firing for completing the full area Al-BSF cell fabrication. The process flow used for Al-BSF full area cell fabrication is shown in Figure 6.2.

6.3 Reaction chemistry

Robbins and Schwartz [38, 182] described chemical transformations during HF-HNO_3 etching as a two-step process, i.e., oxidation of Si to SiO_2 by HNO_3 and then dissolution of this SiO_2 by HF as summarized in equations 6.1 and 6.2. The overall reaction is given in equation 6.3.

$$3Si + 4HNO_3 \rightarrow 3SiO_2 + 4NO + 2H_2O \tag{6.1}$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{6.2}$$

$$3Si + 4NHO_3 + 18HF \rightarrow 3H_2SiF_6 + 4NO + 8H_2O \tag{6.3}$$

The process of dissolution of SiO_2 has been thoroughly studied and well understood. Though HNO_3 is a well-established oxidizing agent, the mechanism of Si oxidation by the same is not well understood. Turner [36] has proposed the electrochemical

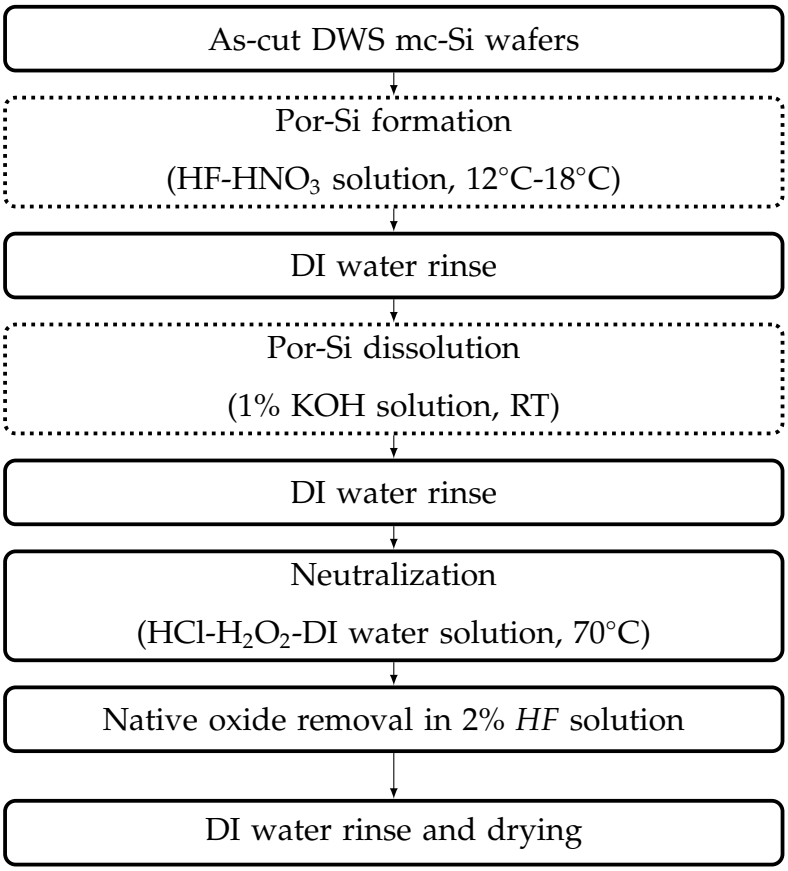

Figure 6.1: Complete process flow diagram for the NCPRE acid texturing scheme. Revised process steps are marked inside dotted boxes.

nature of the Si oxidation with HNO_3 and was also supported by Kooij *et al*. [37]. According to this model, reduction of HNO_3 at the local cathodic sites inject holes into the valence band of Si. The nature of nitrogen intermediates formed as a result of HNO_3 reduction and their role in etching are ambiguous. Abel *et al*. [183] have indicated a possible involvement of nitrogen oxides which may exist in equilibrium with nitrous acid. Robbins and Schwartz [38, 182] proposed HNO_2 as the active oxidizing agent involved in the reaction. Kelly and co-workers [39] proposed NO^+, which is a stronger oxidizing agent, as the key intermediate. Steinert *et al*. [40, 184] carried out a detailed analysis of Si chemical etching in HF - HNO_3 mixture to identify the key nitrogen intermediates involved and to characterize the wafer surface after etching. In HF-rich HF - HNO_3 mixture, UV-visible and Raman spectra revealed the presence of dinitrogen trioxide (N_2O_3) which render the etch solution blue in color. Another important N(III) species identified was ($3NO^+$ NO_3^-) denoted as [$N_4O_6^{2+}$]. The etch rate was observed to be linearly dependent on the Raman peak area of [$N_4O_6^{2+}$]. This direct

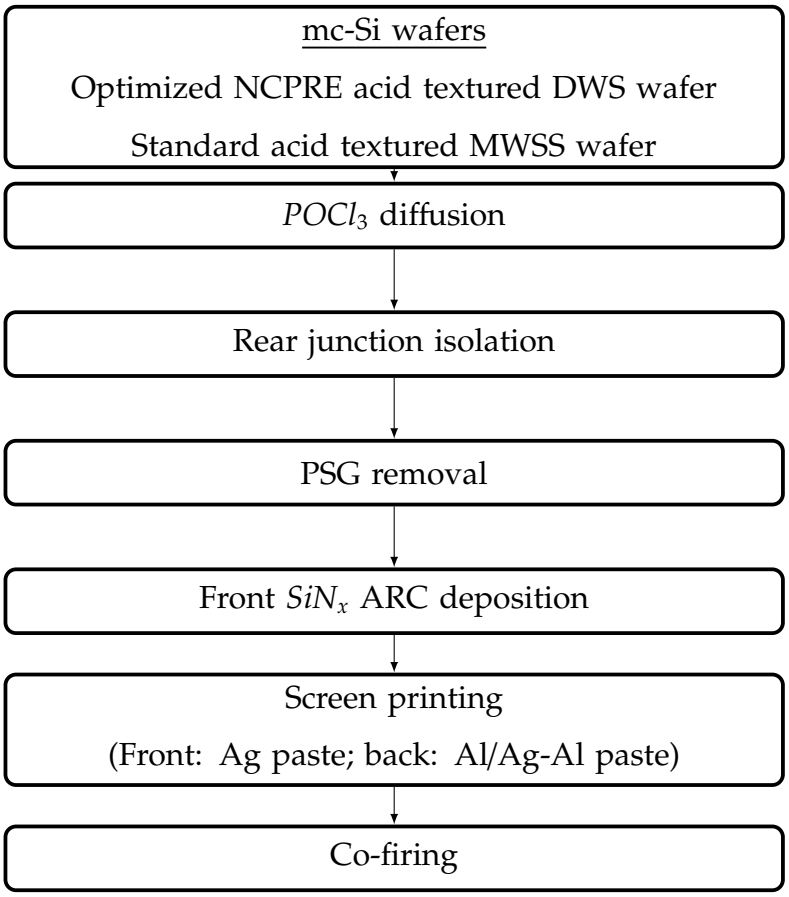

Figure 6.2: Process flow diagram of fabricating full area Al-BSF mc-Si cells.

correlation between $[N_4O_6^{2+}]$ concentration and etch rate lead to conclude NO^+ as the key reactive intermediate involved in the rate-limiting step. If the etching mechanism was proceeding through the two-step process as proposed by Robbins and Schwartz [38, 182], HF-rich etch solution was expected to result in a hydrogen (H)-terminated surface. The HNO_3-rich etch solution with high N(III) intermediate concentration would have yielded an oxygen terminated surface. However, an H-termination was observed on the etched surface even with varying concentration of reactive intermediates or with different composition of etch solution using X-ray photoelectron spectroscopy [41]. With these backgrounds, we adopt a hole initiated fluoride etching mechanism suggested by Allongue *et al*. [185] which was further refined by Kolasinski [42, 186] to explain the mode of etching in our system.

Si exposed to air readily oxidizes to form a SiO_2 layer on the surface [187]. The oxide layer can be removed by a fluoride solution to form a H-terminated Si surface on which etching is being initiated. The solvated F^-, HF, or HF dimer, in the fluorine

solution may be the active species in etching mechanism. Schematic representation of hole initiated *Si* etching process in HF - HNO_3 solution is shown in Figure 6.3. According to Gerischer and Mindt [188], a hole in the valence band makes the surrounding bonds weaker and prone to nucleophilic attack. A hole is injected to the bulk by the oxidant HNO_3 which then diffuses to the *Si* surface as shown in step-1 of Figure 6.3. According to Koker and Kolasinski [42, 189], rate of Si etching (R_A) is decided by the hole formation rate in the bulk and its transport to the surface, given by equation 6.4.

$$R_A \approx [s(HF)Z_w(HF) + s(HF_2^-)Z_w(HF_2^-)]\theta_n, \tag{6.4}$$

Here, the terms with s are sticking coefficients, terms with Z_w corresponds to impingement rates and those with θ_n indicates the coverage of holes on the surface [42, 189]. The nucleophilic attack of fluoride on the surface leads to the formation of Si-F bond which results in an electron in the conduction band (refer step-2 of Figure 6.3). The Si-F bond polarizes the Si-Si backbonds and render these labile for further nucleophilic attack as shown in last two steps of Figure 6.3, which eventually leads to the formation of $SiHF_3$. $SiHF_3$ in solution converts to silicon hexafluoride (SiF_6^{2-}) (see in equation 6.4) [42, 190].

$$SiHF_3 + HF + 2F^- \rightarrow SiF_6^{2-} + H_2 \tag{6.5}$$

This process goes on until the features reach nanoscale. Energy of holes increases if they are confined in small volume of nanoscale. Hence additional energy is required to transfer the holes from bulk to the confined volume which makes the hole-initiated etching a self-limiting process. In this manner, quantum confinement passivates small structures and leads to the formation of nanocrystalline Por-Si films [43, 44, 45].

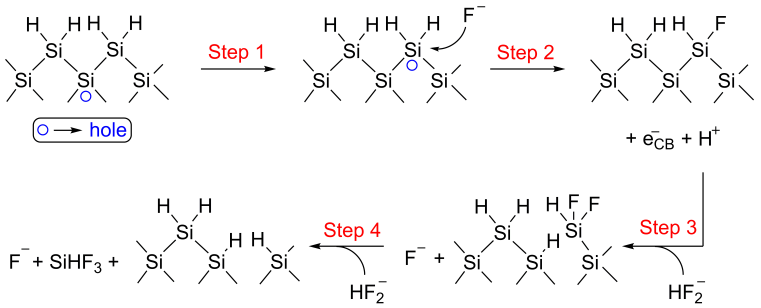

Figure 6.3: Schematic representation of hole initiated etching of *Si* wafers in *HF*-HNO_3 solution. Stepwise progress of the chemical reaction is shown from step-1 to step-4.

Typically, Si etching in HF - HNO_3 mixtures proceeds with the removal of saw damaged lattice creating certain surface morphology. Recently, Acker *et al*. attributed the high etch rate of saw damages to the weak lattice at this region [10]. Distortion of the lattice makes the atoms more reactive, resulting in the preferential etching of the saw damages. In our Si etching acid solution, HF-rich etch mixture was employed for the DWS wafers having lower saw damaged surface as compared to the MWSS wafers. Lattice defects generally account for the formation of relatively bigger textures along the saw damages. The fluoride concentration is increased in the etch mixture by making it HF-rich. A possible outcome of this scenario is the chemisorption of fluoride on overall wafer surface, irrespective of whether it is damaged or not. As fluoride on the wafer surface is autocatalytic towards the reaction, etching proceeds on overall Si surface in HF-rich etch solution resulting in better texture coverage. So, a textured surface can be attained by employing an etch solution with a suitable HF and HNO_3 ratio, even when the initial wafer does not have any defects. Thus HF-rich acid chemistry was applied to highly polished DWS mc-Si wafers to attain desired texture morphology by fine tuning the composition of this etch solution.

6.4 Optimization of NCPRE acid texturing recipe

All the DWS mc-Si wafers were textured using HF-rich acid solution as detailed in section 6.2. Formation of Por-Si layer throughout the wafer surface is the key target in our texturing scheme. As the concentration of HF in acid solution plays a vital role, a parameter 'ρ' is defined as the ratio of volume of HF to total volume of the acid etching solution (containing HF, HNO_3 and DI water). For values of ρ less than 40%, the process was found to be highly active and vigorous resulting in high undesired Si-etch rate at our specified process temperature range. On the other hand, although Por-Si formation was found to be more uniform for ρ greater than 60%, the Si etch rate was very low and inadequate for saw damage removal. Hence, in our process optimization, value of ρ was varied in 40% to 60% range. We experimented with three texturing recipes in details with ρ values of 59% (process A), 52% (process B) and 45% (process C). All the wafers were acid textured individually (not as batch process) in a specially made Teflon bath and nearly 1°C increment in temperature was noticed

before and after Por-Si formation step. The process durations were varied between 1-2 min depending on the solution temperature to maintain uniform Si etching. After Por-Si formation using processes A, B and C, texturing process was completed using remaining process steps as listed in Figure 6.1. The amount of Si-etch per side per min was found as 0.5 μm, 1.9 μm, and 9.1 μm for processes A, B and C, respectively. This increased Si-etch amount or etch-depth with reduced HF concentration in the acid solution is also expected theoretically from etching chemistry of HF-rich acid etch process.

Figure 6.4 shows reflectance of textured samples of the as-cut and after NCPRE acid-textured (using processes A, B, C) for the DWS mc-Si wafers in 300-1000 nm wavelength range. The WAR values of the as-cut, NCPRE textured (using processes A, B, C) DWS mc-Si wafers are calculated as 37.5%, 16.9%, 29.0% and 32.9%, respectively. Figure 6.4 clearly indicates the increased surface reflectance with decreased concentration of HF in the acid etching solution. Spectrophotometer only measures reflectance over a particular circular area of the Si wafer. However, mc-Si wafers have different grains spread all over the wafer surface with varied reflectance for different texturing geometries. For examining the impact of the NCPRE acid texturing processes on complete wafer, reflectance mapping tool of LBIC was employed on these textured wafer surfaces with raster size of 0.5 mm. The AM1.5G solar spectrum holds maximum photon flux around 600 nm wavelength range, and, so the illumination facing surface of solar cells must have minimum reflection around that wavelength. Following this reason, the reflection maps for the representative textured wafers from processes A, B and C, were generated at 658 nm wavelength (nearest to the wavelength of 600 nm available in our LBIC tool) over complete textured wafer surface and the LBIC reflection maps are shown in Figure 6.5. Figure 6.5 indicates that the average reflectance value measured over the entire area of the wafer textured using processes A, B and C are 16.4%, 27.1% and 31.8%, respectively and uniformity of colors there indicates near uniform texturing in each texturing process.

The variation of surface morphology of the NCPRE acid textured wafers were studied by SEM to understand its relationship with reflectance (R) values. The SEM micrographs of the representative wafers are shown in Figure 6.6. For process A, heavily porous textures can be observed (see Figure 6.6(a-1)) all over the wafer. Also,

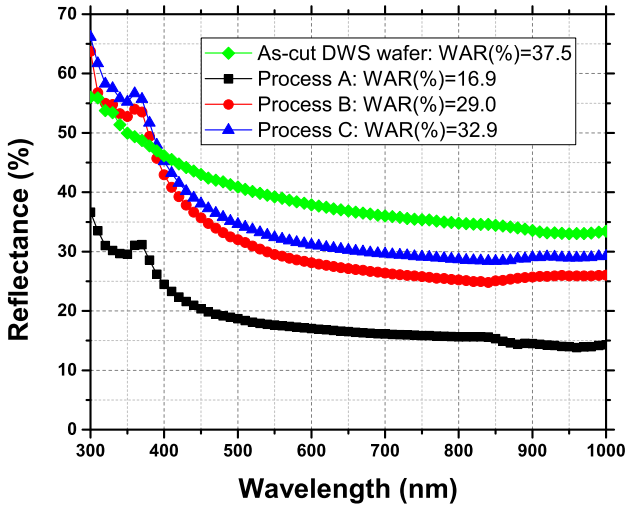

Figure 6.4: Variation of surface reflectance values of the as-cut and NCPRE acid textured (processes A, B, C) DWS mc-Si wafers in 300-1000 nm wavelength range. The wafers were textured using different ρ values in the NCPRE acid texturing process resulting in different WAR values.

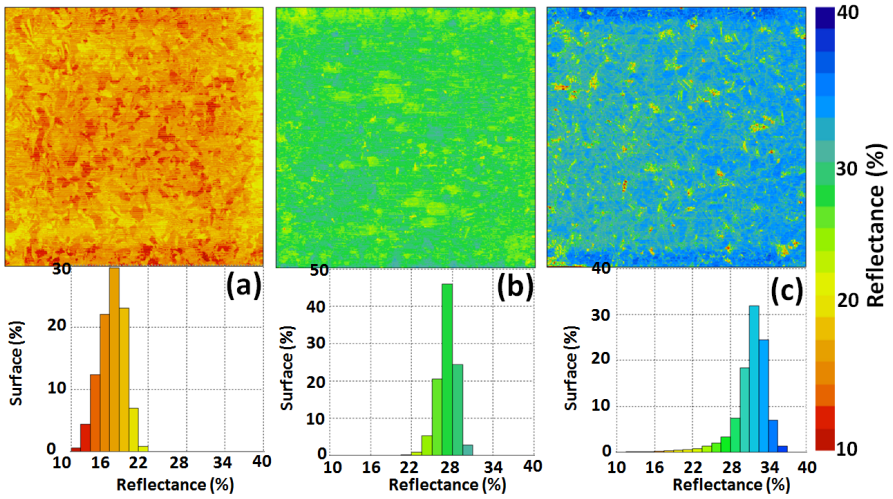

Figure 6.5: Variation of surface reflectance of the NCPRE acid textured DWS mc-Si wafers obtained by reflectance measurement using LBIC using 658 nm wavelength: (a) Process A, (b) Process B, and, (c) Process C.

saw marks and micro-cracks are still visible in the SEM image (see Figure 6.6(a-2)) to confirm inadequate damage removal process. The heavily porous textures, micro-cracks and partially removed saw damages contribute to better light trapping for process A and generate low value of R. As shown in Figure 6.6(b-1) and (b-2), for

process B, more rounded, less porous, scalloped structures were formed. However, large porous textures are formed along the horizontal direction where saw damages were initially present (see Figure 6.6(b-2)) along with the formation of uniform small porous textures on non-damaged areas as well. In Figure 6.6(b-1) and (b-2), we could not observe any hard pits, residual parallel saw marks or micro-cracks. These scalloped texture structure with better surface coverage results in moderate light absorption. For process C (see Figure 6.4), R values are on the higher side. This high Si-etch process recipe removed all the unwanted surface damages, resulted in more flatter and large porous features of a polished Si surface (see Figure 6.6(c-1) and (c-2)), which further increased front surface reflectance as compared to processes A and B.

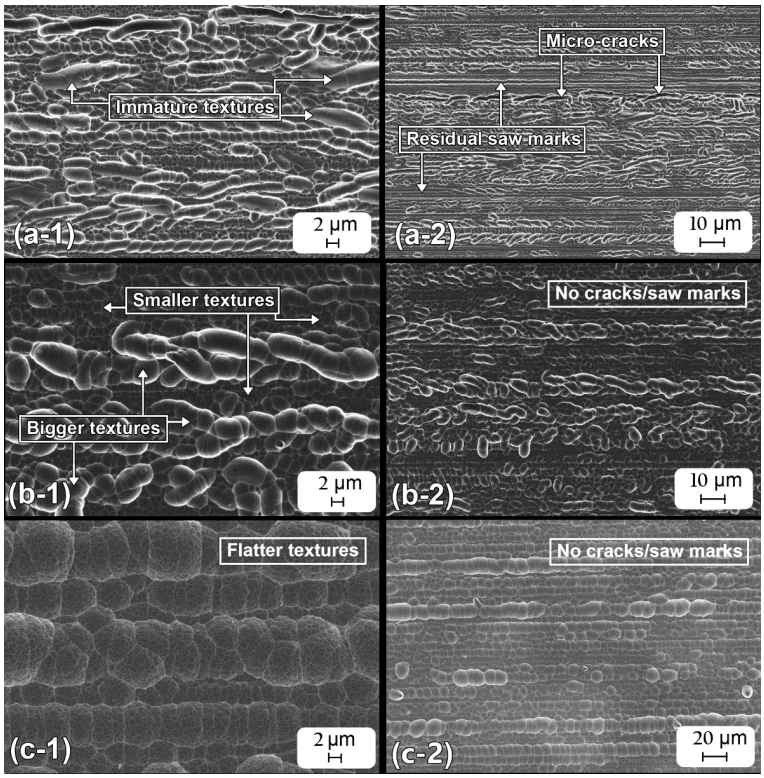

Figure 6.6: SEM images (top view) of the NCPRE acid textured DWS mc-Si wafer surfaces textured using: (a-1) process A (magnification: 5000X), (a-2) process A (magnification: 2000X); (b-1) process B (magnification: 5000X); (b-2) process B (magnification: 2000X); (c-1) process C (magnification: 5000X); (c-2) process C (magnification: 1000X).

The overall impact of the surface texturing process on bulk and emitter properties of the device can be studied by measuring the variations of τ_{Eff} and J_{0e} in the lifetime test structures fabricated as explained in Figure 4.1. Average τ_{Eff} of test $n^+ - p - n^+$

textured structure for processes A, B and C, are measured as 20.9 μs, 86.5 μs and 85.2 μs, respectively. Average J_{0e} of test structure were calculated 4.1×10^{-13} $A\text{-}cm^{-2}$, 1.1×10^{-13} $A\text{-}cm^{-2}$, and 1.3×10^{-13} $A\text{-}cm^{-2}$ for processes A, B and C, respectively.

Uniformity of growth of the ultra thin passivation oxide layer on entire area of the textured wafers needs to be studied for its application. PL images were captured for the representative test structure (carrier lifetime test structure) for each texturing groups from processes A, B and C, and are shown in Figure 6.7. Highly damaged and Por-Si surface in process A has the least PL count and PL intensity, as an average of 4 arbitrary units (a.u.) (see in Figure 6.7.(a)). The PL count reaches maximum as an average of 34 a.u. in process B (see Figure 6.7.(b)). Also, except some grain boundaries, the count is nearly uniform all over the complete wafer. In process C, PL count also has a high average count of 32 a.u. (see Figure 6.7 (c)).

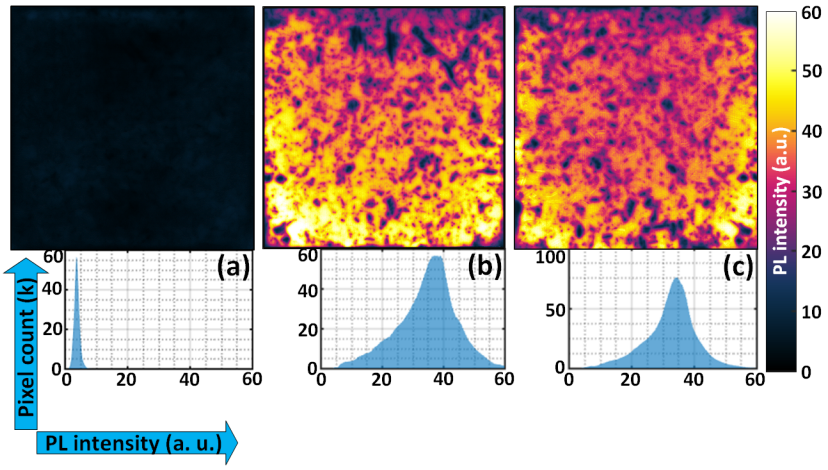

Figure 6.7: PL map lifetime test structures of NCPRE acid textured samples using (a) Process A, (b) Process B, and, (c) Process C. PL count histograms are shown below the PL maps. PL counts shown here are in multiples of thousands.

The summary of material (amount of Si-etch), optical (WAR) and electronic (τ_{Eff} and J_{0e}) properties of the wafers textured using three processes A, B and C, are listed in Table 6.1. For process A, although WAR is quite low, incomplete removal of surface damages (by low Si-etch rate) and increased recombination (evident in its low τ_{Eff} and high J_{0e} values) due to heavily porous textured surface limit its choice for a useful texturing recipe. For the process C, surface is too reflective (WAR~32.9%) resulted by a vigorous exothermic chemical reaction with very high Si-etch rate, also make it

Table 6.1: Values of thickness of Si-etched, WAR, τ_{Eff} and J_{0e} of the NCPRE acid textured DWS mc-Si wafers using processes A, B and C.

Texture recipe	Solution composition, ρ (%)	Material removed per side (μm)	WAR (%)	τ_{Eff} (μs)	J_{0e} (Acm^{-2})
Process A	59	0.5	16.9	20.9	4.1×10^{-13}
Process B	52	1.9	28.9	86.5	1.1×10^{-13}
Process C	45	9.1	32.0	85.2	1.2×10^{-13}

unsuitable as a texturing solution. In process B, we found an optimum acceptable textured geometry with WAR of ~29.0%. Also, LBIC reflectance map, highest τ_{Eff}, lowest J_{0e}, and higher PL counts, confirm best optoelectronic properties of process B textured wafer as compared to those from the other two processes A and C. Also, the amount of Si etched is ~ 1.9 μm per side which is also in accordance with industrial requirements. Therefore, process B is selected as the optimized recipe and in rest of the manuscript this process is referred as the NCPRE acid-texturing scheme for DWS mc-Si wafers.

6.5 Comparison with standard acid textured MWSS wafers

6.5.1 Surface reflectance study

Different grains of mc-Si wafer exhibit different reflectance values after texturing. Therefore, on the representative NCPRE textured DWS and standard acid textured MWSS mc-Si wafers, reflectance was measured at 10 different positions by spectrophotometer in the 300 nm to 1000 nm wavelength range and WAR values were calculated for each position. Similar measurements were also performed for the representative wafers after SiN_X:H ARC deposition. The distribution of these WAR values, before and after ARC, is shown in Figure 6.8. It shows that for the NCPRE textured DWS wafers, WAR values were lagging only by 1% (absolute) from the standard acid textured MWSS one. However, after ARC, both wafers measured almost similar WAR values with mean variation less than 0.2% (absolute). As discussed before, as-cut DWS wafers already exhibit ~ 5% (absolute) higher WAR as compared to as-cut MWSS mc-Si

wafers. So, an additional improvement of 4% (absolute) in light absorption in NCPRE acid textured DWS wafer confirms excellent light trapping properties of the textured surface. While the results of the textured wafers were promising, effectiveness of the texturing can further be established by nearly similar values of WAR with ARC.

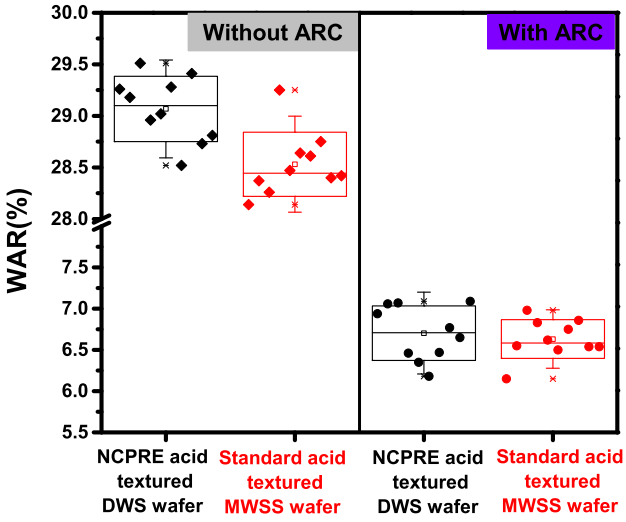

Figure 6.8: Comparison of distributed WAR values of textured wafers (measured at 10 different locations) without and with SiN_x ARC layer for the NCPRE textured DWS and standard acid textured MWSS mc-Si wafers.

Texture uniformity was also confirmed by LBIC reflectance map at single wavelength (658 nm) as shown in Figure 6.9. The reflectance variation also showed similar trends, where the NCPRE textured DWS samples showed mean difference of 1.5% absolute (see Figure 6.9(a) and Figure 6.9(b)) and 0.2% (see Figure 6.9(c) and Figure 6.9(d)) without and with ARC, respectively. As a whole, similar trends are observed in reflectance values of both the textured surfaces with over 90% areas having the desired reflectance range of 24% to 30%. For the ARC deposited textured wafers, the DWS and MWSS textured wafers have low reflecting surface areas with R less than 1.1% of 89% and 96%, respectively. This little difference in R values doesn't create appreciable surface reflection from the NCPRE acid textured DWS wafers as observed in the respective WAR values as shown in Figure 6.8. The spectral reflectance of the textured wafers with and without ARC deposition establishes the light trapping capability of NCPRE acid texturing for DWS wafers.

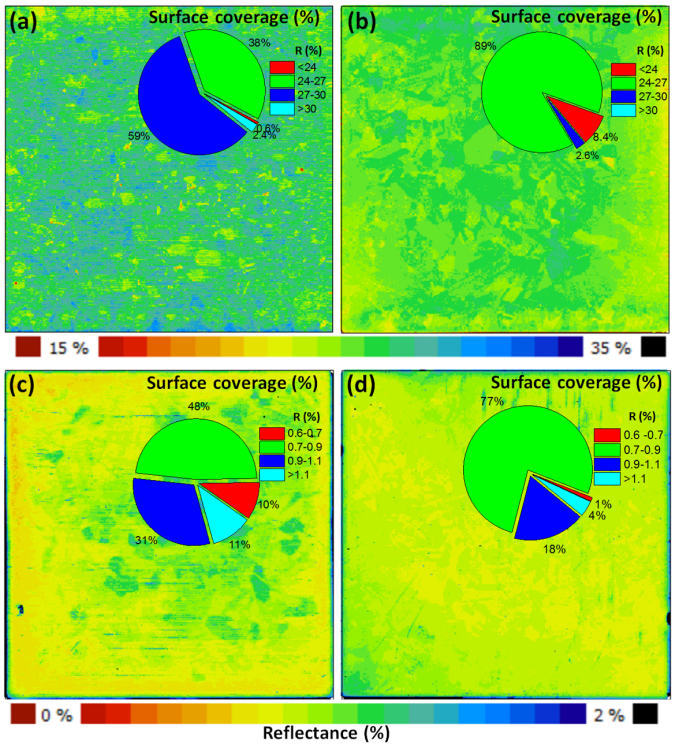

Figure 6.9: Full area single wavelength (658 nm) surface reflectance map of mc-Si wafers measured using the LBIC tool: (a) NCPRE acid textured DWS; (b) standard acid textured MWSS; (c) NCPRE acid textured DWS with ARC; (d) standard acid textured MWSS with ARC.

6.5.2 SEM observations

Surface morphology of the NCPRE acid textured DWS and standard acid textured MWSS mc-Si wafers is examined by SEM at different magnifications on the textured wafers and Figure 6.10 shows the SEM images. The NCPRE acid textured DWS wafers show (see Figure 6.10 (a-1) and Figure 6.10(a-2)) nearly uniform texture coverage, although bigger textures are formed along the parallel saw marks (see Figure 6.10 (a-1)). Uniform texture can also be seen on the standard acid textured MWSS wafers (see in Figure 6.10(b-1) and Figure 6.10(b-2)) in all directions since initial saw damages and crystal defect distributions were random in nature there. A close comparison of high magnified SEM images of textured wafers in Figure 6.10 (a-2) and Figure 6.10(b-2) indicates nearly similar texture pattern with scalloped rounded surface with only difference being DWS wafers having nearly directional arrangement (aligned parallel to sawing directions) of the inverted near-round structures (see in Figure 6.10(a-2)).

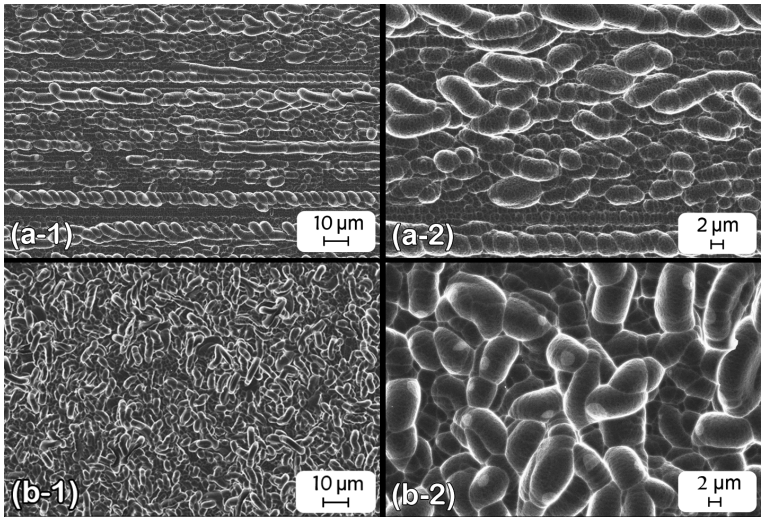

Figure 6.10: SEM images (top view) of acid textured mc-Si wafer surfaces using: (a-1) NCPRE acid textured DWS (magnification: 2000X); (a-2) NCPRE acid textured DWS (magnification: 5000X); (b-1) standard acid textured MWSS (magnification: 2000X); (b-2) standard acid textured MWSS (magnification: 5000X).

6.5.3 Diffusion uniformity study

The uniformity of the P-diffused emitter on the textured wafers is analyzed by R_{Sheet} measurement (after PSG removal) on a 7x7 matrix with 1.5 cm edge exclusion across the complete wafer surfaces. For the NCPRE acid textured DWS and standard acid textured MWSS wafers, R_{Sheet} maps are shown in Figure 6.11. The average R_{Sheet} values look nearly identical (67.7 Ω/sq and 69.8 Ω/sq) with same standard deviation of 1.8 Ω/sq for the NCPRE acid textured DWS and standard acid textured MWSS wafers, respectively. The active P-dopant profiles of the diffused surfaces are shown in Figure 6.12 and nearly identical diffusion profiles are observed for both the textured surfaces. Similar R_{Sheet} distributions (Figure 6.11) and ECV dopant profiles (Figure 6.12) confirm the diffusion uniformity in both types of textured wafers.

6.5.4 Lifetime and cell parameters study

Figure 6.13(a) and Figure 6.13(b) respectively represents the lifetime maps of DWS and MWSS acid textured wafers. Comparable PL images are noticed for both types of test structures with relatively identical distribution of the carrier lifetime values (average value of 84 μs for both). Histograms provided in Figure 6.13(a) and 6.13(b) show an

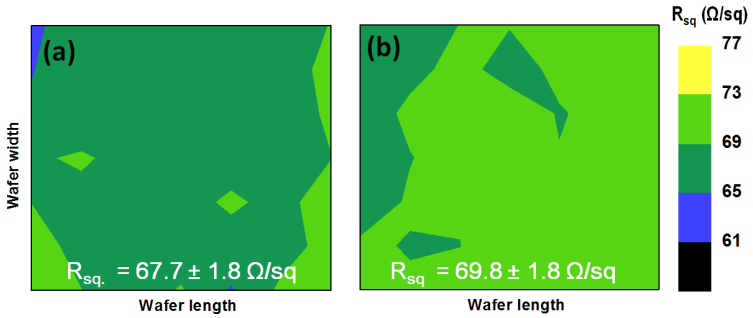

Figure 6.11: R_{Sheet} maps for the tube diffused emitters: (a) NCPRE acid textured DWS wafer (average ~ 67.7Ω/*sq*, standard deviation ~ 1.8Ω/*sq*), (b) standard acid textured MWSS wafer (average ~ 69.8Ω/*sq*, standard deviation ~ 1.8Ω/*sq*).

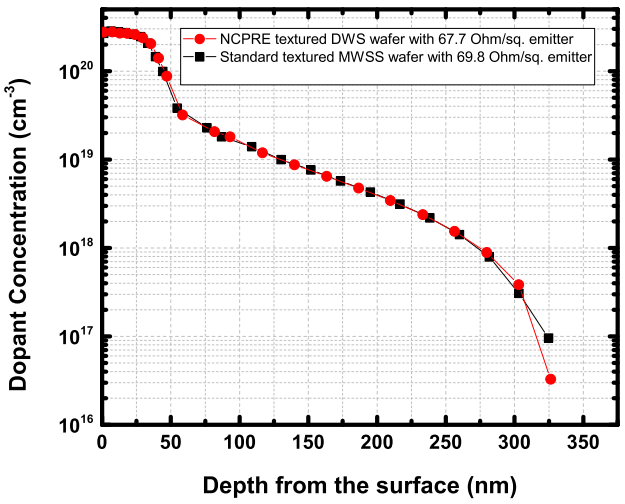

Figure 6.12: Active P-dopant profiles of the tube diffused emitters using both the NCPRE acid textured DWS and standard acid textured MWSS mc-Si wafers.

analogous distribution of PL counts all through the wafer surface area, indicating that the uniformity of NCPRE acid texturing scheme on the DWS wafers is identical to the standard acid textured MWSS wafers.

The batch average (15 cells each) of one sun illuminated I-V parameters of the cells fabricated using the NCPRE acid textured DWS and standard acid textured MWSS mc-Si cells is shown in Table 6.2. The measured J_{SC} of the NCPRE textured DWS and standard acid textured MWSS mc-Si cells are 36.52 mA-cm^{-2} and 36.66 mA-cm^{-2} respectively. The reason for slightly lower value of J_{SC} for the DWS cells can be explained from the slightly higher value of surface reflectance (see Figure 6.8). The values of V_{OC}

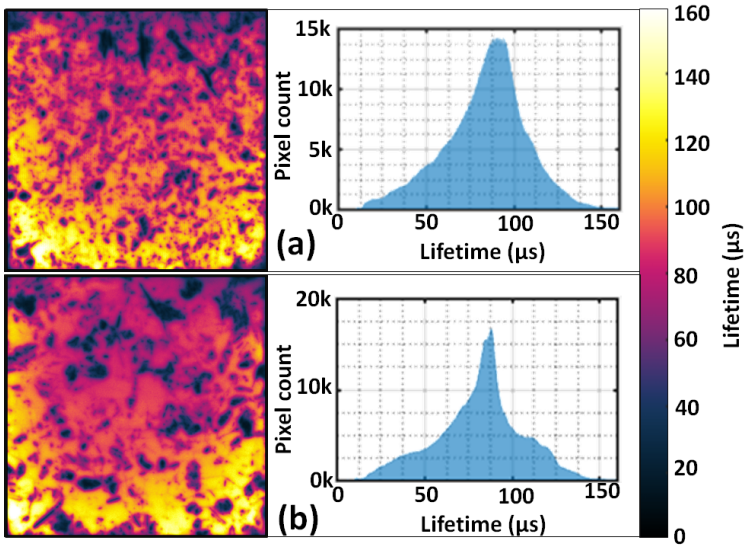

Figure 6.13: Spatially resolved minority carrier lifetime maps of $n^+ - p - n^+$ lifetime structure fabricated on (a) NCPRE acid textured DWS, and, (b) standard acid textured MWSS mc-Si wafers. Lifetime count histograms are also shown beside the respective lifetime maps.

of the NCPRE textured DWS and standard acid textured MWSS mc-Si cells are 631.65 mV and 632.76 mV for the DWS and MWSS cells respectively and have a marginal difference. However, an improvement of FF value by $\sim$ 0.5% (absolute) is observed for the NCPRE acid textured DWS cells (see Table 6.2), which may arise from the horizontally aligned acid-textured surface (see Figure 6.6) for the DWS wafers. Care was taken in screen printing for these DWS cells so that the screen printed front silver fingers must lie parallel to the diamond wire sawing marks. The NCPRE acid textured DWS and standard acid textured MWSS cells have efficiencies of 18.46% and 18.45% respectively. These results thus indicate that the newly proposed NCPRE acid texturing process can effectively be employed for DWS mc-Si wafers without any adverse impact on cell performance.

6.6 Conclusions

An additive-free, non-metallic, energy efficient, industrially viable acid based texturing process, namely, NCPRE acid texturing, for DWS mc-Si wafers is demonstrated. The chemical process for the selection of HF-rich acid solution and process optimization

Table 6.2: The average values of the illuminated I-V parameters for both types of acid-textured mc-Si cells

	J_{SC} $(mA-cm^{-2})$	V_{OC} (mV)	FF (%)	η (%)
NCPRE acid textured DWS	36.52	631.6	80.04	18.46
Standard acid textured MWSS	36.66	632.7	79.55	18.45

of the proposed process is explained in detail. The optical and electrical properties of NCPRE acid textured wafers and cells were comparable to conventional acid textured MWSS mc-Si solar cells. The proposed texturing process does not require any additional changes in Por-Si removal and neutralization process steps, and hence, it can be readily transferred to industry without any additional setting cost. Also, for any industry, switching over to standard acid texturing recipe for texturing MWSS mc-Si wafers can easily be done in the same texturing tool only by changing the ratio of HF, HNO_3, DI water and process bath temperature.

Chapter 7

Industrial Demonstration of NCPRE Additive-free Acid Texturing Process

7.1 Introduction

We were privileged to implement the "NCPRE additive-free acid texturing process" in three of the leading PV manufacturing units in the country. The additive-free process developed using laboratory setup were successfully transferred to industrial acid texturing tool of Rena Technologies GmbH, Schmid GmbH and SC Tools without major process alterations. The summary of I-V performance parameters for the three industrial demonstrations are depicted in Tables 7.1, 7.2 and 7.3. During the time of these industrial demonstrations, PV manufacturing units had already started using DWS wafers in their production lines and additive-based acid texturing process was implemented for texturing DWS mc-Si wafers. The η and performance parameter values of additive-based and additive-free batch of acid textured solar cells were nearly similar. However, more closely distributed performance parameter values were achieved for the third demonstration, which corresponds to the results shown in Table 7.3. Hence, solar cells from the third demonstration trial were used for further analysis and characterization.

Integration of a new process by replacing an established process to a production line is always challenging. Based on the characteristics and properties of the new process, optimization of the subsequent processes may also be essential to translate the complete potential of new process to power conversion efficiency. A detailed analysis

Table 7.1: Summary of AM 1.5 one sun batch average solar cell I-V parameters of the additive-based and additive-free batch of acid textured Al-BSF DWS mc-Si cells from the first demonstration.

	η (%)	I_{SC} (A)	V_{OC} (mV)	FF (%)
Additive-based	18.22	8.82	634	79.91
Additive-free	18.16	8.83	632	79.87

Table 7.2: Summary of AM 1.5 one sun batch average solar cell I-V parameters of the additive-based and additive-free batch of acid textured Al-BSF DWS mc-Si cells from the second demonstration.

	η (%)	I_{SC} (A)	V_{OC} (mV)	FF (%)
Additive-based	18.23	8.96	629	79.44
Additive-free	18.17	8.95	629	79.30

Table 7.3: Summary of AM 1.5 one sun batch average solar cell I-V parameters of the additive-based and additive-free batch of acid textured Al-BSF DWS mc-Si cells from the third demonstration.

	η (%)	I_{SC} (A)	V_{OC} (mV)	FF (%)
Additive-based	18.24	8.87	634	79.70
Additive-free	18.20	8.83	634	79.89

after each stage of processing is required for the same. Hence, detailed performance analysis of the solar cells fabricated using the NCPRE additive-free acid texturing process and additive-based acid texturing process was carried out to assess the scope for further improvement. Based on the analysis, the approximate improvements in performance parameters that can be obtained by further optimization in the processes are estimated in this chapter. In the end, cost analysis of chemicals used for texturing bath preparation is presented for demonstrating the cost advantages of NCPRE acid texturing process.

7.2 Experimental

7.2.1 Texturing

Full square 6 inch, p-type, ~180μm thick, 1-3 Ω-cm resistivity industrial DWS mc-Si wafers were processed using additive-free NCPRE acid texturing and additive-based conventional acid texturing schemes in an industrial texturing tool of Rena technologies GmbH. Additive-free texturing process uses HF-rich acid solution consisting of HF (49% by wt.), HNO_3 (68% by wt.) and DI water (5:3:9 ratio by volume) at 14-15°C for 75 sec for Por-Si formation. For the additive-based conventional acid texturing process, a different volume combination of HF, HNO_3 and DI water (2:5:9 ratio by volume) was used at 10°C for 75 sec. Commercially available texture additive from GP solar was dosed continuously to the HNO_3-rich acid texturing bath. Similar Por-Si dilution and neutralization cum native oxide removal process conditions assured regular production throughput.

7.2.2 Solar cell fabrication

For our industrial chemical texturing trial, the industry has processed NCPRE acid textured wafers in one of their older diffusion furnace, which uses a targeted R_{sheet} of 90 Ω/sq diffusion profiles for p-n junction formation. However, all their high efficiency aluminum back surface field (Al-BSF) mc-Si cells including additive-based acid textured wafers used in this work underwent much shallower diffusion of R_{sheet} ~ 120 Ω/sq in the regular production line. Both the sets of diffused wafers were processed further to complete the fabrication of full area Al-BSF cells using industrial production tools under similar process conditions. The schematic illustration of the complete processes involved in cell fabrication are summarized in Figure 7.1.

7.3 Optimum SDE and process bath preparation

The amount of saw damage removed during the Por-Si formation step was varied in the NCPRE additive-free HF rich acid texturing process by altering the solution composition. A lower etch rate was observed in a diluted acid solution (by adding

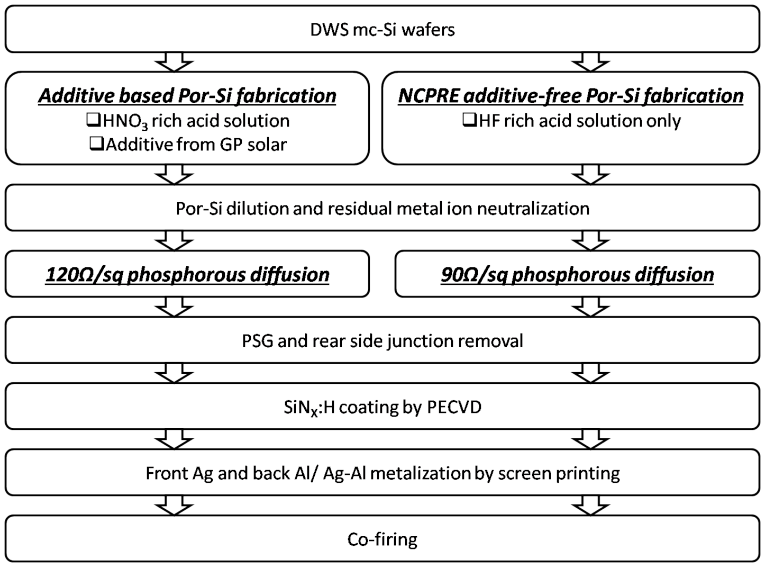

Figure 7.1: Schematic representation of the processes involved in fabricating full area Al-BSF solar cells. The difference in the process parameters are highlighted.

DI water to the existing acid solution) and an increased etch rate was observed with higher concentration of HNO_3 in the HF-rich acid bath. In chapter 6, the optimum combination of surface reflectance and surface passivation were obtained when ~ 2 μm of saw damages were etched from both the sides of the DWS mc-Si wafers in the additive-free acid texturing solution. Though the wafers with less than 1.5 μm saw damage etching per side exhibit low surface reflectance (WAR < 18%), large number of defects and residual saw damages severely influence the uniformity of phosphorous diffusion and effectiveness of SiN_X:H passivation. Furthermore, inadequate saw damage etching leads to residual saw mark impressions, defects and prominent cracks which drastically affect the overall performance and reliability of the fabricated cells and modules [191, 192]. Increased saw damage removal per side was achieved in the later case by increasing the HNO_3 concentration in the existing acid bath. mc-Si wafers with > 3 μm saw damage etching per side in Por-Si process resulted in lesser surface defects, wire impressions and cracks with flatter and larger surface textures. However, these textures exhibited poor light absorption with WAR > 34%. Hence, keeping the NCPRE acid textured solution HF-rich is mandatory for obtaining excellent texture coverage on the entire wafer surface area. The selection of the optimum acid texturing process conditions such as temperature of the texture bath, solution composition etc., for achieving targeted ~ 2 μm saw damage etch per side are the key steps in designing

and preparing the process bath for Por-Si fabrication.

The SEM images of the surface texture obtained for additive-based and additive-free acid textured mc-Si wafers after final Por-Si dilution and residual metal-ion neutralization are shown in Figure 7.2. Bigger textures are seen mainly along the wire saw marks for both the additive-based (see Figure 7.2 (a-1) and (a-2)) and additive-free (see Figure 7.2(b-1) and (b-2)) acid textured DWS mc-Si wafers. The initial surface defects and damages present along the saw marks can be attributed to the formation of bigger textures, where the acid texturing reaction progresses at much faster rate compared to defect-less areas. These SEM images for both the types of acid textured wafers show irregular and smaller textures formed on the other areas also. This is explained in terms of chemisorption of F^- in HF-rich solution and its auto-catalytic reaction nature leading to the formation of smaller textures all over the wafer surface irrespective of the presence of surface damages for additive-free acid texturing scheme. The angular (45° tilted) view SEM images (see Figure 7.2(a-2) and (b-2)) indicate that the size distribution of textures are different for both the sets of acid textured wafers. The textures formed after additive-free acid process looks more uniformly size distributed, whereas the additive-based textures have better substrate coverage with uneven size distributions. The SEM images clearly show that the HF-rich additive-free acid texturing process under optimized process conditions is capable of producing similar surface textures as that of additive-based acid textured mc-Si samples.

7.4 Surface reflectance study

The optical properties of the acid textured wafers are examined by comparing its WAR values with as-cut DWS mc-Si wafers. The variation in average surface reflectance values of an as-cut DWS mc-Si wafer, representative wafers from the additive-based and additive-free acid textured batches are plotted in Figure 7.3. As-cut DWS wafers were highly reflective with WAR > 38% because of the presence of relatively thinner saw damage layer and polished nature of the diamond wire cut Si surface. The reflectance values of the additive-based acid textured wafers (as-textured without ARC) shown in Figure 7.3 (see blue curve) indicate that the additive-based texturing process reduce the surface reflectance (WAR) by nearly 10% absolute (from ~ 38% to ~ 28%) without ARC

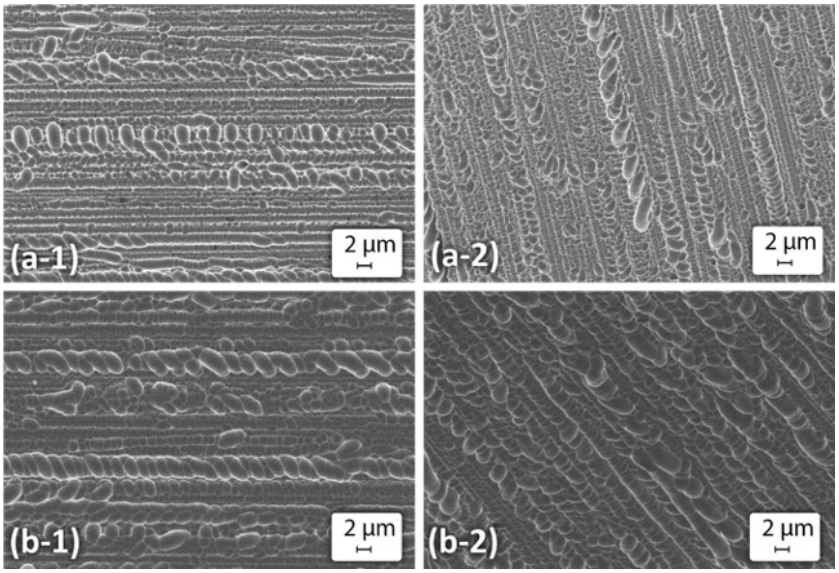

Figure 7.2: FESEM images of acid textured wafers: (a-1) additive-based (magnification: 5000X, top view); (a-2) additive-based (magnification: 5000X, angular view); (b-1) additive-free (magnification: 5000X, top view); (b-2) additive-free (magnification: 5000X, angular view).

layer. Importantly, NCPRE acid textured wafers also exhibit surface reflectance values (see red curve in Figure 7.3) and WAR distributions similar to that of additive-based acid textured DWS mc-Si wafers. These surface reflectance values with similar WAR value distributions indicate that the front surface reflection loss of proposed NCPRE additive-free acid texturing scheme is comparable to that of additive-based industrial acid texturing process.

7.5 Minority carrier lifetime study

The τ_{Eff} values of the symmetrical lifetime samples depend on several factors such as surface texture uniformity, diffusion homogeneity and passivation quality of the dielectric layer etc. Hence a non-diffused, but chemically passivated representative sample from both the batches of acid textured wafers were also included for Sinton carrier lifetime measurements. In such case, the difference in measured τ_{Eff} values of the chemically passivated samples would be a direct indicator of their surface texture quality. The variation in τ_{Eff} values as a function of carrier injection level for the lifetime test structures and chemically passivated acid textured wafers are depicted in

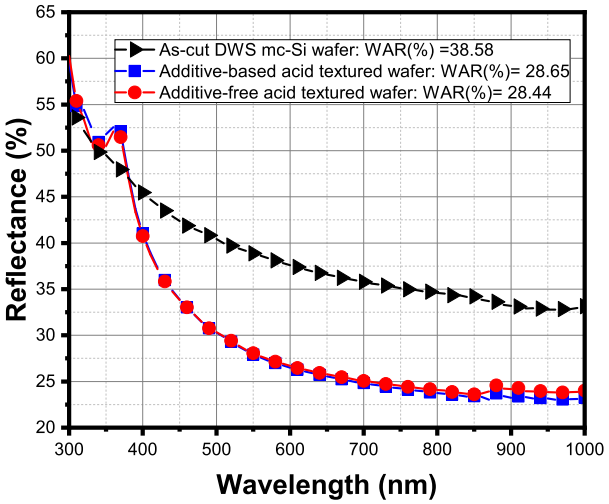

Figure 7.3: Variation in front surface reflectance values of the representative as-cut DWS mc-Si wafer, additive-based acid textured DWS mc-Si wafer (as-textured without ARC) and additive-free acid textured DWS mc-Si wafer (as-textured without ARC).

Figure 7.4. The τ_{Eff} values of the diffused lifetime test samples are noticed to be 54 μs and 72 μs at 2×10^{15} cm^{-3} for additive-based and additive-free groups, respectively. The measured lifetimes values of additive-free diffused lifetime samples were always ~10-20 μs greater than additive-based lifetime samples for the entire minority carrier injection level of interest ranging from 1×10^{15} cm^{-3} to 1×10^{16} cm^{-3}. This results establish that the SiO_2-SiN_x:H stack passivates the additive-free acid textured emitter better than the additive-based acid textured emitter. However, the τ_{Eff} values of the non-diffused, chemically passivated samples were 88 μs and 109 μs at 2×10^{15} cm^{-3} for the additive-based and additive-free acid textured mc-Si wafers, respectively. Here also ~ 20 μs improvement in τ_{Eff} values is observed for additive-free chemically passivated sample over the additive-based acid textured chemically passivated wafers. Similar variation in τ_{Eff} values for the acid textured samples after chemical passivation and after diffusion (passivated by SiN_X:H) suggest the better surface texture quality of the additive-free textured wafers over the reference additive-based samples.

Figure 7.5 represents the inverse Auger corrected lifetime curves plotted against excess carrier concentration extracted from Sinton quasi steady state photo-conductance (QSSPC) measurements. The J_{0e} values are extracted for the diffused lifetime samples from the slope of the curve shown in Figure 7.5 at high level injection conditions. The

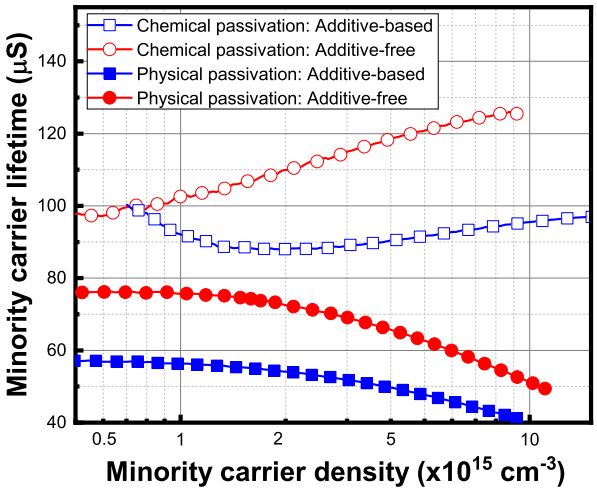

Figure 7.4: Variation in minority carrier lifetime (τ_{Eff}) as a function of injection level for the symmetrical lifetime test structures fabricated on additive-based and additive-free acid textured DWS mc-Si wafers using chemical passivation (not-diffused samples) and physical passivation (diffused samples).

J_{0e} value for the lifetime samples from the additive-based and additive-free group were 107 $fA-cm^{-2}$ and 90 $fA-cm^{-2}$, respectively. These extracted J_{0e} values establish that additive-free acid textured wafers can quantitatively suppress the emitter recombination further by a maximum of 17 $fA-cm^{-2}$ in comparison to the existing additive-based acid textured wafers. The one sun iV_{OC} measured for additive-based and additive-free lifetime samples were 646 mV and 651 mV, respectively. Higher iV_{OC} values again confirms the better passivating nature of the additive-free acid textured surface compared to the additive-based acid textured samples.

Further, the PL images of the samples (test structures used for lifetime measurements) were captured using Lumisolar cell tool of Greateyes for evaluating texture quality and uniformity for its application on complete 6 inch mc-Si wafers. The PL images of the representative samples with PL count distribution histograms are shown in Figure 7.6. A fairly uniform distribution of textures and the quality of textures formed after additive-based process can be inferred from Figure 7.6(a). Similar defect distributions (see in Figure 7.6(b)) with a slightly higher average PL intensity counts (see Figure 7.6(c)) are noticed for additive-free acid textured lifetime samples. Uniform PL intensity counts depicted in Figure 7.6(b) certifies the texture uniformity across the

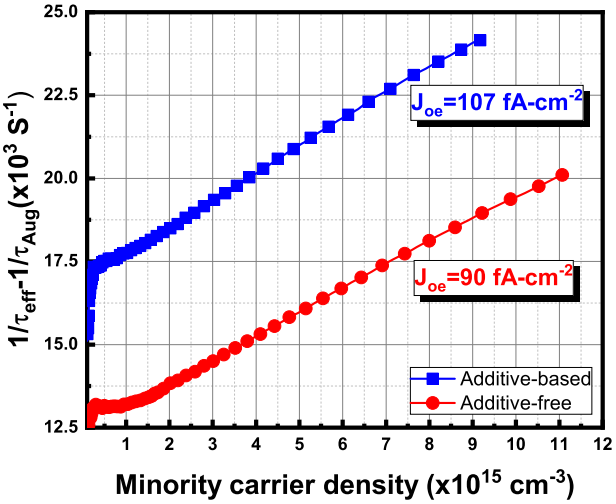

Figure 7.5: Variation in Auger corrected inverse lifetime as a function of injection level for the symmetrical lifetime test structures fabricated on additive-based and additive-free acid textured emitter diffused DWS mc-Si wafers passivated by SiN_X:H.

wafer for additive-free acid process. The change in PL intensity counts for lifetime test structures directly correlate to its surface texture quality or the effectiveness of the SiO_2-SiN_x:H stack for passivating the acid textured emitters. Hence, the PL images in Figure 7.6 also supports the improved minority carrier lifetime of ~ 10 - 20 μs measured for additive-free samples in Sinton QSSPC measurements.

7.6 Cell results

Comparison of the measured solar cell parameters for the groups were already shown in Table 7.3 at the start of this chapter. Similar batch average η of 18.24% and 18.20% were noted for the additive-based and additive-free cells, respectively. Negligibly small improved batch average efficiency (0.04% absolute) was noticed for additive-based group which originates from the difference in J_{SC} values. However, this gain in η remains insignificant considering the cost of texture additives (see section 7.8) and the use of optimized fabrication process recipes of the additive-based acid textured wafers as compared to our additive-free acid textured wafers. Similar average V_{OC} was measured for both the groups of cells. An absolute 0.19% improved batch average FF value (79.70% for additive-based and 79.89% for additive-free) indicates the competency of

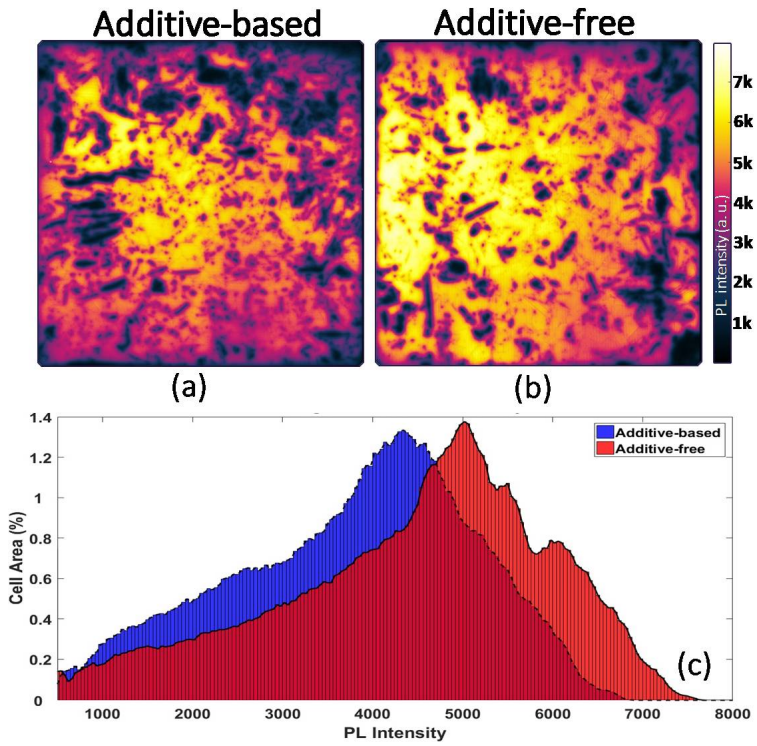

Figure 7.6: Spatially resolved PL intensity maps of the lifetime test structures fabricated on DWS acid textured samples using the (a) additive-based, and, (b) additive-free processes; (c) the PL intensity count histograms of the symmetrical test samples from both the types of textured wafers.

contact formation mechanism achieved on newly textured cells. The contact formation in cells was evaluated with respect to their R_S values. Detailed loss analysis based on the J_{SC}, V_{OC} and R_S values for the representative cells was carried out to investigate the potential of proposed texturing scheme in industrial production environment, as explained in the following sections. The J-V curves of the representative cells chosen from both the batches of cells are depicted in Figure 7.7.

The wavelength dependent EQE, IQE and reflectance values for the cells are plotted in Figure 7.8 for the wavelength ranging from 350 nm to 1050 nm. Higher EQE values were noticed for additive-based acid textured solar cells especially in the blue wavelength ranges. Almost similar IQE values of additive-based and additive-free cells for the entire wavelength range confirms similar bulk material quality as well as surface passivation. This implies that the variation in EQE or J_{SC} is due to the difference in front surface reflectance of the cells. The reflectance and WAR values of the acid textured wafers measured earlier (see Figure 7.3) confirmed that both additive-based

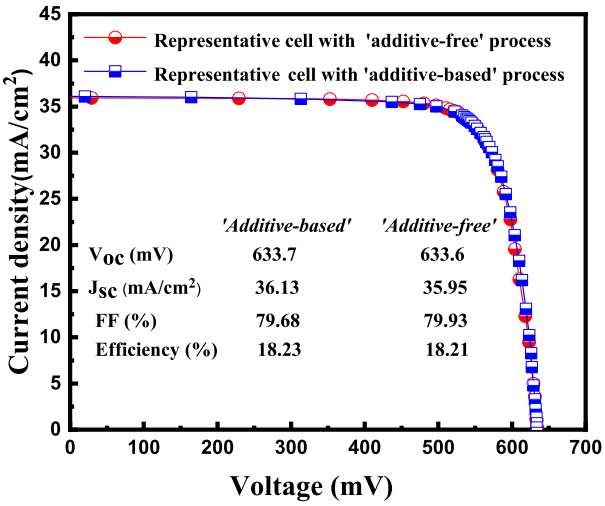

Figure 7.7: Comparison of the measured J-V curves for the additive-based and additive-free acid textured DWS mc-Si Al-BSF representative solar cells.

and additive-free acid textured mc-Si wafers have similar light absorption properties. However, the light trapping capabilities of the textured surface at cell level must also be evaluated after ARC layer deposition. Interestingly, after ARC layer deposition, the overall reflectance of the cells were different (as seen in Figure 7.8) and a significant 1.2% difference in WAR values is noticed (see legend of reflectance curves in Figure 7.8).

Further, the SR of the representative cells from both the types of textured mc-Si wafers was measured using Semilab PV-200 LBIC tool over the entire 156.75 × 156.75 mm^2 cell area for evaluating recombination mechanisms at different regions of the cells. SR values corresponding to short wavelength (λ < 500nm) and long wavelength (λ > 800 nm) indicate the quality of front and rear surface passivation of the cell, respectively. Better surface passivation is specified by high magnitude of SR near the surface. Similarly, middle wavelength (600 < λ < 900 nm) SR accounts for the quality of bulk material. Diffusion length (L) and surface recombination velocities (FSRV for front surface and BSRV for back surface) are the set of parameters used as a measure for evaluating the substrate quality and surface passivation. FSRV, BSRV and L values are extracted from the IQE, reflectance and emitter phosphorous diffusion profiles. The IQE and reflectance maps for the representative cells from both the batches at four available wavelengths (407 nm, 658 nm, 877 nm and 984 nm) in the LBIC system are

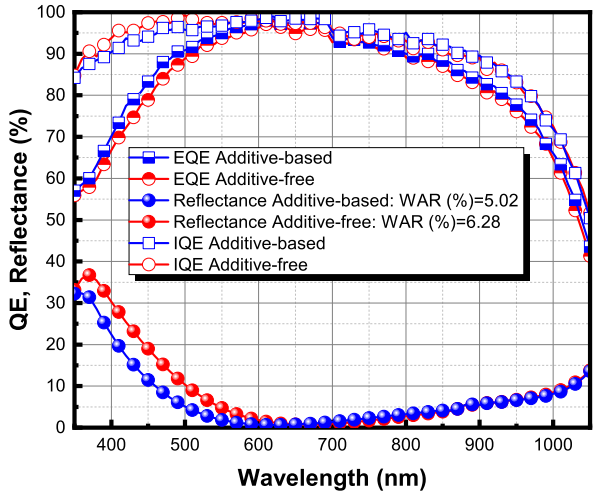

Figure 7.8: Comparison of the measured EQE, IQE and front surface reflectance values for the additive-based and additive-free acid textured DWS mc-Si Al-BSF representative solar cells.

shown in Figure 7.9. The LBIC generated IQE maps follow the similar trends as seen in localized QE measurements (see Figure 7.8). Nearly similar IQE values for middle wavelength range (600 nm to 900 nm) in Benthem IQE tool (see Figure 7.8) indicates that both types of cells were fabricated using mc-Si wafers of similar grade. The average IQE values for the additive-based acid textured cells are 91.14%, 92.39% and 80.63% for 407 nm, 877 nm and 984 nm wavelength, respectively. For the additive-free acid textured cells, these values are 93.81%, 95.20% and 83.74% at 407 nm, 877 nm and 984 nm wavelength, respectively. This consistent and significant enhancement in IQE values observed for shorter and longer wavelengths for the entire cell area implies the reduced recombination kinetics induced at the front and rear surface for the additive-free textured mc-Si cells.

The LBIC generated reflectance maps of representative cells are shown in Figure 7.10. The reflectance maps also follow the similar trends as seen in Benthem QE system (see reflectance in Figure 7.8). The additive-based and additive-free cells exhibited almost similar reflectance for all three available wavelengths except 407 nm. The average R values calculated from LBIC reflectance maps shown in Figure 7.10 for additive-based and additive-free representative cells are 4.05% and 4.1% at 658 nm, 7.85% and 7.64% at 877 nm and 9.6%, and, 9.8% at 984 nm wavelength respectively. The

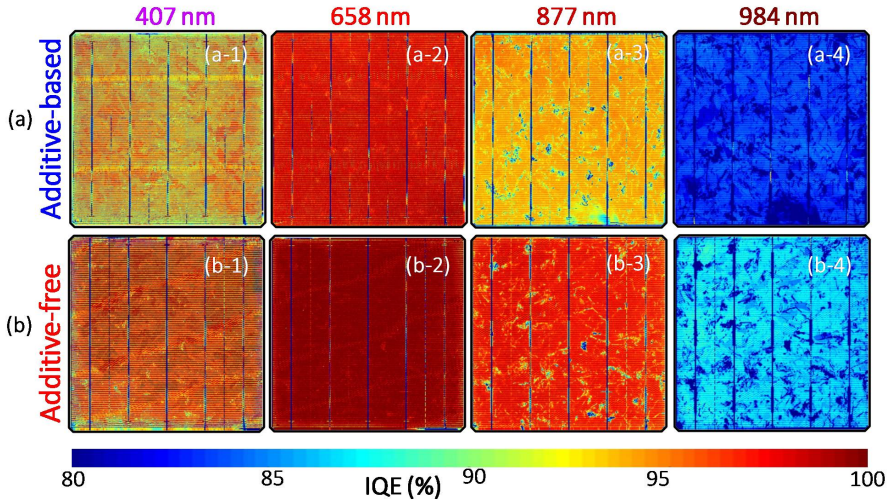

Figure 7.9: LBIC full area single wavelength IQE maps of the representative solar cells fabricated using: (a) additive-based, and (b) additive-free acid textured mc-Si wafer at (1) 407 nm, (2) 658 nm, (3) 877 nm and (4) 984 nm incident wavelengths.

additive-free acid textured cells exhibited higher average reflectance (30.9% average value in LBIC maps and 30% in Bentham QE measurements) compared to the additive-based acid textured cells (24.2% average value in LBIC maps and 23% in Bentham QE measurements) at 407 nm. These LBIC captured reflectance maps thus conclude that the effect of poor short wavelength reflectance (contributing to an increase in WAR value) for the additive-free acid textured mc-Si cells.

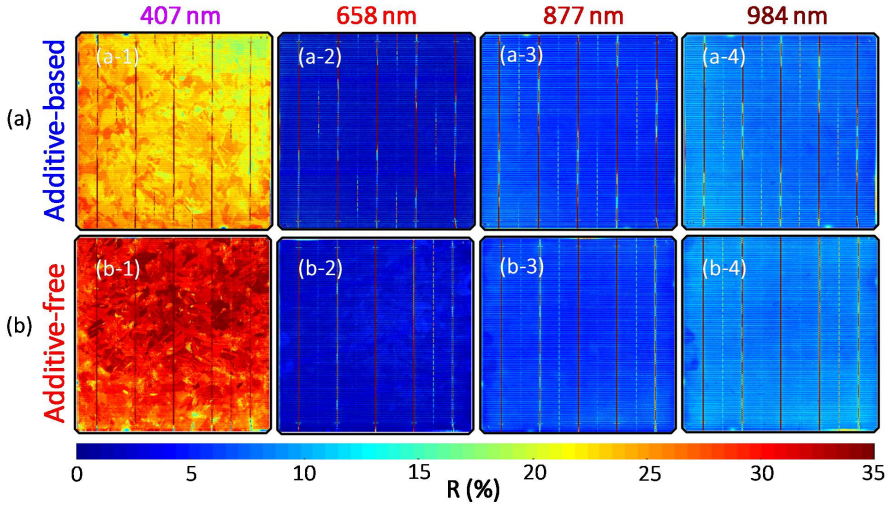

Figure 7.10: LBIC full area single wavelength reflectance maps of the representative solar cells fabricated using: (a) additive-based and (b) additive-free acid textured mc-Si wafer at (1) 407 nm, (2) 658 nm, (3) 877 nm and (4) 984 nm incident wavelengths

The FSRV and BSRV maps of the representative cells are generated following the methods proposed by Sharma et al. [177, 178]. FSRV values can be precisely estimated from the spectral response in the short wavelength range (400 nm $\leq \lambda \leq$ 460 nm) of the solar cells having Gaussian emitter diffusion profiles. Hence, the LBIC generated SR maps at 407 nm and the measured ECV profiles shown in Figure 7.14 are used for estimating FSRV maps in the present case. BSRV values of the rear side p^+-p interface is estimated by considering the SR at two different wavelengths (λ_1, λ_2) such that their absorption length (L_λ) falls in the bulk region ($25\mu m \leq L_{\lambda 1} \leq 50\ \mu m$) and close to rear side ($L_{\lambda 2} \geq 100\ \mu m$)) [178]. So, we have used two of the nearly available wavelengths 877 nm ($L_\lambda \approx 20\ \mu m$) and 984 nm ($L_\lambda \approx 125\ \mu m$) in the LBIC system for generating BSRV maps. Figure 7.11 and Figure 7.12 represents FSRV and BSRV maps for the additive-based and additive-free acid textured cells, respectively. The mean and standard deviation values of the FSRV calculated from the maps indicated in Figure 7.11 are 5.42 ± 2.52× 10^4 *cm-s*$^{-1}$ and 2.53 ± 1.25× 10^4 *cm-s*$^{-1}$, respectively for the additive-based and additive-free batch representative mc-Si cells. This reduction in average FSRV values quantitatively substantiate the enhancement in better blue response achieved for additive-free batch of cells. This again confirms the better passivating nature of additive-free textured emitters. An excellent average BSRV values less than 300 *cm-s*$^{-1}$ are noticed for both the additive-based and additive-free batch representative full area Al-BSF solar cells. However, a minor reduction in BSRV values were observed for the additive-free acid textured cells over the other. The mean and standard deviation values of the BSRV calculated from Figure 7.12 are 299 ± 49 *cm-s*$^{-1}$ and 275 ± 47 *cm-s*$^{-1}$ for additive-based and additive-free textured cells, respectively. The Ag-Al and Al back metalization process parameters remained same for both the batch of cells. Hence this minor improvement in BSRV values for full area Al-BSF cells can be related to the better rear surface texture quality of the additive-free acid textured mc-Si wafers.

The front Ag contact formation to the diffused n^+ layer through ARC layer depends on various components such as surface texture morphology [193], diffusion profiles and R_{sheet} values [194, 195], ARC layers [196], paste composition [197, 198] and co-firing profile [195, 199]. The ARC layer deposition conditions, paste composition and the firing profiles used were similar for both the types of acid textured cells.

Different diffusion profiles (120 Ω/sq for the additive-based group and 90 Ω/sq for

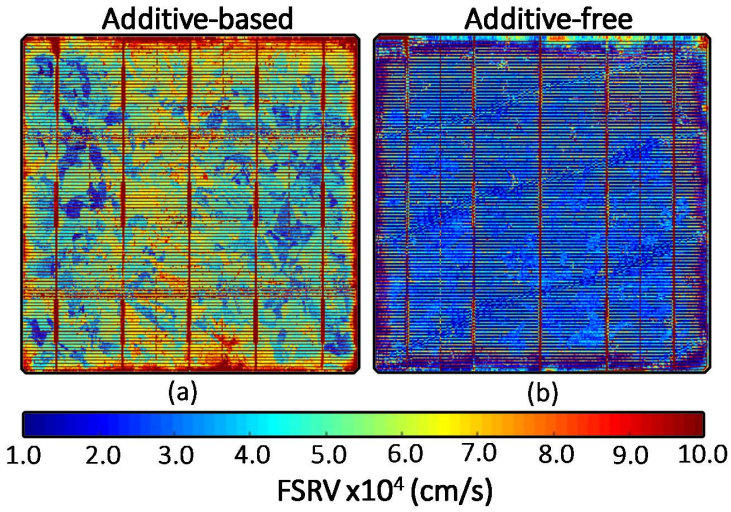

Figure 7.11: Full area FSRV maps of the representative Al-BSF solar cells fabricated using: (a) additive-based, and, (b) additive-free acid textured DWS mc-Si wafers.

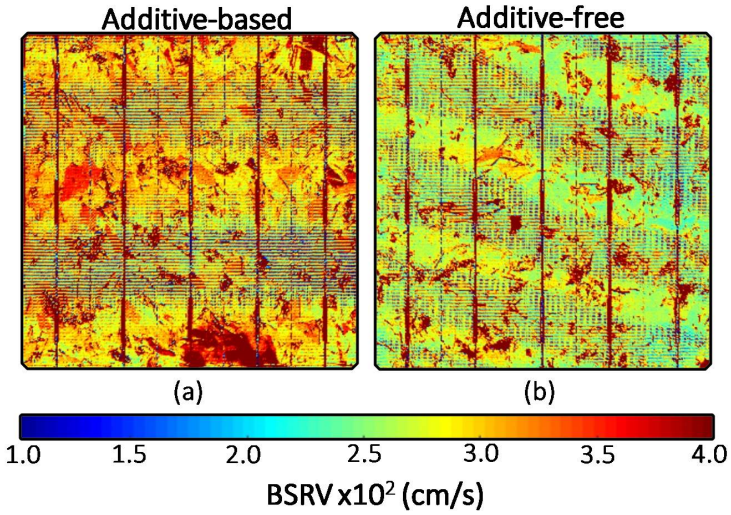

Figure 7.12: Full area BSRV maps of the representative Al-BSF solar cells fabricated using: (a) additive-based, and, (b) additive-free acid textured DWS mc-Si wafers.

the additive-free group) used for emitter formation would impact the contact resistance. However, similar peak surface concentration of $3\times10^{20}cm^{-3}$ used in both the diffusion profiles (see ECV profiles in Figure 7.14) should result in similar range of emitter contact resistance values. We have used R_S map of the representative cells for comparing the contact formation mechanisms on the newly proposed acid textured surface. The R_S maps of the representative cells were generated following the interpolation method proposed by Kampwerth *et al.* [179]. The generated R_S maps of the representative

cells are shown in Figure 7.13 along with their histogram distributions. The histogram in Figure 7.13 (c) clearly indicates that the additive-free batch of cells have slightly improved and wide range of distributed R_S values compared to the additive-based acid textured cells. The mean and standard deviation values of the R_S calculated from the maps indicated in Figure 7.13 were 380 ± 60 mΩcm^2 and 340 ± 90 mΩcm^2 for the additive-based and additive-free batch of cells, respectively. The brighter regions in the maps represents high R_S and is due to the presence of the broken fingers. However, this breakage of metal fingers have not affected the overall lumped R_S values of the cells because of the higher density of finger mesh with 106 fingers. The darker regions in Figure 7.13 (b) represents low R_S regimes and the comparatively uniformly size distributed textures formed for the additive-free acid texturing (see SEM images in Figure 7.2) and the relatively heavier diffusion (90 Ω/sq) can be the reason for the same.

The batch average shunt resistance (R_{Sh}) values are 80 kΩ-cm^2 and 120 kΩ-cm^2 for the additive-based and additive-free acid textured mc-Si cells, respectively. This lower R_S and improved R_{Sh} values resulted due to comparatively uniformly distributed textures and relatively heavier diffusion of the additive-free acid textured cells and thus can be considered for the improved batch average FF values (see Table 7.3). These R_S maps and batch FF values hence confirms that the textures formed after the additive-free acid texturing scheme does not adversely impact the contact formation and is favorable for large area industrial cell production.

7.7 Opportunities for further improvement

We have analyzed the impact of different phosphorous diffusions for the additive-based and additive-free acid textured wafers here. The phosphorous dopant profiles of the textured wafers (used for cell fabrication) are measured after diffusion and PSG etching and the R_{sheet} corrected diffusion profiles are depicted in Figure 7.14. The R_{sheet} maps of the diffused wafers are also shown in Figure 7.14. Measured R_{sheet} values and ECV profiles clearly indicate that the additive-free acid textured wafers underwent deeper diffusion (90 Ω/sq) compared to regular production line diffusion process (120 Ω/sq) with the additive-based texturing. The obvious consequence of these deeper junctions are poor SR in the blue wavelength regions, hence resulting in lower J_{SC} for

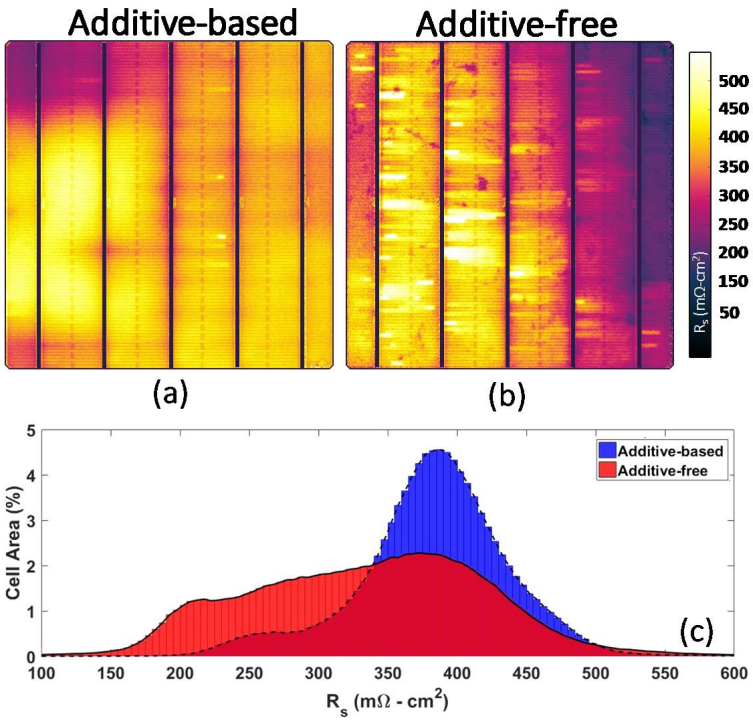

Figure 7.13: Spatially resolved series resistance (R_S) maps of the DWS mc-Si solar cells fabricated using (a) additive-based, and, (b) additive-free acid textured processed wafers. R_S distribution histograms all along the cell area are depicted in (c).

the additive-free cells. PC1D simulations were performed to fit and model the additive-free acid textured cells performance for quantifying the variation in SR or J_{SC} in blue wavelength region due to the difference in emitter diffusion profiles. Simulated EQE and IQE responses obtained for the cells with 90 Ω/sq and 120 Ω/sq diffusion profiles are compared in Figure 7.15. Measured R values (by spectrophotometer) of additive-free acid textured wafers after ARC deposition (see red reflectance curve in Figure 7.15) and the 90 Ω/sq diffusion profile shown in Figure 7.14 (red curve) are considered as an input to the PC1D simulator models. Also, the matched spectral response are further evaluated by replacing the 90 Ω/sq profile with the 120 Ω/sq diffusion profile. The J_{SC} values extracted from the simulated EQE, IQE curves shown in Figure 7.15 are 35.9 mA/cm^2, 38.6 mA/cm^2, respectively, for the 90Ω/sq emitter and 36 mA/cm^2, 38.7 mA/cm^2, respectively, for the 120 Ω/sq emitter. Clear enhancement in both EQE and IQE values is noticed for the simulated 120 Ω/sq diffused cells over the experimental data based 90 Ω/sq simulated diffused cells in the blue regions and it has raised the J_{SC} by ~0.1 mA/cm^2. This improvement in blue response obtained for the 120 Ω/sq emitter

is because of sharp change in carrier concentration and critical p-n junction placement, eventually resulting in better electric field for charge separation and improved carrier collection. These simulations suggest that NCPRE additive-free acid textured mc-Si solar cells would have yielded similar J_{SC} and η as that of additive-based acid textured cells with 120 Ω/sq diffused emitter.

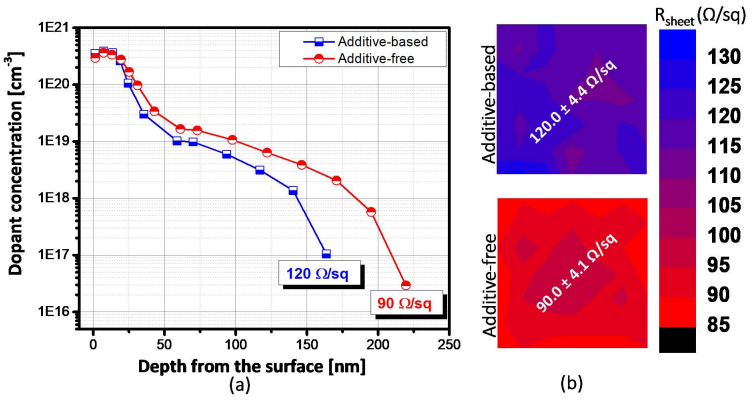

Figure 7.14: (a) Active phosphorous dopant impurity profiles of the emitters used for the fabrication of additive-based and additive-free acid batches of full area Al-BSF solar cells. (b) The measured R_{sheet} distribution maps of the emitters across the diffused wafers

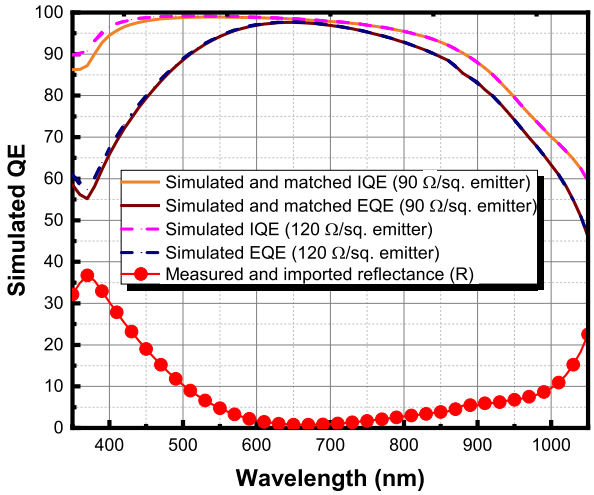

Figure 7.15: Simulated EQE and IQE responses of the full area Al-BSF cells modeled using PC1D simulator using the 90 Ω/sq and 120 Ω/sq emitter diffusion profiles.

To assure maximum photo-generation in solar cells, ARC layer thickness is ad-

justed in such way that the minimum reflectance point falls near 620 nm (region where maximum photon flux in available AM1.5 solar spectrum). In this particular industrial line, their ARC deposition process is optimized for additive-based acid textured mc-Si wafer surface. For convenience, same deposition process parameters were also used for our additive-free acid textured mc-Si wafers, which has slightly different topography compared to additive-based acid wafers as mentioned in section 7.3. As a result, under similar ARC deposition conditions, the minimum reflection point for additive-based and additive-free textured wafers were found at 620 nm and 670 nm, respectively. For the additive-free batch of cells, this shifted reflectance curves has resulted in 1.2% increase in WAR and a consequent reduction in J_{SC}. Since the surface texture size distributions were different (see the SEM images in Figure 7.2) for both the types of textured wafers, we propose re-optimization of ARC layer thickness on the additive-free acid textured wafers targeting minimum reflection in the 600 -6 30 nm range. This would essentially result in similar front surface reflectance values and yield improved EQE and J_{SC} values.

The PL intensity ($\phi(i, j)$) and difference in quasi-fermi levels ($V(i, j)$) in semiconductors are related as,

$$V(i, j) = V_T(i, j) \ln \frac{\phi(i, j)}{C(i, j)} \tag{7.1}$$

where $V_T(i, j)$ and $C(i, j)$ are local thermal voltage and calibration constant, respectively. From this relation, relative PL intensity count from a solar cell is a direct indicator of the generated potential (V_{OC}) on the cell. Figure 7.16 (a) and (b) represents the PL images of the additive-based and additive-free representative cells, respectively under open circuit conditions. The PL count histograms of the cells are depicted below the PL images in Figure 7.16. Similar and uniform PL count distributions over the entire sample area as shown in Figure 7.16 confirm that the SiN_x:H ARC layer uniformly passivates both the additive-based acid textured 120 Ω/sq and additive-free acid textured 90 Ω/sq emitters . In a recent study, Shanmugam *et al.* [194] reported 19 $fA - cm^{-2}$ reduction in J_{0e} and a corresponding 4 mV gain in iV_{OC} for 130 Ω/sq emitters over 90 Ω/sq emitter for the lifetime test structures fabricated on acid textured mc-Si samples. In the present study, the additive-free acid textured lifetime test structures exhibits a similar reduction in J_{0e} of 17 $fA - cm^{-2}$ and enhancement in iV_{OC} of 5mV over the additive-based lifetime samples (see section 7.5) when both the kinds of samples

were subjected to identical emitter diffusions and dielectric passivation. These results justify that the better short wavelength response obtained for the additive-free acid textured wafers (due to the improved surface texture quality) is nearly compensated with increased Auger recombination in 90 Ω/sq emitter, resulting in similar potential generation i.e., PL counts) to that of the additive-based acid textured 120 Ω/sq emitter solar cells. The important implication of the result is that the additive-free acid textured batch of cells can generate better V_{OC} by employing the 120 Ω/sq shallow diffusion.

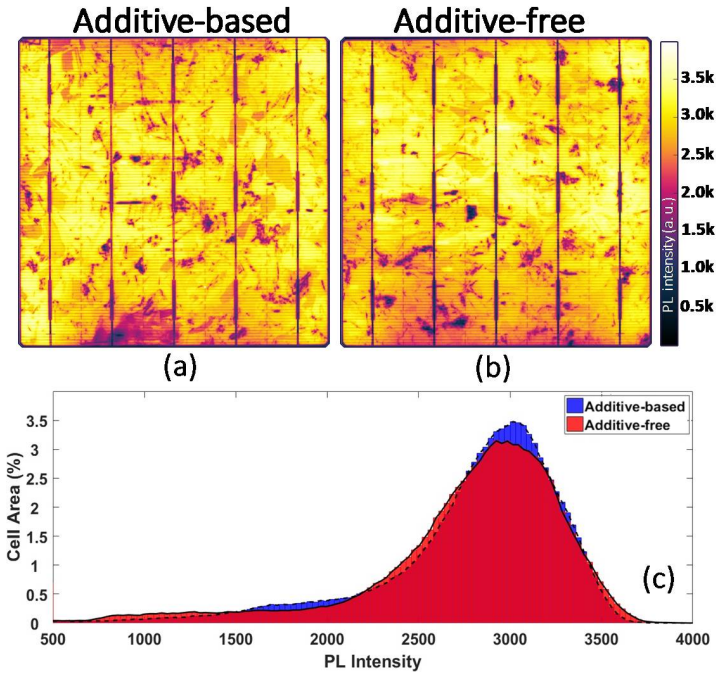

Figure 7.16: Spatially resolved PL intensity maps of the representative DWS mc-Si solar cells fabricated using (a) additive-based, and, (b) additive-free acid textured processed wafers. PL intensity count histograms are shown beneath the PL maps.

7.8 Cost and safety analysis

An approximate cost analysis of both the additive-based and additive-free acid texturing processes is carried out in terms of used process chemicals. For our calculation, as an industry standard, we have considered 600000 wafers to be processed in a single acid texturing bath. The cost per wafer (in US Dollars ($)) is calculated in terms of the cost per wafer for preparing the acid bath for each method. The texture additive was dosed intermittently into the acid textured solution and a total of 70 liters of additive

Table 7.4: Approximate chemical cost involved for the preparation of acid solution bath for additive-based and additive-free texturing processes.

Acid texturing process			
Additive-based		Additive-free	
Chemical used	Cost ($)	Chemical used	Cost ($)
HF(71 l)	1115.71	HF(120 l)	1885.71
HNO_3(165 l)	1579.30	HNO_3(70 l)	670.00
DI water (163 l)	0.80	DI water (209 l)	1.02
Texture additive (70 l)	3440.00	Texture additive (NA)	-
Total cost	6135.81	Total cost	2556.73
Cost per wafer	0.0102	Cost per wafer	0.0042

was used for texturing of 600000 wafers in the additive-based texturing process. However, dosing of acids during the complete process was not taken into consideration here. This is because the dosing pattern remains similar in both the processes. From Table 7.4, it is evident that the chemical cost per wafer for preparing the acid bath for additive-based and additive-free method are approximately 0.0102$ and 0.0042$, respectively. The chemical solution cost is dominated by the costly texture additives. Hence the chemical cost involved in acid bath preparation for additive-free texturing process is nearly 60% economical than the other. Another interesting fact is that since the NCPRE acid texturing process doesn't require any additional chemicals than those used in the existing SWS mc-Si acid texturing and DWS additive-based acid texturing, no additional precautions related to environmental and accidental hazards are required during chemical waste disposal process.

7.9 Conclusions

NCPRE additive-free acid texturing process, was demonstrated for texturing and cell fabrication of large area DWS mc-Si wafers in industrial environment without altering the production throughput. Additive-free acid-textured wafers and cells exhibited

excellent optical, electronic and electrical properties compared to the existing additive-based acid textured wafers and cells. Further, the pathways for improving the performance of additive-free textured cells are proposed after a comprehensive loss analysis. The chemical cost analysis suggested that the additive-free acid texturing process can reduce the chemical cost involved in preparing the acid bath by 60% compared to the existing additive-based acid texturing process.

Chapter 8

Metal Assisted Chemical Etching Process for Texturing DWS mc-Si Wafers

8.1 Motivation

Fabrication of fine nanostructures, commonly known as b-Si features is one of the potential solution for overcoming the texturing difficulty associated with DWS mc-Si wafers. Several competing technologies such as MACE [166, 167, 200], RIE [14], laser etching [132] etc. are reported for b-Si fabrication. Among these, MACE has emerged as the most viable technology for PV applications because of its low processing cost and high throughput. MACE process is capable of generating wide range of nano-structures from fine porous textures to high aspect ratio needle-shaped structures simply by fine-tuning the process parameters [164, 167, 168]. In spite of the recent studies proposing MACE as a universal texturing process for both c-Si and mc-Si solar cell production [15, 201, 202, 203], the potential of MACE process over acid texturing is not fully realized yet.

As discussed in chapter 3, currently the b-Si textured mc-Si wafers are not directly used for solar cell fabrication, as the PECVD SiN_X:H ARC is incapable of effectively passivating these tiny porous features with high density of surface defects. Hence, controlled etching of MACE b-Si features to generate more wider nano-structures, that can be passivated by PECVD SiN_X:H ARC is adopted for assuring higher performance

in MACE nano-textured mc-Si solar cells. Different processes such as alkaline etching [173], acid etching [135, 166], NSR process [162, 165] and RIE [133] were previously reported for b-Si surface modification. Among these, acid etching is expected to be employed in the industry as the transfer chemistry is well known and widely used in industry.

This chapter starts with the discussion of MACE b-Si generation process and optimization of acid etching for achieving nano-textures with optimal surface recombination and reflection. Acid etching process using HF - HNO_3 solution for the surface modification of b-Si features is discussed. Later, a comprehensive performance parameter analysis of MACE nano-textured and acid textured industrial mc-Si solar cells is performed to demonstrate the advantages and potential of nano-textures over micron-sized iso-textures.

8.2 Optimization of MACE nano-texturing process

8.2.1 Process details

DWS mc-Si wafers of base resistivity of 1-3 Ω-cm and size of 5 cm × 5 cm were used for MACE process optimization. Figure 8.1 represents the process flow used for sample fabrication and characterization. SDE of the samples were performed in concentrated alkaline solution. Ag nanoparticles were deposited on SDE samples using 0.01M $AgNO_3$ solution. The wafers were then etched in HF and H_2O_2 solution for b-Si formation. b-Si structures were modified by etching the wafers in HF - HNO_3 solution at room temperature for 20, 40 and 60 sec. Thereafter, residual metal ions present on the wafer surface are eliminated by treating the wafers with HNO_3 solution at room temperature for 10 min. Quine-hydrone in methanol (QHM) solution was used for chemical passivation of samples.

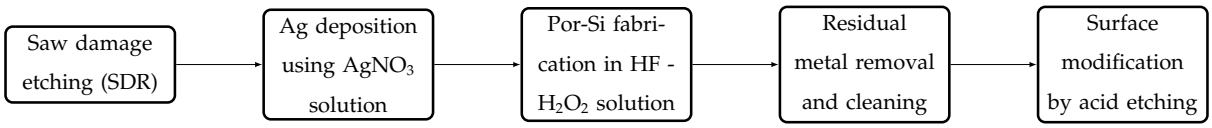

Figure 8.1: Process flow for b-Si fabrication and b-Si surface modification.

Figure 8.2 (a) represents the randomly distributed Ag nano-particles with size

ranging from 20 nm to 500 nm on SDE DWS mc-Si wafers. Size of the b-Si features depends on the size of Ag nano-particles. The b-Si surface features obtained after treating the Ag nano-particle deposited mc-Si wafers with HF - H_2O_2 solution for 2 min are shown in Figure 8.2 (b). As seen in Figure 8.2 (b), b-Si surface is highly porous, consists of fine features with lot of surface defects, which act as heavy recombination cites during carrier transport. Hence, surface modification is needed for b-Si based solar cells for ensuring reduced surface recombination at the emitter and rear sides of the solar cells.

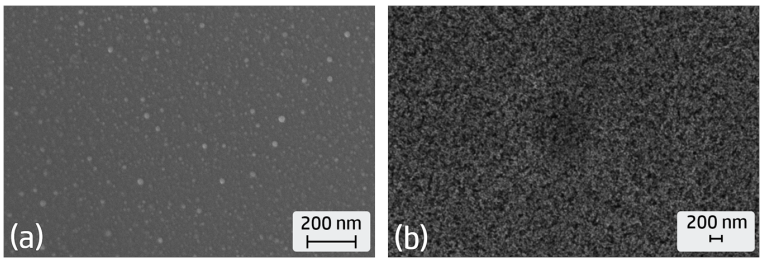

Figure 8.2: SEM images of mc-Si wafers with (a) Ag nano-particles, and, (b) b-Si features after HF - H_2O_2 treatment.

Figure 8.3 depicts the SEM images of b-Si surface treated with HF - HNO_3 solution for 20 sec, 40 sec and 60 sec. HF - HNO_3 helps to widen/open up the nano-pores to form inverted scallop/pit structure and the size of these structures increases with HF - HNO_3 processing time. It is also noted that, the size/ dimensions of surface textures obtained by acid etching of MACE b-Si samples are in nano-meter range for all three groups.

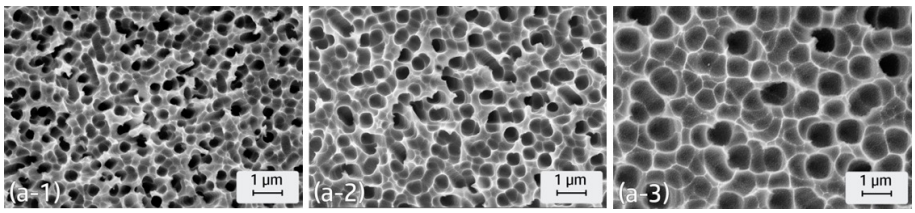

Figure 8.3: SEM images of b-Si surfaces after etching in HF - HNO_3 solution for (a-1) 20 sec, (a-2) 40 sec and (a-3) 60 sec.

The surface reflectance and WAR values of the b-Si surface and acid etched b-Si surfaces are shown in Figure 8.4. The reflectance values of the conventionally acid textured DWS mc-Si wafer is shown as reference in Figure 8.4. b-Si samples showed

excellent light absorption for the entire wavelength range of 300-1000 nm with an impressive WAR of 3.5%. Surface reflectance values have increased to certain level after HF - HNO_3 surface modification for different etching times. However, all acid etched b-Si samples still have lower WAR values as compared to the reference sample. These reflectance curves clearly indicate the light trapping abilities of MACE acid etched b-Si samples over the conventional acid textured samples currently used in industry.

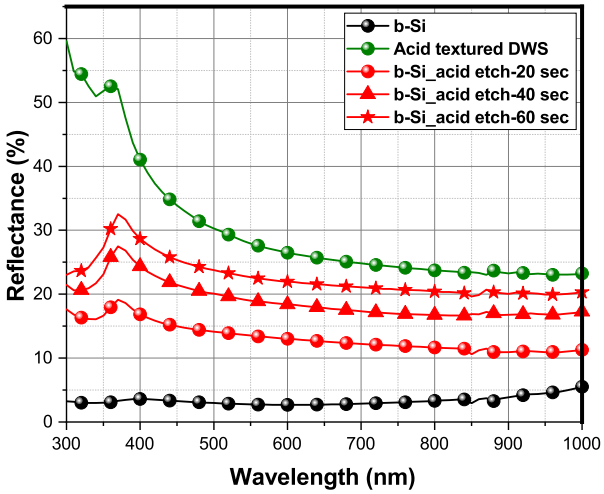

Figure 8.4: Comparison of surface reflectance values of b-Si and acid etched b-Si surfaces.

The acid textured DWS, b-Si and b-Si surface modified samples were chemically passivated using QHM solution, after HCl cleaning and HF dip. The PL images of the passivated samples are shown in Figure 8.5. Figure 8.5 (a) and 8.5 (b) represents the PL images of acid textured DWS and b-Si samples, respectively. Poor PL counts in Figure 8.5 (b) confirms the poor passivation quality of b-Si surface compared to acid textured DWS mc-Si samples. This indicates that the high density of defects present on the b-Si seen in Figure 8.2 are extremely difficult to get passivated. However, the PL images in Figure 8.5 (c), 8.5 (d) and 8.5 (e) suggests that the HF - HNO_3 surface modification step improves surface quality. The measured τ_{Eff} at $1{\times}10^{15}$ cm^{-3} MCD of the chemically passivated samples are listed in Table 8.1 along with WAR values and average PL counts over the entire sample area. 60 sec acid etched b-Si samples exhibited excellent surface passivation properties similar to that of acid textured DWS

(similar range of PL counts and τ_{Eff}) and outstanding light trapping properties with nearly 8% lower WAR than that of acid textured DWS samples. These results suggest that b-Si modification process by acid etching process is effective in bringing down the WAR values of DWS mc-Si wafers to nearly 20% without compromising on the τ_{Eff} values.

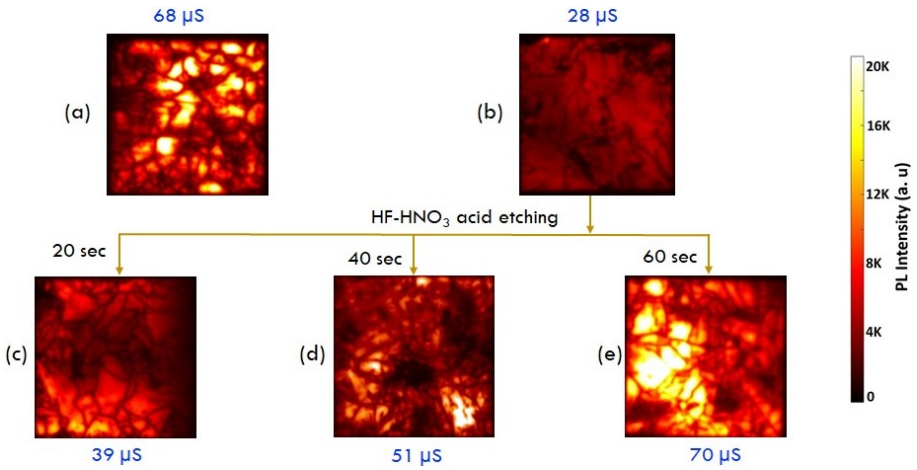

Figure 8.5: PL images of chemically passivated mc-Si wafers with (a) acid textured, (b) b-Si, and acid etched surfaces for (c) 20 sec, (d) 40 sec and (f) 60 sec.

Table 8.1: Summary of WAR values, τ_{Eff} and average PL counts of b-Si and modified b-Si surfaces.

Sample Name (-)	WAR (%)	Effective carrier lifetime (μs)	Average PL count (-)
Acid textured DWS	28.6	68	6223
b-Si	3.5	28	3139
b-Si_acid etch-20 sec	12.3	39	3700
b-Si_acid etch-40 sec	18.3	51	3983
b-Si_acid etch-60 sec	20.9	70	6502

In the following sections, the performance and two diode parameters of solar cells fabricated on acid etched MACE b-Si wafers and conventional acid textured DWS mc-Si samples are compared for demonstrating the advantage of nano-textures over iso-textures. The process details, morphological, optical and electronic properties of

acid textured (micron-sized iso-texture) and MACE nano-textured samples used for solar cell fabrication (after surface modification by acid etching) are presented. Further a detailed loss analysis of performance parameter and comparison of two diode parameters of acid textured and MACE nano-textured solar cells are performed using advanced characterization techniques such as PL images, LBIC maps and lock-in thermography.

8.3 Texturing and solar cell fabrication

Industrial grade 156.75 × 156.75 mm^2 p-type DWS mc-Si wafers were used for solar cell fabrication. Acid texturing process used is a combination of HF, HNO_3 and DI water solution at temperature of 10-12°C for simultaneous saw damage etching (SDE), and micron-sized inverted scallop-like texture was created. The MACE nano-texturing process used in industry also consisted of four steps: (i) SDE in acid solution, (ii) silver (Ag) nano-particle deposition by soaking the SDE mc-Si wafers in silver nitrate ($AgNO_3$) solution, (iii) Ag assisted silicon etching in HF-hydrogen peroxide (H_2O_2) solution for b-Si nano-structure generation, and (iv) b-Si modification by etching in HF - HNO_3 acid solution. Both the sets of textured wafers after essential native oxide cum residual metal ion etching in HF-HCl solution, underwent phosphorous diffusion, phospho-silicate glass etching and junction isolation, silicon nitride ARC deposition and front silver and back Ag-Al metalization to complete the Al-BSF solar cell fabrication in an industrial line.

8.4 Comparison of morphological, optical and electronic properties of textured mc-Si surfaces

The high resolution SEM images shown in Figure 8.6 indicate that the inverted pit-like nano-textures (Figure 8.6 (b-1 to b-3) obtained by acid etching of MACE b-Si samples (MACE nano-textures) are smaller (diameter in the range of 300-500 nm) and more uniformly distributed compared to micron-sized iso-textures (Figure 8.6 (a-1 to a-3)) obtained by acid texturing. Acid texturing process nucleates on surface defects and saw damages and hence, requires uniform layer of sufficient surface damages for producing

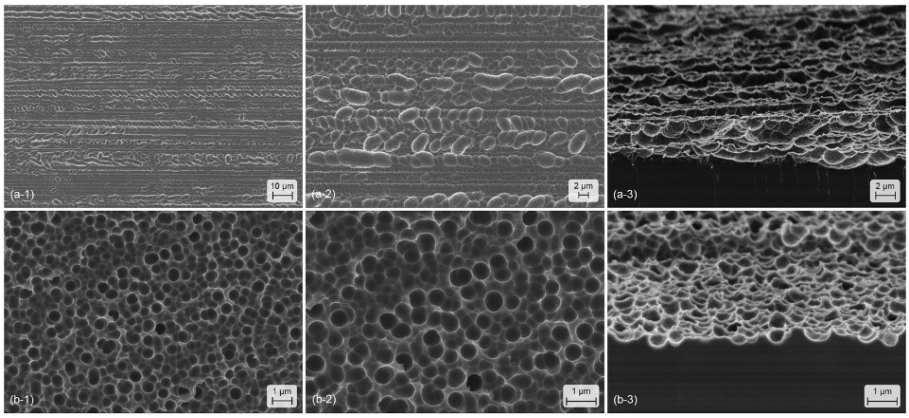

Figure 8.6: SEM images of textured DWS mc-Si wafers. (a-3) and (b-3) are tilted cross section images, and the others are top view images. (a-1) to (a-3) acid textured, (b-1) to (b-3) MACE nano-textured.

uniform 2-4 μm sized inverted scalloped textures as obtained in MWSS mc-Si wafers. However DWS method produce relatively polished wafers, and as a consequence, acid texturing results in non-uniform texture generation with larger textures forming mainly along the wire saw mark directions and the places where saw damages were initially present. In contrast, the nano-textures formed by MACE process are uniformly distributed across the wafer surface area and are independent of initial morphology of the as-cut wafers due to the uniform etching behavior of Ag nano-particle assisted chemical etching of silicon samples in H_2O_2 - HF solution regardless of crystallographic planes, as reported elsewhere [165, 168]. Hence, the subsequent etching of b-Si samples in isotropic HF - HNO_3 solution also produces uniform inverted pits-like textures across the DWS mc-Si wafer surface.

The surface reflectance of the samples are compared in Figure 8.7. WAR of 28.65% and 19.53% were estimated for acid textured and MACE nano-textured wafer surfaces, respectively. The effective minority carrier lifetime of chemically passivated acid textured and MACE nano-textured samples are shown in Figure 8.8. Similar range of effective carrier lifetime values are measured for both the groups of textured samples.

8.5 Solar cell I-V results

The AM 1.5G I-V characteristics of representative solar cells are shown in Figure 8.9 and the batch average performance parameters are listed in the inset of the Figure Nearly

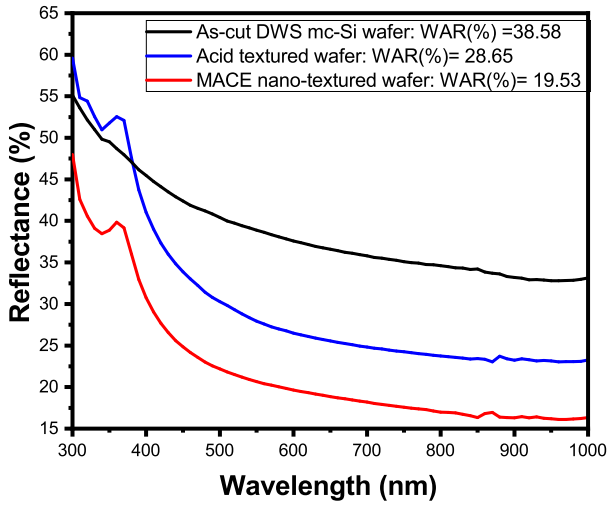

Figure 8.7: Wavelength dependent total surface reflectance values of representative as-cut, acid textured and MACE nano-textured DWS mc-Si wafers.

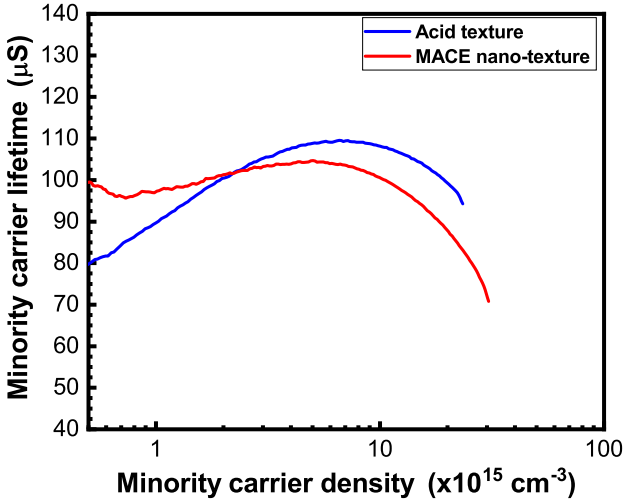

Figure 8.8: Minority carrier density dependent minority carrier lifetime values of QHM passivated acid textured, and MACE nano-textured DWS mc-Si wafers.

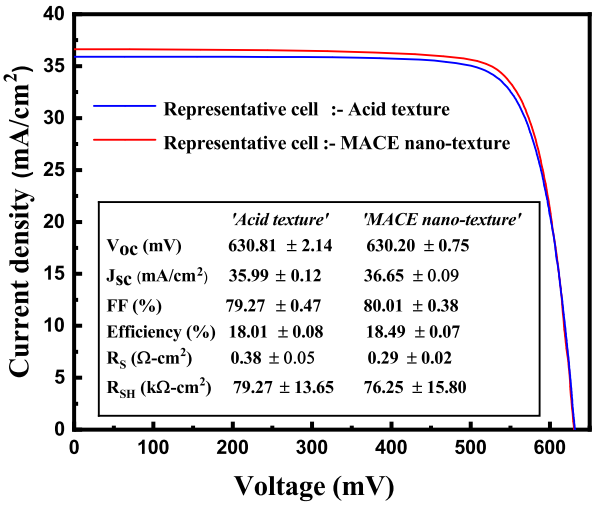

Figure 8.9: Comparison of one sun J-V characteristics of acid textured and MACE nano-textured representative Al-BSF cells. The batch average value of performance parameters for differently textured solar cells are listed in inset of the J-V plots.

0.5% (absolute) enhancement in power conversion efficiency (η) measured for MACE nano-textured solar cells over iso-textured solar cells is in good agreement with the recent literature [15, 166, 168]. The J_{SC} of MACE nano-textured cells is higher by 0.66 mA.cm^{-2}, likely due to lower surface reflection even after ARC coating, and this trend is consistent with the literature reports [15, 200]. V_{OC} on the other hand is marginally lower by 0.61 mV for the MACE nano-textured cells, and this trend is consistent with literature reports [165, 166]. FF values for the MACE nano-textured cells are higher by 0.74% (absolute). MACE nano-textured cells have significantly lower R_S than the acid textured cells, whereas the shunt resistance (R_{SH}) values are comparable. Generally, the FF values of industrial acid textured mc-Si solar cells are marginally lower than alkaline pyramidal textured c-Si solar cells [14, 15]. Our results show that the adoption of MACE nano-texturing process can narrow down this difference further. These results suggest that evaluating the MACE nano-texturing processes only in terms of surface reflection (WAR or J_{SC}) and passivation quality (J_{0e} or V_{OC}) may not describe the complete potential of MACE nano-texturing for both c-Si and mc-Si solar cell applications. In addition, FF of silicon solar cells is influenced by both recombination and resistive losses. Hence, a detailed analysis of various components of losses were conducted and presented in the following sections.

8.5.1 Open circuit voltage analysis

PL intensity count of a solar cell in open circuit represents the quasi fermi-level separation, and hence the open circuit voltage of solar cells [204]. PL intensity distribution across the cell area for acid textured and MACE nano-textured solar cells, and the corresponding intensity histogram are shown in Figure 8.10 . Excitation at 660 nm was used for PL. The reflectance of the cells at 658 nm were found to be nearly identical (see Figure 8.11) and hence no corrections for surface reflection is applied to the PL intensity maps. The PL intensity distribution of the acid textured cells are seen to have slightly higher peak than that of MACE nano-textured cells. This correlates well with the marginally higher V_{OC} for the acid textured cells. It is instructive to compare the lifetime data presented in Figure 8.8, where a marginally higher effective lifetime was obtained for the MACE nano-textured wafers compared to the acid textured wafers, with QHM passivation, for excess minority carrier density below 2×10^{15} cm^{-3}. The PL intensity histograms show the opposite trend, suggesting that the PECVD SiN_X:H passivation of the MACE nano-textured cell is not as effective as the QHM passivation. A better passivation of MACE nano-texture may be achieved with atomic layer deposition (ALD) process due to the conformal deposition capability of ALD, as illustrated using aluminum oxide in [164]. The PL intensity histogram of the MACE nano-textured cells is much tighter than that of the acid textured cell, indicating similar or better process uniformity of MACE nano-texturing.

8.5.2 Short circuit current analysis

LBIC measurements at four wavelengths (407 nm, 658 nm, 877 nm, and 984 nm) were used for analyzing the difference in J_{SC} by mapping the spectral response (IQE & reflectance) of representative solar cells. The IQE and reflectance maps are shown in Figure 8.11. The largest difference in IQE is seen at 407 nm, higher by 0.89% (absolute) for the acid textured cells. This further confirms that the marginally higher V_{OC} seen in the case of acid textured cells is due to better surface passivation, as discussed in subsection 8.5.1. It is clear that the small differences seen in IQE are inadequate to explain the 1.5% higher J_{SC} for the MACE nano-textured cells. The reflectance maps show that the MACE nano-textured wafers result in consistently lower reflectance at all

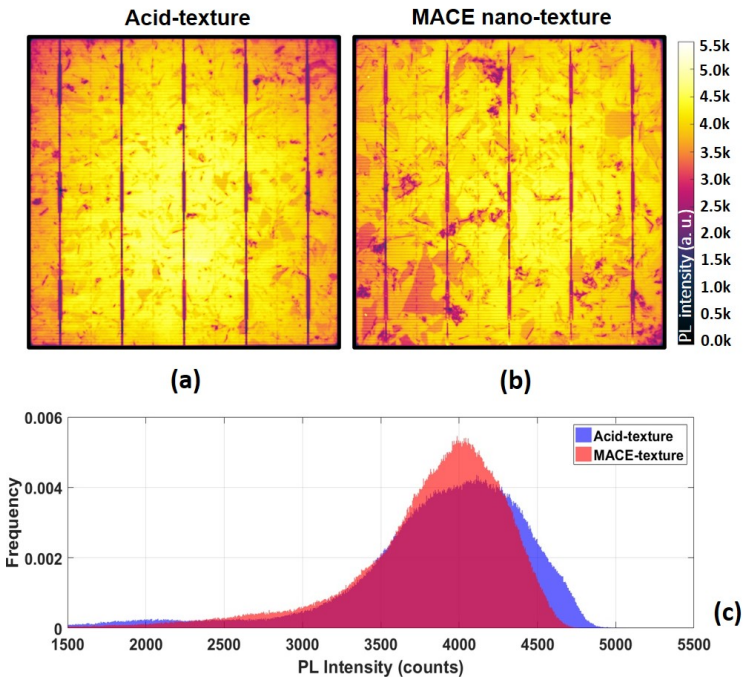

Figure 8.10: Spatially resolved PL intensity distributions of (a) acid textured and (b) MACE nano-textured representative Al-BSF solar cells captured at open circuit condition.

wavelengths, except at 658 nm, where the difference in reflectance is negligible. Based on this analysis, we can conclude that the higher J_{SC} in MACE nano-textured cells is due to improved light trapping.

8.5.3 FF loss analysis

A two diode model based FF loss analysis of silicon solar cells proposed in [205] was applied to the cells, and the results are summarized in Table 8.2. FF($J_{01-limit}$) refers to the apparent FF value without considering the effect of non-idealistic factors such as recombination current density (J_{02}), R_S, and R_{SH}, and the other parameters listed in the Table co-relates to absolute value of loss in FF due to J_{02}, R_S, and R_{SH}. **The J_{01} and J_{02} values of the representative cells are measured using Suns-V_{OC} technique. The J_{01} value was 7.21 $\times$ 10^{-13} A-cm^{-2} and 7.42 $\times$ 10^{-13} A-cm^{-2} (measured at 7 points across the cell area), respectively. Similarly, the J_{02} value measured at 7 different locations of the value was 1.97 $\times$ 10^{-8} A-cm^{-2} and 1.78 $\times$ 10^{-8} A-cm^{-2} for acid textured and MACE nano-textured solar cells, respectively.** The FF loss analysis indicate that the

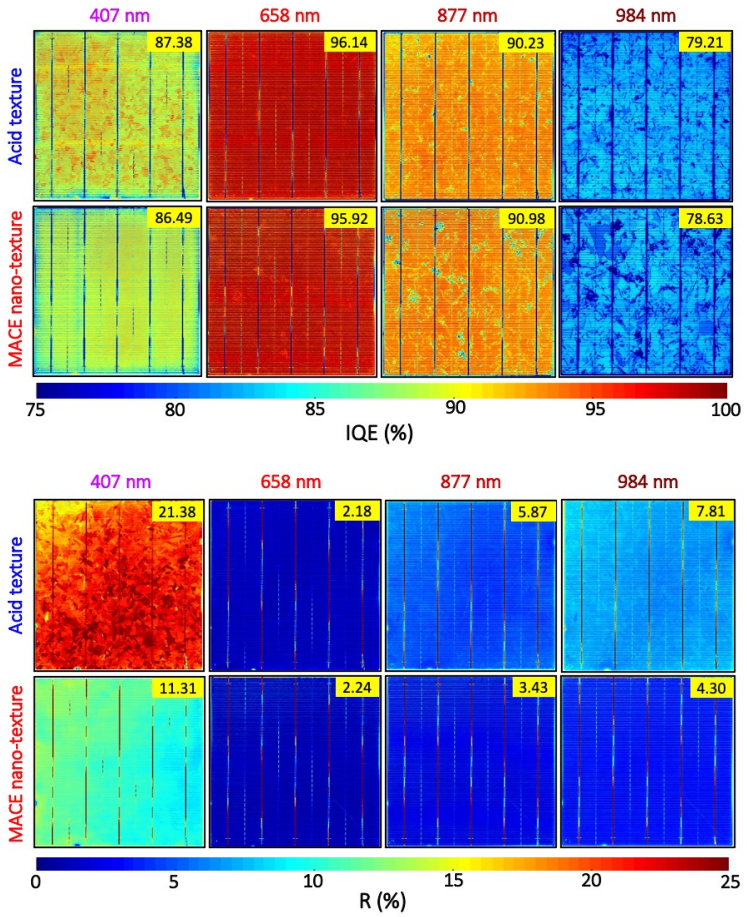

Figure 8.11: (a) IQE and (b) reflectance maps of acid textured and MACE nano-textured representative Al-BSF solar cells measured at four wavelengths. The wafer average in each case is shown at the top right corner.

improved FF values measured for MACE nano-textured solar cells was mainly due to the lower R_S.

Table 8.2: Summary of FF loss analysis for acid textured and MACE nano-textured solar cells.

Texture	FF losses (%)			FF($J_{01-limit}$) (%)	Measured FF (%)
	FF(J_{02})	FF(R_S)	FF(R_{SH})		
Acid	1.80	1.82	0.01	83.44	79.81
MACE	1.88	1.42	0.02	83.47	80.15

In DLIT measurements, four lock-in thermographic images captured under dark conditions (three images at forward bias (0.5 V, 0.55 V, and 0.6 V) and one image at reverse bias condition (-1 V)) are used for generating the local dark current density (J_{01} and J_{02}) and ohmic shunt (ohmic shunts are expressed in terms of parallel conductance (G_p)) maps. DLIT method provides pixel to pixel variation of FF, J_{01}, J_{02}, and G_p values of a solar cells with the help of a Local I-V 2 software discussed elsewhere [206, 207, 208]. Lumped J_{SC} and R_{SH} values of 35.90 mA-cm^{-2} and 360 mΩ-cm^2 (for acid textured representative cell), and 36.64 mA-cm^{-2} and 270 mΩ-cm^2 (for MACE nano-textured representative cell), (obtained from one sun lighted I-V characteristics, refer Figure 8.9), respectively are given as the input to local I-V software for generating the FF, recombination, and conductance maps. For J_{02} maps, the ideality factor (n_2) of second diode in the two diode model was fixed to 2 ($n_2 = 2$). The results are summarized in Figure 8.12, where sub-figures (a-1), (a-2), (a-3), and (a-4) and (b-1), (b-2), (b-3), and (b-4), respectively represents the FF, J_{01}, J_{02} and G_p maps of acid textured and MACE nano-textured representative mc-Si solar cells. The Local I-V 2 software generated FF maps in Figure 8.12 (a) and (b) also agree that the pixel to pixel FF values of MACE nano-textured representative solar cell are better compared to acid textured representative solar cell. Nearly an improvement in FF value of 0.5% (average) is noticed for MACE nano-textured solar cells over iso-textured solar cells, in good agreement with the I-V results shown in Figure 8.9. While examining the J_{01} and J_{02} maps, it can be clearly seen that the lower FF regions in Figure 8.12 (a) and (b) are clearly mapped to higher J_{01} or J_{02} at the exact localized regions in Figure 8.12 (c)-(f). The J_{01} contributing defects are more seen for MACE nano-textured representative cells while the effect of J_{02} shunts were

more severe for acid textured samples especially at edges of solar cells. The number of localized ohmic shunts were higher for MACE nano-textured representative cell than acid textured cell, in agreement with the lumped shunt values of the solar cells. However, this is not valid for all acid textured and MACE nano-textured solar cells as the batch average shunt values of MACE nano-textured solar cells are nearly identical to that of acid textured cells (refer Figure 8.9). In addition, we have also seen that the contribution of the shunt resistance to FF loss is negligibly smaller and nearly identical for both the representative cells. Comparable range and distribution of J_{01}, J_{02} and G_p values confirm that MACE nano-texturing process does not introduce any additional localized recombination or ohmic shunt paths across the solar cell area, rather offers lower R_S to carrier flow compared to acid textured solar cells.

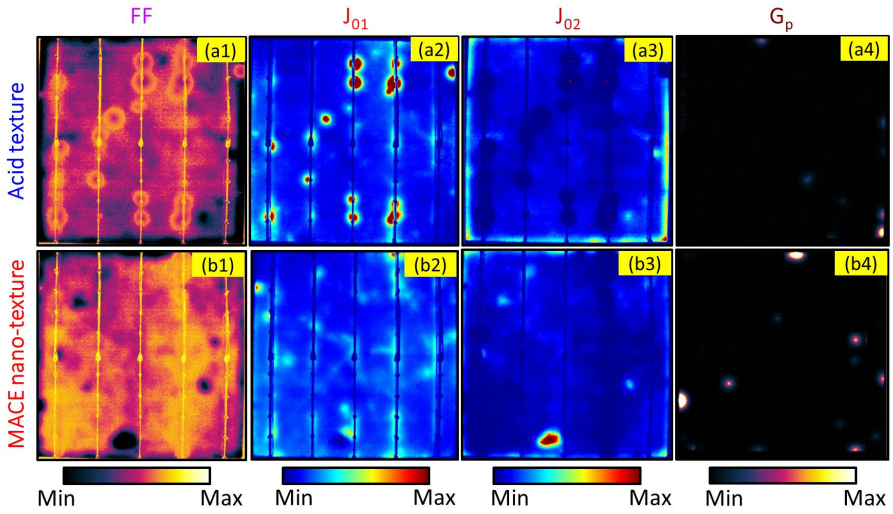

Figure 8.12: Local IV2 software generated (1) FF (scaled from 75 to 83%), (2) J_{01} (scaled from 0 to 5×10^{-12} A-cm^{-2}), (3) J_{02} (scaled from 0 to 5×10^{-7} A-cm^{-2}), and (4) G_p (scaled from 0 to 1×10^{-3} S-cm^{-2}) maps of (a) acid textured and (b) MACE nano-textured Al-BSF mc-Si solar cells.

The series resistance maps generated from biased PL images [179] are shown in Figure 8.13 for representative cells. Histograms of distributed R_S are compared in Figure 8.13 (c). Histogram shows a nearly 100 mΩ-cm^2 lower R_S for the MACE nano-textured cell. The distribution of R_S is also tighter for the MACE nano-textured device, indicating a more uniform underlying process. Notable difference in values of distributed R_S and lumped R_S (shown in the inset of Figure 8.9 - extracted using

the Bowden method [176]) is expected due to the difference in R_S estimation method as reported elsewhere [209, 210, 211]. However the difference in the peak values of the distributed R_S is approximately matching with the difference in the lumped R_S values. Since all metallization process conditions are identical, we hypothesize that the difference in R_S may be attributed to the contact resistance, as the surface texture could play an important role in how the Ag contacts the emitter [193, 209].

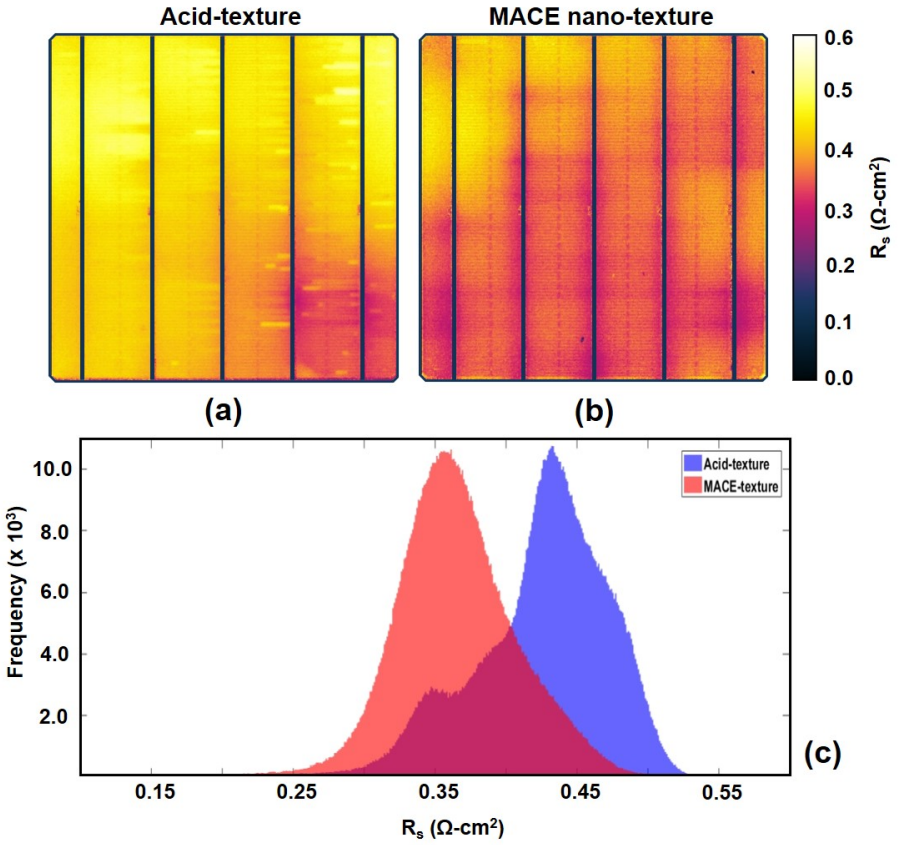

Figure 8.13: Full area spatial variation of distributed R_S values of acid textured and MACE nano-textured mc-Si solar cells.

To investigate the contact formation mechanism on differently textured surfaces, SEM images of Ag particles contacted to the emitter region are analyzed after etching the front silver grid contacts. As reported in previous studies [212, 213, 214, 215, 216, 217], typical screen printed Ag/n^+-Si interface region consists of four distinct components: bulk silver, thin interfacial glass layer, Ag crystallites, and silicon. Since, the phosphorous diffusion process conditions, front metal paste composition and the co-firing profile used are identical for both acid textured and MACE nano-textured solar cells, no considerable difference in bulk Ag layer and n^+ emitter characteristics are expected.

In addition, according to Ag crystallite model [212, 213, 214], the primary current transport mechanism is via either by direct contact of Ag crystallite with bulk Ag or by tunneling through the thin interfacial glass layer present between the bulk Ag and Ag crystallites. Firstly, the bulk Ag metal layer is etched by soaking the pieces of both acid textured and MACE nano-textured solar cells in hydrochloric acid (HCl) - HNO_3 solution at room temperature for 2 hours, thus exposing the interfacial glass layer. The SEM images after this step are shown in Figure 8.14. These SEM images confirm the presence of interfacial glass layer in both types of textured samples. A more uniformly distributed interface layer is observed on MACE nano-textured surface than on acid textured surface. The same samples were subsequently sonicated in DI water for 10 min, and then dipped in 5% HF at room temperature for 5 min for completely removing the interfacial glass layer [218]. The SEM images taken subsequently are shown in Figure 8.14. Previous studies established that for pyramidal textured screen printed c-Si solar cells, Ag crystallites form densely at the tips of pyramids and the density of pyramidal textures inversely co-relates to contact resistance [193, 209]. However, to the best of our knowledge, such studies are not reported on mc-Si solar cells. Figure 8.14 shows that the Ag crystallites are formed mainly along the boundaries of the textures in both types of samples. The SEM images indicate that MACE nano-textured surface has more Ag crystallites per unit area than acid textured surface, due to the smaller textures resulting from the MACE process. This result in smaller contact resistance and thus a lower R_S in MACE nano-textured mc-Si solar cells.

8.6 Conclusions

Cost effective method for the fabrication of nano-textures on mc-Si wafers are demonstrated using a combination of MACE and acid etching process. MACE process was used for b-Si generation and acid etching process was optimized for opto-electronic properties for generating nano-textures suitable for solar cell fabrication. The potential and advantages of nano-textures over micron-sized textures are demonstrated through a detailed comparative analysis of performance parameters and two diode parameters of conventional acid textured and MACE nano-textured industrial DWS mc-Si Al-BSF solar cells. The analysis shows that acid etching of tiny MACE b-Si nano-features

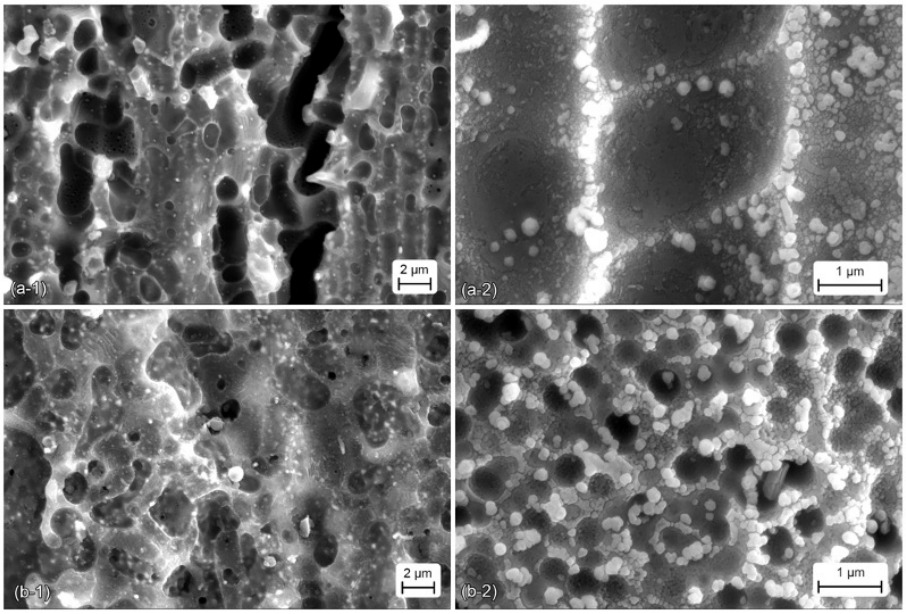

Figure 8.14: Top view SEM images of interfacial glass layer obtained by etching the bulk Ag for (a-1) acid textured and (b-1) MACE nano-textured samples. (a-2) and (b-2), are the top view SEM images of the samples after removal of the glass layer for acid textured and MACE nano-textured samples respectively.

results in nano-textures with significantly lower surface reflection of ~9% (without ARC) and ~1.5% (with ARC) and similar surface passivation properties as compared to the acid textured mc-Si samples. Nearly 100 mΩ-cm^2 lower batch average series resistance values were measured for MACE nano-textured mc-Si solar cells. Similar to alkaline textured c-Si solar cells, elevated portions of textures or the boundary of inverted scallop-like textures were found to be the favorable sites for denser Ag crystallite precipitation, which is responsible for the conduction in screen printed solar cells. It is found that the presence of denser textures lead to more number of Ag crystallite precipitation per unit area in MACE nano-textured surface than in iso-textured surface, which directly correlates to series resistance.

Chapter 9

Cell to Module Optical Loss Analysis of MACE Inverted Pyramid Textured Surfaces

9.1 Motivation

Recently, several groups demonstrated that inverted pyramid textures obtained by different b-Si surface modification processes can offer excellent surface passivation properties and importantly, very low WAR in the range of 16% without ARC [162, 165]. However, lower WAR values are reported for inverted nano-pyramids obtained from MACE b-Si features by RIE or NSR processes. Acid texturing (HF-HNO_3 etching followed by dilute KOH rinse) was also reported for the fabrication of inverted random pyramids previously and the WAR of such inverted pyramid textured samples were in the range of 19-20% [166, 200]. It suggested a scope for improving the anti-reflective properties of inverted nano-pyramids obtained by acid etching of MACE b-Si samples.

Integration of solar cells in to an encapsulated module results in additional electrical, optical and FF losses, jointly known as cell to module (CTM) loss [219, 220, 221, 222, 223]. Optical losses mainly correspond to absorption losses within the material used for encapsulation (e. g. glass, encapsulant and backsheet.) and reflection losses from the interface of different materials occurring due to the mismatch in their refractive indices values. Both morphology and light trapping capabilities of the surface textures influence the CTM factor, especially the optical losses [224, 225, 226]. Hence, it is impor-

tant to study and evaluate the performance of any new textures not only at cell level, but also at module level after encapsulation. Irrespective of the recent advancements reported in the literature, there were no significant efforts made towards modeling and studying the optical losses in MACE inverted pyramid textured mc-Si solar cells and modules.

In the first part of this chapter, we discuss a process flow for fabricating low reflective (WAR in the range of 16%) inverted pyramid textures using the combination of MACE and acid etching. Further, we demonstrate that inverted pyramid texture model of module ray-tracer software of PV Lighthouse can be used for accurately estimating the optical losses of MACE inverted pyramid textured mc-Si solar cells and modules. We find that adoption of MACE inverted pyramid texturing over acid texturing enhances the photo-generation in mc-Si modules by $\sim 0.5\%$ and that the total photo-generation current density in mc-Si solar modules approach 99.6% of that in random pyramid textured c-Si modules.

9.2 MACE inverted texturing process

9.2.1 Process details

The process details of MACE b-Si process and surface modification by acid etching are the same as we discussed in previous chapter. In addition, the acid etched b-Si (referred as nano-textures in the second part) mc-Si samples underwent an additional post-etching in 1% dilute KOH solution for 30 sec at room temperature to form inverted nano-pyramid textures. Three different groups of inverted pyramid textures are fabricated by etching three different groups of pit-like nano-textures in KOH solution and the morphological, optical and electronic properties of the two groups are compared. The complete process used for the fabrication and characterization of inverted pyramid textures are listed in Figure 9.1.

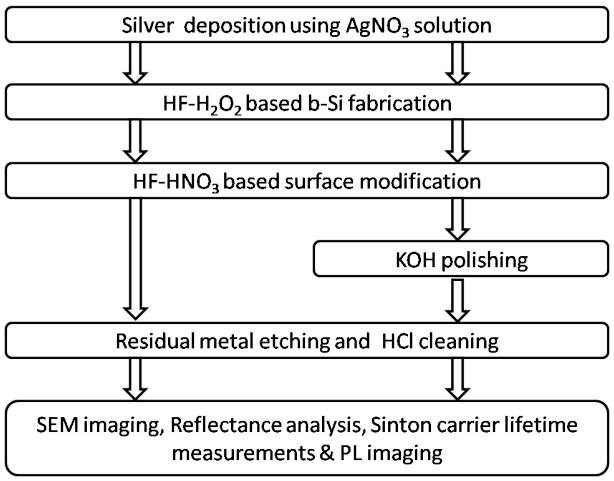

Figure 9.1: Process flow for fabrication and characterization of inverted pyramid textures on DWS mc-Si wafers.

9.3 Characterization of inverted pyramid textures

Figure 9.2 depicts SEM images of acid etched b-Si samples for 20 sec, 40 sec and 60 sec without and with KOH polishing step. Combination of HF - HNO_3 and KOH treatment results in more smoother, flatter and inverted pyramid like structures from that of inverted pits formed by only HF - HNO_3 etching. High resolution SEM images of acid etched samples in Figure 9.3 clearly illustrate the significance of KOH polishing for reducing the porosity of nano-textures obtained by acid etching of b-Si samples. However, quality of the textured surfaces should be evaluated with respect to reflection and surface recombination.

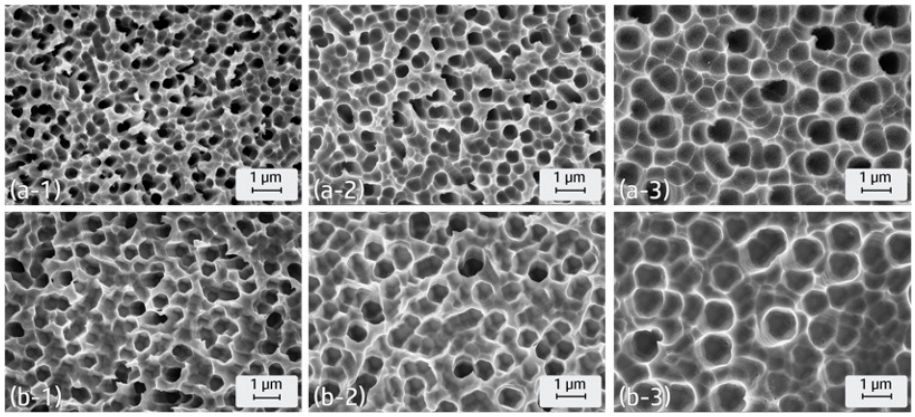

Figure 9.2: SEM images of acid etched b-Si surfaces for 20 sec, 40 sec and 60 sec; (a1-3) without and (b1-3) with KOH polishing.

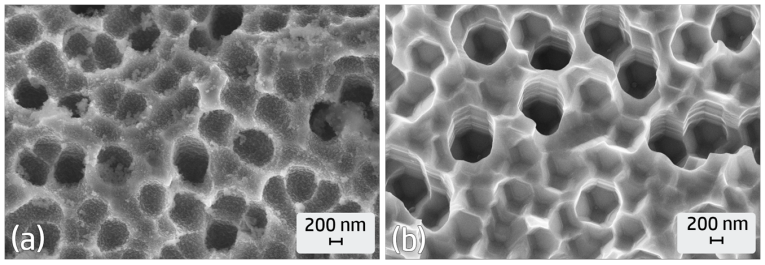

Figure 9.3: High resolution SEM images of acid etched b-Si surfaces; (a) without and (b) with KOH polishing.

The surface reflectance and WAR values of acid textured DWS, MACE b-Si, three group of inverted pit-like nano-textures (discussed in last chapter) and inverted nano-pyramid textures are shown in Figure 9.4. After KOH etching, the reflectance values have increased further for all three group of acid etched samples. This implies that the porous inverted scalloped pits obtained after HF - HNO_3 treatment traps light more efficiently compared to random inverted pyramids obtained by HF - HNO_3 treatment and KOH polishing. However, both inverted pit-like and inverted pyramid nano-texture groups have lower WAR values compared to acid textured sample. These reflectance curves illustrate the light trapping abilities of inverted nano-pyramids over the conventional acid textured wafers.

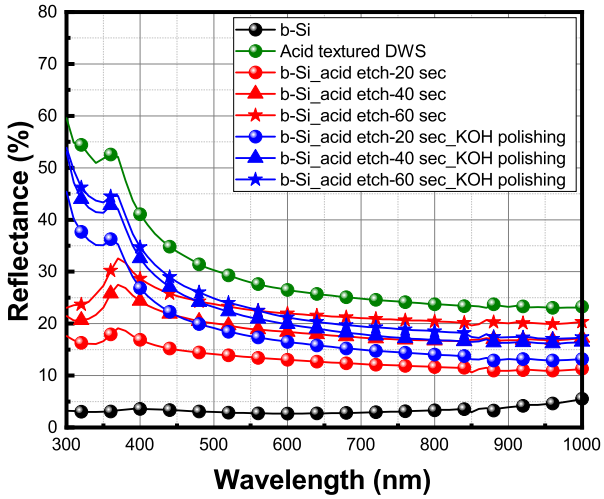

Figure 9.4: Comparison of surface reflectance values of acid textured, b-Si, three group of inverted pit-like nano-textured and three group of inverted nao-pyramid textured samples.

The enhanced PL counts in Figure 9.5 (d), Figure 9.5 (f) and Figure 9.5 (h) over Figure 9.5 (c), Figure 9.5 (e) and Figure 9.5 (g) affirm that KOH polishing after HF - HNO_3 step has major impact on suppressing the surface recombination. In other words, inverted nano-pyramid textured samples has significantly lower surface recombination than in pit-like nano-textured samples. The measured τ_{eff} at 1×10^{15} cm^{-3} minority carrier density of the chemically passivated samples are listed in Table 9.1 along with WAR values and average PL counts over the entire sample area. All the three groups of inverted pyramid textured samples showed excellent surface passivation properties similar to that of acid textured DWS (similar range of PL counts and τ_{Eff}) and outstanding light trapping properties with WAR lesser than that of acid textured DWS samples. In summary, the optimized inverted nano-pyramid textured samples (referred as b-Si_acid etch-20sec_KOH in Table 9.1) offers nearly 16-17% lower WAR values with similar surface passivation properties as that in case of acid textured DWS mc-Si samples. The light trapping abilities of these inverted pyramid textures are evaluated further at both cell level and module level (after encapsulation) using Sunsolve ray tracer simulator from PV lighthouse. The optical losses in MACE inverted nano-pyramid textured samples are benchmarked against both random pyramidal textured c-Si and iso textured mc-Si solar cells in the following sections.

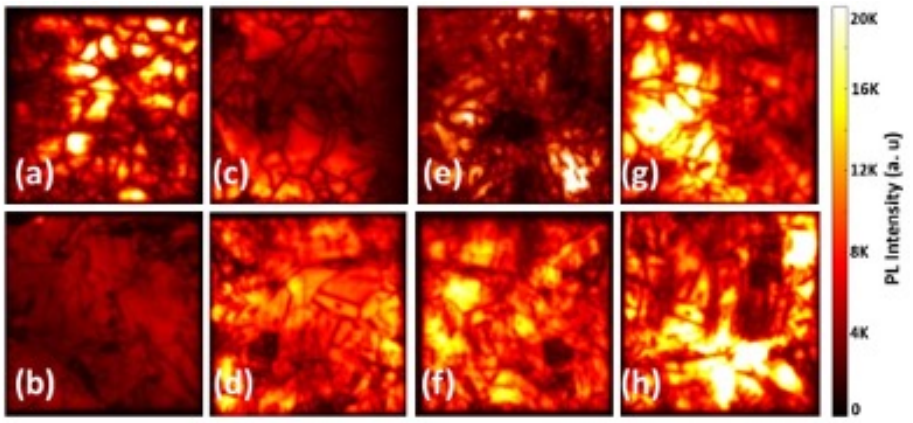

Figure 9.5: PL images of chemically passivated mc-Si wafers with (a) acid textured, (b) b-Si, and modified b-Si surfaces for 20 sec, 40 sec and 60 sec; (c, e, g) without and (d, f, h) with KOH polishing.

The surface morphology of random pyramid textured c-Si, iso-textured mc-Si, and

Table 9.1: Summary of WAR values, τ_{Eff} and average PL counts of b-Si and modified b-Si surfaces.

Sample Name (-)	WAR (%)	Effective carrier lifetime (μs)	Average PL count (-)
Acid textured DWS	28.6	68	6223
b-Si	3.5	28	3139
b-Si_acid etch-20sec	12.3	39	3700
b-Si_acid etch-40secec	18.3	51	3983
b-Si_acid etch-60sec	20.9	70	6502
b-Si_acid etch-20sec_KOH	16.8	72	6960
b-Si_acid etch-40sec_KOH	20.01	74	7233
b-Si_acid etch-60sec_KOH	21.16	78	8249

inverted nano-pyramid textured mc-Si samples analyzed by field emission scanning electron microscopy (FESEM) are depicted in Figure 9.6 (a-c). As seen in Figure 9.6 (c), the side-length and height (depth) of inverted pyramid textures were in the range of 400 - 600 nm and 200 - 300 nm, respectively. These range of values were used to estimate the approximate values of side-length to height (L/H) ratio and texture angle (ω), which were used as input parameters to the inverted pyramid texture model of module ray-tracer simulator. The average size of random pyramid textures and iso-textures (see Figure 9.6 (a) and (b)) were in the range of 2-6 μm. However, in simulations, the size of random pyramids and iso-textures were fixed to 4 μm.

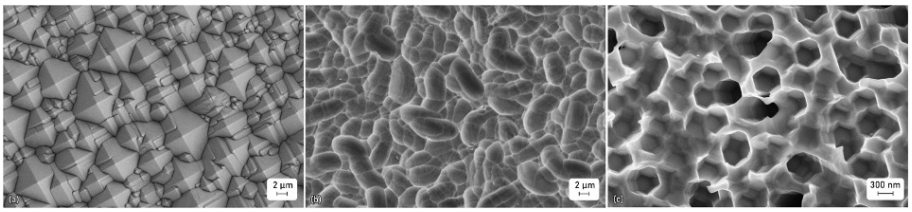

Figure 9.6: High resolution top-down SEM images of (a) random pyramid textured c-Si, (b) iso-textured mc-Si, and (c) inverted nano-pyramid textured mc-Si surfaces.

SiN_X:H ARC layer of thickness 75-80 nm and n of 2.1 (at 630 nm) was deposited using a plasma enhanced chemical vapor deposition (PECVD) system, Plasmalab-100, from Oxford Instruments. The wavelength dependent surface reflectance of textured

wafers without and with ARC were measured using an integrating sphere spectrophotometer from Perkin Elmer (Lambda-950). These reflectance curves were used for validating simulation results.

9.4 Simulation setup

Both inverted pyramid and inverted cone texture models of SunSolve module ray-tracer simulator generated closely matched surface reflectance values for the MACE inverted textures shown in Figure 9.6 (c). However, inverted pyramid texture model predicted reflectance of MACE inverted textures more accurately than inverted cone texture model. The inverted pyramid model and its underlying space are shown in Figure 9.7, where ω, L and H, respectively represent the texture angle, base width and height of inverted pyramid textured unit cell. Combination of ω and L/H ratio can be used for modeling shallow to high aspect ratio inverted pyramids for a wide range of dimensions. This implies that the impact of b-Si surface modification by acid etching (HF - HNO_3 etching followed by dilute KOH rinse) can be captured in the simulation by varying the L/H ratio and ω for quantifying the optical losses of the modified b-Si solar cells before and after conversion to module. From recent literature [162, 165], it has been observed that the surface passivation properties of inverted nano-pyramid textures with low L/H ratio (<2) were extremely poor. Hence, those structures were not considered in this investigation. In addition, our previous study confirmed that the inverted pyramid textures shown in Figure 9.6 are optimal for mc-Si solar cell fabrication as these textures posses excellent optical and passivation properties. The results were in good agreement with Zheng *et al.* and Jiang *et al.* [162, 165]. The range of ω and L/H ratio values extracted from the SEM images shown in Figure 9.6 were calibrated to measured reflectance values for closely examining the optical CTM losses. Nearly identical reflectance values were achieved in simulations for ω and L/H ratio of 44° and 2.07, respectively. For estimating the CTM losses in alkaline textured c-Si and acid textured mc-Si cells and modules, well established random pyramid and spherical cap models as described elsewhere were used [225, 227, 228].

The thickness, n and extinction coefficient (k) of PECVD SiN_X:H ARC measured by ellipsometry were given as inputs to the simulator for modeling the ARC characteristics.

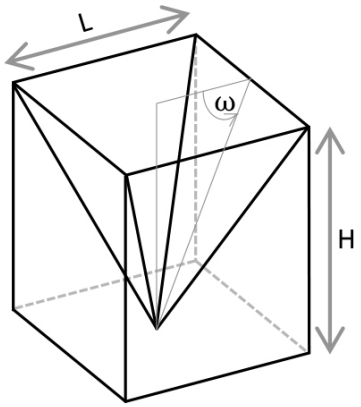

Figure 9.7: Schematic representation of the inverted pyramid texture unit cell model of module ray-tracer simulator.

Module encapsulating materials such as glass, EVA and backsheet collected from one of the module manufacturer, characterized for their optical properties, were utilized in the simulation for closely estimating the optical losses in industrial PV modules. The measured reflectance and transmittance curves of free standing glass, EVA and backsheet are given in Figure 9.8. Further, the wavelength dependent n and k values of glass and EVA samples were extracted from their reflectance and transmittance curves (depicted in Figure 9.8) following the method described in [229, 230]. The transmittance and reflectance curves of backsheet shown in Figure 9.8 were directly fed as input parameters to the simulator for modeling the backsheet layer. The measured thickness of glass, EVA, and backsheet were 2 mm, 0.45 mm, and 0.3 mm, respectively and the same values were given as inputs for ray-tracer simulations. The cell areas considered were 244.3 cm^2 (pseudo-square) and 245.7 cm^2 (full square), respectively for c-Si and mc-Si cells. Single cell module (with an additional spacing of 0.1 mm at each side of the cell) lay out was used for examining the module characteristics. 5,00,000 rays per simulation were used for generating the results presented in the following sections.

9.5 Reflectance study before encapsulation

The accuracy of SunSolve module ray-tracer texture models are tested by comparing the simulated and experimentally measured reflectance values as shown in Figure

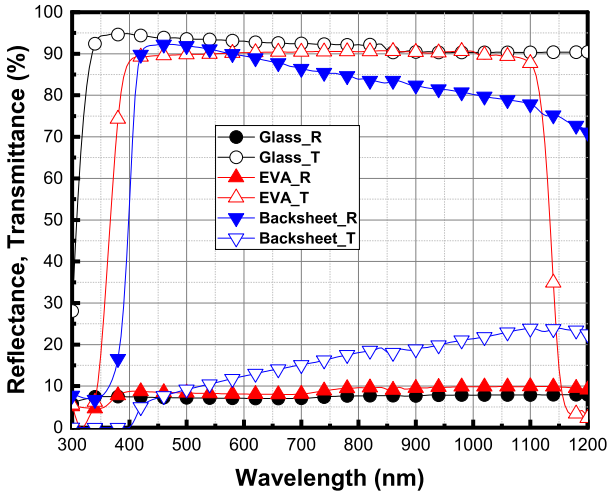

Figure 9.8: The measured reflectance and transmittance curves of glass, EVA and backsheet.

9.9 and Figure 9.10, respectively without (as-textured) and with SiN_X:H ARC. Nearly identical match of simulated curves (represented by hollow circles) to experimental measurements (represented by filled circles) were achieved for the different textures. As expected, random pyramid textured c-Si samples produced significantly lower surface reflectance than iso-textured mc-Si wafers. Nearly 1.5% difference in WAR was noticed between the measured and simulated reflectance values for pyramid textured samples. This can be attributed to the large variation in texture size and presence of larger pyramids (see Figure 9.6 (a)). Both simulation and experimental results confirm that inverted nano-pyramids shown in Figure 9.6 (c) invariably reduce the reflectance of mc-Si wafers with a nearly 7% lower WAR value than iso-textures. However, the reflectance values of inverted pyramid textured mc-Si wafers were still nearly 3-4% higher than alkaline textured c-Si wafers.

Figure 9.10 shows the plots of simulated and measured surface reflectance of samples after SiN_X:H ARC deposition. All three texture models provided excellent fit to measured reflectance after ARC for the same set of geometric parameters (ω, texture size, L/H ratio etc.) used for simulating the reflectance curves depicted in Figure 9.9. The results assure the credence of random pyramid, inverted pyramid, and spherical cap models. After ARC, the difference in WAR of pyramid textured c-Si and inverted pyramid textured mc-Si was narrowed to nearly 1.3%.

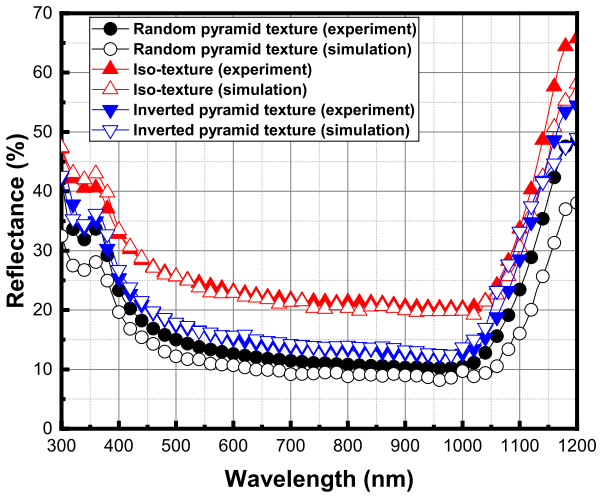

Figure 9.9: Comparison of measured and simulated wavelength dependent surface reflectance values of as-textured random pyramid textured c-Si, iso-textured mc-Si and inverted nano-pyramid textured mc-Si samples.

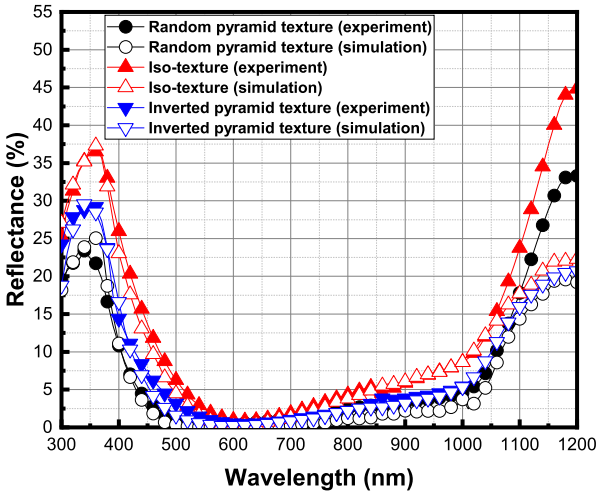

Figure 9.10: Comparison of measured and simulated wavelength dependent surface reflectance values of random pyramid textured c-Si, iso-textured mc-Si and inverted nano-pyramid textured mc-Si wafers after ARC.

9.6 Optical losses in cells

Optical losses (expressed in terms of generation current density) in not-encapsulated cells estimated from ray-tracer simulations are summarized in Table 9.2. The excellent light trapping properties of random pyramid textures have suppressed front external reflection loss to as low as 0.65 mA-cm^{-2}, which is 2.45 mA-cm^{-2} and 0.95 mA-cm^{-2} lower than in iso-textured and inverted pyramid textured mc-Si solar cells, respectively. The front surface escape loss in random pyramid textures were higher than iso-texture samples. The inverted pyramid textured cells showed moderate front surface escape loss, indicating that the surface reflection from inverted pyramid textures is more diffusive than in random pyramid textures and less diffusive than in iso-textures. The total absorption current losses (absorption in SiN_X:H ARC and rear Aluminum) were nearly similar for all three types of solar cells. Overall, random pyramid textures outperformed with an effective generation current density of 40.90 mA-cm^{-2}, which is 88.3% of the ideal maximum generation current density that can be obtained for silicon solar cells under AM 1.5G spectrum illumination. Simulation results suggest that, adoption of inverted nano-pyramid texture over iso-texture enhances the generation current density in mc-Si solar cells by 1.21 mA-cm^{-2} before encapsulation.

Table 9.2: Summary of optical losses (expressed in terms of generation current density, mA-cm^{-2}) in differently textured solar cells before encapsulation.

	Random pyramid	Iso-texture (spherical cap)	Inverted pyramid
Reflected front	0.65	3.13	1.62
Escaped front	0.75	0.42	0.64
ARC absorption	0.27	0.21	0.24
Rear absorption	3.73	3.75	3.79
Bulk Si absorption	40.90	38.80	40.01

9.7 Reflectance of encapsulated modules

The simulated total surface reflectance values of module test structures are shown in Figure 9.11. The impact of light coupling due to front metalization was not considered in the simulation. After encapsulation, the difference in surface reflectance values among the differently textured samples narrowed down further. The WAR values of random pyramid textured c-Si, iso-textured mc-Si and inverted pyramid textured mc-Si modules were 4.5%, 4.8% and 4.6%, respectively. The n value of glass and EVA are in the range of 1.5 at 630 nm. Hence, encapsulation of solar cell should result in graded n suitable for further enhancement in light trapping. However, for random pyramid textures, the total surface reflection increased substantially after encapsulation. Reduction in surface reflection due to the graded n values were mainly noticed in the blue wavelength range. For the middle wavelength region (550 nm to 900 nm), the reflectance values were nearly same for differently textured modules. As the glass used in this study was non-textured at front, potentially designed for reducing soil accumulation, reflection from the front side of the glass (shown in Figure 9.8) was significant. Unlike ARC deposited cells, the constant reflection from the glass acts as the limiting factor in lowering the surface reflectance in modules irrespective of the difference in front surface escape of light rays due to difference in texture morphology.

In summary, the relative advantage of pyramid textures over the others for light trapping was significantly reduced after encapsulation. The WAR of inverted nanopyramids was only 0.1% higher than random pyramid textures after encapsulation. The reflectance curves in Figure 9.11 confirms the importance of evaluating the light trapping properties not only at cell level (after ARC), but also after encapsulation. However, comparison of the absorption losses in various components used for module fabrication is essential for estimating the photo-generation in differently textured modules.

9.8 Optical losses in encapsulated modules

The simulated wavelength dependent optical losses in encapsulated inverted nanopyramid textured cells are shown in Figure 9.12. Similar to random pyramid textured

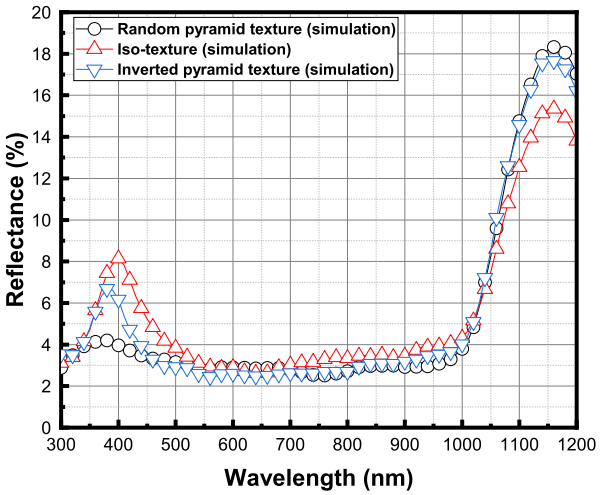

Figure 9.11: Simulated wavelength dependent total surface reflectance values of random pyramid textured c-Si, iso-textured mc-Si and inverted nano-pyramid textured mc-Si modules.

and iso-textured modules, absorption in glass, EVA, and aluminum rear contact of the cell, reflectance from front surface and front surface escape were the major components that contributed heavily to the optical losses in inverted pyramid textured solar modules. The optical loss (in terms of generation current density) of inverted nano-pyramid textured modules were compared with random pyramid textured and iso-textured modules in Table 9.3. CTM losses such as reflection from the front of encapsulated cell, absorption losses in glass, EVA and backsheet were not significantly different for the three differently textured cells. The pseudo-square shape can be reason for the marginally higher rear escape loss of random pyramid textured modules than the other two.

Similar to not-encapsulated solar cells, the difference in front surface escape is significant, suggesting that the texture morphology and light trapping properties impact the photo-generation in solar cells even after encapsulation. Similar front surface reflection for the three groups of solar cells after encapsulation indicate that the difference in total surface reflectance seen in Figure 9.11 was due to the variation in front surface escape losses associated with different surface textures. The magnitude of front reflection before encapsulation and front escape after encapsulation were changed significantly for all groups of solar cells. This indicates that lower external reflectance

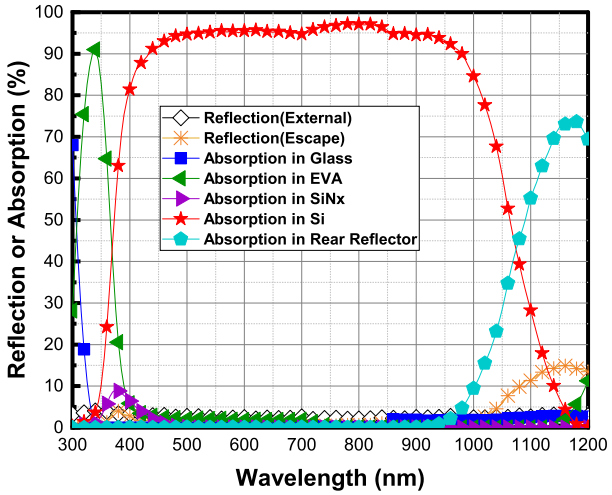

Figure 9.12: Simulated wavelength dependent optical (absorption and reflection) losses for the inverted nano-pyramid textured mc-Si Al-BSF solar cell after module encapsulation.

is not the only factor which decides the reflection losses after encapsulation, the light trapping properties and diffusive nature of light rays associated with texture geometry also play a vital role. It was previously reported that, the reflections from iso-textures are more diffusive compared to that from upright pyramid textures [227, 231]. As a consequence, the total internal reflection of diffused rays occurring at the glass-air interface contribute to reduction in the escape of reflected rays for iso-textures. However, for random pyramid textures, the majority of the reflected light falls within the escape angle of glass-air interface and hence are not reflected back internally. Interestingly, the front escape current density value of inverted pyramid textured modules was 0.09 mA-cm^{-2} lower than iso-textured modules, and only 0.04 mA-cm^{-2} higher than random pyramid textured modules. This suggests better light trapping than in iso-textures and enhanced total internal reflection at the glass-air interface compared to pyramid textures have resulted in moderate front escape loss in inverted nano-pyramid textured modules.

Nearly 1% higher generation current (referred as solar cell bulk absorption in Table 9.3) was obtained for random pyramid textured cells over iso-textured cells, which is in good agreement with a previous study [225]. Our results establish that the photo-generation in mc-Si module can be enhanced from 38.47 mA-cm^{-2} to 38.69 mA-

Table 9.3: Summary of optical losses (expressed in terms of generation current density, mA-cm^{-2}) in differently textured solar cells after module encapsulation.

	Random pyramid	Iso-texture (spherical cap)	Inverted pyramid
Reflected front	1.17	1.15	1.14
Escaped front	0.93	1.06	0.97
Escaped rear	0.05	0.02	0.02
ARC absorption	0.18	0.16	0.17
Rear cell absorption	3.64	3.86	3.75
Glass absorption	0.40	0.44	0.39
EVA absorption	1.06	1.15	1.17
Backsheet absorption	0.00	0.00	0.00
Bulk Si absorption	38.84	38.47	38.69

cm^{-2} (~0.5%), by choosing MACE inverted nano-pyramid texturing over conventional acid texturing. More importantly, with MACE inverted nano-pyramid texturing the photo-generation current in mc-Si solar modules will approach 99.6% of that in random pyramid textured c-Si modules, which would narrow down the performance gap of mc-Si and c-Si modules significantly.

The bar diagram of CTM generation current density loss for differently textured Al-BSF solar cells is depicted in Figure 9.13. Iso-textured solar cell exhibited the lowest CTM generation loss of 0.32 mA-cm^{-2} and random pyramid textured solar cell showed the largest CTM loss of 2.08 mA-cm^{-2}. CTM generation current density loss of MACE inverted pyramid textured cell was 1.37 mA-cm^{-2}, which is significant compared to iso-textured cells. Hence, our results establish that the performance enhancement achieved by adopting advanced texturing schemes at cell level are not completely translated to module performance due to CTM losses, especially for low-reflective textures. However, even after the higher CTM loss, the generation current density is considerably higher for MACE inverted pyramid textured modules than of iso-textured modules. Hence, MACE inverted nano-pyramid texturing scheme has the potential for replacing the conventional acid texturing as it assures better performance

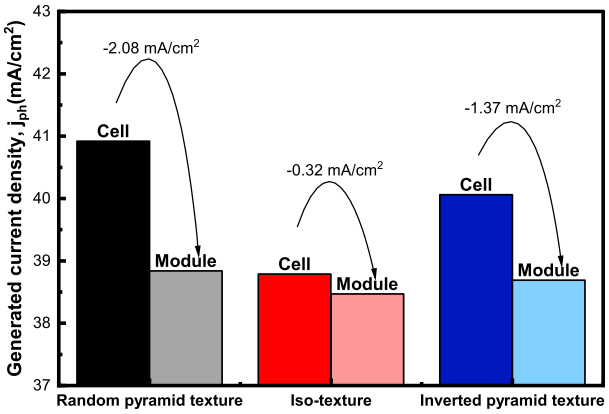

Figure 9.13: Bar chart describing the optical CTM loss in random pyramid textured, iso-textured and inverted nano-pyramid textured modules.

at module level along with additional process advantages like cost-effectiveness and higher production throughput.

9.9 Conclusion

Process flow for the fabrication of low reflective (WAR of 16%) inverted pyramid textures using the combination of MACE and acid texturing was discussed. The process optimizations were conducted by comparing the opto-electronic properties of inverted pyramid textures with iso-textures and inverted-pit like nano-textures. Inverted pyramid texture model of SunSolve module ray-tracer software of PV Lighthouse was utilized for estimating the optical losses associated with MACE inverted pyramid textures. In our simulations, inverted pyramid textures showed moderate CTM generation loss, which was nearly 0.7 mA-cm^{-2} lower than the random pyramid textured and 1.05 mA-cm^{-2} higher than the iso-textured solar cells. Most importantly, the simulations establish that adoption of inverted nano-pyramid texturing over acid texturing would enhance the generation current in mc-Si modules by ~0.5% and in such a case, the total photo-generation current in mc-Si modules approaches 99.6% of that in modules with random pyramid textured cells.

Chapter 10

Advanced Texturization Schemes by Unconventional Processes

10.1 Motivation

So far, we have discussed industry viable processes developed for texturing large wafers. These processes need not be the best methods in terms of light harvesting efficiency. Alkaline and acid texturing methods continued to dominate c-Si and mc-Si industry because of their high production throughput and cost-effectiveness. There were several attempts to develop alternate texturing schemes that produce surface textures which exhibit better light trapping properties than random pyramid textures and iso-textures. Array of ordered nano-wires and regular inverted pyramid textures (on c-Si wafers) are some of them. However, fabrication of these structures utilize complex and expensive photo-lithography steps, which limits their application for industrial production.

In this chapter, we present experimental results on some of the lithography-free process steps that are developed for the fabrication of advanced textures like nano-wires and regular inverted pyramids. They are unconventional unit processes for PV applications and are not currently transferable to industrial environment. Use of CL instead of photo-lithography, RIE for directional etching and MACE for anisotropic etching are some of the methods explored for the fabrication of vertical nano-wires and inverted pyramid textures on polished c-Si wafers. We shall discuss these processes and their application for the fabrication of advanced textures in this chapter.

10.2 Colloidal lithography (CL)

CL process consists of two major steps; transfer of colloidal beads on to silicon wafers and size reduction of beads to expose silicon surface for directional etching. We have tried using both silica and polystyrene (PS) beads as mask. Spin coating method was used to transfer the beads. Colloidal solution preparation and size reduction process for PS and silica beads are different. It is observed that PS beads form uniform and closely packed mono-layers of colloidal masks than silica beads in all our experiments. Hence, CL process steps are explained with respect to PS beads. For all the CL related experiments, chemically mechanically polished (CMP) 2 inch diameter <100> c-Si wafers were used.

10.2.1 Transfer of colloidal beads

Spin coating process was preferred over other methods such as dip-coating, evaporation and Langmuir-Blodgett coating as it provides better uniformity, coverage and mono-layer packing of colloidal particles for large area device applications [107, 232]. Prior to spin coating, the silicon wafers were soaked in APTES ((3-Aminopropyl)triethoxysilane) solution for 60 min at room temperature for improving the adhesion property of Si surfaces to colloidal particles. Zeta 3D images of PS bead coated samples with and without surface functionalization are shown in Figure 10.1. The influence and need of surface functionalization is clearly visible, with APTES functionalized samples showing > 95% coverage of mono-layer compared to non-functionalized samples.

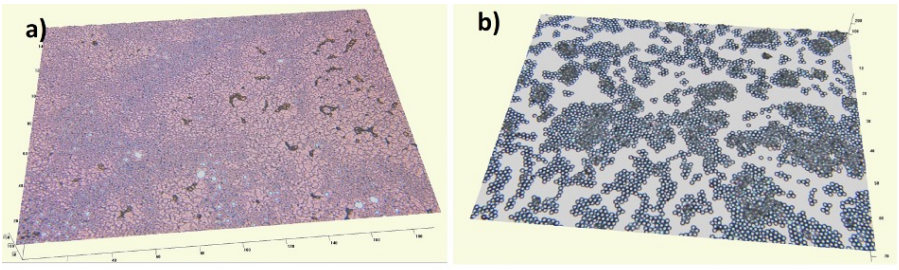

Figure 10.1: Zeta 3D images of PS beads spin coated samples (a) with and (b) without prior surface functionalization.

PS colloidal solution was prepared by mixing the PS beads solution with a surfactant solution in the ratio of 4:1 (by volume). Surfactant solution was prepared by

adding a drop of Triton X-100 to methanol (1:400 ratio by volume). PS beads were then transferred on to Si surface by a three step spin coating process, which is summarized in Table 10.1. The spin coating process parameters are optimized for obtaining hexagonally close packed mono-layers of PS beads as shown in Zeta 3D images in Figure 10.1 (a) and SEM images in Figure 10.2 (a) and (b).

Table 10.1: The parameters used for spin coating of mono-layers of PS beads.

Step1			Step2			Step3		
Time	Speed	Acc.	Time	Speed	Acc.	Time	Speed	Acc.
10	400	208	120	800	416	10	1400	624

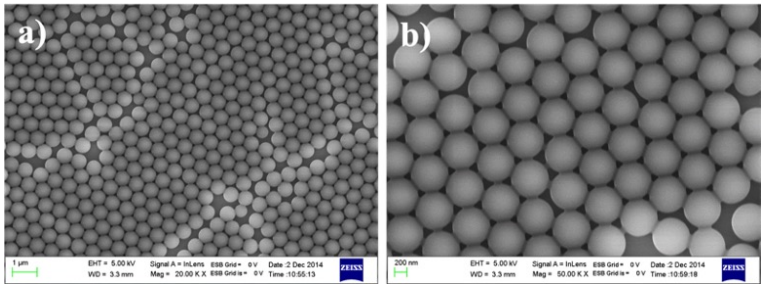

Figure 10.2: SEM images of hexagonally packed mono-layers of PS beads.

Further, the diameter of the beads are trimmed to expose silicon surface for etching. O_2 plasma of RIE system was used for trimming the diameter of PS beads. 25 sccm of O_2 plasma at a chamber pressure of 25 mTorr and RF power of 80 W were used for tailoring the bead size. Figure 10.3 represents a series of SEM images of PS beads after O_2 plasma treatment for different process times varying from 1 min to 6 min. Etching of PS beads in O_2 plasma follows anisotropic behavior with higher etch rates in the vertical direction than of that in the lateral direction, eventually loosing the spherical shape of PS beads especially for higher etching times. The etch profile of PS beads followed a nearly linear profile with an approximate etch rate of 100 nm/min.

10.3 Fabrication of silicon nano-wires

Selective etching of Si substrate by both dry etching and wet etching methods were applied for the fabrication of highly ordered vertical nano-wires using PS bead as a

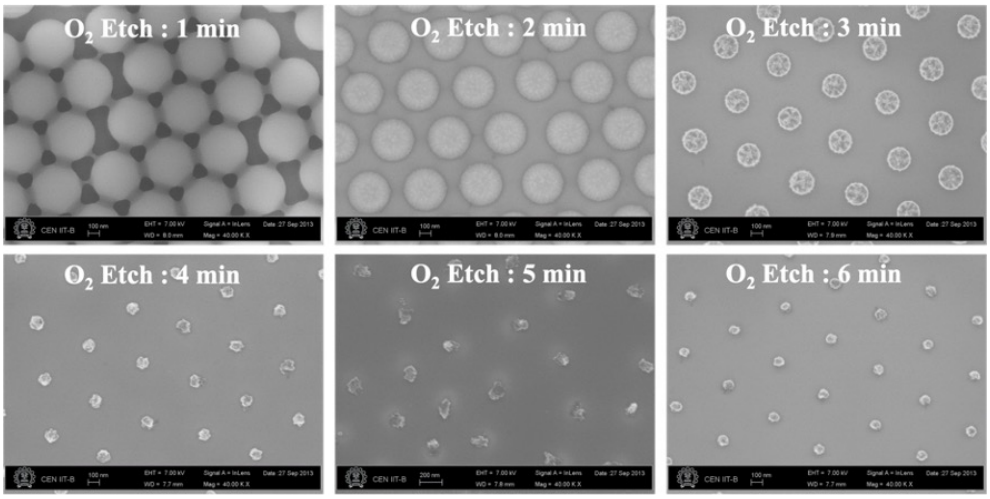

Figure 10.3: SEM images of trimmed PS beads after the O_2 plasma etching for 1-6 min.

mask. In dry etching, both single step RIE and Bosch time multiplexed deep RIE (DRIE) methods were tried. Combination of CL and MACE also produced highly ordered nano-wires. In this section, we will discuss about the etching routes used for the fabrication of silicon nano-wires.

10.3.1 Inductive coupled plasma (ICP) reactive ion etching

The single step (PlasmaLab 100 ICP 180 from Oxford instruments) etch system use fluorine plasma generated from SF_6, CF_4 and C_4F_8 gases for etching silicon substrates. Both SF_6 and CF_4 etching results in isotropic etch profiles. Hence, combination of C_4F_8 and SF_6 was used for generating vertical nano-wires shown in Figure 10.4. The gas flow ratio of C_4F_8 and SF_6 were fixed to 100 sccm and 60 sccm, respectively and the etching process was carried out for a chamber pressure of 13 mTorr and ICP power of 1200 W. Anisotropic etching has resulted in array of nano-wires with a maximum height of 1 μm. High aspect ratio nano-wires were not produced for higher etching times as top portion of the nano-wires started getting etched because of the poor etch selectivity to PS beads resulting in porous nano-wires as shown in Figure 10.4 (a) and (b).

10.3.2 Deep reactive ion etching (DRIE)

Since the single step RIE process showed poor selectivity for the fabrication of high aspect ratio nanopillars, Bosch time-multiplexed DRIE process was applied in a com-

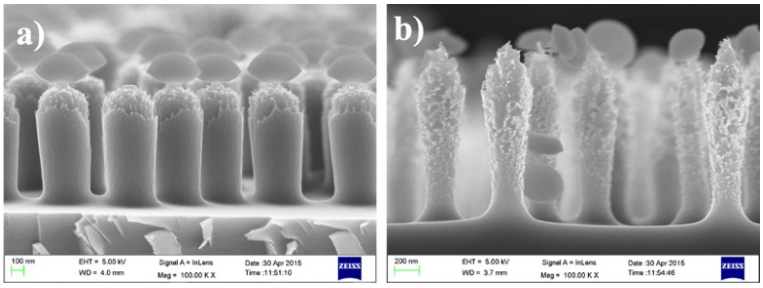

Figure 10.4: SEM images of Si nano-wires obtained by ICP RIE for (a) 90 sec and (b) 120 sec.

mercial inductive coupled plasma etcher of SPTS LPX Pegasus system. Alternated cycles of SF_6 (80 sccm) and of C_4F_8 (200 sccm), respectively were applied for etching the unprotected areas and for depositing the fluorinated polymer to protect the side walls of the resultant etched structures. Figure 10.5 represents the SEM images of high aspect ratio silicon nano-wires obtained for different DRIE process durations. DRIE process showed better selectivity, anisotropy and high etch rate compared to the single step RIE process for silicon etching. The etch rate was approximately 3 μm/min. Uprooting of the pillars were observed only for longer etching durations or when the nano-wire height was more than 4 μm. However, DRIE process introduced side undulations to the side of silicon nano-wires.

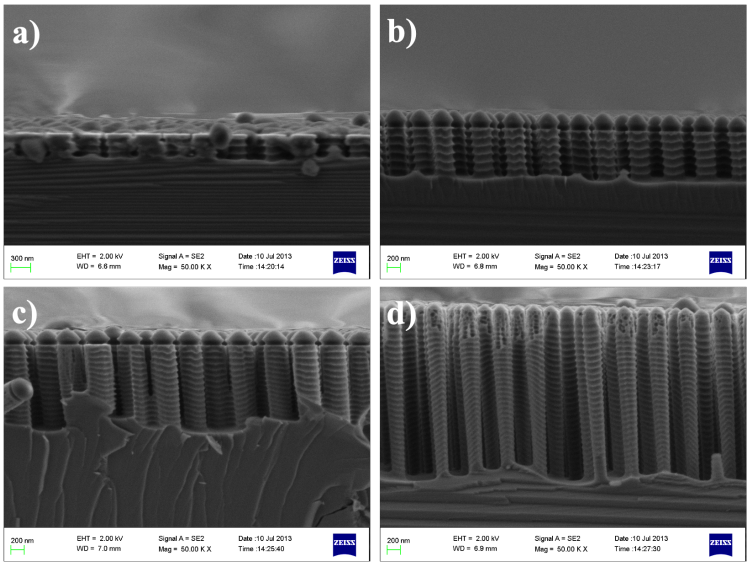

Figure 10.5: SEM images of Si nano-wires obtained by deep RIE for (a) 30 sec, (b) 60 sec, (c) 90 sec, and (d) 120 sec.

10.3.3 Sidewall smoothing of DRIE nanowires

The nano-wires fabricated by DRIE process have a minimum sidewall undulation of 25-30 nm, which needs to be reduced further for ensuring conformal deposition for dielectric for passivation. Thermal oxidation followed by a HF dip was tried for reducing the surface undulations and roughness of DRIE nano-wires. Figure 10.6 (a), (b) and (c), respectively represents the SEM images of DRIE nano-wires before, after first round and after second round of thermal oxidation and HF dip. The sidewall undulation for the nano-wires shown in Figure 10.6 are estimated using Image-J software and is summarized in Table 10.2. It is observed that the waviness was reduced to 14 nm after couple of cycles of oxidation and HF etching. However, reduction in nano-wire diameter/ volume and application of high temperature processes like thermal oxidation, which adds to higher thermal budget were the obvious disadvantage of this approach.

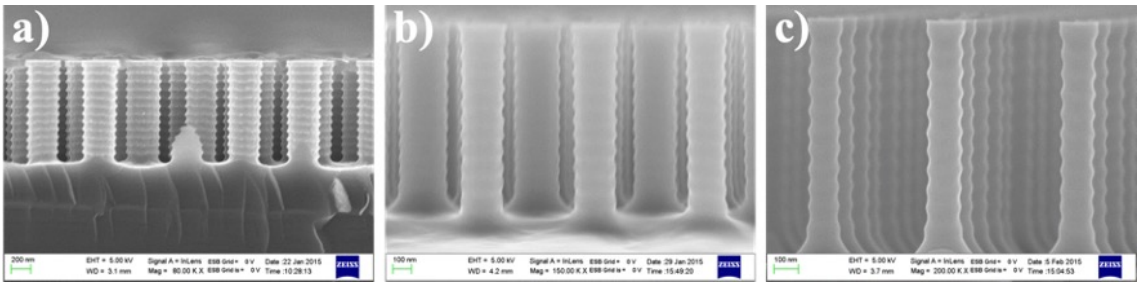

Figure 10.6: SEM images of DRIE nano-wires (a) before and after (b) first and (c) second cycle of oxidation and HF strip.

Table 10.2: Characteristics table of nano-wires before and after oxidation and HF strip.

Process	Undulations (nm)	Diameter of NW (nm)
Before Oxidation and HF strip	26	450
After 1^{st} cycle of Oxidation and HF strip	20.12	320
After 2^{nd} cycle of Oxidation and HF strip	14.76	210

10.3.4 Metal Assisted Chemical Etch

Figure 10.7 represents the schematics of the nano-wire fabrication using a combination of CL and MACE. A thin layer (30 nm) of Au film deposition by sputtering followed by lifting-off of PS beads in toluene solution by sonication were used to produce the patterns. MACE is carried out in HF:H_2O_2:DI water (in the ratio of 1:3:9 by volume) at room temperature for different time periods such as 30, and 90 sec to measure the etch rate and to check the smoothness of sidewall profiles. Height of nano-wires was measured from the SEM images shown in Figure 10.8 (a) and (b) and linear fit was used to find the etch rate, which was in the range of 400 nm/min. Although the etch rate is less compared to RIE processes, the side wall profiles are smoother and adequate for conformal film deposition compared to the nano-wires obtained by RIE processes.

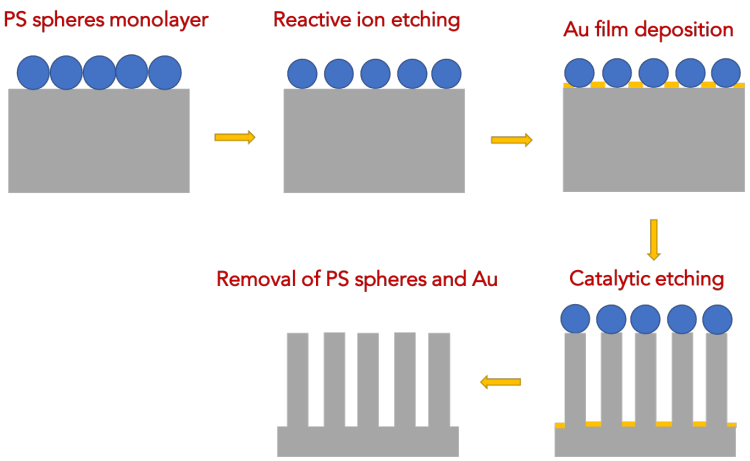

Figure 10.7: Process flow used for fabrication of nano-wires using the combination of CL and MACE.

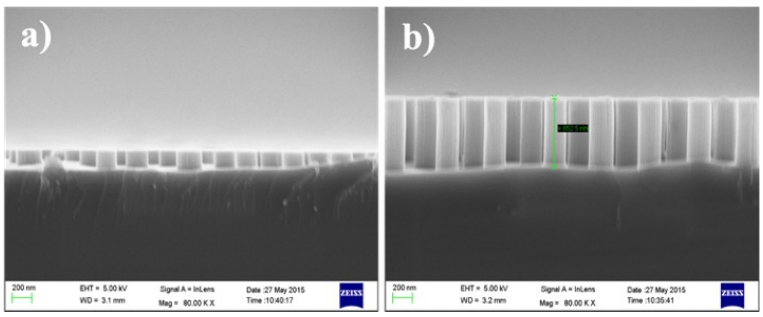

Figure 10.8: Cross sectional SEM images of nano-wires fabricated using a combination of CL and MACE for (a) 30 sec and (b) 90 sec.

10.4 Inverted pyramid texturing

10.4.1 CL and TMAH etching

In the previous sections, we have discussed different combinations of CL and etching processes for the fabrication of vertically aligned nano-wires. The same approach by replacing the MACE process with anisotropic KOH or TMAH etching is used for the fabrication of ordered inverted pyramid textures. The process schematic is shown in Figure 10.9. Instead of Au layer, ICP-CVD silicon nitride was used as a mask for TMAH etching. The SEM images of the inverted pyramids obtained after TMAH etching for 1 min and 3 min, respectively are shown in Figure 10.10 (a) and (b). This method allows to fabricate hexagonally packed regular inverted pyramid textures uniformly across the wafer surface without the use of photo-lithography.

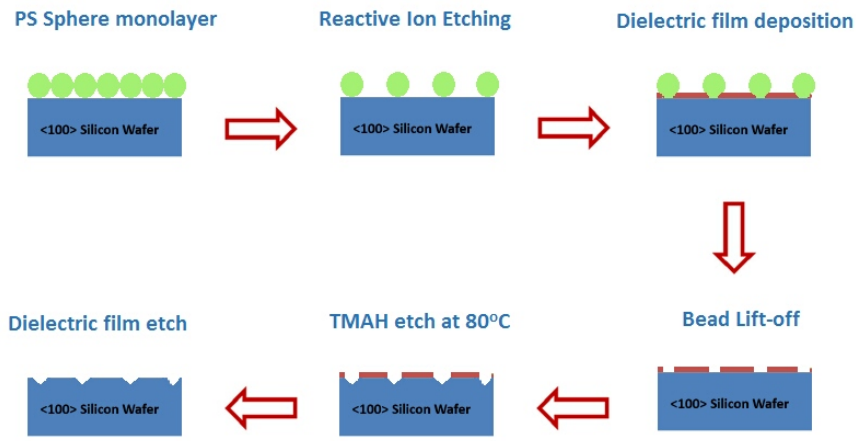

Figure 10.9: Process flow for used for inverted pyramid fabrication using a combination of CL and TMAH etching.

10.4.2 One-step Copper assisted chemical etch

As discussed previously in chapter 3, the lateral etching characteristics of Si in Cu based MACE process and the difference in electron supply of Cu^{2+} at higher temperatures can produce random inverted pyramid textures [233]. Hence, we have also optimized the one step Cu based MACE process for inverted pyramid generation and the optimized

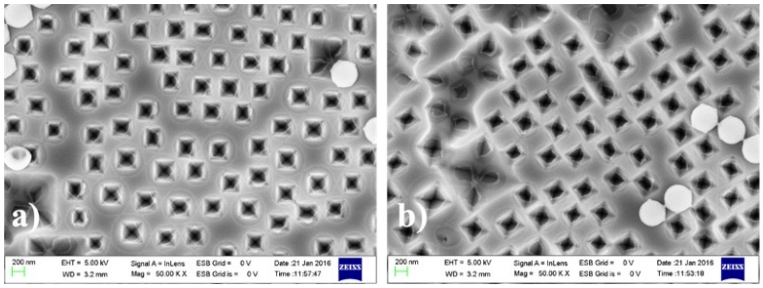

Figure 10.10: Top-down SEM images of regular inverted pyramids obtained after TMAH etching for (a) 1 min and (2) min.

process conditions are as follows; 3 mM $Cu(NO)_3$, 4.6 M HF and 0.5 mM H_2O_2 at 80°C. SEM images of inverted pyramid textures formed after one step Cu based MACE process for 3 min and 5 min are shown in Figure 10.11 (a) and (b), respectively. The size and distribution of these textures were highly non-uniform and random as shown in Figure 10.11 compared to uniformly distributed inverted pyramids shown in Figure 10.10. However, the WAR values of inverted textures were in the range of 6-7%, respectively, which is significantly lower than upright random pyramid textures. In addition, significantly lower amount of silicon is removed during the one step etching process than in alkaline texturing process. These results indicate the potential of advanced texturing schemes. However further investigations targeting towards the passivation and contact formation are essential for confirming the same.

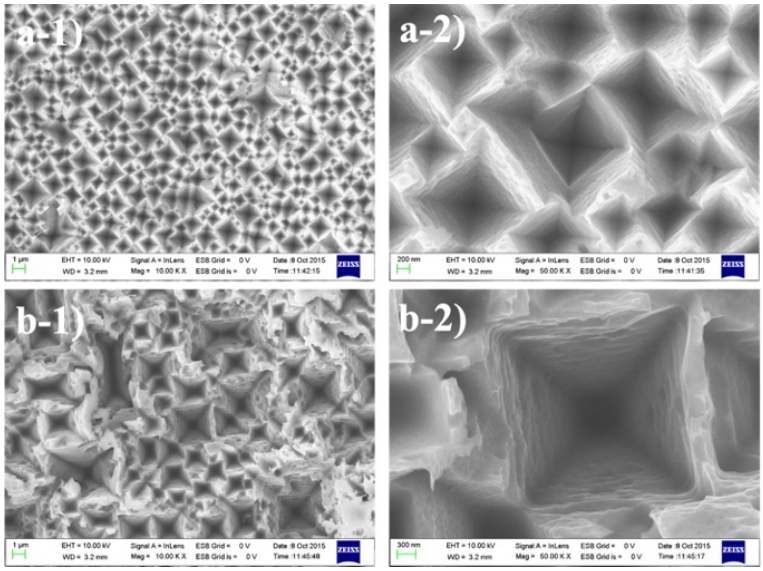

Figure 10.11: The SEM images of inverted pyramid textures obtained by one-step Cu assisted MACE etching for (a-1) and (a-2) 3 min and (b-1) and (b-2) 5 min.

10.5 Conclusions

In this chapter, preliminary experiments on various top-down approaches for fabricating nano-wires were presented. CL followed by an etching method was proposed to avoid the complex and expensive photo-lithography steps for the fabrication of nano-wires. Combination of CL and DRIE produced highly ordered hexagonally packed different aspect ratio nano-wire arrays. However, 25-30 nm of sidewall scallops/ undulations were observed for DRIE nano-wires. Use of MACE process instead of DRIE produced hexagonally packed nano-wires without any sidewall undulations.

In the subsequent section, fabrication of inverted pyramid textures on (100) c-Si wafers using a combination of CL and TMAH etching was discussed. Highly ordered and hexagonally packed inverted nano-pyramid textures were achieved by this method. In the final part of the chapter, we demonstrated the use of single step Cu based MACE etching process for random inverted pyramidal texture generation. The one step MACE process is a potential candidate for conventional alkaline texturing process favoring the cost advantage, lower material loss and better light trapping.

Chapter 11

Conclusions and Future Directions

This thesis describes various industrial chemical processes developed for addressing the texturing difficulties of DWS wafers. In chapter 5, a novel cost-effective SDR process, followed by silicate based alkaline etching process was demonstrated for the fabrication of random pyramid textures of height and size in the range of 2-4 μm, uniformly across the DWS c-Si wafer surface. The novel SDR process completely removes the unwanted saw damages, residues and other contaminants introduced during wire sawing process. The morphological, optical and electronic properties of novel alkaline textured wafers and performance parameters of solar cells were compared and benchmarked against conventional alkaline textured MWSS and existing alkaline textured (TMAH based SDR process followed by alkaline etching) DWS c-Si wafers and solar cells. Comparable performance parameters for the three group of alkaline textured solar cells substantiated the potential of our texturing process for industrial applications favoring cost advantages due to significantly reduced cost of NaOCl solution (US \$3/litre) compared to TMAH solution (US \$250/litre).

The wet texturing difficulty was more severe for DWS mc-Si wafers as single step acid texturing process was used for SDR and texturing of mc-Si wafers in industry. PV manufacturing units were using expensive additive-based acid texturing process for processing DWS mc-Si wafers in their production lines. In this regard, an additive-free, energy-efficient acid texturing process was developed using laboratory set-up. The developed process use a different combination of PV grade chemicals (HF-rich HF - HNO_3), hence can be immediately transfered to any industrial acid texturing tool. An insight to the underlying mechanism of HF-rich acid texturing process was

discussed in chapter 6. Similar performance of the NCPRE additive-free acid textured solar cells compared to conventional acid textured MWSS solar cells fabricated using laboratory tools (discussed in chapter 7) and additive-based acid textured mc-Si solar cells fabricated in industry environment in three leading PV manufacturing units in the country (discussed in chapter 7) demonstrated the performance potential of the proposed texturing process. Further, a detailed cost analysis of chemicals used for bath preparation was conducted. The analysis suggested that adoption of additive-free texturing process over additive-based texturing process can reduce the chemical cost by 60%. Also, detailed analysis showed that the performance of additive-free textured solar cells can be improved further by adjusting the unit step processes conditions according to the new textures.

MACE nano-texturing process emerged as the next generation texturing process for mc-Si wafers and is equally applicable for c-Si solar cells as well, which make it as a universal texturing process silicon solar cells. In this context, fabrication of inverted pit-like nano-texture using a combination of MACE and acid etching processes are demonstrated in chapter 8. Optimized MACE nano-textures yield nearly 12% lower WAR values with similar passivation properties as compared to acid textured samples. Later, the potential of nano-textures over iso-textures was demonstrated by comparing the performance parameters and two diode model parameters of the solar cells by advanced characterization and mapping techniques. It is noticed that nano-textures not only suppress the surface reflection, but also offers significantly lower contact resistance, which contribute to remarkable improvement in FF values. An investigation on the cause of reduced contact resistance is detailed by analyzing the contact formation of Ag contacts to P diffused emitter in chapter 8.

Further, a low cost approach for the fabrication of inverted pyramid textures from MACE inverted pit nano-textures (discussed in chapter 8) is demonstrated and a detailed investigation of morphological, optical and electrical properties were conducted in chapter 9. Later, a comprehensive analysis of optical losses in inverted pyramid textured mc-Si solar cells and modules are estimated from SunSolve ray-tracer simulations. Moderate CTM generation current loss was noticed for inverted pyramid textured solar cells, which was nearly 0.7 mA-cm^{-2} lower than the random pyramid textured and 1.05 mA-cm^{-2} higher than the iso-textured solar cells. Importantly, our study established

that the adoption of MACE inverted pyramid textures over iso-textures enhance the total generation current density in mc-Si modules by ~0.5% and approach to 99.6% of that in random pyramid textured c-Si modules.

Even though several concrete concluding remarks are made at the end of each chapters, we believe that further work in the following directions would make this work better.

- Implementation of the low-cost SDR process (developed for DWS c-Si wafers) in industrial production lines for analyzing process bath stability for batch processing. This would helps us to estimate the cost advantages of proposed process accurately.

- Industrial implementation details and chemical cost analysis of additive-free acid texturing process are already presented. However, a detailed comparison of performance after module encapsulation is crucial, especially the sensitivity analysis of performance parameters before and after encapsulation. The reliability study (including the wafer breakage rate) for a batch of minimum 6 lakh wafers is essential for ensuring industrial viability.

- The potential of MACE b-Si process is not fully utilized yet because of the limited passivation properties of SiN_x:H ARC layer. Recent studies suggests that application of ALD Al_2O_3 film would passivate the b-Si surface better. Hence, a detailed investigation towards passivating the b-Si surface by advanced techniques would result in complete utilization of anti-reflective properties of b-Si features.

- One of the identified advantage of MACE nano-texture is the ability to offer lower contact resistance than iso-textures. Even though, an investigation was directed towards investigating the cause for lower series/ contact resistance, a direct measure of exact value of contact resistance in differently textured solar cells are not conducted yet due to lack of resources at our side. Hence, contact resistance measurement by TLM technique or some other established methods would provide an absolute value of contact resistance, which may be more insightful for understanding the current conduction. In addition, the impact of lower contact resistance/ R_S after encapsulation needs to be examined critically as wires and

interconnects used for module encapsulation also contribute to additional R_S in PV modules.

- Lower contact resistance in nano-textured solar cells suggested that adoption of MACE nano-texturing over alkaline pyramidal texturing could lower the contact resistance in c-Si further. However, a detailed investigation is needed in this direction as the geometry of textures also impacts the Ag crystallite precipitation. Comparative study of contact formation mechanism in upright pyramid textures, nano-pit-like textures, inverted nano-pyramid textures and iso-textures is essential for completely understanding the impact of size and morphology of textures on contact formation.

- CTM generation loss analysis is estimated from ray tracing simulations. An attempt to validate the simulation results by fabricating mini modules would provide a complete insight to the problem addressed in chapter 9.

- In chapter 10, some of the advanced texturization schemes like nano-wire texturing, inverted pyramid texturing are discussed. However, the results are presented in the lines of SEM images and in some case in terms of reflectance measurements. The other aspects such as surface passivation and contact formation mechanism in such textures needs to be investigated further.

Publications and Patents

Journal Papers

- **K. P. Sreejith**, Ashok K. Sharma, Prabir K. Basu, Anil Kottantharayil, "A Comprehensive Study Detailing the Potential of Metal Assisted Chemical Etched (MACE) Nano-textures over Conventional Micron-sized Iso-textures for Industrial Multicrystalline Silicon Solar Cell Applications" accepted for publication in *Solar Energy*.

- **K. P. Sreejith**, Ashok K. Sharma, Siddharth Behera, Anil Kottantharayil, Prabir K. Basu, "A low cost additive-free acid texturing process for large area commercial diamond-wire-sawn multicrystalline silicon solar cells", *Solar Energy*, 205, pp.263-274, 2020. **DOI: 10.1016/j.solener.2020.05.018**

- **K. P. Sreejith**, Ashok K. Sharma, Sandeep Kumbhar, Anil Kottantharayil, Prabir K. Basu, An additive-free non-metallic energy efficient industrial texturization process for diamond wire sawn multicrystalline silicon wafers, *Solar Energy*, 169, pp.162-172, 2019. **DOI: 10.1016/j.solener.2019.03.062**

- Ashok K. Sharma,Suchismita Mitra, **K. P. Sreejith**, Durga Prasad Khatri, Almouzzam Khan, Anil Kottantharayil, Hemanta Ghosh A comprehensive analysis of recombination and resistive losses in silicon solar cells induced by co-firing process, *Surfaces and Interfaces*, pp.101260, 2021. **DOI: 10.1016/j.surfin.2021.101260**

- Prabir K. Basu, Sandeep Kumbhar, **K. P. Sreejith**, Tarun S. Yadav, Anil Kottantharayil, B. M. Arora, K. L. Narasimhan, Ashok K. Sharma, Active area cell efficiency (19%) monocrystalline silicon solar cell fabrication using low-cost processing with small footprint laboratory tools, *Bulletin of Materials Science*, 42:33,

2019. **DOI: 10.1007/s12034-018-1711-2**

- Prabir K. Basu, **K. P. Sreejith**, Tarun S. Yadav, Anil Kottantharayil, Ashok K. Sharma, Novel low-cost alkaline texturing process for diamond-wire-sawn industrial monocrystalline silicon wafers, *Solar Energy Materials and Solar Cells*, 185, pp.406-414, 2018. **DOI: 10.1016/j.solmat.2018.05.047**

Under Review

- **K. P. Sreejith**, Ashok K. Sharma, Prabir K. Basu, Anil Kottantharayil, "A Etching Methods for Texturing Industrial Multi-crystalline Silicon Wafers: A Comprehensive Review" under review in *Solar Energy Materials and Solar Cells*.

- **K. P. Sreejith**, Tanushree J. B. Nath, Anil Kottantharayil, "Comprehensive Cell to Module Optical Loss Analysis of Metal Assisted Chemically Etched Inverted Pyramid Textured Multi-crystalline Silicon Solar Cells and Modules by Ray Tracing Method" under review in *IEEE Journal of Photovoltaics*.

Conference Papers

- **K. P. Sreejith**, Ashok Kumar Sharma, Siddharth Behera, Sandeep Kumbhar, Prabir Basu and Anil Kottantharayil, Optimization of MACE black silicon surface morphology in multi-crystalline wafers for excellent opto-electronic properties, *2020 IEEE 47th Photovoltaic Specialists Conference (PVSC)*, 2020, Calgary, Canada.

- **K. P. Sreejith**, Ashok Kumar Sharma, Sandeep Kumbhar, Almouzzam Khan, Nimisha Sreekumar, Tarun S. Yadav, Anil Kottantharayil, Prabir Kanti Basu, Double Layer Anti-reflective Coating on Alkaline Textured Diamond Wire Sawn Multicrystalline Wafers for Superior Light Trapping and Enhanced Surface Passivation, *10th International Conference on Materials for Advanced Technologies (ICMAT)*, 2019, Singapore.

- **K. P. Sreejith**, Ashok K. Sharma, Sandeep Kumbhar, Anzar Gani, D.N Singh, Anil Kottantharayil, Prabir K. Basu,, Industrial Demonstration of 18.5% Max-

imum Efficiency Inline-diffused Additive-free Acid-textured DWS Multicrystalline Silicon Solar Cells, *SiliconPV 2019 / nPV Workshop*, 2019, Leuven, Belgium. **DOI:10.1063/1.5123859**

- **K. P. Sreejith**, Ashok K. Sharma, Sandeep Kumbhar, Anil Kottantharayil, Prabir K. Basu, A New Additive-free Industrial Chemical Texturing Process for Diamond Wire Sawn mc-Si Wafers, *Proc. of 19th International Workshop on Physics of Semiconductor Devices (IWPSD)*, December, 2017, Delhi, India. **DOI:10.1007/978-3-319-97604-4_48**

- Tanushree J. B. Nath, **K. P. Sreejith**, Anil Kottantharayil, Assessment of Optical Properties of Metal Assisted Chemically Etched Black Silicon Surface Morphology in Multi-crystalline Cells and Modules by Ray-tracer Simulations, *5th IEEE International Conference on Emerging Electronics (ICEE)*, August, 2020.

- Ashok Kumar Sharma, Siddharth Behera, **K. P. Sreejith**, Suchismita Mitra, Hemanta Ghosh, Anil Kottantharayil, Troubleshooting the efficiency variation in PERC Silicon solar cell pilot production line using advanced imaging characterization techniques, *5th IEEE International Conference on Emerging Electronics (ICEE)*, August, 2020

- Resmi E, **K. P. Sreejith**, Anil Kottantharayil, 2D Distribution of Fe Concentration in mc-Si Wafers Using Opto-Electrical Characterization, *International Conference on Purification and Recycling of Electronic Materials*, March, 2020, Hyderabad, India.

- Nimisha Sreekumar, **K. P. Sreejith**, Sandeep Kumbhar, Ashok Kumar Sharma, B M Arora, K L Narasimhan, Anil Kottantharayil, Optimization of PECVD Silicon nitride Films for Improved Thickness Uniformity and Reduced Blue Absorption loss in Industrial Solar Cells, *20th International Workshop on Physics of Semiconductor Devices (IWPSD)*, December, 2019, Kolkata, India.

- Sandeep Kumbhar, **K. P. Sreejith**, Ashok Kumar Sharma, B M Arora, K L Narasimhan, Prabir Kanti Basu, Anil Kottantharayil, Optimization of Tube Diffused Low Doped Phosphorous Emitter for High Efficiency Silicon Solar Cells, *20th International Workshop on Physics of Semiconductor Devices (IWPSD)*, December, 2019, Kolkata, India.

- Ashok Kumar Sharma, Siddharth Behera, **K. P. Sreejith**, Tarun S. Yadav, Anil Kottantharayil, Prabir K. Basu, Exploration of Mapping Techniques for Troubleshooting in Industrial Crystalline Si Wafer Solar Cells, *20th International Workshop on Physics of Semiconductor Devices (IWPSD)*, December, 2019, Kolkata, India.

- Siddharth Behera, **K. P. Sreejith**, Almouzzam Khan, Sandeep Kumbhar, Anil Kottantharayil, Prabir K. Basu, Ashok Kumar Sharma, Optimization of Front Metal Contact Design of Industrial Silicon Solar Cell using Photoluminescence Imaging Technique, *3rd International Conference on Solar Energy Photovoltaic (ICSEP)*, December, 2019, Bhubaneswar, India

- Tarun S. Yadav, Ashok Kumar Sharma, Sandeep Kumbhar, **K. P. Sreejith**, Nimisha Sreekumar, Almouzzam Khan, Anil Kottantharayil, Prabir Kanti Basu, Comparison of NaOCl based Cost Effective Silicon Oxide with Other Oxides used for Passivation of Industrial Monocrystalline Silicon Wafers, *10th International Conference on Materials for Advanced Technologies (ICMAT)*, 2019, Singapore.

- Rajul Jain, Siddharth Behera, **K. P. Sreejith**, Anil Kottantharayil, Prabir Kanti Basu, Ashok Kumar Sharma, Mapping of Bulk Diffusion Length and Effective Back Surface Recombination Velocity in Silicon Solar Cells, *4th IEEE International Conference on Emerging Electronics (ICEE)*, December, 2017, Delhi, India. **DOI:10.1109/ICEE44586.2018.8937904**

Patents

- P. K. Basu and **Sreejith K. P.**, An additive-free industrial texturing process for diamond wire cut (DWC) multicrystalline Silicon wafers, Indian patent, 201721022615, Filed.

Bibliography

[1] The International Energy Agency, "Snapshot of Global PV Markets 2020," <https://iea-pvps.org/snapshot-reports/snapshot-2020/>, Tech. Rep., 2020, last access: March 2020.

[2] Markus Fischer, "International Technology Roadmap for Photovoltaic Eleventh Edition, April 2020," <https://itrpv.vdma.org/en/>, Tech. Rep., 2020, Last access: August 2020.

[3] A. Bidiville, I. Neulist, K. Wasmer, and C. Ballif, "Effect of debris on the silicon wafering for solar cells," *Solar Energy Materials and Solar Cells*, vol. 95, no. 8, pp. 2490–2496, 2011.

[4] A. Kumar and S. N. Melkote, "Diamond wire sawing of solar silicon wafers: a sustainable manufacturing alternative to loose abrasive slurry sawing," *Procedia Manufacturing*, vol. 21, pp. 549–566, 2018.

[5] U. Gangopadhyay, S. Dhungel, P. Basu, S. Dutta, H. Saha, and J. Yi, "Comparative study of different approaches of multicrystalline silicon texturing for solar cell fabrication," *Solar Energy Materials and Solar Cells*, vol. 91, no. 4, pp. 285–289, 2007.

[6] P. K. Basu, D. Sarangi, K. D. Shetty, and M. B. Boreland, "Liquid silicate additive for alkaline texturing of mono-Si wafers to improve process bath lifetime and reduce IPA consumption," *Solar Energy Materials and Solar Cells*, vol. 113, pp. 37–43, 2013.

[7] P. K. Basu, S. Chakraborty, Z. Hameiri, and M. B. Boreland, "Novel non-metallic non-acidic approach to generate sub-wavelength surface structures for inline-diffused multicrystalline silicon wafer solar cells," *Applied Surface Science*, vol. 307, pp. 689–697, 2014.

[8] K. Chen, Y. Liu, X. Wang, L. Zhang, and X. Su, "Novel texturing process for diamond-wire-sawn single-crystalline silicon solar cell," *Solar Energy Materials and Solar Cells*, vol. 133, pp. 148–155, 2015.

[9] H. Park, S. Kwon, J. S. Lee, H. J. Lim, S. Yoon, and D. Kim, "Improvement on surface texturing of single crystalline silicon for solar cells by saw-damage etching using an acidic solution," *Solar Energy Materials and Solar Cells*, vol. 93, no. 10, pp. 1773–1778, 2009.

[10] J. Acker, T. Koschwitz, B. Meinel, R. Heinemann, and C. Blocks, "HF/HNO_3 etching of the saw damage," *Energy Procedia*, vol. 38, pp. 223–233, 2013.

[11] U. Gangopadhyay, K. Kim, S. Dhungel, U. Manna, P. Basu, M. Banerjee, H. Saha, and J. Yi, "A novel low cost texturization method for large area commercial mono-crystalline silicon solar cells," *Solar Energy Materials and Solar cells*, vol. 90, no. 20, pp. 3557–3567, 2006.

[12] T.-C. Wang, H.-Y. Lee, C.-T. Lee, Y.-C. Cheng, and H.-W. Chen, "Investigated performance improvement of the micro-pressure sandblast-treated multi-crystalline Si wafer sliced using diamond wire sawing," *Solar Energy*, vol. 161, pp. 220–225, 2018.

[13] X. M. Liu, W. H. Chen, M. Li, and L. Zhou, "Texture for diamond wire sawn multicrystalline silicon wafers by a vapor etching method," *Acta Photonica Sinica*, vol. 1, p. 024, 2015.

[14] J. Benick, A. Richter, R. Müller, H. Hauser, F. Feldmann, P. Krenckel, S. Riepe, F. Schindler, M. C. Schubert, M. Hermle *et al.*, "High-efficiency n-type HP mc silicon solar cells," *IEEE Journal of Photovoltaics*, vol. 7, no. 5, pp. 1171–1175, 2017.

[15] K. Chen, J. Zha, F. Hu, X. Ye, S. Zou, V. Vähänissi, J. M. Pearce, H. Savin, and X. Su, "MACE nano-texture process applicable for both single-and multi-crystalline diamond-wire sawn Si solar cells," *Solar Energy Materials and Solar Cells*, vol. 191, pp. 1–8, 2019.

[16] B. Hoex. The free online resource about photovoltaic manufacturing. <https://pv-manufacturing.org>. Last access: May 2021.

[17] P. Basu, H. Dhasmana, D. Varandani, B. Mehta, and D. Thakur, "A cost-effective alkaline multicrystalline silicon surface polishing solution with improved smoothness," *Solar Energy Materials and Solar Cells*, vol. 93, no. 10, pp. 1743–1748, 2009.

[18] J. D. Hylton, *Light coupling and light trapping in alkaline etched multicrystalline silicon wafers for solar cells*. Ph. D thesis, Utrecht University, April 2006.

[19] U. Gangopadhyay, S. Dhungel, K. Kim, U. Manna, P. Basu, H. Kim, B. Karunagaran, K. Lee, J. Yoo, and J. Yi, "Novel low cost chemical texturing for very large area industrial multi-crystalline silicon solar cells," *Semiconductor Science and Technology*, vol. 20, no. 9, p. 938, 2005.

[20] P. Basu, H. Dhasmana, N. Udayakumar, F. Khan, and D. Thakur, "Regulated low cost pre-treatment step for surface texturization of large area industrial single crystalline silicon solar cell," *Solar Energy Materials and Solar Cells*, vol. 94, no. 6, pp. 1049–1054, 2010.

[21] U. Gangopadhyay, S. Dhungel, A. Mondal, H. Saha, and J. Yi, "Novel low-cost approach for removal of surface contamination before texturization of commercial monocrystalline silicon solar cells," *Solar Energy Materials and Solar cells*, vol. 91, no. 12, pp. 1147–1151, 2007.

[22] O. Tabata, R. Asahi, H. Funabashi, K. Shimaoka, and S. Sugiyama, "Anisotropic etching of silicon in TMAH solutions," *Sensors and Actuators A: Physical*, vol. 34, no. 1, pp. 51–57, 1992.

[23] P. K. Basu, D. Sarangi, and M. B. Boreland, "Single-component damage-etch process for improved texturization of monocrystalline silicon wafer solar cells," *IEEE Journal of Photovoltaics*, vol. 3, no. 4, pp. 1222–1228, 2013.

[24] H. Nakaya, M. Nishida, Y. Takeda, S. Moriuchi, T. Tonegawa, T. Machida, and T. Nunoi, "Polycrystalline silicon solar cells with V-grooved surface," *Solar Energy Materials and Solar Cells*, vol. 34, no. 1-4, pp. 219–225, 1994.

[25] G. Willeke, H. Nussbaumer, H. Bender, and E. Bucher, "A simple and effective light trapping technique for polycrystalline silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 26, no. 4, pp. 345–356, 1992.

[26] E. Wefringhaus, C. Kesnar, and M. Löhmann, "Statistical approach to the description of random pyramid surfaces using 3D surface profiles," *Energy Procedia*, vol. 8, pp. 135–140, 2011.

[27] P. Singh, R. Kumar, M. Lal, S. Singh, and B. Das, "Effectiveness of anisotropic etching of silicon in aqueous alkaline solutions," *Solar Energy Materials and Solar Cells*, vol. 70, no. 1, pp. 103–113, 2001.

[28] L. Sun and J. Tang, "A new texturing technique of monocrystalline silicon surface with sodium hypochlorite," *Applied Surface Science*, vol. 255, no. 22, pp. 9301–9304, 2009.

[29] M. Moynihan, C. Connor, B. Barr, S. Tiffany, W. Braun, G. Allardyce, J. Rentsch, and K. Birmann, "IPA free texturing of mono-crystalline solar cells," *Proc. 25th European Photovoltaic Solar Energy Conference and Exhibition, Valencia, Spain*, pp. 1332–1336, 2010.

[30] P. K. Basu, "Alkaline pyramidal texturing processes for industrial monocrystalline silicon wafer solar cells," *Society for Materials Chemistry Bulletin*, vol. 8, pp. 1–6, 2019.

[31] A. Merlos, M. Acero, M. Bao, J. Bausells, and J. Esteve, "TMAH/IPA anisotropic etching characteristics," *Sensors and Actuators A: Physical*, vol. 37, pp. 737–743, 1993.

[32] U. Gangopadhyay, K. Kim, S. Dhungel, P. Basu, and J. Yi, "Low-cost texturization of large-area crystalline silicon solar cells using hydrazine mono-hydrate for industrial use," *Renewable Energy*, vol. 31, no. 12, pp. 1906–1915, 2006.

[33] Y.-T. Cheng, J.-J. Ho, S.-Y. Tsai, Z.-Z. Ye, W. Lee, D.-S. Hwang, S.-H. Chang, C.-C. Chang, and K. L. Wang, "Efficiency improved by acid texturization for multi-crystalline silicon solar cells," *Solar Energy*, vol. 85, no. 1, pp. 87–94, 2011.

[34] P. Basu, H. Dhasmana, N. Udayakumar, and D. Thakur, "A new energy efficient, environment friendly and high productive texturization process of industrial multicrystalline silicon solar cells," *Renewable Energy*, vol. 34, no. 12, pp. 2571–2576, 2009.

[35] R. Einhaus, E. Vazsonyi, J. Szlufcik, J. Nijs, and R. Mertens, "Isotropic texturing of multicrystalline silicon wafers with acidic texturing solutions," in *26^{th} IEEE Photovoltaic Specialists Conference*, 1997, pp. 167–170.

[36] D. Turner, "On the mechanism of chemically etching germanium and silicon," *Journal of the Electrochemical Society*, vol. 107, no. 10, p. 810, 1960.

[37] E. S. Kooij, K. Butter, and J. Kelly, "Silicon etching in HNO_3/HF solution: charge balance for the oxidation reaction," *Electrochemical and Solid State Letters*, vol. 2, no. 4, p. 178, 1999.

[38] B. Schwartz and H. Robbins, "Chemical etching of silicon: IV. etching technology," *Journal of the Electrochemical Society*, vol. 123, no. 12, pp. 1903–1909, 1976.

[39] M. T. Kelly, J. K. Chun, and A. B. Bocarsly, "High efficiency chemical etchant for the formation of luminescent porous silicon," *Applied Physics Letters*, vol. 64, no. 13, pp. 1693–1695, 1994.

[40] M. Steinert, J. Acker, M. Krause, S. Oswald, and K. Wetzig, "Reactive species generated during wet chemical etching of silicon in HF/HNO_3 mixtures," *The Journal of Physical Chemistry B*, vol. 110, no. 23, pp. 11 377–11 382, 2006.

[41] M. Steinert, J. Acker, S. Oswald, and K. Wetzig, "Study on the mechanism of silicon etching in HNO_3-rich HF/HNO_3 mixtures," *The Journal of Physical Chemistry C*, vol. 111, no. 5, pp. 2133–2140, 2007.

[42] K. W. Kolasinski, "The mechanism of Si etching in fluoride solutions," *Physical Chemistry Chemical Physics*, vol. 5, no. 6, pp. 1270–1278, 2003.

[43] V. Lehmann and U. Gösele, "Porous silicon formation: A quantum wire effect," *Applied Physics Letters*, vol. 58, no. 8, pp. 856–858, 1991.

[44] M. Marso, M. Berger, M. Thonissen, H. Luth, H. Munder *et al.*, "An extended quantum model for porous silicon formation," *Journal of The Electrochemical Society*, vol. 142, no. 2, pp. 615–620, 1995.

[45] L. Koker and K. W. Kolasinski, "Photoelectrochemical etching of Si and porous Si in aqueous HF," *Physical Chemistry Chemical Physics*, vol. 2, no. 2, pp. 277–281, 2000.

[46] S. Narayanan, "Large area multicrystalline silicon solar cells in high volume production environment history, status, new processes, technology transfer issues," *Solar Energy Materials and Solar Cells*, vol. 74, no. 1-4, pp. 107–115, 2002.

[47] P. Panek, M. Lipinski, and J. Dutkiewicz, "Texturization of multicrystalline silicon by wet chemical etching for silicon solar cells," *Journal of Materials Science*, vol. 40, no. 6, pp. 1459–1463, 2005.

[48] T. Bruton, "General trends about photovoltaics based on crystalline silicon," *Solar Energy Materials and Solar Cells*, vol. 72, no. 1-4, pp. 3–10, 2002.

[49] M. A. Green, "Crystalline and thin-film silicon solar cells: state of the art and future potential," *Solar Energy*, vol. 74, no. 3, pp. 181–192, 2003.

[50] Y. Nishimoto, T. Ishihara, and K. Namba, "Investigation of acidic texturization for multicrystalline silicon solar cells," *Journal of the Electrochemical Society*, vol. 146, no. 2, p. 457, 1999.

[51] K. Kim, S. Dhungel, S. Jung, D. Mangalaraj, and J. Yi, "Texturing of large area multi-crystalline silicon wafers through different chemical approaches for solar cell fabrication," *Solar Energy Materials and Solar Cells*, vol. 92, no. 8, pp. 960–968, 2008.

[52] M. Ju, M. Gunasekaran, K. Kim, K. Han, I. Moon, K. Lee, S. Han, T. Kwon, D. Kyung, and J. Yi, "A new vapor texturing method for multicrystalline silicon solar cell applications," *Materials Science and Engineering: B*, vol. 153, no. 1-3, pp. 66–69, 2008.

[53] J. Nievendick, M. Zimmer, F. Souren, J. Haunschild, and J. Rentsch, "Relation between solar cell efficiency and crystal defect etching induced by acidic texturization on multicrystalline silicon material," *Solar Energy Materials and Solar Cells*, vol. 105, pp. 159–166, 2012.

[54] G. Kulesza, P. Panek, and P. Zikeba, "Time efficient texturization of multicrystalline silicon in the HF/HNO_3 solutions and its effect on optoelectronic parameters of solar cells," *Archives of Civil and Mechanical Engineering*, vol. 14, no. 4, pp. 595–601, 2014.

[55] A. Hauser, I. Melnyk, P. Fath, S. Narayanan, S. Roberts, and T. Bruton, "A simplified process for isotropic texturing of mc-Si," in *Proceedings of 3rd World Conference on Photovoltaic Energy Conversion*, vol. 2, 2003, pp. 1447–1450.

[56] B. Schwartz and H. Robbins, "Chemical etching of silicon: III. a temperature study in the acid system," *Journal of the Electrochemical Society*, vol. 108, no. 4, p. 365, 1961.

[57] A. Hauser, I. Melnyk, E. Wefringhaus, F. Delahaye, G. Vilsmeier, and P. Fath, "Acidic texturisation of mc-Si using a high throughput in-line prototype system with no organic chemistry," in *Proceedings of the 19th European Photovoltaic Solar Energy Conference*, 2004, pp. 1094–1097.

[58] D. MacDonald, A. Cuevas, M. J. Kerr, C. Samundsett, D. Ruby, S. Winderbaum, and A. Leo, "Texturing industrial multicrystalline silicon solar cells," *Solar Energy*, vol. 76, no. 1-3, pp. 277–283, 2004.

[59] A. Schneider, G. Bühler, F. Huster, K. Peter, and P. Fath, "Impact of individual process steps on the stability of silicon solar cells studied with a simple mechanical stability tester," in *Conference on PV in Europe from PV Technology to Energy Solutions*, 2002, Retrieved from: <https://www.hahn.uni-konstanz.de/typo3temp/secure_downloads/80509/0/c1a75342f8b3f9ea368f16ca6e2e3f1fc52b7526/Paper-Rom-AS.pdf>.

[60] T. Geipel, S. Pingel, J. Dittrich, Y. Zemen, G. Kropke, M. Wittner, and J. Berghold, "Comparison of acidic and alkaline textured multicrystalline solar cells in a solar panel production," *Power*, vol. 4, no. 3, p. 9, 2009.

[61] J. Arumughan, T. Pernau, A. Schneider, R. Kopecek, and P. Fath, "Processing and characterisation of isotropically, alkaline and mechanically textured mc-si buried contact solar cells: A comparative study," Retrieved from: <https://www.hahn.uni-konstanz.de/typo3temp/secure_downloads/80509/0/b98d0558214037ddda432133e6e65e7d84d88c29/Prasad_2CV-3-30.pdf>.

[62] RENA. High throughput solution for texturing of multi crystalline Si with low coo. <https://www.rena.com/en/products/green-energy/cell-inline/intexr/>. Last access: June 10, 2020.

[63] SCHIMID. Perfect wafer surfaces at the lowest process costs. <https://schmid-group.com/en/business-units/photovoltaics/cell/acid-texturing/>. Last access: June 10, 2020.

[64] SINGULUS. Smart solutions to drive the future. <https://www.singulus.de/fileadmin/media/pdf/stangl/linea-0909.pdf>. Last access: June 10, 2020.

[65] S. Zhou, C. Zhou, W. Wang, Y. Tang, J. Chen, B. Yan, and Y. Zhao, "Experimental study on the elimination of over-plating problems in industrial manufacturing of large-area acidic-textured laser-doped multi-crystalline solar cells," *Solar Energy Materials and Solar Cells*, vol. 108, pp. 44–49, 2013.

[66] P. K. Basu, F. Law, S. Vinodh, A. Kumar, P. Richter, F. Bottari, and B. Hoex, "0.4% absolute efficiency increase for inline-diffused screen-printed multicrystalline silicon wafer solar cells by non-acidic deep emitter etch-back," *Solar Energy Materials and Solar Cells*, vol. 137, pp. 193–201, 2015.

[67] P. K. Basu, J. Li, V. Shanmugam, and A. Khanna, "Heavy phosphorous tube-diffusion and non-acidic deep chemical etch-back assisted efficiency enhancement of industrial multicrystalline silicon wafer solar cells," *RSC Advances*, vol. 6, no. 42, pp. 35 928–35 935, 2016.

[68] M. Lippold and E. Kroke, "*HF-HNO_3-H_2SO_4*-mixtures for etching multicrystalline silicon wafers: etching rates, bath analytics and surface texture," in *Proceedings of the 26th European Photovoltaic Solar Energy Conference*, 2011, pp. 1800–1802.

[69] E. S. Marstein, H. J. Solheim, D. N. Wright, and A. Holt, "Acidic texturing of multicrystalline silicon wafers," in *31st IEEE Photovoltaic Specialists Conference, 2005.*, 2005, pp. 1309–1312.

[70] R. Watanabe, S. Abe, S. Haruyama, T. Suzuki, M. Onuma, and Y. Saito, "Evaluation of a new acid solution for texturization of multicrystalline silicon solar cells," *International Journal of Photoenergy*, vol. 2013, 2013.

[71] M. Lippold, F. Buchholz, C. Gondek, F. Honeit, E. Wefringhaus, and E. Kroke, "Texturing of SiC-slurry and diamond wire sawn silicon wafers by *HF-HNO_3-H_2SO_4* mixtures," *Solar Energy Materials and Solar Cells*, vol. 127, pp. 104–110, 2014.

[72] J. D. Plummer, *Silicon VLSI technology: fundamentals, practice and modeling*. Pearson Education India, 2009.

[73] J. D. Plummer and P. B. Griffin, "Material and process limits in silicon VLSI technology," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 240–258, 2001.

[74] X. Li, T. Abe, and M. Esashi, "Deep reactive ion etching of pyrex glass using SF_6 plasma," *Sensors and Actuators A: Physical*, vol. 87, no. 3, pp. 139–145, 2001.

[75] R. Legtenberg, H. Jansen, M. De Boer, and M. Elwenspoek, "Anisotropic reactive ion etching of silicon using $SF_6/O_2/CHF_3$ gas mixtures," *Journal of the Electrochemical Society*, vol. 142, no. 6, p. 2020, 1995.

[76] G. Oehrlein, R. Tromp, Y. Lee, and E. Petrillo, "Study of silicon contamination and near-surface damage caused by CF_4/H_2 reactive ion etching," *Applied Physics Letters*, vol. 45, no. 4, pp. 420–422, 1984.

[77] G. S. Oehrlein and H. L. Williams, "Silicon etching mechanisms in a CF_4/H_2 glow discharge," *Journal of Applied Physics*, vol. 62, no. 2, pp. 662–672, 1987.

[78] S. Winderbaum, O. Reinhold, and F. Yun, "Reactive ion etching (RIE) as a method for texturing polycrystalline silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 46, no. 3, pp. 239–248, 1997.

[79] F. Restrepo and C. Backus, "On black solar cells or the tetrahedral texturing of a silicon surface," *IEEE Transactions on Electron Devices*, vol. 23, no. 10, pp. 1195–1197, 1976.

[80] E. Palik, O. Glembocki, I. Heard Jr, P. Burno, and L. Tenerz, "Etching roughness for (100) silicon surfaces in aqueous KOH," *Journal of Applied Physics*, vol. 70, no. 6, pp. 3291–3300, 1991.

[81] Q.-B. Vu, D. A. Stricker, and P. M. Zavracky, "Surface characteristics of (100) silicon anisotropically etched in aqueous KOH," *Journal of the Electrochemical Society*, vol. 143, no. 4, p. 1372, 1996.

[82] Y. Inomata, K. Fukui, and K. Shirasawa, "Surface texturing of large area multicrystalline silicon solar cells using reactive ion etching method," *Solar Energy Materials and Solar Cells*, vol. 48, no. 1-4, pp. 237–242, 1997.

[83] D. Ruby, S. H. Zaidi, S. Narayanan, B. M. Damiani, and A. Rohatgi, "RIE-texturing of multicrystalline silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 74, no. 1-4, pp. 133–137, 2002.

[84] D. S. Ruby, S. H. Zaidi, and S. Narayanan, "Plasma-texturization for multicrystalline silicon solar cells," in *28th IEEE Photovoltaic Specialists Conference*, 2000, pp. 75–78.

[85] J. Yoo, G. Yu, and J. Yi, "Large-area multicrystalline silicon solar cell fabrication using reactive ion etching (RIE)," *Solar Energy Materials and Solar Cells*, vol. 95, no. 1, pp. 2–6, 2011.

[86] K.-S. Lee, M.-H. Ha, J. H. Kim, and J.-W. Jeong, "Damage-free reactive ion etch for high-efficiency large-area multi-crystalline silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 95, no. 1, pp. 66–68, 2011.

[87] J. Yoo, K.-M. Han, and J.-S. Cho, "Solar cell fabrication using two-step textured quasi-single crystalline silicon by alkaline and RIE texturing processes," *Vacuum*, vol. 128, pp. 118–122, 2016.

[88] C. Gerhards, C. Marckmann, R. Tolle, M. Spiegel, P. Fath, G. Willeke, E. Bucher, J. Creager, and S. Narayanan, "Mechanically V-textured low cost multicrystalline silicon solar cells with a novel printing metallization," in *26th IEEE Photovoltaic Specialists Conference*, 1997, pp. 43–46.

[89] J. Nievendick, J. Specht, M. Zimmer, L. Zahner, W. Glover, D. Stüwe, and J. Rentsch, "Formation of a honeycomb texture for multicrystalline silicon solar cells using an inkjetted mask," *Physica Status Solidi (RRL)- Rapid Research Letters*, vol. 6, no. 1, pp. 7–9, 2012.

[90] N. Borojevic, A. Lennon, and S. Wenham, "Light trapping structures for silicon solar cells via inkjet printing," *Physica Status Solidi (a)*, vol. 211, no. 7, pp. 1617–1622, 2014.

[91] W. Chen, X. Liu, M. Li, C. Yin, and L. Zhou, "On the nature and removal of saw marks on diamond wire sawn multicrystalline silicon wafers," *Materials Science in Semiconductor Processing*, vol. 27, pp. 220–227, 2014.

[92] C. M. Chong, S. R. Wenham, and M. A. Green, "High-efficiency, laser grooved, buried contact silicon solar cells," *Applied Physics Letters*, vol. 52, no. 5, pp. 407–409, 1988.

[93] T.-H. Her, R. J. Finlay, C. Wu, S. Deliwala, and E. Mazur, "Microstructuring of silicon with femtosecond laser pulses," *Applied Physics Letters*, vol. 73, no. 12, pp. 1673–1675, 1998.

[94] C. H. Crouch, J. E. Carey, J. M. Warrender, M. J. Aziz, E. Mazur, and F. Y. Génin, "Comparison of structure and properties of femtosecond and nanosecond laser-structured silicon," *Applied Physics Letters*, vol. 84, no. 11, pp. 1850–1852, 2004.

[95] M. Abbott and J. Cotter, "Optical and electrical properties of laser texturing for high-efficiency solar cells," *Progress in Photovoltaics: Research and Applications*, vol. 14, no. 3, pp. 225–235, 2006.

[96] L. Dobrzański and A. Drygała, "Laser processing of multicrystalline silicon for texturization of solar cells," *Journal of Materials Processing Technology*, vol. 191, no. 1-3, pp. 228–231, 2007.

[97] M. Halbwax, T. Sarnet, P. Delaporte, M. Sentis, H. Etienne, F. Torregrosa, V. Vervisch, I. Perichaud, and S. Martinuzzi, "Micro and nano-structuration of silicon by femtosecond laser: application to silicon photovoltaic cells fabrication," *Thin Solid Films*, vol. 516, no. 20, pp. 6791–6795, 2008.

[98] S. Kontermann, T. Gimpel, A. Baumann, K.-M. Guenther, and W. Schade, "Laser processed black silicon for photovoltaic applications," *Energy Procedia*, vol. 27, pp. 390–395, 2012.

[99] H. Morikawa, D. Niinobe, K. Nishimura, S. Matsuno, and S. Arimoto, "Processes for over 18.5% high-efficiency multi-crystalline silicon solar cell," *Current Applied Physics*, vol. 10, no. 2, pp. S210–S214, 2010.

[100] D. Zielke, D. Sylla, T. Neubert, R. Brendel, and J. Schmidt, "Direct laser texturing for high-efficiency silicon solar cells," *IEEE Journal of Photovoltaics*, vol. 3, no. 2, pp. 656–661, 2012.

[101] M. A. Green, "The passivated emitter and rear cell (PERC): From conception to mass production," *Solar Energy Materials and Solar Cells*, vol. 143, pp. 190–197, 2015.

[102] Y. Lv, Y. Zhuang, W. Wang, W. Wei, J. Sheng, S. Zhang, and W. Shen, "Towards high-efficiency industrial p-type mono-like Si PERC solar cells," *Solar Energy Materials and Solar Cells*, vol. 204, p. 110202, 2020.

[103] J.-S. Chiu, Y.-M. Zhao, S. Zhang, and D.-S. Wuu, "The role of laser ablated backside contact pattern in efficiency improvement of mono crystalline silicon PERC solar cells," *Solar Energy*, vol. 196, pp. 462–467, 2020.

[104] P. Colson, R. Cloots, and C. Henrist, "Experimental design applied to spin coating of 2D colloidal crystal masks: a relevant method?" *Langmuir*, vol. 27, no. 21, pp. 12 800–12 806, 2011.

[105] V. Krivitsky, L.-C. Hsiung, A. Lichtenstein, B. Brudnik, R. Kantaev, R. Elnathan, A. Pevzner, A. Khatchtourints, and F. Patolsky, "Si nanowires forest-based on-chip biomolecular filtering, separation and preconcentration devices: nanowires do it all," *Nano Letters*, vol. 12, no. 9, pp. 4748–4756, 2012.

[106] F. Iskandar, M. Abdullah, H. Yoden, and K. Okuyama, "Silica films containing ordered pores prepared by dip coating of silica nanoparticles and polystyrene beads colloidal mixture," *Journal of Sol-gel Science and Technology*, vol. 29, no. 1, pp. 41–47, 2004.

[107] H. Deckman and J. Dunsmuir, "Applications of surface textures produced with natural lithography," *Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena*, vol. 1, no. 4, pp. 1109–1112, 1983.

[108] M. Winzer, M. Kleiber, N. Dix, and R. Wiesendanger, "Fabrication of nano-dot- and nano-ring-arrays by nanosphere lithography," *Applied Physics A*, vol. 63, no. 6, pp. 617–619, 1996.

[109] C. Haginoya, M. Ishibashi, and K. Koike, "Nanostructure array fabrication with a size-controllable natural lithography," *Applied Physics Letters*, vol. 71, no. 20, pp. 2934–2936, 1997.

[110] W. Nositschka, C. Beneking, O. Voigt, and H. Kurz, "Texturisation of multicrystalline silicon wafers for solar cells by reactive ion etching through colloidal masks," *Solar Energy Materials and Solar Cells*, vol. 76, no. 2, pp. 155–166, 2003.

[111] J. W. Yang, J. I. Sim, H. M. An, and T. G. Kim, "Fabrication of nanometer-scale pillar structures by using nanosphere lithography," *Journal of the Korean Physical Society*, vol. 58, no. 42, pp. 994–997, 2011.

[112] H. Nishikawa, S. Maenosono, Y. Yamaguchi, and T. Okubo, "Self-assembling process of colloidal particles into two-dimensional arrays induced by capillary immersion force: A simulation study with discrete element method," *Journal of Nanoparticle Research*, vol. 5, no. 1-2, pp. 103–110, 2003.

[113] N. Blondiaux, E. Scolan, G. Franc, and R. Pugin, "Manufacturing of superhydrophobic surfaces combining nanosphere lithography with replication tech-

niques," in *12th IEEE International Conference on Nanotechnology (IEEE-NANO)*, 2012, pp. 1–6.

[114] A. Burgers, J. Bultman, C. Beneking, W. Nositschka, O. Voigt, and H. Kurz, "Silicon solar cells textured by reactive ion etching with natural lithography," *16th European Photovoltaic Solar Energy Conference*, 2000.

[115] K. Tomono, H. Furuya, S. Miyamoto, Y. Okamura, M. Sumimoto, Y. Sakata, R. Komatsu, and M. Nakayama, "Investigations on hydrobromination of silicon in the presence of silicon carbide abrasives as a purification route of kerf loss waste," *Separation and Purification Technology*, vol. 103, pp. 109–113, 2013.

[116] M. Hecini, N. Drouiche, and O. Bouchelaghem, "Recovery of cutting fluids used in polycrystalline silicon ingot slicing," *Journal of Crystal Growth*, vol. 453, pp. 143–150, 2016.

[117] K. I. Ishikawa, H. Suwabe, S.-i. Itoh, and M. Uneda, "A basic study of the behavior of slurry action at multi-wire saw," in *Key Engineering Materials*, vol. 238, 2003, pp. 89–92.

[118] H. J. Möller, "Basic mechanisms and models of multi-wire sawing," *Advanced Engineering Materials*, vol. 6, no. 7, pp. 501–513, 2004.

[119] Bidiville, A and Wasmer, K and Kraft, R and Ballif, C, "Diamond wire-sawn silicon wafers-from the lab to the cell production," <https://infoscience.epfl.ch/record/143997>, Tech. Rep., 2020, last access: July 2021.

[120] N. Watanabe, Y. Kondo, D. Ide, T. Matsuki, H. Takato, and I. Sakata, "Characterization of polycrystalline silicon wafers for solar cells sliced with novel fixed-abrasive wire," *Progress in Photovoltaics: Research and Applications*, vol. 18, no. 7, pp. 485–490, 2010.

[121] B. R. Lawn, A. Evans, and D. Marshall, "Elastic/plastic indentation damage in ceramics: the median/radial crack system," *Journal of the American Ceramic Society*, vol. 63, no. 9-10, pp. 574–581, 1980.

[122] D. Marshall, B. Lawn, and A. Evans, "Elastic/plastic indentation damage in ceramics: the lateral crack system," *Journal of the American Ceramic Society*, vol. 65, no. 11, pp. 561–566, 1982.

[123] B. Lawn and R. Wilshaw, "Indentation fracture: principles and applications," *Journal of Materials Science*, vol. 10, no. 6, pp. 1049–1081, 1975.

[124] T. G. Bifano, T. A. Dow, and R. O. Scattergood, "Ductile-regime grinding: a new technology for machining brittle materials," *Journal of Manufacturing Science and Engineering*, pp. 185–189, 1991.

[125] K. Tomono, S. Miyamoto, T. Ogawa, H. Furuya, Y. Okamura, M. Yoshimoto, R. Komatsu, and M. Nakayama, "Recycling of kerf loss silicon derived from diamond-wire saw cutting process by chemical approach," *Separation and Purification Technology*, vol. 120, pp. 304–309, 2013.

[126] C. Yang, H. Wu, S. Melkote, and S. Danyluk, "Comparative analysis of fracture strength of slurry and diamond wire sawn multicrystalline silicon solar wafers," *Advanced Engineering Materials*, vol. 15, no. 5, pp. 358–365, 2013.

[127] Y. Zhuang, S. Zhong, Z. Huang, and W. Shen, "Versatile strategies for improving the performance of diamond wire sawn mc-Si solar cells," *Solar Energy Materials and Solar Cells*, vol. 153, pp. 18–24, 2016.

[128] Multi-Tex. (2018) The revolution of acid texturing process. <http://www.gpsolar.de/materials/chemikalien/multi-tex/>. Last access: Auguest 28, 2018.

[129] K. Krieg, N. Jenek, and M. Zimmer, "Texturization of multicrystalline DWS wafers by $HF/HNO_3/H_2SO_4$ at elevated temperature," in *AIP Conference Proceedings*, vol. 1999, no. 1, 2018, p. 050004.

[130] H. Takato, I. Sakata, K. Mase, S. Ishibashi, T. Harada, Y. Kondo, and H. Asai, "Method for fabricating substrate for solar cell," Nov. 21 2013, US Patent App. 13/982,104.

[131] K. Nishioka, K. Ikematsu, Y. Ota, and K. Araki, "Sandblasting durability of acrylic and glass Fresnel lenses for concentrator photovoltaic modules," *Solar Energy*, vol. 86, no. 10, pp. 3021–3025, 2012.

[132] J. Ding, S. Zou, J. Choi, J. Cui, D. Yuan, H. Sun, C. Wu, J. Zhu, X. Ye, and X. Su, "A laser texturing study on multi-crystalline silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 214, p. 110587, 2020.

[133] J. Jin, H. Shen, P. Zheng, K. S. Chan, X. Zhang, and H. Jin, "> 20.5% diamond wire sawn multicrystalline silicon solar cells with maskless inverted pyramid like texturing," *IEEE Journal of Photovoltaics*, vol. 7, no. 5, pp. 1264–1269, 2017.

[134] H. Savin, P. Repo, G. Von Gastrow, P. Ortega, E. Calle, M. Garín, and R. Alcubilla, "Black silicon solar cells with interdigitated back-contacts achieve 22.1% efficiency," *Nature Nanotechnology*, vol. 10, no. 7, p. 624, 2015.

[135] S. Wang, X. Gou, S. Zhou, J. Huang, Q. Huang, J. Qiu, Z. Xu, and H. Shen, "Effect of surface structure on electrical performance of industrial diamond wire sawing multicrystalline Si solar cells," *International Journal of Photoenergy*, 2018.

[136] X. Li and P. Bohn, "Metal-assisted chemical etching in HF/H_2O_2 produces porous silicon," *Applied Physics Letters*, vol. 77, no. 16, pp. 2572–2574, 2000.

[137] Y. Harada, X. Li, P. W. Bohn, and R. G. Nuzzo, "Catalytic amplification of the soft lithographic patterning of Si. nonelectrochemical orthogonal fabrication of photoluminescent porous Si pixel arrays," *Journal of the American Chemical Society*, vol. 123, no. 36, pp. 8709–8717, 2001.

[138] S. Chattopadhyay and P. W. Bohn, "Direct-write patterning of microstructured porous silicon arrays by focused-ion-beam Pt deposition and metal-assisted electroless etching," *Journal of Applied Physics*, vol. 96, no. 11, pp. 6888–6894, 2004.

[139] Z. Huang, H. Fang, and J. Zhu, "Fabrication of silicon nanowire arrays with controlled diameter, length, and density," *Advanced Materials*, vol. 19, no. 5, pp. 744–748, 2007.

[140] C.-C. Huang, C.-H. Su, W.-M. Li, T.-Y. Liu, J.-H. Chen, and C.-S. Yeh, "Bifunctional Gd_2O_3/C nanoshells for MR imaging and NIR therapeutic applications," *Advanced Functional Materials*, vol. 19, no. 2, pp. 249–258, 2009.

[141] D. Dimova-Malinovska, M. Sendova-Vassileva, N. Tzenov, and M. Kamenova, "Preparation of thin porous silicon layers by stain etching," *Thin Solid Films*, vol. 297, no. 1-2, pp. 9–12, 1997.

[142] K. Tsujino and M. Matsumura, "Helical nanoholes bored in silicon by wet chemical etching using platinum nanoparticles as catalyst," *Electrochemical and Solid-State Letters*, vol. 8, no. 12, pp. C193–C195, 2005.

[143] W. Choi, T. Liew, M. Dawood, H. I. Smith, C. Thompson, and M. Hong, "Synthesis of silicon nanowires and nanofin arrays using interference lithography and catalytic etching," *Nano Letters*, vol. 8, no. 11, pp. 3799–3802, 2008.

[144] S.-W. Chang, V. P. Chuang, S. T. Boles, C. A. Ross, and C. V. Thompson, "Densely packed arrays of ultra-high-aspect-ratio silicon nanowires fabricated using block-copolymer lithography and metal-assisted etching," *Advanced Functional Materials*, vol. 19, no. 15, pp. 2495–2500, 2009.

[145] Z. Huang, T. Shimizu, S. Senz, Z. Zhang, X. Zhang, W. Lee, N. Geyer, and U. Gosele, "Ordered arrays of vertically aligned [110] silicon nanowires by suppressing the crystallographically preferred <100> etching directions," *Nano Letters*, vol. 9, no. 7, pp. 2519–2525, 2009.

[146] S. Chattopadhyay, X. Li, and P. W. Bohn, "In-plane control of morphology and tunable photoluminescence in porous silicon produced by metal-assisted electroless chemical etching," *Journal of Applied Physics*, vol. 91, no. 9, pp. 6134–6140, 2002.

[147] C.-Y. Chen, C.-S. Wu, C.-J. Chou, and T.-J. Yen, "Morphological control of single-crystalline silicon nanowire arrays near room temperature," *Advanced Materials*, vol. 20, no. 20, pp. 3811–3815, 2008.

[148] K. Peng, A. Lu, R. Zhang, and S.-T. Lee, "Motility of metal nanoparticles in silicon and induced anisotropic silicon etching," *Advanced Functional Materials*, vol. 18, no. 19, pp. 3026–3035, 2008.

[149] K. Tsujino and M. Matsumura, "Boring deep cylindrical nanoholes in silicon using silver nanoparticles as a catalyst," *Advanced Materials*, vol. 17, no. 8, pp. 1045–1047, 2005.

[150] Z. Huang, N. Geyer, P. Werner, J. De Boor, and U. Gösele, "Metal-assisted chemical etching of silicon: A review: In memory of prof. ulrich gösele," *Advanced Materials*, vol. 23, no. 2, pp. 285–308, 2011.

[151] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang, "Enhanced thermoelectric performance of rough silicon nanowires," *Nature*, vol. 451, no. 7175, pp. 163–167, 2008.

[152] A. I. Hochbaum, D. Gargas, Y. J. Hwang, and P. Yang, "Single crystalline mesoporous silicon nanowires," *Nano Letters*, vol. 9, no. 10, pp. 3550–3554, 2009.

[153] G. Flätgen, S. Wasle, M. Lübke, C. Eickes, G. Radhakrishnan, K. Doblhofer, and G. Ertl, "Autocatalytic mechanism of H_2O_2 reduction on Ag electrodes in acidic electrolyte: experiments and simulations," *Electrochimica Acta*, vol. 44, no. 25, pp. 4499–4506, 1999.

[154] R. Zeis, T. Lei, K. Sieradzki, J. Snyder, and J. Erlebacher, "Catalytic reduction of oxygen and hydrogen peroxide by nanoporous gold," *Journal of Catalysis*, vol. 253, no. 1, pp. 132–138, 2008.

[155] J. Huang, R. Sen, and E. Yeager, "Oxygen reduction on platinum in 85% orthophosphoric acid," *Journal of The Electrochemical Society*, vol. 126, no. 5, p. 786, 1979.

[156] Y. Li, R. Lenigk, X. Wu, B. Gruendig, S. Dong, and R. Renneberg, "Investigation of oxygen-and hydrogen peroxide-reduction on platinum particles dispersed on poly (o-phenylenediamine) film modified glassy carbon electrodes," *Electroanalysis: An International Journal Devoted to Fundamental and Practical Aspects of Electroanalysis*, vol. 10, no. 10, pp. 671–676, 1998.

[157] X. Cai, K. Kalcher, G. Kölbl, C. Neuhold, W. Diewald, and B. Ogorevc, "Electrocatalytic reduction of hydrogen peroxide on a palladium-modified carbon paste electrode," *Electroanalysis*, vol. 7, no. 4, pp. 340–345, 1995.

[158] Z. Huang, X. Zhang, M. Reiche, L. Liu, W. Lee, T. Shimizu, S. Senz, and U. Gosele, "Extended arrays of vertically aligned sub-10 nm diameter [100] Si nanowires by metal-assisted chemical etching," *Nano Letters*, vol. 8, no. 9, pp. 3046–3051, 2008.

[159] H. Fang, Y. Wu, J. Zhao, and J. Zhu, "Silver catalysis in the fabrication of silicon nanowire arrays," *Nanotechnology*, vol. 17, no. 15, p. 3768, 2006.

[160] Z. Huang, Y. Wu, H. Fang, N. Deng, T. Ren, and J. Zhu, "Large-scale $Si_{1-x}Ge_x$ quantum dot arrays fabricated by templated catalytic etching," *Nanotechnology*, vol. 17, no. 5, p. 1476, 2006.

[161] K. Peng, J. Hu, Y. Yan, Y. Wu, H. Fang, Y. Xu, S. Lee, and J. Zhu, "Fabrication of single-crystalline silicon nanowires by scratching a silicon surface with catalytic metal particles," *Advanced Functional Materials*, vol. 16, no. 3, pp. 387–394, 2006.

[162] C. Zheng, H. Shen, T. Pu, Y. Jiang, Q. Tang, W. Yang, C. Chen, C. Rui, and Y. Li, "High-efficient solar cells by the Ag/Cu-assisted chemical etching process on diamond-wire-sawn multicrystalline silicon," *IEEE Journal of Photovoltaics*, vol. 7, no. 1, pp. 153–156, 2016.

[163] J. Zha, T. Wang, C. Pan, K. Chen, F. Hu, X. Pi, and X. Su, "Constructing submicron textures on mc-Si solar cells via copper-catalyzed chemical etching," *Applied Physics Letters*, vol. 110, no. 9, p. 093901, 2017.

[164] K. Chen, T. P. Pasanen, V. Vähänissi, and H. Savin, "Effect of MACE parameters on electrical and optical properties of ALD passivated black silicon," *IEEE Journal of Photovoltaics*, vol. 9, no. 4, pp. 974–979, 2019.

[165] Y. Jiang, H. Shen, T. Pu, C. Zheng, Q. Tang, K. Gao, J. Wu, C. Rui, Y. Li, and Y. Liu, "High efficiency multi-crystalline silicon solar cell with inverted pyramid nanostructure," *Solar Energy*, vol. 142, pp. 91–96, 2017.

[166] G. Su, R. Jia, X. Dai, K. Tao, H. Sun, Z. Jin, and X. Liu, "The influence of black silicon morphology modification by acid etching to the properties of diamond wire sawn multicrystalline silicon solar cells," *IEEE Journal of Photovoltaics*, vol. 8, no. 4, pp. 937–942, 2018.

[167] A. Kumagai, "Texturization using metal catalyst wet chemical etching for multicrystalline diamond wire sawn wafer," *Solar Energy Materials and Solar Cells*, vol. 133, pp. 216–222, 2015.

[168] P. Zhang, R. Jia, K. Tao, S. Jiang, X. Dai, H. Sun, Z. Jin, Z. Ji, X. Liu, C. Zhao *et al.*, "The influence of Ag-ion concentration on the performance of mc-Si silicon solar cells textured by metal assisted chemical etching (MACE) method," *Solar Energy Materials and Solar Cells*, vol. 200, p. 109983, 2019.

[169] D. Kumar, S. K. Srivastava, P. Singh, M. Husain, and V. Kumar, "Fabrication of silicon nanowire arrays based solar cell with improved performance," *Solar Energy Materials and Solar Cells*, vol. 95, no. 1, pp. 215–218, 2011.

[170] S. K. Srivastava, D. Kumar, M. Sharma, R. Kumar, P. Singh *et al.*, "Silver catalyzed nano-texturing of silicon surfaces for solar cell applications," *Solar Energy Materials and Solar Cells*, vol. 100, pp. 33–38, 2012.

[171] F. Toor, J. Oh, and H. M. Branz, "Efficient nanostructured blacksilicon solar cell by copper-catalyzed metal-assisted etching," *Progress in Photovoltaics: Research and Applications*, vol. 23, no. 10, pp. 1375–1380, 2015.

[172] J. Oh, H.-C. Yuan, and H. M. Branz, "An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures," *Nature Nanotechnology*, vol. 7, no. 11, p. 743, 2012.

[173] F. Cao, K. Chen, J. Zhang, X. Ye, J. Li, S. Zou, and X. Su, "Next-generation multi-crystalline silicon solar cells: Diamond-wire sawing, nano-texture and high efficiency," *Solar Energy Materials and Solar Cells*, vol. 141, pp. 132–138, 2015.

[174] D. Kane and R. Swanson, "Measurement of the emitter saturation current by a contactless photoconductivity decay method," in *IEEE photovoltaic specialists conference*, 1985, pp. 578–583.

[175] H. Müllejans, W. Zaaiman, and R. Galleano, "Analysis and mitigation of measurement uncertainties in the traceability chain for the calibration of photovoltaic devices," *Measurement Science and Technology*, vol. 20, no. 7, p. 075101, 2009.

[176] S. Bowden and A. Rohatgi, "Rapid and accurate determination of series resistance and fill factor losses in industrial silicon solar cells," in *17th European Photovoltaic Solar Energy Conference, Munich, Germany*, 2001, Retrieved from: <https://iea-pvps.org/snapshot-reports/snapshot-2020/>.

[177] A. Sharma, S. Agarwal, and S. Singh, "Determination of front surface recombination velocity of silicon solar cells using the short-wavelength spectral response," *Solar Energy Materials and Solar Cells*, vol. 91, no. 15-16, pp. 1515–1520, 2007.

[178] A. Sharma, S. Singh, N. S. Bisht, H. Kandpal, and Z. H. Khan, "Effect of air ambient on surface recombination and determination of diffusion length in silicon wafer using photocurrent generation method," *Solar Energy*, vol. 85, no. 5, pp. 1137–1143, 2011.

[179] H. Kampwerth, T. Trupke, J. Weber, and Y. Augarten, "Advanced luminescence based effective series resistance imaging of silicon solar cells," *Applied Physics Letters*, vol. 93, no. 20, p. 202102, 2008.

[180] A. Stapf, P. Nattrodt, C. Gondek, and E. Kroke, "Etching SiC-slurry and diamond wire-sawn silicon wafers with HF-HCl-Cl_2 mixtures: Parameter influences on etch rates and surface structures," *Physica Status Solidi (a)*, vol. 214, no. 10, p. 1700152, 2017.

[181] J. Giesecke, M. Schubert, B. Michl, F. Schindler, and W. Warta, "Minority carrier lifetime imaging of silicon wafers calibrated by quasi-steady-state photoluminescence," *Solar Energy Materials and Solar Cells*, vol. 95, no. 3, pp. 1011–1018, 2011.

[182] H. Robbins and B. Schwartz, "Chemical etching of silicon: I," *Journal of the Electrochemical Society*, vol. 106, no. 6, pp. 505–508, 1959.

[183] E. Abel and H. Schmidt, "Kinetics of nitrous acid III, kinetics of the decomposition of nitrous acid," *International Journal of Research in Physical Chemistry and Chemical Physics*, vol. 134, p. 279, 1928.

[184] M. Steinert, J. Acker, A. Henßge, and K. Wetzig, "Experimental studies on the mechanism of wet chemical etching of silicon in HF/HNO_3 mixtures," *Journal of the Electrochemical Society*, vol. 152, no. 12, pp. C843–C850, 2005.

[185] P. Allongue, V. Kieling, and H. Gerischer, "Etching mechanism and atomic structure of H-Si (111) surfaces prepared in NH_4F," *Electrochimica Acta*, vol. 40, no. 10, pp. 1353–1360, 1995.

[186] K. W. Kolasinski, "Etching of silicon in fluoride solutions," *Surface Science*, vol. 603, no. 10-12, pp. 1904–1911, 2009.

[187] F. Li, M. K. Balazs, and S. Anderson, "Effects of ambient and dissolved oxygen concentration in ultrapure water on initial growth of native oxide on a silicon (100) surface," *Journal of the Electrochemical Society*, vol. 152, no. 8, pp. G669–G673, 2005.

[188] H. Gerischer and W. Mindt, "The mechanisms of the decomposition of semiconductors by electrochemical oxidation and reduction," *Electrochimica Acta*, vol. 13, no. 6, pp. 1329–1341, 1968.

[189] L. Koker and K. W. Kolasinski, "Laser-assisted formation of porous Si in diverse fluoride solutions: Reaction kinetics and mechanistic implications," *The Journal of Physical Chemistry B*, vol. 105, no. 18, pp. 3864–3871, 2001.

[190] E. S. Kooij and D. Vanmaekelbergh, "Catalysis and pore initiation in the anodic dissolution of silicon in HF," *Journal of the Electrochemical Society*, vol. 144, no. 4, pp. 1296–1301, 1997.

[191] J. van Mölken, U. Yusufoğlu, A. Safiei, H. Windgassen, R. Khandelwal, T. Pletzer, and H. Kurz, "Impact of micro-cracks on the degradation of solar cell performance based on two-diode model parameters," *Energy Procedia*, vol. 27, pp. 167–172, 2012.

[192] M. Demant, M. Oswald, T. Welschehold, S. Nold, S. Bartsch, S. Schoenfelder, and S. Rein, "Micro-cracks in silicon wafers and solar cells: Detection and rating of mechanical strength and electrical quality," in *29^{th} Solar Energy Conference and Exhibition*, 2014, pp. 390–396.

[193] A. Khanna, P. K. Basu, A. Filipovic, V. Shanmugam, C. Schmiga, A. G. Aberle, and T. Mueller, "Influence of random pyramid surface texture on silver screen-printed contact formation for monocrystalline silicon wafer solar cells," *Solar Energy Materials and Solar Cells*, vol. 132, pp. 589–596, 2015.

[194] V. Shanmugam, J. Cunnusamy, A. Khanna, P. K. Basu, Y. Zhang, C. Chen, A. F. Stassen, M. B. Boreland, T. Mueller, B. Hoex *et al.*, "Electrical and microstructural analysis of contact formation on lightly doped phosphorus emitters using thick-film Ag screen printing pastes," *IEEE Journal of Photovoltaics*, vol. 4, no. 1, pp. 168–174, 2014.

[195] I. B. Cooper, K. Tate, J. S. Renshaw, A. F. Carroll, K. R. Mikeska, R. C. Reedy, and A. Rohatgi, "Investigation of the mechanism resulting in low resistance Ag thick-film contact to Si solar cells in the context of emitter doping density and contact firing for current-generation ag paste," *IEEE Journal of Photovoltaics*, vol. 4, no. 1, pp. 134–141, 2014.

[196] A. Kalio, A. Richter, C. Schmiga, M. Glatthaar, and J. Wilde, "Study of dielectric layers for bifacial n-type silicon solar cells with regard to optical properties, surface passivation quality, and contact formation," *IEEE Journal of Photovoltaics*, vol. 4, no. 2, pp. 575–580, 2014.

[197] M. Hörteis, T. Gutberlet, A. Reller, and S. W. Glunz, "High-temperature contact formation on n-type silicon: basic reactions and contact model for seed-layer contacts," *Advanced Functional Materials*, vol. 20, no. 3, pp. 476–484, 2010.

[198] M. M. Hilali, K. Nakayashiki, C. Khadilkar, R. C. Reedy, A. Rohatgi, A. Shaikh, S. Kim, and S. Sridharan, "Effect of Ag particle size in thick-film Ag paste on the electrical and physical properties of screen printed contacts and silicon solar cells," *Journal of the Electrochemical Society*, vol. 153, no. 1, pp. A5–A11, 2006.

[199] C. Jiang, Z. Li, H. Moutinho, L. Liang, A. Ionkin, and M. Al-Jassim, "The effect of front-side silver metallization on underlying n^+-p junction in multicrystalline silicon solar cells," in *38th IEEE Photovoltaic Specialists Conference*, 2012, pp. 003 365–003 370.

[200] X. Dai, R. Jia, G. Su, H. Sun, K. Tao, C. Zhang, P. Zhang, Z. Jin, and X. Liu, "The influence of surface structure on diffusion and passivation in multicrystalline silicon solar cells textured by metal assisted chemical etching (MACE) method," *Solar Energy Materials and Solar Cells*, vol. 186, pp. 42–49, 2018.

[201] S. K. Srivastava, P. Singh, A. Srivastava, P. Prathap, S. Kumar, C. Rauthan, and D. Aswal, "Nanostructured black silicon for efficient thin silicon solar cells: Potential and challenges," in *Recent Advances in Thin Films*. Springer, 2020, pp. 549–623.

[202] Y. Zhao, Y. Liu, W. Chen, J. Wu, Q. Chen, H. Tang, Y. Wang, and X. Du, "Regulation of surface texturization through copper-assisted chemical etching for silicon solar cells," *Solar Energy*, vol. 201, pp. 461–468, 2020.

[203] R. Tong, W. Zhang, X. Ke, D. Liu, and Z. Zhang, "Influence of surface structure on the performance of mono-like Si PERC solar cell," *Materials Science in Semiconductor Processing*, vol. 126, p. 105662.

[204] B. Hallam, B. Tjahjono, T. Trupke, and S. Wenham, "Photoluminescence imaging for determining the spatially resolved implied open circuit voltage of silicon solar cells," *Journal of Applied Physics*, vol. 115, no. 4, p. 044901, 2014.

[205] A. Khanna, T. Mueller, R. A. Stangl, B. Hoex, P. K. Basu, and A. G. Aberle, "A fill factor loss analysis method for silicon wafer solar cells," *IEEE Journal of Photovoltaics*, vol. 3, no. 4, pp. 1170–1177, 2013.

[206] O. Breitenstein, "Nondestructive local analysis of current–voltage characteristics of solar cells by lock-in thermography," *Solar Energy Materials and Solar Cells*, vol. 95, no. 10, pp. 2933–2936, 2011.

[207] S. Rißland and O. Breitenstein, "Evaluation of recombination velocities of grain boundaries measured by high resolution lock-in thermography," *Energy Procedia*, vol. 38, pp. 161–166, 2013.

[208] O. Breitenstein and D. Sontag, "Lock-in thermography based local solar cell analysis for high efficiency monocrystalline hetero junction type solar cells," *Solar Energy Materials and Solar Cells*, vol. 193, pp. 157–162, 2019.

[209] P. K. Basu, A. Khanna, and Z. Hameiri, "The effect of front pyramid heights on the efficiency of homogeneously textured inline-diffused screen-printed monocrystalline silicon wafer solar cells," *Renewable Energy*, vol. 78, pp. 590–598, 2015.

[210] J. Chen, Z. R. Du, F. Ma, F. Lin, D. Sarangi, B. Hoex, and A. G. Aberle, "Accurate extraction of the series resistance of aluminum local back surface field silicon wafer solar cells," *Solar Energy Materials and Solar Cells*, vol. 133, pp. 113–118, 2015.

[211] S. Behera, K. Sreejith, A. Khan, S. Kumbhar, A. Kottantharayil, P. K. Basu, and A. K. Sharma, "Optimization of front metal contact design of industrial Si solar cells using photoluminescence imaging technique," *Materials Today: Proceedings*, vol. 39, pp. 1925–1929, 2021.

[212] G. Schubert, F. Huster, and P. Fath, "Physical understanding of printed thick-film front contacts of crystalline Si solar cellsreview of existing models and recent developments," *Solar Energy Materials and Solar Cells*, vol. 90, no. 18-19, pp. 3399–3406, 2006.

[213] C. Ballif, D. Huljić, G. Willeke, and A. Hessler-Wyser, "Silver thick-film contacts on highly doped n-type silicon emitters: structural and electronic properties of the interface," *Applied Physics Letters*, vol. 82, no. 12, pp. 1878–1880, 2003.

[214] C.-H. Lin, S.-Y. Tsai, S.-P. Hsu, and M.-H. Hsieh, "Investigation of Ag-bulk/glassy-phase/Si heterostructures of printed Ag contacts on crystalline Si solar cells," *Solar Energy Materials and Solar Cells*, vol. 92, no. 9, pp. 1011–1015, 2008.

[215] Z. Li, L. Liang, A. Ionkin, B. Fish, M. Lewittes, L. Cheng, and K. Mikeska, "Microstructural comparison of silicon solar cells front-side Ag contact and the evolution of current conduction mechanisms," *Journal of Applied Physics*, vol. 110, no. 7, p. 074304, 2011.

[216] V. Shanmugam, J. Cunnusamy, A. Khanna, P. K. Basu, Y. Zhang, C. Chen, A. F. Stassen, M. B. Boreland, T. Mueller, B. Hoex *et al.*, "Electrical and microstructural analysis of contact formation on lightly doped phosphorus emitters using thick-

film Ag screen printing pastes," *IEEE Journal of Photovoltaics*, vol. 4, no. 1, pp. 168–174, 2013.

[217] J. Qin, W. Zhang, S. Bai, and Z. Liu, "Study on the sintering and contact formation process of silver front side metallization pastes for crystalline silicon solar cells," *Applied Surface Science*, vol. 376, pp. 52–61, 2016.

[218] P. Ferrada, C. Portillo, E. Cabrera, R. Kopecek, M. Poncebustos, M. Kogan, V. Del Campo, and E. Fuentealba, "Selective chemical etching for studying the front side contact in thick film screen printed crystalline p-type silicon solar cells," *Journal of the Chilean Chemical Society*, vol. 60, no. 2, pp. 2905–2910, 2015.

[219] J. M. Gee, W. K. Schubert, H. L. Tardy, T. D. Hund, and G. Robison, "The effect of encapsulation on the reflectance of photovoltaic modules using textured multicrystalline-silicon solar cells," in *Proceedings of 1st IEEE World Conference on Photovoltaic Energy Conversion-WCPEC (A Joint Conference of PVSC, PVSEC and PSEC)*, vol. 2, 1994, pp. 1555–1558.

[220] J. Y. Yang, Y. K. Ahn, P. H. Huh, J. G. Nam, M. Park, M. G. Kim, J. Y. Lee, Y. G. Ji, and D. S. Kim, "Research on decrease of cell to module loss for crystalline silicon photovoltaic module," *Journal of Renewable and Sustainable Energy*, vol. 5, no. 5, p. 052003, 2013.

[221] I. Haedrich, U. Eitner, M. Wiese, and H. Wirth, "Unified methodology for determining CTM ratios: Systematic prediction of module power," *Solar Energy Materials and Solar Cells*, vol. 131, pp. 14–23, 2014.

[222] T.-h. Jung, H.-e. Song, H.-k. Ahn, and G.-h. Kang, "A mathematical model for cell-to-module conversion considering mismatching solar cells and the resistance of the interconnection ribbon," *Solar Energy*, vol. 103, pp. 253–262, 2014.

[223] M. H. Saw, Y. S. Khoo, J. P. Singh, and Y. Wang, "Cell-to-module optical loss/gain analysis for various photovoltaic module materials through systematic characterization," *Japanese Journal of Applied Physics*, vol. 56, no. 8S2, p. 08MD03, 2017.

[224] S. C. Baker-Finch and K. R. McIntosh, "Reflection of normally incident light from silicon solar cells with pyramidal texture," *Progress in Photovoltaics: Research and Applications*, vol. 19, no. 4, pp. 406–416, 2011.

[225] S. C. Baker-Finch, K. R. McIntosh, and M. L. Terry, "Isotextured silicon solar cell analysis and modeling 1: Optics," *IEEE Journal of Photovoltaics*, vol. 2, no. 4, pp. 457–464, 2012.

[226] J. Greulich, A.-K. Volk, N. Wöhrle, I. Haedrich, M. Wiese, M. Hermle, and S. Rein, "Optical simulation and analysis of iso-textured silicon solar cells and modules including light trapping," *Energy Procedia*, vol. 77, pp. 69–74, 2015.

[227] K. R. McIntosh, M. D. Abbott, and B. A. Sudbury, "Ray tracing isotextured solar cells," *Energy Procedia*, vol. 92, pp. 122–129, 2016.

[228] K. R. McIntosh, T. G. Allen, S. C. Baker-Finch, and M. D. Abbott, "Light trapping in isotextured silicon wafers," *IEEE Journal of Photovoltaics*, vol. 7, no. 1, pp. 110–117, 2016.

[229] E. Shaaban, "Calculation of the optical constants of amorphous semiconducting $As_{40}S_{60}$, $As_{40}S_{35}Se_{25}$ and $As_{40}Se_{60}$ thin films from transmittance and reflectance measurements," *Journal of Applied Sciences*, vol. 6, no. 2, pp. 340–346, 2006.

[230] D. C. Look and J. H. Leach, "On the accurate determination of absorption coefficient from reflectance and transmittance measurements: Application to Fe-doped GaN," *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 34, no. 4, p. 04J105, 2016.

[231] S. C. Baker-Finch, *Rules and tools for understanding, modelling and designing textured silicon solar cells*. Ph. D thesis, The Australian National University, March 2012.

[232] H. Deckman and J. Dunsmuir, "Natural lithography," *Applied Physics Letters*, vol. 41, no. 4, pp. 377–379, 1982.

[233] Y. Wang, L. Yang, Y. Liu, Z. Mei, W. Chen, J. Li, H. Liang, A. Kuznetsov, and D. Xiaolong, "Maskless inverted pyramid texturization of silicon," *Scientific Reports*, vol. 5, p. 10843, 2015.

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