Investigation of Junction-Less Transistor (JLT) for CMOS Scaling

A thesis submitted in partial fulfillment of
the requirements for the degree of

Doctor of Philosophy

by

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To my family.

Thesis Approval

The thesis entitled

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CERTIFICATE OF COURSE WORK

This is to certify that **Suresh Gundapaneni** (Roll No. 08407602) was admitted to the candidacy of Ph.D. degree on Jul 2008, after successfully completing all the courses required for the Ph.D. programme. The details of the course work done are given below.

S.No	Course Code	Course Name	Credits
1	EE 661	Physical Electronics	6
2	EE 669	VLSI Technology	6
3	EE 671	VLSI Design	6
4	EE 705	VLSI Design lab	6
5	EE 721	Hardware Description	6
6	EE 620	Physics of Transistors	6
7	EE 666	High power semiconductor devices	6
8	EE 668	System Design	6
9	EE 672	Microelectronics lab	6
10	EES 801	Seminar	4
11	HS 699	Communication and Presentation Skills	PP
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DECLARATION

I declare that this written submission represents my ideas in my own words and where others ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that Chapter 2 of this thesis contain the work that we have published in *IEEE Electron Device Letters,* vol. 32, no. 3, pp. 261 263, 2011, Chapter 3 contain the work we published in *IEEE Electron Device Letters,* vol. 32, no. 10, pp. 1325-1327, 2011, Chapter 5 contains the work we published in *IEEE Transactions on Electron Devices,* vol. 59, no. 4, pp. 1023-1029, 2012 and Chapter 6 contain the joint work done along with Mr. Naveen Kumar Neelapala.

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IIT Bombay **Suresh Gundapaneni**

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Abstract

As its channel scales down to the sub-20nm regime, the conventional metal oxide semiconductor (MOS) Field Effect Transistor (FET) requires super-steep doping profiles at the source-channel and channel-drain junctions. Device architectures that do not have any junctions in the source-channel-drain path will therefore be of interest for scaling to ultra short channel lengths.

We propose a novel highly scalable source-drain-junction free FET which we call the Bulk Planar Junction-Less Transistor (BPJLT). This builds upon the idea of an isolated ultra-thin highly-doped device layer whose volume is fully depleted in the OFF state and is around flat-band in the ON state. Here the leakage current depends on the effective device layer thickness, and we show that with well doping and/or well bias, this can be controllably made less than the physical device layer thickness in a bulk planar junction-isolated structure. We demonstrate by extensive device simulations that these additional knobs for controlling short-channel-effects (SCEs) reduce the OFF state leakage current by orders of magnitude for similar ON state currents, making the BPJLT highly scalable.

We also propose the use of high-κ spacer to improve the electrostatic integrity and thereby the scalability of silicon junctionless transistors (JLTs) and BPJLTs for the first time. Using extensive simulations of n-channel JLTs and BPJLTs, we demonstrate that the high-κ spacers improve the electrostatic integrity of JLTs and BPJLTs at sub 22nm gate lengths. Electric field that fringes through the high-κ spacer to the device layer on either sides of the gate result in an effective increase of electrical gate length in OFF state. However the effective gate length is unaffected in the ON state. Hence, the OFF state leakage current is reduced by several orders of magnitude with the use of high-κ spacer with concomitant improvements in subthreshold swing and drain induced barrier lowering. A marginal improvement in ON state current is observed with the use of high-κ spacer and this is related to the reduction in parasitic resistance in the silicon under the spacer due to fringe fields. We observe the static power consumption to be lowered by orders of magnitude with the use of high-κ spacers. However, an increased delay

with high-κ spacers suggests the usage to be limited to low standby power applications, a zone where JLT can be a potential alternative.

We evaluate the effect of quantum confinement on the ON state characteristics and the effect of band-to-band tunneling along the channel on the OFF state characteristics of n-channel JLTs for the first time. In the ON state, we solve the coupled Schrödinger-Poisson equations and based on the total integrated electron density in the confinement direction, we show that the performance of junctionless transistors would degrade due to the quantization effects in the ON state, i.e. flat band condition. However the degradation is significantly smaller in comparison with the fully depleted inversion mode MOSFET.

In the OFF state, we evaluate the impact of band-to-band tunneling along the channel on characteristics of n-channel JLTs for the first time. The JLT has a heavily doped channel which is fully depleted in the OFF state. This results in a significant band overlap between the channel and drain regions - and thereby a large band-to-band tunneling of electrons from the channel to drain in an n-channel JLT. This leads to a non-negligible increase in the OFF state leakage current. In case of n-channel devices, tunneling of electrons from the valence band of the channel to the conduction band of drain would leave behind holes in the channel, which would raise the channel potential and thereby trigger the parasitic bipolar junction transistor (BJT) formed by the source, channel and drain regions induced in a JLT in OFF state. Tunneling current is observed to be a strong function of the drain voltage, silicon body thickness and doping of a JLT and hence we present guidelines to optimize the device for high ON to OFF current ratio. The dependence of tunneling current on the drain voltage suggests that the JLT may be more useful for low power applications. Finally it is shown that the bulk planar JLT we have proposed has significantly lower leakage than its SOI counterpart.

We have developed the process flow for the fabrication of poly-Si channel junctionless transistor with poly-Si gate which if further developed can be potentially suitable display applications.

Contents

List of Tables

List of Figures

Nomenclature

AMAT	Applied Materials
BHF	Buffered hydrofluoric acid
BJT	Bipolar junction transistor
BPJLT	Bulk planar junctionless transistor
BTBT	Band to band tunneling
CEN	Centre of excellence in nanoelectronics
CMOS	Complementary metal oxide semiconductor
DIBL	Drain induced barrier lowering
DSA	Double side aligner
EOT	Effective oxide thickness
ETSOI	Extremely thin silicon on insulator
FDDG	Fully depleted double gate
GAA	Gate all around
GeOI	Germanium on insulator
GIDL	Gate induced drain leakage
HP	High performance
ICPCVD	Inductively coupled plasma chemical vapor deposition

IPA	Isopropyl alcohol
ITO	Indium tin oxide
JLT	Junctionless transistor
LOP	Low operating power
LPCVD	Low pressure chemical vapor deposition
LSP	Low standby power
LTO	Low temperature oxide
MOSFET	Metal oxide semiconductor field effect transistor
PVD	Physical vapour deposition
RCA	Radio corporation of America
RF	Radio frequency
RIE	Reactive ion etching
RTP	Rapid thermal processing
SCE	Short channel effects
SEM	Scanning electron microscope
SOI	Silicon on insulator
SS	Subthreshold swing
TEM	Transmission electron microscope
VeSFET	Vertical slit field effect transistor

Chapter 1

Introduction

Complementary metal oxide semiconductor (CMOS) technology revolutionized the human life style for more than four decades. It would have been hard to think of life today with out silicon CMOS technology. The CMOS technology had advanced with a double the number of on-chip transistors every generation, reducing the physical device size. A smaller sized transistor comes with an advantage of improved performance and packing density. This is referred as scaling and had enabled the Moore's law to happen [1].

Continued scaling of CMOS technology has now reached to the atomic scale dimensions, in order to serve the next generation low standby power (LSP), low operating power (LOP) and high performance (HP) requirements. While the often referred short channel effects (SCEs) like drain induced barrier lowering (DIBL), gate induced drain leakage (GIDL), gate tunneling leakages and leakage current problems are challenging on one side, realizing the transistor for the next generations itself have become a much more challenging task [2]. This is because of the ultra-steep doping profile requirements at the source-drain junctions.

1.1 Conventional MOSFET

Metal oxide semiconductor field effect transistor (MOSFET) is a four terminal semiconductor device. The schematic of this device is shown in Fig. 1.1. It has five regions viz., source, drain, channel, gate and gate dielectric. The source and drain regions are doped with an impurity that is complementary to that of the channel. For example, in an n-channel MOSFET, the source and drain regions are doped with n-type impurity and the channel is p-type doped. Usually, in the traditional MOSFET, the workfunction of the gate material is similar to that of

the source/drain regions. For n-channel operation the drain is biased at a higher potential with respect to the source. When no bias is applied to the gate terminal, the current between source and drain is very small due to the high potential barrier for electrons between source and channel - this is called the OFF state of the transistor. When a positive bias is applied on the gate terminal, the minority carriers in the substrate gets attracted towards the channel surface due to the electric field developed across the gate dielectric (hence, the field effect). The accumulation of minority carriers in the channel, inverts the type of free carriers available near the surface of the channel. Hence, this state is called inversion. The inverted channel acts as a conducting layer between the source and drain. Hence a high current starts to flow between the source and drain - this is called the ON state of the transistor. The ON and OFF states described here together makes the MOSFET to act as a switch. The ideal switching behaviour one would like to have is shown in Fig. 1.2. When the voltage applied at the control gate is less than some pre-defined threshold voltage (V_T), the switch should be OFF, i.e., the current should be zero and once the control gate voltage is above V_T, the device should be ON with a finite amount of current (indicated as I_{ON}), between source and drain. However, the MOSFET can not achieve an ideal switching behaviour. The current versus voltage transfer characteristics of MOSFET looks like shown in Fig. 1.3. Normally for n-channel operation the gate is operated in the positive voltage regime. The region of gate to source voltages (V_{GS}) between 0V and V_T is called the subthreshold region where the current increases exponentially with gate voltage. The above-threshold region is for gate voltage greater than V_T. Depending on the bias applied to the drain, the MOSFET is said to operate in either saturation region (for high drain to source voltage) or in linear region (for a low drain to source voltage). For a very low or negative bias at the gate, the current tends to increase due to an affect called as gate induced drain leakage (GIDL), which will be explained in detail in subsequent sections.

1.2 Short channel effects in a scaled transistor

In Fig. 1.4 shows the typical I_D versus V_{GS} characteristics of short and long channel devices. It can be clearly observed that the OFF current increases drastically in a short channel device. Along with this, lowering of V_T, large V_T variation with drain bias, reduced slope of transfer characteristics in the sub-threshold region, etc., are observed in short channel devices compared to a long channel device. All of these are extremely undesirable factors, collectively

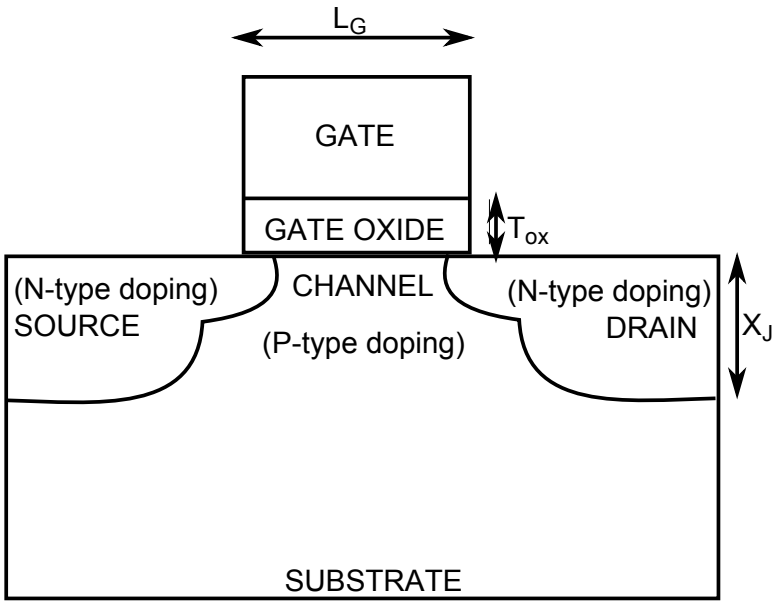


Figure 1.1: Schematic of the conventional metal oxide semiconductor field effect transistor (MOSFET)

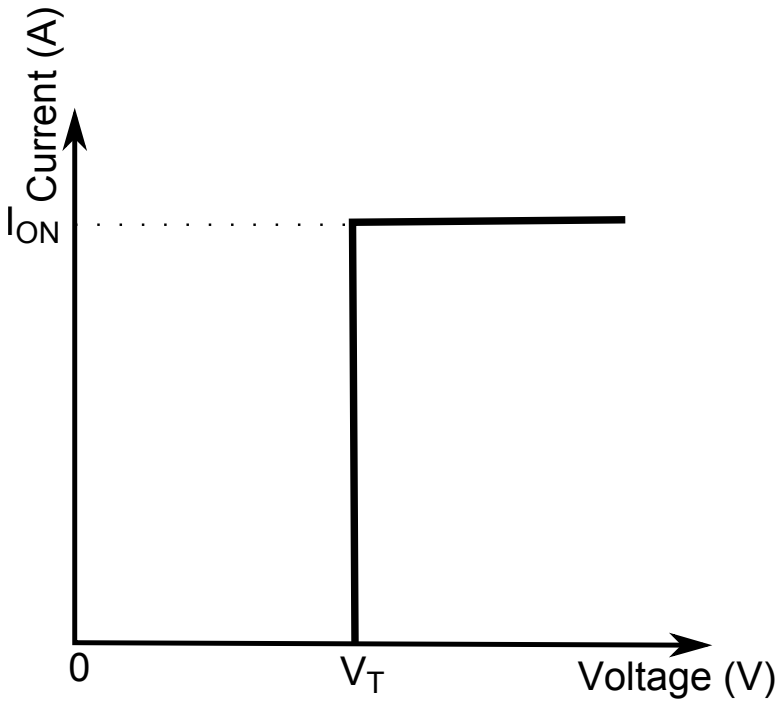


Figure 1.2: Current versus voltage plot of an ideal switch.

known as short channel effects and need to be addressed. We explain in details each of the short channel effects below.

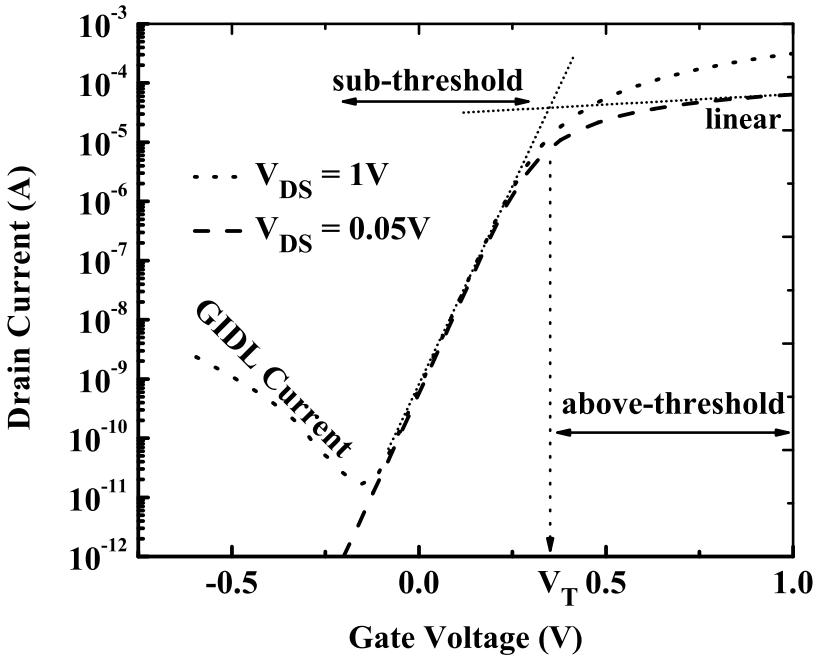


Figure 1.3: Typical drain current versus gate voltage plot of a MOSFET. The plot shown is for a L_G of 250nm, just to illustrate the regions of MOSFET transfer characteristics.

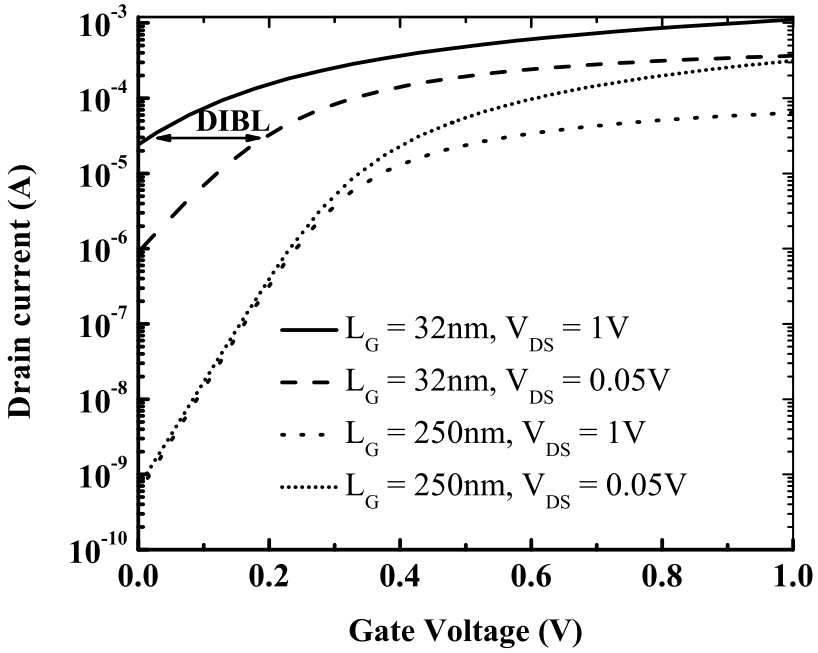


Figure 1.4: Typical drain current versus gate voltage plot of a short channel (L_G =32nm) and a long channel (L_G=250nm) MOSFET.

1.2.1 Sub-threshold swing

Sub-threshold swing (SS) is defined as the variation in the gate voltage required to have a decade variation in current. For a MOSFET this is given by the following equation [5]:

$$SS = (kT/q) * ln(10) * (1 + (C_D/Cox)) \tag{1.1}$$

where, T is the temperature in degrees kelvin, q is the charge of electron, C_D is the depletion capacitance, Cox is the gate oxide capacitance. Even if we neglect the second term as it is far less than 1 (i.e., when $Cox \gg C_D$), SS is limited by the first term to 60 mV/Decade. Higher SS means that the device can have a fewer orders of change in drain current from the OFF state to the V_T, which in turn means a higher OFF current for a given V_T.

1.2.2 Drain Induced Barrier Lowering (DIBL)

Ideally, we need to operate the MOSFET in 1-D mode, i.e., only gate voltage controlling the current of the device. But, as the channel lengths are going small, the drain starts to behave as a second gate, i.e., I_D is not only controlled by the gate voltage but is also controlled by the drain voltage[3, 4]. This is called as the 2-D behaviour of the transistor. In a long channel device any increase in V_{DS} is accounted by lowering the band only in the drain side. As the channel length is decreased this increase in V_{DS} account in lowering the source to channel barrier (which should be actually controlled by the gate)[6]. An example for this is shown in Fig. 1.5, where only the conduction band edge is shown along the source-channel-drain for 32nm and 250nm gate length devices. It can be observed that the source-channel barrier is lowered significantly for a 32nm device compared to a 250nm MOSFET. Effect of DIBL is noticed in the transfer characteristics as a decrease in threshold voltage as shown in Fig. 1.4. This also results in the non-saturation behaviour of the transistor (I_D keeps on increasing with V_{DS}). Low V_T again leads to an increase of OFF current. However there will be an increase in ON current of the transistor, but the increase in ON current is not as high as the increase in OFF current, hence degrading the ON/OFF current ratio of the device. There are several ways to address DIBL [5] like (a) Increase the gate control by decreasing the oxide thickness, which in turn increases the direct tunneling current through the gate oxide. and (b) By increasing the substrate doping, which in turn keeps the source and drain apart (with less coupling) by decreasing the depletion

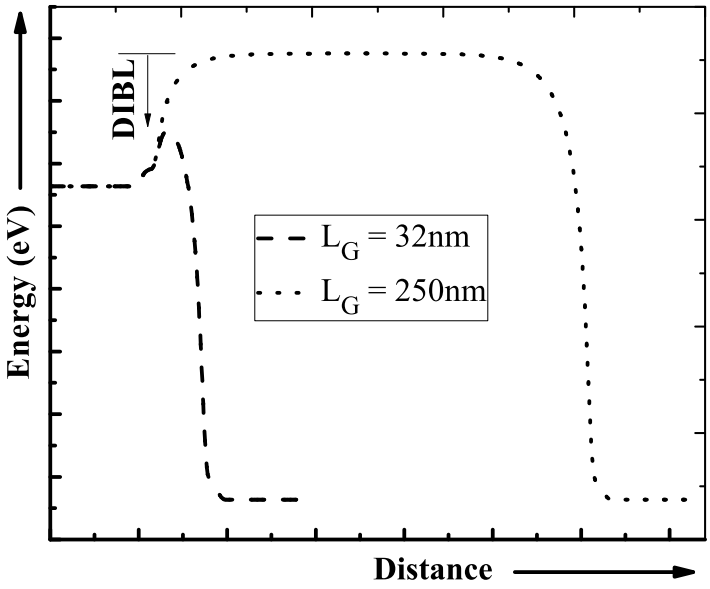


Figure 1.5: Conduction band edge along the source-channel-drain for a short channel (L_G =32nm) and a long channel (L_G=250nm) MOSFET.

region widths. (c) By using a different material which has a lower dielectric constant instead of Si, so that the drain coupling to the source is reduced.

1.2.3 Channel length modulation

When the drain voltage becomes more than the gate overdrive, there will be pinch off occurring towards the drain end by a length of $\triangle L_G$ [5, 7] as shown in Fig. 1.6.

There will be an I_D variation due to this given as [5]:

$$I_D = I_{Dsat}/(1 - \triangle L_G/L_G) \tag{1.2}$$

In a long channel device this $\triangle L_G$ is not much significant compared to the L_G. But, in a short channel device this becomes significant and will be a function of V_{DS}. The device shows a non-saturation behaviour which in turn reduces V_T there by the ON/OFF current ratio. Here V_T is a strong function of L_G and decreases significantly at lower channel lengths [5, 8]. This is often termed in literature as V_T-roll off with L_G.

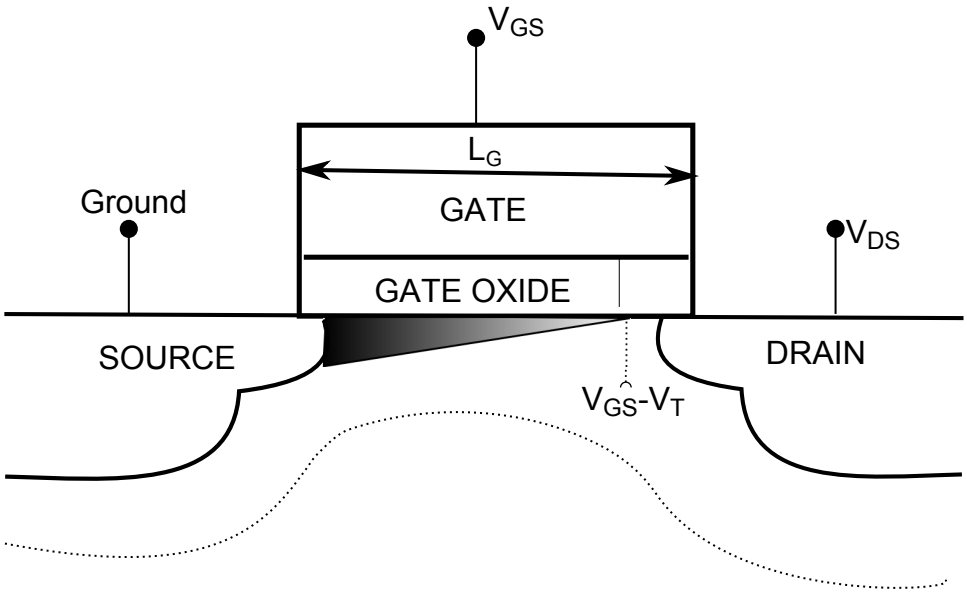


Figure 1.6: Schematic illustrating the channel length modulation affect. It can be seen here that when the drain voltage applied is above V_{GS}-V_T, the drain side of the channel is pinched-off resulting in channel length modulation.

1.2.4 Velocity saturation

The velocity of carriers is known to saturate due to mobility saturation at higher electric fields. A constant field scaling (i.e., scaling all parameters equally) would have been helpful to maintain the same electric fields in the scaled down transistor. However, the scaling trend followed by semiconductor industries is not a constant field one[5]. For example, oxide thickness is scaled more and supply voltages are scaled less. This had resulted in an increased electric fields in the nano-scale MOSFET. As electric field increases the velocity gets saturated. This would not have been be a problem if the saturation occurs at drain voltages greater than the gate overdrive. But, in a nano-scale MOSFET, this is observed at lower drain voltages itself, resulting in a decreased ON current (as the current is saturating earlier). We can easily identify weather the saturation is due to velocity saturation or due to V_{DS}, from the I_D-V_{DS} characteristics. If there are equal increments of current for equal increments of gate overdrive then the saturation is due to velocity saturation, whereas if there is a square dependency of I_D on overdrive then it is due to increase in V_{DS} above the gate overdrive [5].

1.2.5 Gate oxide leakage

SiO_2 is a good insulator to be used in the MOS structure. But, when gate oxide thickness is reduced less than 3nm or 2nm, tunneling probability increases and result in an increase of

the oxide leakage current [4, 9]. Using a high-k dielectric is used to solve this problem to some extent, as a high-k dielectric can provide a similar gate electric field even with a physically thick high-k gate dielectric. This can reduce the direct tunneling leakage.

1.2.6 Gate Induced Drain Leakage (GIDL)

Scaling results in an increase of field in oxide as well as in the gate-drain overlap region. For a high drain bias and a low gate bias, the electric field in the gate/drain overlap region is very high. This increase in the field actually depletes the carriers in the drain overlap region as shown in Fig. 1.7 (a). Fig. 1.7(b) shows the band diagram in the vertical direction in the gate/drain overlap region. It can be seen that there is a significant band overlap between the valance band of the drain to the conduction band of the drain in the overlap region. This band overlap triggers band-to-band tunneling between the valance band and conduction band of the drain. The electron and hole pair generated due to band to band tunneling will be swept to the drain and substrate respectively.

1.2.7 Hot carrier effects

After fabricating a certain device there should not be a drift in performance of the device over time. But hot carrier effect leads to the drift over certain period of operation. This is more dominant in short channel devices where the electric field is higher.

The three kinds of possible hot carrier injection mechanisms are illustrated in Fig. 1.8. (a) Carriers generated due to impact ionization on the drain side can multiply and can lead to a heavy substrate current. (b) the carriers having energy higher than the silicon/gate dielectric conduction band offset can lead to a conduction current to the gate. (c) The sufficiently high energy electrons can damage the silicon-gate dielectric interface leading to degradation in important device parameters like drain current, threshold voltage etc. [10, 11]

1.2.8 Statistical Fluctuation of Dopant Atoms

Most widely used doping methods in semiconductors are by ion implantation or by in-situ doping during thin film deposition. The amount of doping in these methods are estimated by pure statistics. In addition, the CMOS processing involves several high temperature anneal steps. The diffusion of dopant in the anneal steps is also based on statistics. When it comes to

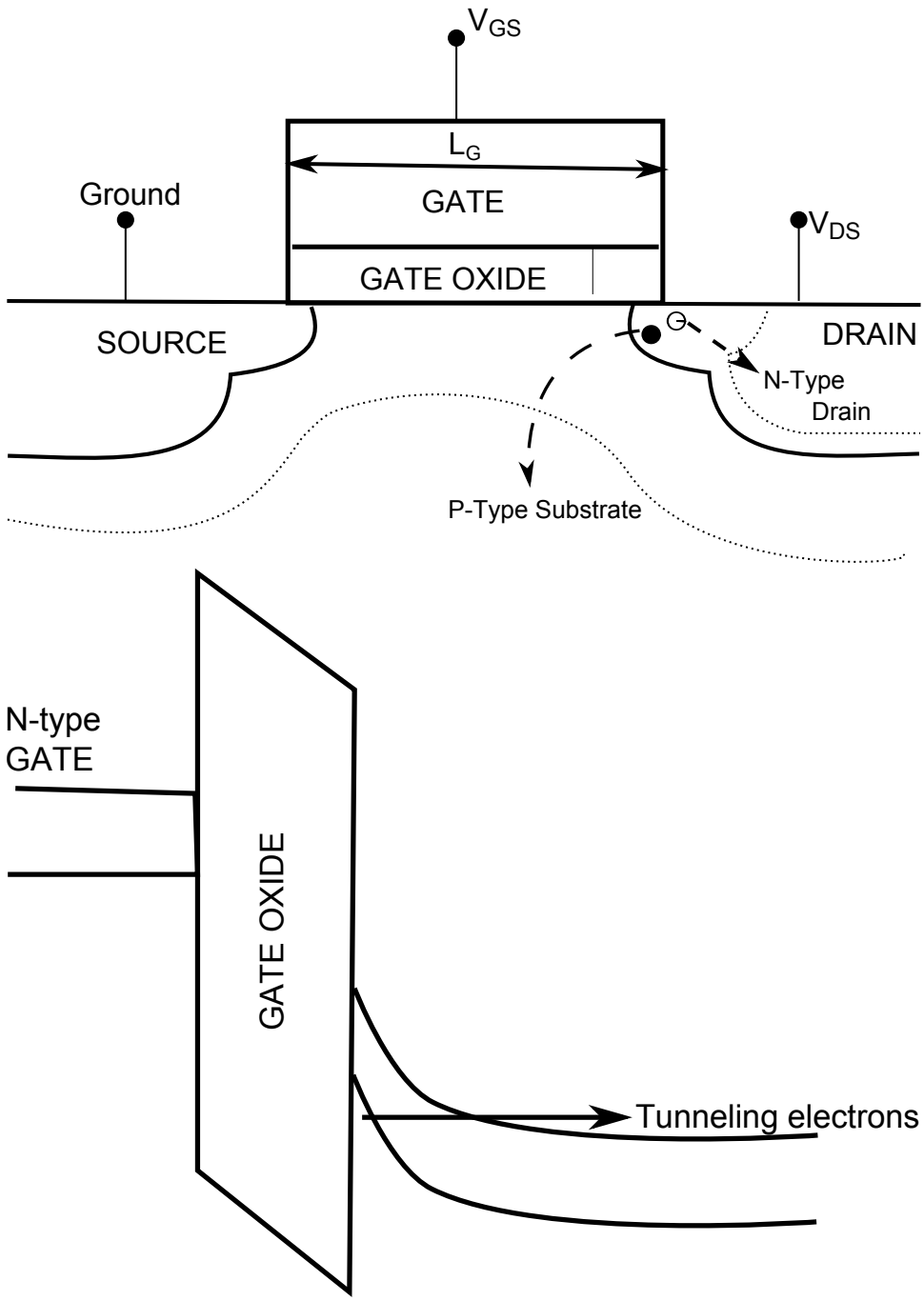


Figure 1.7: Schematic illustrating the Gate Induced Drain Leakage affect. (a) Electron hole pair generation because of tunneling in the gate overlap over the drain. (b) Band diagram in the vertical direction of MOSFET, in the gate overlap region on the drain.

an ultra-scaled device, the volume of the semiconductor in the channel have shrunk down to few atoms and the dopant atoms are only a fraction of these. This makes the magnitude of doping in the channel a highly variable quantity. Also the position of the dopants are random. Both the number and position impact the device variability.

As the channel lengths were scaled down, the doping in the channel was scaled up to im-

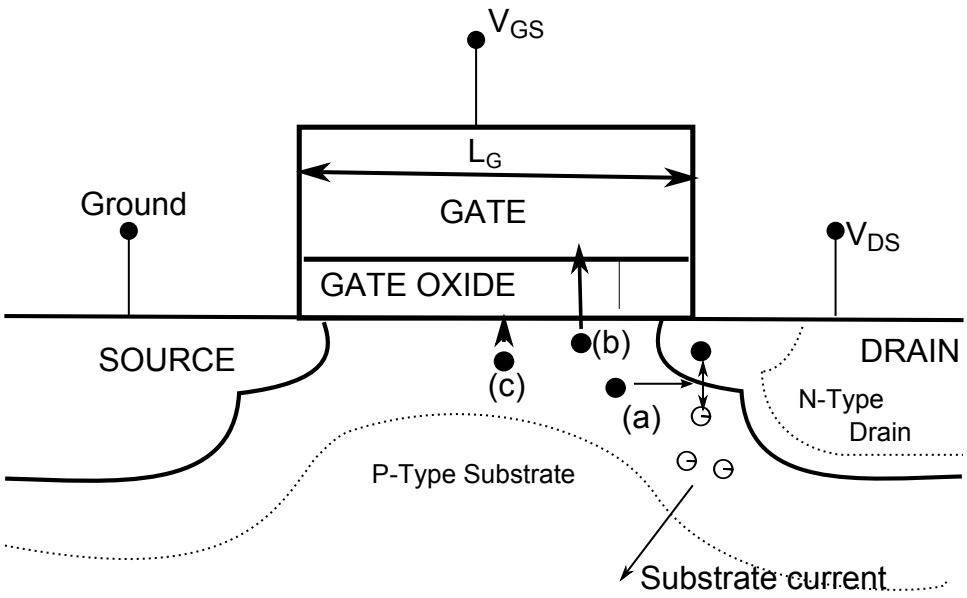


Figure 1.8: Schematic illustrating the hot carrier affects in MOSFETs. See the text in Section 1.2.7 for discussion of processes marked as (a), (b) and (c).

prove the short channel behaviour of the device. This in turn increased the variability of the device. In addition, heavy doping in the channel also degrades the mobility because of scattering. An alternative set of devices, with undoped channels, were brought forward to address the issue of dopant fluctuations. Extremely thin silicon on insulator (ETSOI) and Fin FETs are examples of such devices. Undoped channels have lower variability and improved the mobility when compared to the conventional bulk MOSFETs. Schematic of the ETSOI device structure is shown in Fig. 1.9. However, when the channel lengths are scaled down to sub-20nm regime, these devices also suffer variability due to dopant fluctuations. This is due to the dopant atoms from source/drain diffusing into the channel region. An extremely sharp doping will be necessary to address the issue. One device that can address this issue to some extent is the junctionless transistor.

1.3 Junction-Less Transistor (JLT)

Some of the process challenges for scaling the CMOS devices can be reduced by a device which do not need any junctions and this is the main advantage of junctionless transistor. Unlike the conventional MOSFET, JLTs have heavy channel doping and is fully depleted in the OFF state. For this purpose, a gate metal which has a large workfunction difference to that of the channel is needed. Gate bias need to be applied to bring the channel out-of depletion and to see

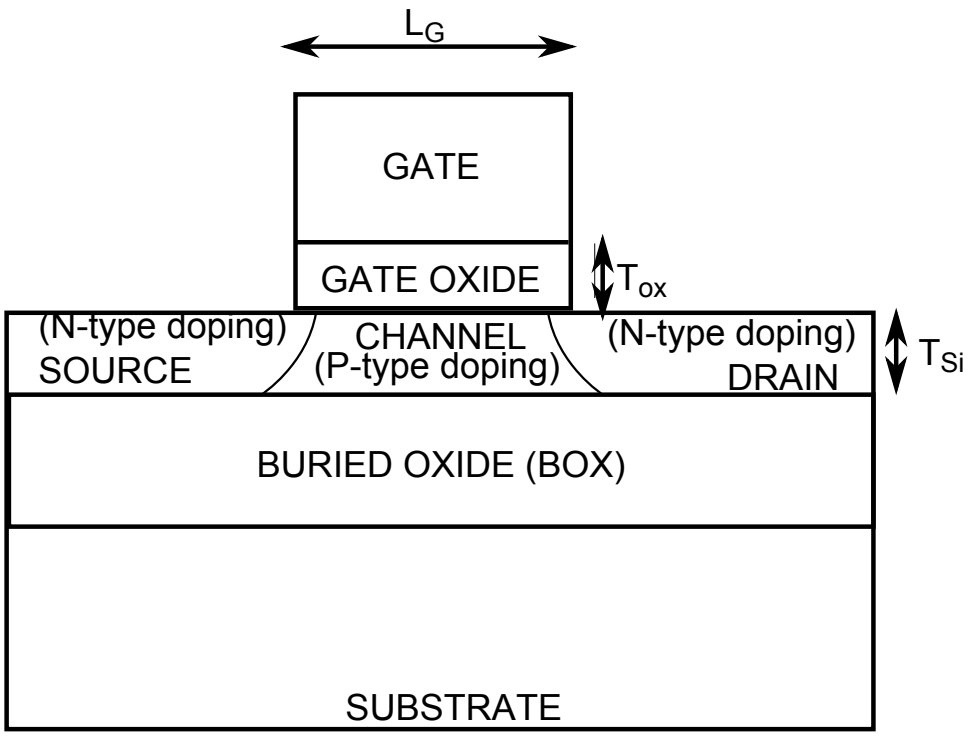


Figure 1.9: Schematic of an extremely thin silicon on insulator (ETSOI) FET.

a conduction between source and drain. As there is a single semiconducting silicon bar with uniform doping from the source to channel, it can be modelled as a resistor whose resistance can by modulated by the gate. However, for a reasonable conductance between source and drain, the doping of the semi-conductor bar need to be very high. On the other hand, the depletion width in a heavily doped semiconductor is very small and this demands an ultra thin silicon body for a JLT.

1.3.1 Theory of junctionless transistors

The schematic representation of junctionless transistor is shown in Fig. 1.10. It can be seen that for an n-channel operation, the source, channel and drain are of n-type doping and the gate is of a p-type workfunction ($\sim$ 5.1 eV). Since the workfunction difference between the n-type channel and the p-type gate is of $\sim$ 1eV, there is a depletion in the channel, where the depletion is decided by the doping of the channel region (thin depletion width for high doping and vice-versa). Channel can be made fully depleted by choosing an extremely thin channel and low channel doping in the range of 10nm and 10^{19} respectively. Once the channel is fully depleted, the current between the source and drain becomes very small. As shown in the I_D-V_{DS} characteristics in Fig. 1.11 the current is very small when the gate is at 0V. Also, it can

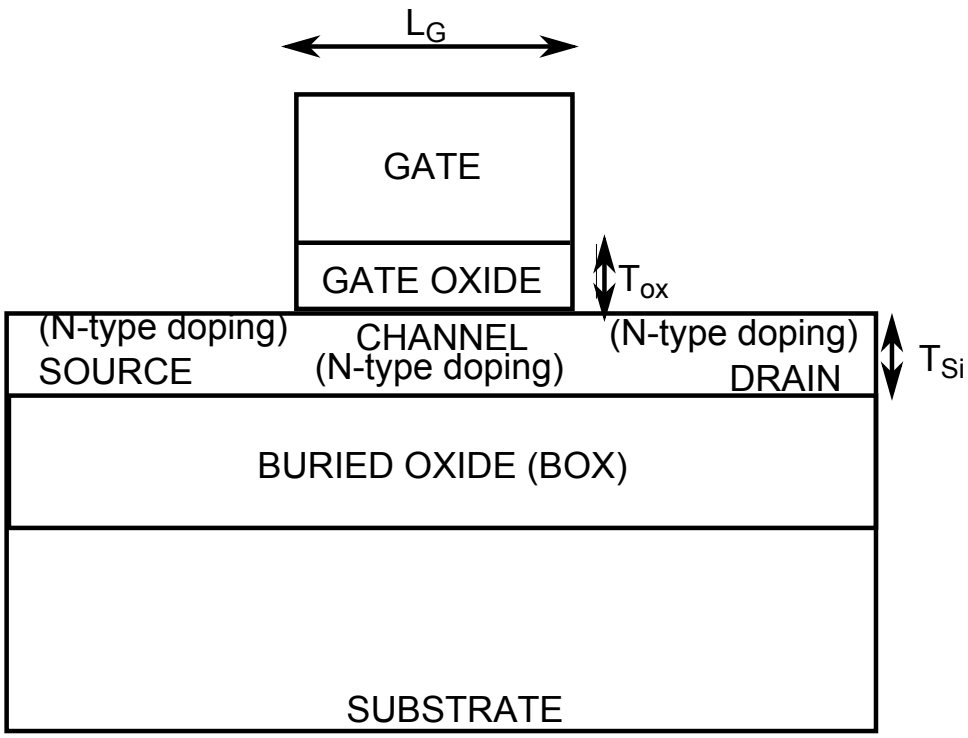


Figure 1.10: Schematic of an SOI junctionless transistor.

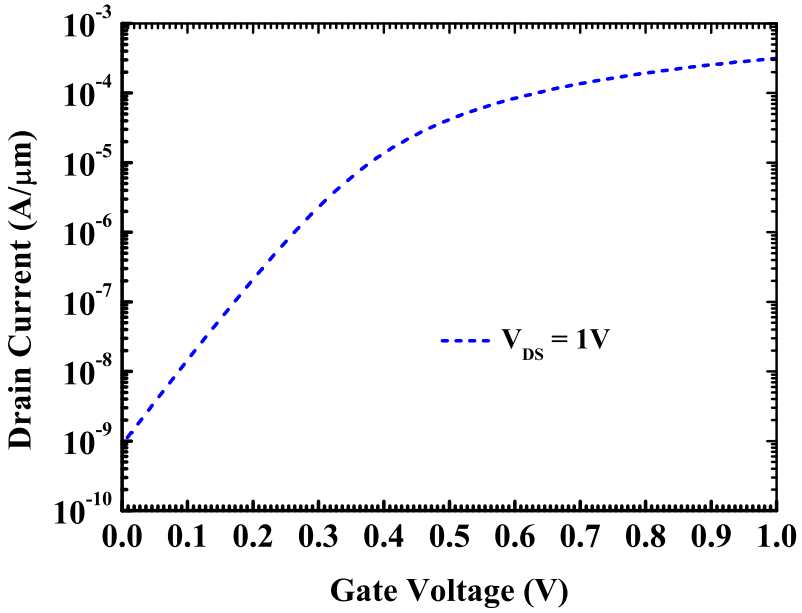


Figure 1.11: Typical I_D-V_{GS} characteristics of junctionless transistors.

be seen in the band diagram (Fig. 1.12) for V_{GS} =0V, that there exists a barrier between the source and the channel due to depletion of carriers in the channel. There exists a similar barrier between the source and channel, even in the conventional MOSFET. Once a positive gate bias

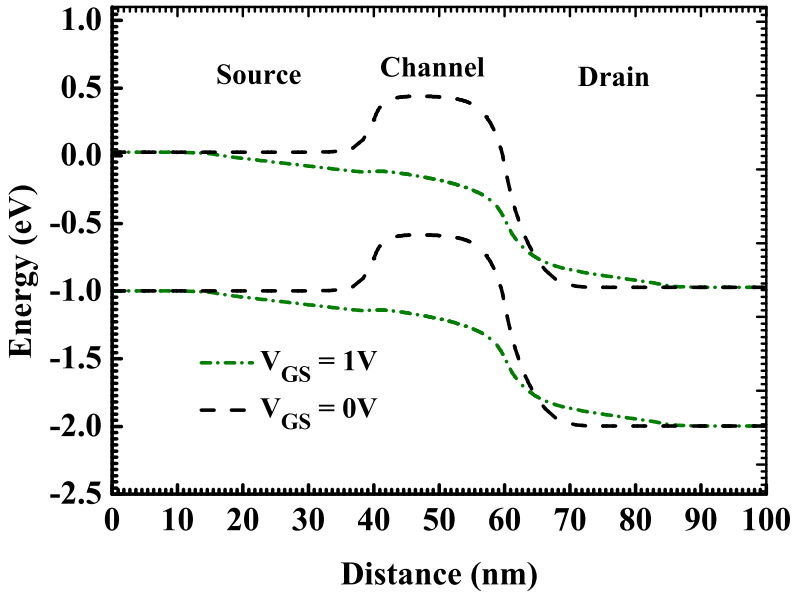


Figure 1.12: Lateral band diagram on JLT both on the ON and OFF states.

is applied (note this is for an n-channel operation), the channel is now brought out of depletion and the barrier between the source and channel is reduced. This results in a high drain current for a non-zero drain bias. When the voltage applied at the gate is approximately equal to the workfunction difference between the gate and channel, the device is brought into the flat-band condition and the transistor is said to be turned ON.

However, all this is valid when the channel thickness is less than its depletion width, else, the device will not be turn OFF at zero gate bias. For example, if the depletion width calculated is 10nm and the channel thickness is 20nm, the device will conduct due to the drain to source bias, even for a zero gate bias, i.e., the device can not be turned OFF. Hence it is important to maintain a very thin semiconductor thickness in junctionless transistors to have a proper switching characteristics.

1.4 Review of Junctionless Transistors

Realizing the metallurgical junctions beyond 32nm node for a metal oxide semiconductor field effect transistor (MOSFET) has become extremely challenging due to the need of ultra steep doping profiles [2]. Recently, new kind of device designs, based on the Lilienfeld's first transistor architecture [12] which do not have any metallurgical junctions, were proposed [13–

17] and successfully fabricated on silicon [2, 18, 19]. New designs include nanowire gate all around (GAA) architectures [13, 15, 18], vertically stacked devices [20], tri-gated nanowire architectures with a silicon on insulator (SOI) [2] and bulk substrates [16]. Planar architectures on bulk substrates were also proposed to further simplify fabrication process [17]. Junctionless transistors have an ultra thin device layer of highly doped semiconductor which is volume depleted in the OFF state (at zero gate bias) due to its workfunction difference with that of the gate electrode. This results in very low leakage current [2]. A positive gate bias forces the device layer to flatband and then into accumulation, resulting in an increase in the drain to source current [2]. The gate of junctionless transistor modulates the resistance of the heavily doped semiconductor, hence, the device can be seen as a gated resistor [2, 21].

Trigate junctionless transistors (JLTs) with channel length of 1 μm were demonstrated on silicon-on-insulator (SOI) substrates [2]. Recently 50nm [18] and 26nm [22] gate length JLTs performance have been reported. P-channel JLTs on Germanium-on-insulator (GeOI) substrates [23] and N-channel JLTs with poly-Si nanowire channels have also been reported [19]. It has been shown that JLT can be a good candidate for flash memory [24–26], because of which this concept was applied to NAND flash [27] and 3D integrated flash memories like vertical-stacked-array-transistor memory for solid state drives [28] and bit cost scalable memories [29–31]. This device was also shown as a suitable candidate for dynamic and static random access memory [12, 32] applications. Recent studies also include temperature dependence of electrical characteristics [33], effects of strain on JLT performance [34], its ballistic nature at shorter channel lengths [35, 36], and radio frequency (RF) performance analysis [37]. These devices are known to offer several advantages over the conventional MOSFETs, viz., 1. Better scalability [38], 2. Reduced fabrication process complexity [17, 25], 3. Low electric field during the ON state of the device [17, 39], 4. Impact ionization induced sharp sub-threshold slope at a drain bias of 1.5V [40], and 5. High mobility [34].

We here list out the milestones during the evolution of JLTs. These architectures include, the gate all around junctionless transistor, known as a nanowire pinch-off FET [13] and Vertical Slit FET (VeSFET) [20]. The schematics of nanowire pinch-off FET and VeSFET are shown in Fig. 1.13. The VeSFET is a double gated junctionless transistor wherein the two gates can be operated independently. Independent gate architecture allows the designer to realize logic functions such as AND, OR etc. Its vertical assembly, makes the VeSFET an attractive device for 3D integration[20]. However, scaling the channel length to ultra short regime would be

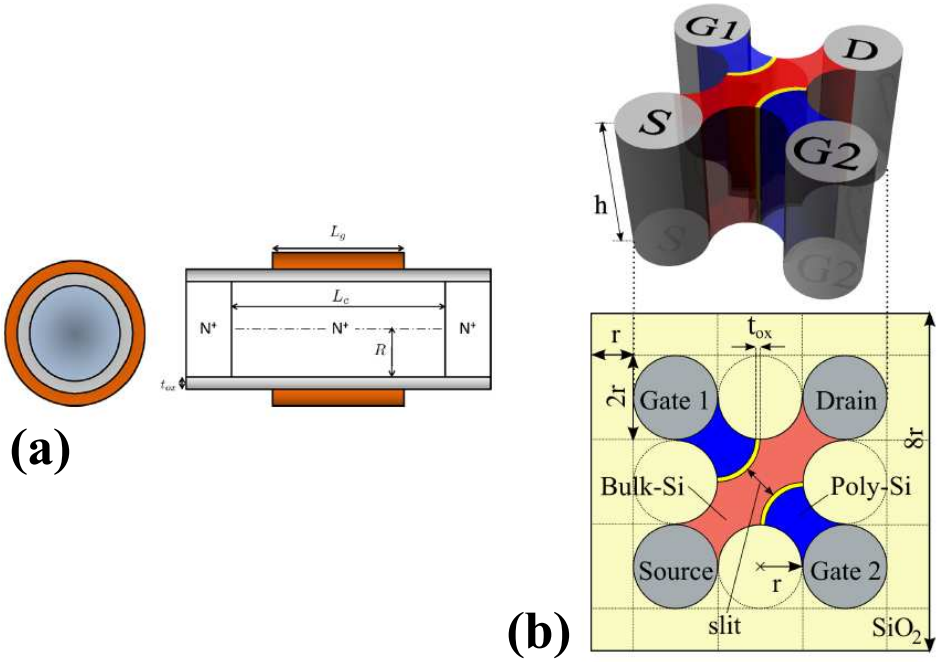


Figure 1.13: Schematic representation of (a) nnaowire pinch-off FET [13] (b) Vertical Slit FET (VeSFET) [20]

difficult due to the circular nature of the gate.

The first junctionless transistor was fabricate by Colinge et al, in 2010. They have shown the JLTs as a potential device alternative to the conventional MOSFETs. The ON current demonstrated at 1μm channel length are on par with the conventional MOSFET [2]. They have demonstrated a device with negligible DIBL, near-ideal subthreshold slope etc. The cross-sectional TEM image along with the I_D - V_{GS} characteristics of a long channel tri-gate JLT are shown on Fig.1.14. Even in the recent short channel ($\sim$ 50nm) junctionless transistor fabricated by Colinge et at., they show that the electrostatic integrity is intact [41].

Later, it was shown by Choi et al., [18], that a short channel length ($\sim$ 50nm) GAA junctionless FET has an unacceptable variability with nanowire width variations. A large shift ($\sim$ 3V) in threshold voltage is observed just by doubling the width of nanowire (see Fig. 1.15). An inversion mode transistor fabricated with a similar process flow does not have such a variability.

Very recently, Rios et al. [22], have a contridicting version of results shown by [2] and [41]. They show that for a given OFF current JLTs have lower ON current with an increased short channel effects. The summary of the results demonstrated by Rios et al., are shown in Fig. 1.16.

In view of the above mentioned shortcomings of junctionless transistors, there is a tremen-

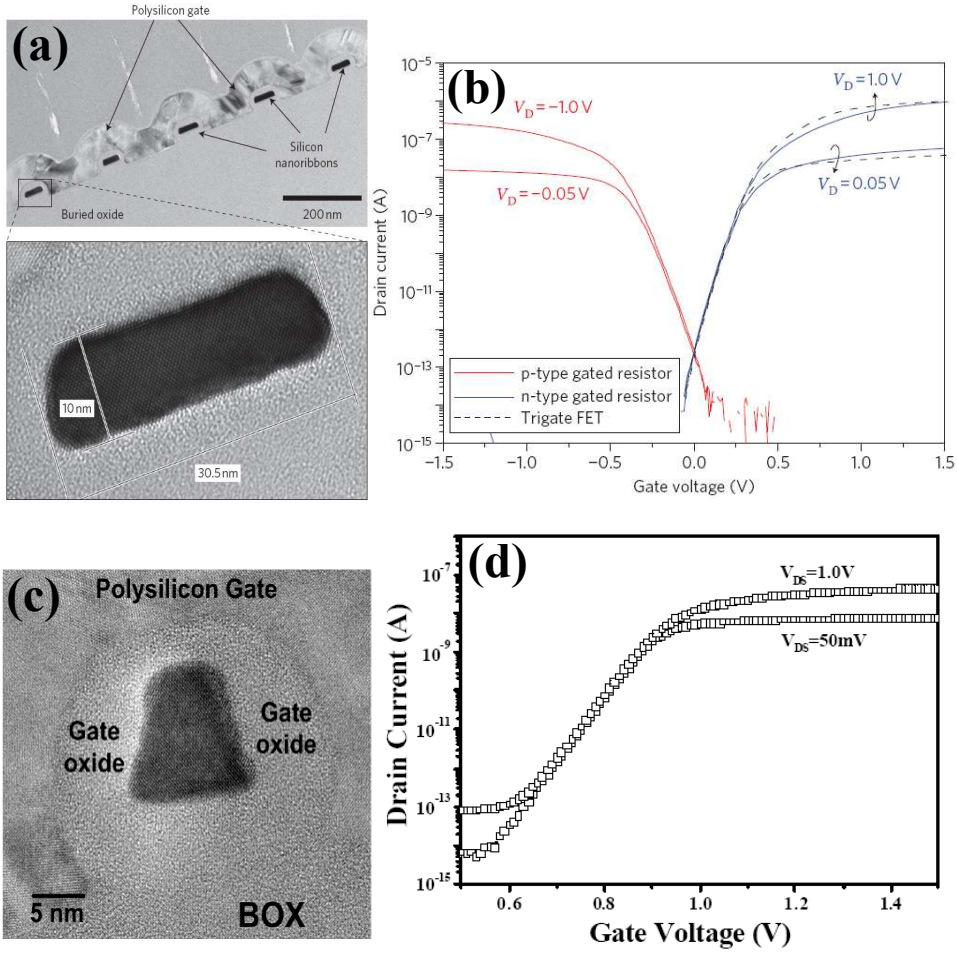


Figure 1.14: (a)-(b) Cross-sectional TEM image and I_D - V_{GS} plot of 1μm channel length tri-gate JLT fabricated by Colinge et al. (c)-(d) Cross-sectional TEM image and I_D - V_{GS} plot of 50nm channel length tri-gate JLT fabricated by Colinge et al. [2, 41]

dous need for reducing the short channel effects to make the device an attractive alternative for low standby power applications. Our proposals of JLT architectures were in this direction [17, 42]. The architectures proposed by us are shown in Fig. 1.17.

1.5 Scope of the Present Work

In this work, we have first understood the needs of the CMOS devices at sub-20nm gate lengths with focus on improving the novel junctionless transistor architectures, so as to meet the requirements of low standby power applications. We identified that the normal planar SOI junctionless FETs have issues with the electrostatic integrity and variability. Also, it was identified that these devices have an advantage when it comes to the source/drain doping, but would demand an ultra thin body silicon on insulator down to 5nm thickness. Fabrication of such

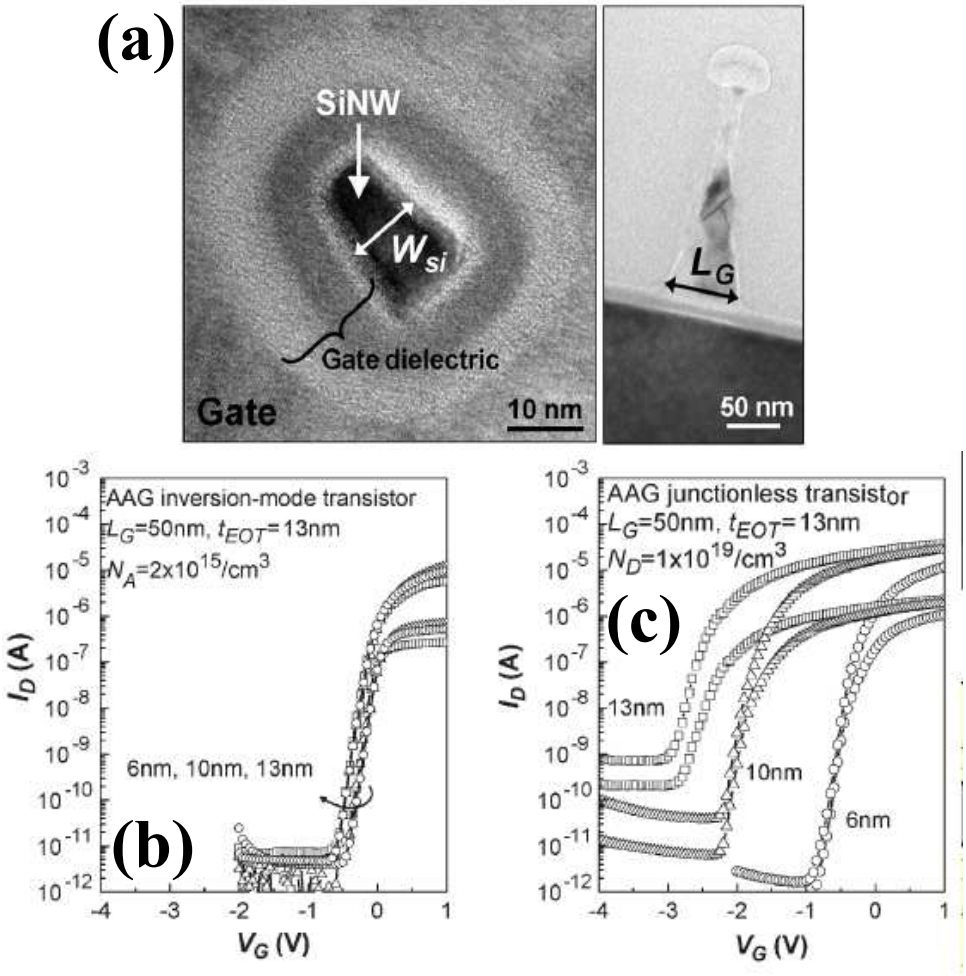


Figure 1.15: (a)Cross-sectional image of 50nm channel length gate all around (GAA) JLT. I_D - V_{GS} plot of 50nm channel length (b) inversion mode FET (c) junctionless FET. [18]

wafers with uniform SOI thickness is technologically challenging and is expensive.

An alternative device architecture, which we call as bulk planar junctionless transistor (BPJLT) is proposed to make the process flow simple and less expensive compared to SOI and/or non-planar junctionless FETs. A junction isolation for junctionless transistors is studied as this can be achieved just by ion-implantation which is comparatively easy and cheep than the smart cut way of making SOI wafers. As the junction isolation we propose is only in the vertical direction and not in lateral direction of source, channel and drain, this device will retain all the properties of junctionless FETs. In addition, the p-n junction formed for isolation purpose adds to the depletion of channel by the gate. This makes the BPJLT to have superior electrostatic integrity compared to the SOI counterparts. Further having the device electrostatics dependant substrate, we can use the substrate doping and/or substrate bias as additional knobs for tuning the device.

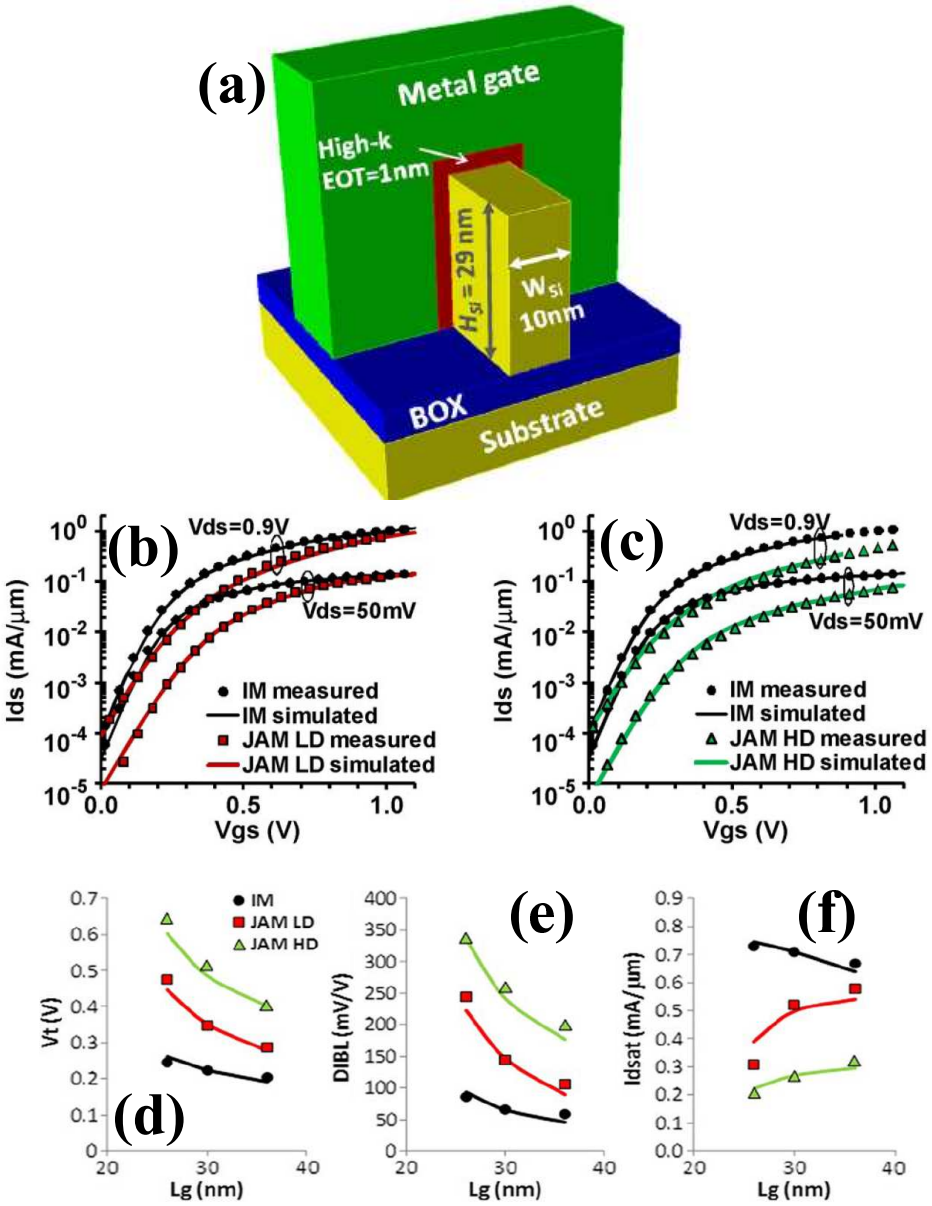


Figure 1.16: (a) Schematic representation of 26nm channel length tri-gate JLT from Intel. (b)-(c) I_D - V_{GS} plot of 30nm channel length junctioless accumulation mode (JAM) transistor with heavily doped (HD) and lightly doped (LD) channel in comparison with inversion mode (IM) transistor (d)-(f) variation of threshold voltage, DIBL and saturation drain current with channel length for JAM-HD, JAM-LD and IM devices. [22]

We have investigated a junctionless transistor architecture with high-k spacers to further improve the device electrostatics. High-k spacers allow the fringing fields to control the channel depletion. Since the junctionless transistor is a fully depleted device in the OFF state, the fringed fields through the high-k spacers enhance the channel depletion, making the effective channel length longer than the physical gate length and this is only in the OFF state. In the ON state, the device is in (or around) flat-band. This makes the device to negligible effect of spacers in

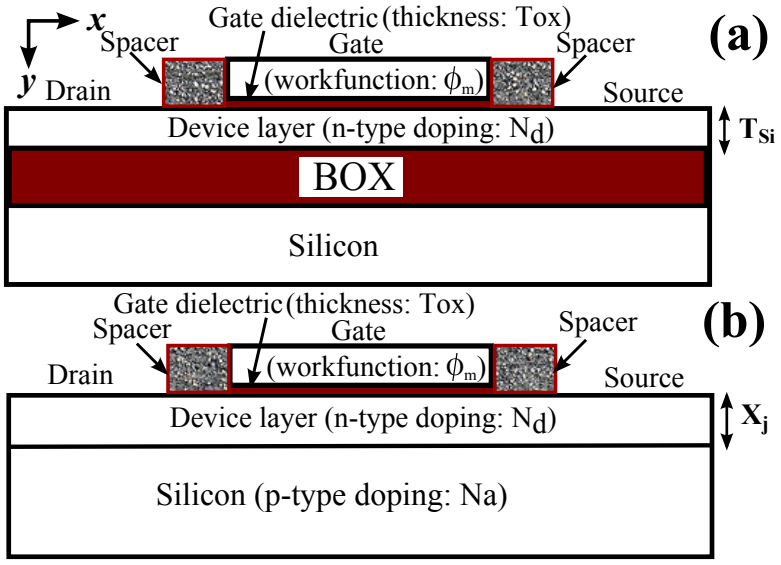


Figure 1.17: (a) - (b) Schematic representation of JLT and BPJLT with spacers.

the ON state. Both these effects together result in several orders of improvement in the OFF current for the same (or similar) ON currents.

It is known that the gate induced drain leakage (GIDL) is a very important phenomenon to study at short channel lengths and this is caused by band to band tunneling. In the course of study, we have identified that the dominant leakage component in the OFF state of JLT is also due to band to band tunneling, but, this is not like the conventional GIDL. Here, the tunneling happens in the lateral direction (i.e., along the transport direction), unlike the GIDL which is in the vertical direction (i.e., perpendicular to transport). The excess carriers accumulated in the channel due to BTBT in the OFF state is observed to trigger the parasitic bipolar transistor in the JLT, resulting in a very high OFF state current. However, we observed that this is very dominant only in the SOI junctionless FETs and can be subsided by the BPJLT.

We also investigate on the effect of quantum confinement on the performance of the JLT. As it has around flat band operation in the ON state, we observe that the quantum confinement effects are minimal in JLTs when compared to conventional MOSFETs. According to our investigation, junctionless transistors are potential candidate devices for low power applications. One such application is the displays. However, devices suitable for display application need to be transparent in nature. As the JLTs require very thin semi-conductive layer, we can think of very thin Si or poly-Si channel layer which has very less absorption and could potentially be a transparent material. We present here the attempts made to fabricate the thin-film junctionless FETs with poly-Si as the active device layer. We were able to make these devices, which

however needs improvements in the future work.

1.6 Organization of the Report

Chapter 2 presents the architecture of JLTs on bulk silicon, known as bulk planer JLT. In Chapter 3, we present a way to reduce the OFF state leakage current of JLTs. The ON and OFF state behavioural studies of JLTs were presented in Chapter 4 and Chapter 5. The poly-Si junctionless thin film transistor process developed for a possible display application is described in Chapter 6. We conclude by discussing the scope for future work in Chapter 7.

Chapter 2

Bulk Planar Junction-less Transistor (BPJLT)

2.1 Introduction

Junctionless transistors have the following advantages compared to the conventional MOSFETs: (i) greatly simplified process flow as halo/extension and deep source/drain implants are avoided (ii) implant activation anneal after gate stack formation is avoided resulting in low thermal budgets and hence provides flexibility in the choice of materials for gate dielectric and gate metal. However the SOI junctionless devices require aggressive scaling of the SOI film thickness and channel width to 5nm or below [14] , and gate work functions in excess of 5.5eV for highly scaled n-channel devices. Uniform ultra-thin(5nm) SOI substrates will be technologically challenging and expensive to produce. A recent proposal for a bulk junctionless device [16] solves some of these problems but suffers from the process complexity of a tri-gate architecture and the limitation of a high gate work function (5.5eV).

We propose a new bulk planar device architecture - the BPJLT, which is a source-drain-junction free transistor accompanied with a junction isolation. It is thus junctionless in the source-channel-drain path, but needs a junction in the vertical direction for isolation purposes. The advantages of the BPJLT over the existing junctionless transistor versions are (i) the full compatibility to the industry standard planar bulk twin well CMOS process flow (ii) lower cost (iii) better scalability and (iv) the presence of two additional controls for tuning the device performance. The device retains the advantage of low thermal budget after gate formation.

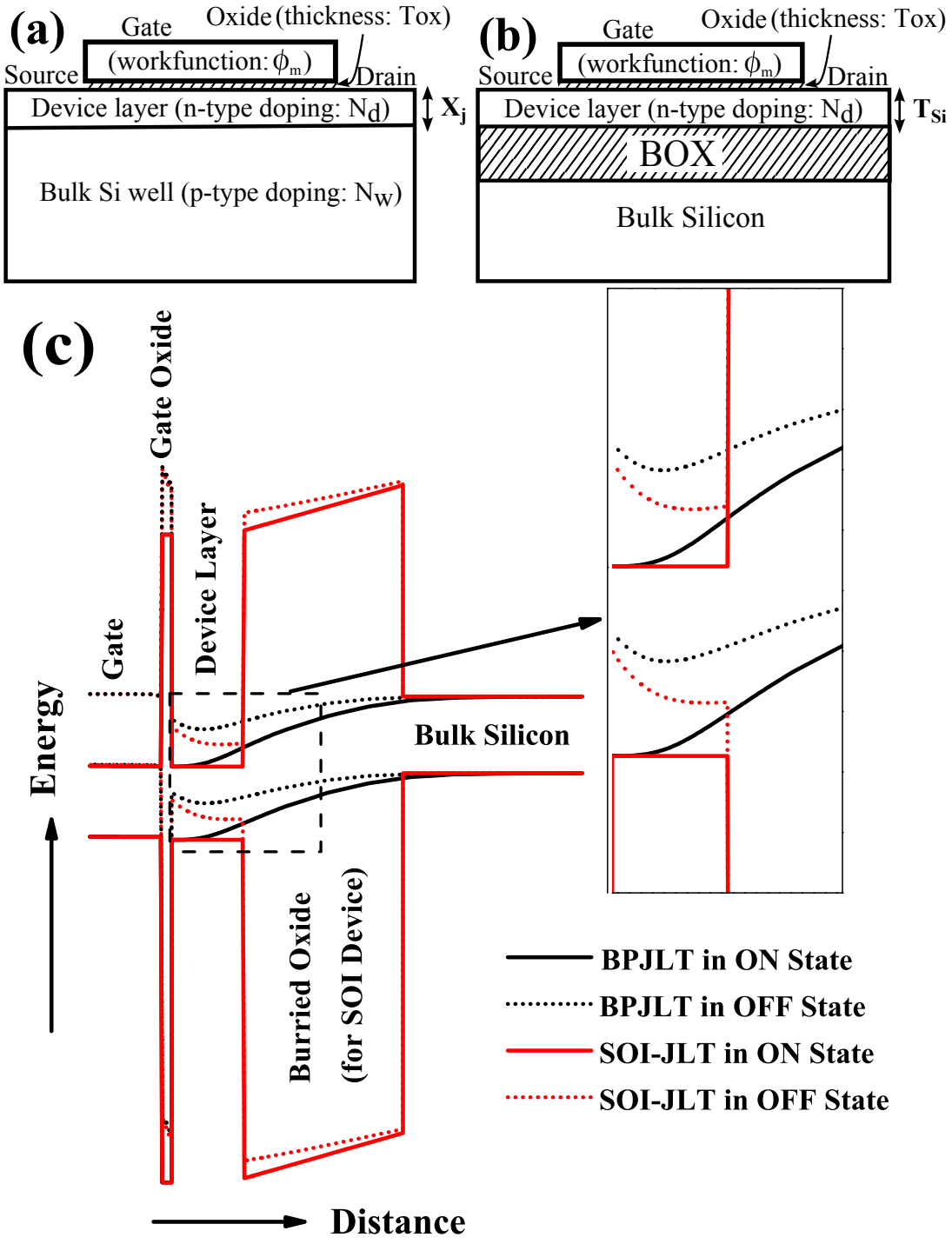


Figure 2.1: (a) and (b) Schematic representation of Bulk planar and SOI junctionless n-channel transistors respectively. (c) Band diagram in vertical direction of the device taken at the mid of the channel, describe the band structure when gate voltage V_{GS} =0V (OFF state) and 1V (ON state) of both SOI and Bulk devices. Inset shows the band diagram in the n-type or SOI layer for better clarity. $T_{Si} = X_j$ = 10nm, L_g = 20nm, N_d = 1.5 x 10^{19} cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, $N_w = 10^{18}$ cm^{-3}, V_{DD} = 1V.

2.2 Device Structure and Operation

Fig. 2.1(a) show the proposed device architecture for n-channel operation. A thin n-type "device layer" is formed on a p-type silicon forming a junction with junction depth of X_j. A gate stack with a gate dielectric and gate metal of work function of 5.1eV are formed on top of the n-type layer as shown. Also shown is an n-channel SOI-JLT (Fig. 2.1(b)) for comparison. The dielectric isolation used in SOI architecture is replaced by junction isolation in BPJLT. Both devices have uniform lateral doping, i.e. the source, drain and the channel have identical doping. The gates of both the devices is a metal with p-type work function, separated from the channel by a thin dielectric.

When zero bias is applied to the gate of the SOI-JLT, the n-doped silicon will be depleted of carriers, resulting in no conduction between source and drain. As a positive bias is applied to the gate, the thin SOI device layer comes out of depletion and results in a conducting channel between source and drain.

In the proposed BPJLT on the other hand, when zero gate bias is applied, the device layer is depleted from both top and bottom because of its work function difference with the gate electrode on one side and the oppositely doped substrate on the other. The portion of the physical device layer that is depleted by the gate at zero bias is the "effective device layer". As a positive bias is applied to the gate, this effective device layer comes out of depletion and results in a conducting channel between source and drain.

To prove the concept, we have simulated both the structures with the parameters mentioned in the caption of Fig. 2.1. The band diagram along a vertical cross-sectional cut through the middle of the channel is shown in Fig 2.1(c). It is seen that in the OFF state, the device layers are depleted in both devices. In the ON state, the SOI-JLT device layer is uniformly in flatband, whereas for the BPJLT a fraction of the device layer at the top - corresponding to the effective device layer - is in flatband, the rest of it still remaining depleted. Thus a continuous conduction channel is formed in the ON state in both devices, whose thickness equals the physical (effective) device layer thickness for the SOI-JLT (BPJLT). The thinner effective device layer in the case of the BPJLT suggests that it would exhibit better electrostatic integrity than the SOI-JLT.

Table 2.1: Device parameters used for evaluating BPJLT

Parameter	Value
Device layer thickness (T_{Si}) of SOI-JLT	10 nm
Junction depth (X_j) of BPJLT	10 nm
Donor doping in device layer (N_d)	1.5x10^{19} cm^{-3}
EOT of gate dielectric (T_{ox})	1 nm
Gate work function (ϕ_m)	5.1 eV
Well doping (N_w)	5x10^{17} to 5x10^{18} cm^{-3}
Drain Supply Voltage(V_{DD})	1 V
Channel length (L_g)	10 nm to 1 μm

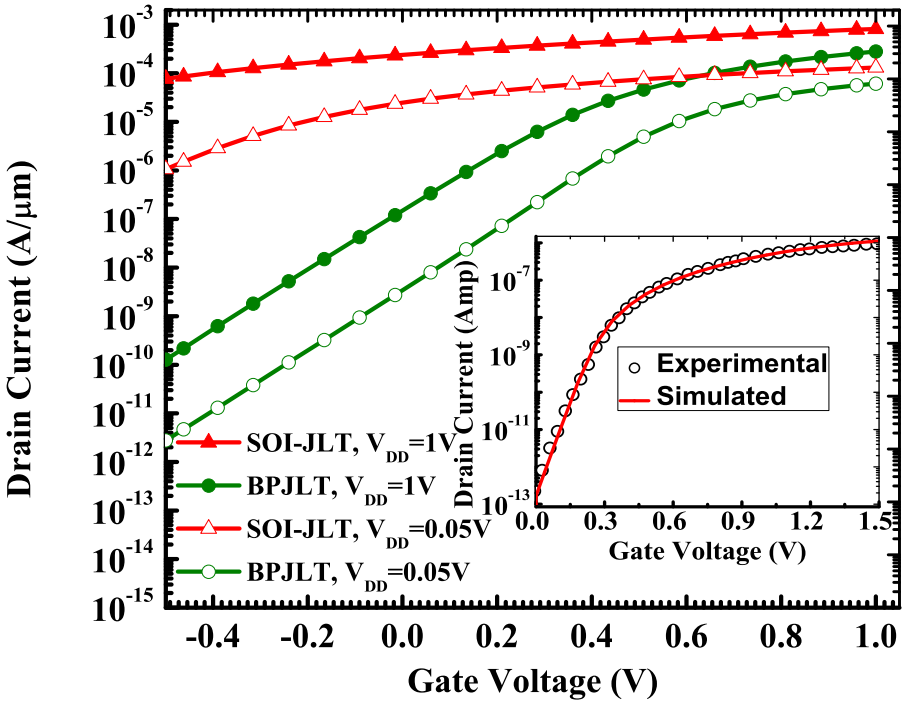


Figure 2.2: I_D-V_{GS} characteristics of a 10nm channel length SOI-JLT and BPJLT with T_{Si} = X_j = 10nm, N_d = 1.5 x 10^{19} cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, N_w = 5x10^{18} cm^{-3}, V_{DD} = 0.05V and 1V. The inset shows the model calibration against nonplanar SOI-JLT experimental I_D-V_{GS} data from [2].

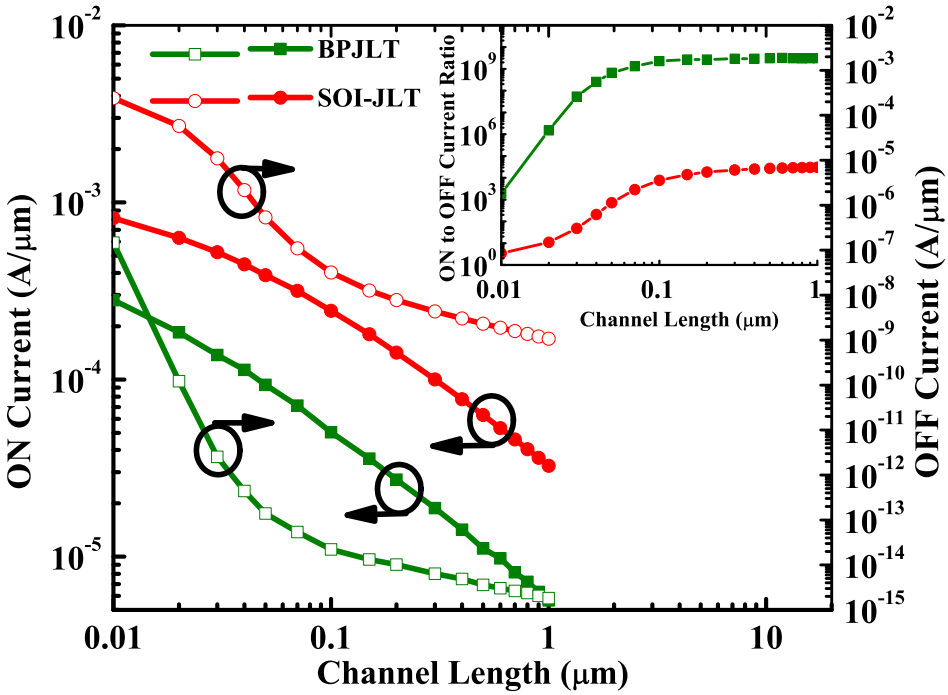


Figure 2.3: ON current (in solid symbols) and OFF current (in open symbols) of both SOI and Bulk planar junctionless transistor for L_g from 1μm to 10nm. In the inset is the ON to OFF current ratio of both SOI and Bulk planar junctionless device for L_g from 1μm to 10nm. T_{Si} = X_j = 10nm, N_d = 1.5 x 10^{19} cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, N_w = 5x10^{18} cm^{-3}, V_{DD} = 1V.

2.3 Results and Discussions

3-D Simulations of the Bulk and SOI based junctionsless transistors were carried out using the SENTAURUS 3-D device simulator [43]. This solves the self-consistent drift-diffusion equations for electrons and holes; direct gate tunnelling was not included under the assumption of a high-k metal-gate stack, whereas models for well-to-drain non-local tunnelling(NLT) [44], bandgap narrowing and Schottky-Read-Hall mechanisms were included. The mobility model includes both doping and transverse-field dependence. Its high channel doping degrades the JLT mobility somewhat, whereas the small surface field in ON state (as seen in Fig.2.1(c)) enhances the mobility; overall they translate to comparable performance between JLT and conventional devices [2] . The inset of Fig. 2.2 shows the calibration of our model parameters to experimental SOI-JLT data [2]. The device parameters used in our BPJLT and SOI-JLT simulations are listed in Table 2.1.

Fig. 2.3 shows the scaling behaviour of a BPJLT and an SOI-JLT for channel lengths varying from 1μm down to 10nm. We see that as the channel length of SOI-JLT is scaled to 10nm for a given gate metal work-function (say 5.1eV) and device layer thickness (say 10nm),

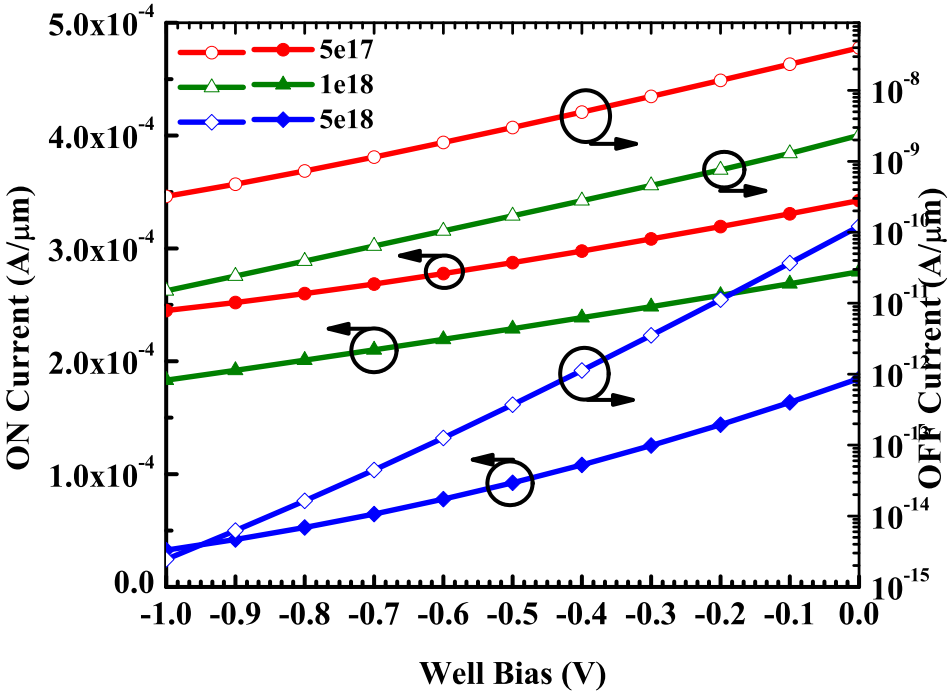


Figure 2.4: ON current (in solid symbols) and OFF current (in open symbols) of Bulk planar junctionless transistor with well dopings(N_w) of 5x10^{17} cm^{-3}, 10^{18} cm^{-3} and 5x10^{18} cm^{-3} for an applied well bias varying from 0V to -1V. T_{Si} = X_j = 10nm, N_d = 1.5 x 10^{19} cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, V_{DD} = 1V.

the subthreshold leakage increases drastically, resulting in an I_{ON}/I_{OFF} of 3. This is illustrated by the dotted curve in Fig.2.2, viz. the I_D-V_{GS} plot of a 10nm channel length SOI-JLT. Using an extremely thin (5nm) device layer together with a high work-function (5.5eV) metal-gate seems to resolve this electrostatics problem to some extent[14] but places tight - and potentially expensive - material and process constraints. Current density distribution plots derived from device simulation confirm what might be intuitively surmised: the leakage current density is concentrated towards the bottom portion of the device layer. This was of course to be expected from the nearly flat bands at the bottom of the device layer (in the vicinity of the BOX) that we had seen in Fig. 2.1(c). We have addressed the aforementioned challenges with a novel device structure that reduces process cost and complexity, and introduces tunable device parameters to optimize the I_{ON}/I_{OFF}. This is illustrated in Fig. 2.2 which compares the I_D-V_{GS} plot of 10nm channel length BPJLT and SOI-JLT devices. Obviously the BPJLT has superior I_{ON}/I_{OFF}, smaller drain-induced-barrier-lowering (DIBL) and subthreshold slope. This establishes the superior electrostatic integrity and, therefore, scalability of the BPJLT which comes from having an effective device layer thickness that can be as thin as half its physical thickness. Essentially the BPJLT has the advantage of a device layer that can be electrostatically

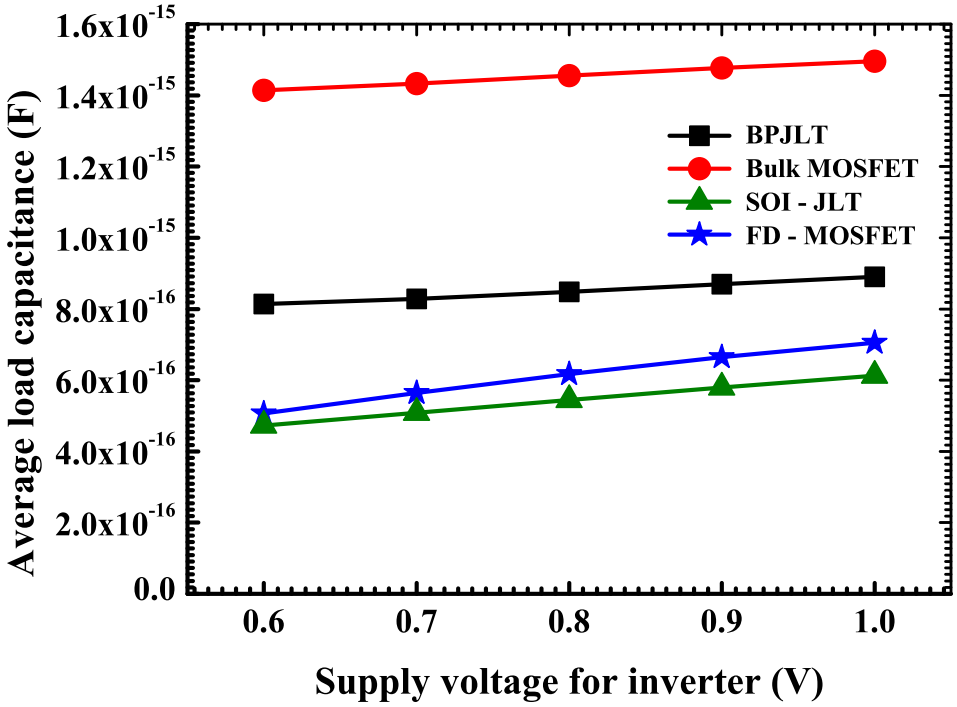


Figure 2.5: Average load capacitance vs. supply voltages for BPJLT, Bulk MOSFET, SOI-JLT and FD-MOSFET. [45] Device parameters are as specified in Table 2.2

defined by tuning the well bias and/or the well doping. In this particular case the SOI-JLT has an effective (and physical) device layer thickness of 10nm, whereas the BPJLT has an effective device layer thickness of about 5nm, the bottom 5nm being depleted because of the built-in junction potential. Again, this can be seen from the band diagram in Fig. 2.1(c) which shows depletion of the device layer by both the gate and the well. The control of the effective device layer thickness by well-doping and well-bias are illustrated in Fig. 2.4, which shows an eight order of magnitude tuning range for I_{OFF} with I_{ON} varying less than 50 percent when both of these knobs are turned simultaneously. We have seen that this translates to a threshold voltage tunability of 25 percent of the supply voltage.

The junction isolation of BPJLT would however comes with a capacitance that could increase the delay of operation. That is the ease of fabrication of BPJLT should be traded for an increased delay. S.R Marni have evaluated the dynamic performance of BPJLT [45]. Salient results of [45] are given below for completeness. The parameters used for evaluating the dynamic performance are listed in Table 2.2. Fig. 2.5 shows the average load capacitance vs. supply voltage for four different technologies. It can be inferred that the average capacitance of BPJLT is higher than its SOI counterpart and - a similar trend can be observed between the Bulk and SOI versions of conventional MOSFETs. Fig. 2.6 shows the average power consumption vs. delay

Table 2.2: Device parameters used to evaluate the dynamic performance of BPJLT [45]

Parameter	**NMOS**	**PMOS**
Device layer thickness (T_{Si}) / Junction depth (X_j)		
BPJLT	5nm	5nm
SOI JLT	3nm	3nm
Bulk MOSFET	20nm	20nm
FD-MOSFET	2nm	2nm
Channel Doping (N_d) / (N_a)		
BPJLT	5x10^{19} cm^{-3}	5x10^{19} cm^{-3}
SOI JLT	5x10^{19} cm^{-3}	5x10^{19} cm^{-3}
Bulk MOSFET	1.2x10^{19} cm^{-3}	1.2x10^{19} cm^{-3}
FD-MOSFET	5x10^{13} cm^{-3}	5x10^{13} cm^{-3}
EOT of gate dielectric (T_{ox})	1 nm	1nm
Gate work function (ϕ_m		
BPJLT	5.1eV	4.08eV
SOI JLT	5.1eV	4.08eV
Bulk MOSFET	4.08eV	5.1eV
FD-MOSFET	4.66eV	4.66eV
Well doping (N_w)	5x10^{18}	5x10^{18} cm^{-3}
Drain Supply Voltage(V_{DD})	0.6V to 1 V	0.6V to 1 V
Channel length (L_g)	15 nm	15 nm

for four different technologies computed by simulating a 3-stage ring oscillator circuits and it is observed that the BPJTL compares with its SOI counterpart, in the way the bulk MOSFET compares to its SOI counterpart.

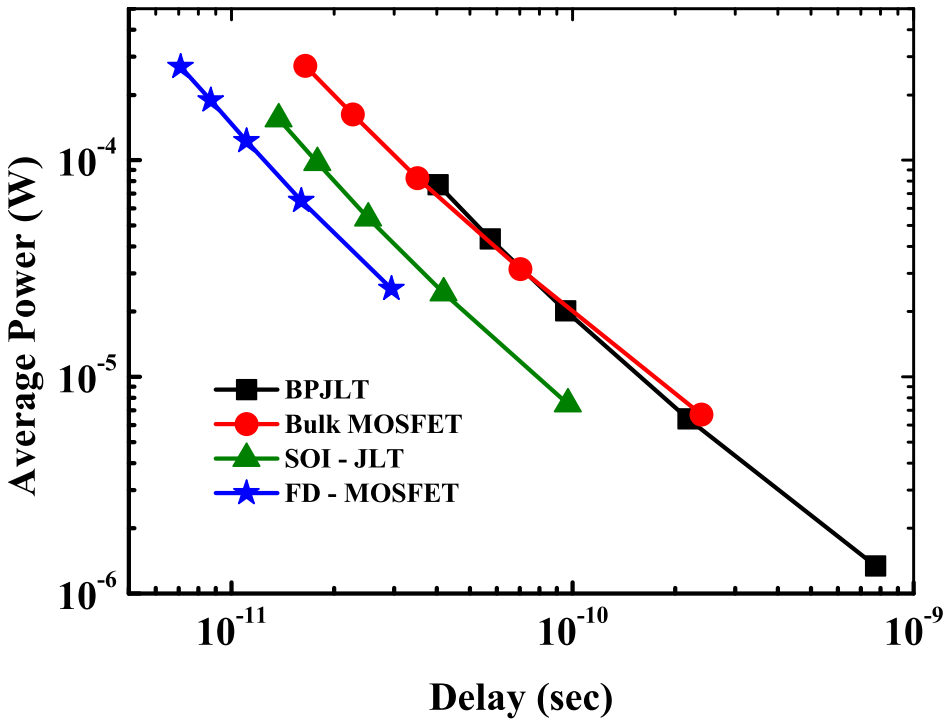


Figure 2.6: Average power consumption vs. delay for BPJLT, Bulk MOSFET, SOI-JLT and FD-MOSFET. [45] Device parameters are as specified in Table 2.2

2.4 Summary

Junctionless transistors obviate the need for very-well-controlled source/drain implants and anneals, and thereby simplify the integration of high-k/metal gate stacks. However their optimal operation requires uniform ultra-thin device layers which are technologically challenging and expensive to produce. We have proposed a bulk planar junctionless transistor that can relax this stringent requirement of device layer thickness by upto 50 percent and can account of better electrostatics as there is an additional substrate control over the channel. Besides having better scalability than its SOI counterpart the BPJLT provides two additional controls on device characteristics, viz. well doping and well bias. The advantages like ease of fabrication and low cost of fabrication of BPJLT can be traded against delay for low standby power applications.

Chapter 3

Junction-less Transistor with High-κ spacers

3.1 Introduction

Although JLTs relax the technological challenges of device scaling, they are not completely free from short channel effects (SCEs) when the physical gate length of the device is scaled to sub-20nm regime and the electrostatic integrity is seen to degrade [46]. Studies of device architecture of under-lapped gate FinFETs with high-κ spacers have shown that extension regions can be electrically induced resulting in supression of SCEs [47]. Use of high-κ spacers or the combination of high-κ and low-κ (i. e., dual-κ) spacers for alternate transport devices like tunnel FETs were found to improve more of the device ON state performance than the electrostatic integrity [44, 48]. Though high-κ spacers are known to be useful for better operation of short-channel devices, the effects are not same among different novel devices. For example, the consequences of the use of high-κ spacers are not exactly the same in the case of MOSFETs and Tunnel-FETs. Unlike MOSFETs, JLTs operate at high vertical electric field in the channel in OFF state and at low field in ON state. Hence, it would be interesting to investigate and optimize the effect of spacers on the operation of junctionless transistors (JLTs).

We propose a novel device architecture with high-κ spacers placed on either sides of the gate of a JLT. Effect of the dielectric constant (κ_{sp}) of the spacer on the device characteristics has been studied. We show in the subsequent sections that the use of high-κ spacers for JLT can improve the electrostatic integrity of the device to a great extent at sub-22nm gate lengths resulting in lower OFF state leakage current. A marginal improvement is seen in the ON state

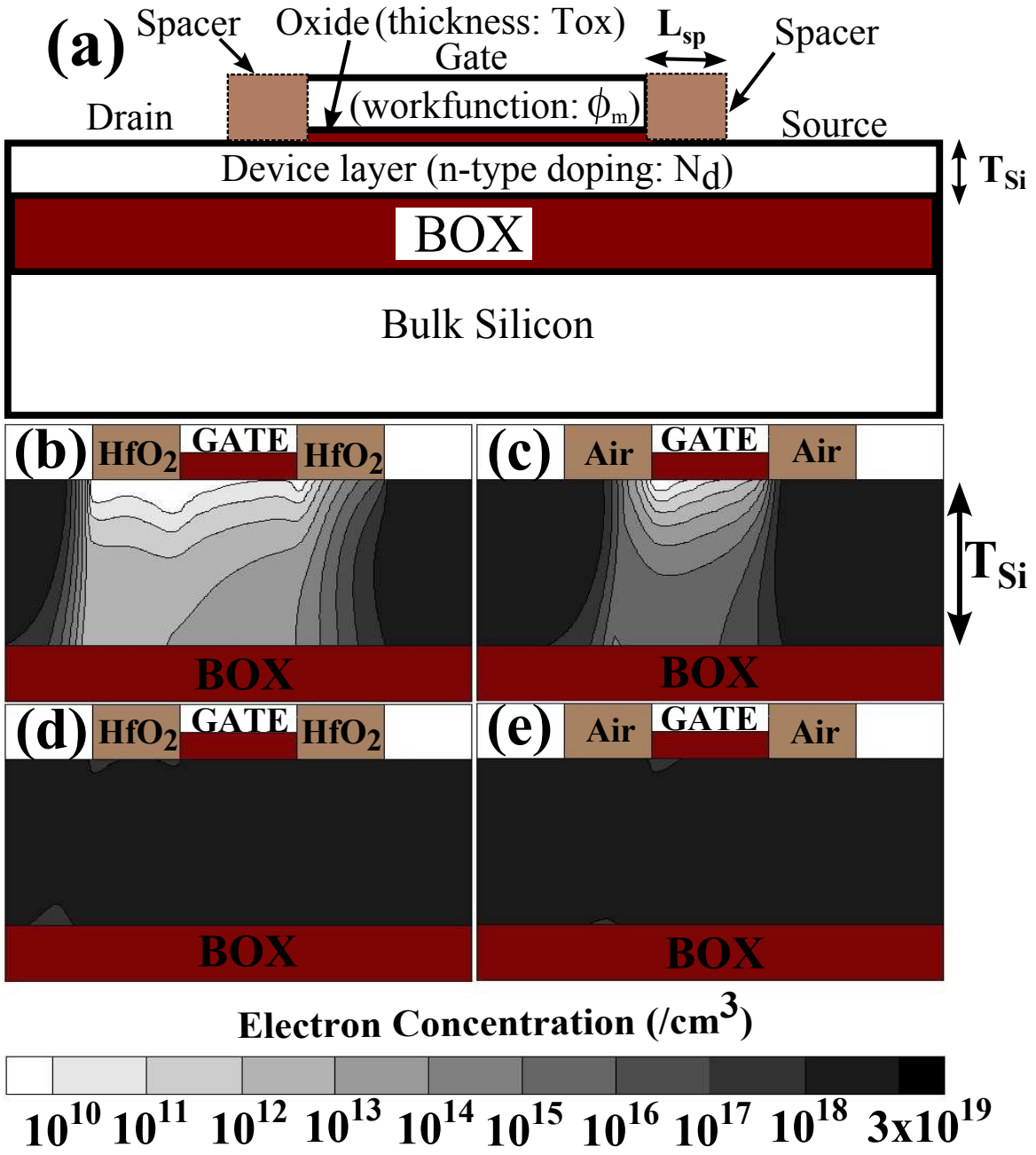


Figure 3.1: (a) Schematic representation of the structure of junctionless transistor (JLT) with spacers. (b)-(e) electron concentration in the channel for a JLT with HfO_2 (κ_{sp}=21) and air (κ_{sp}=1) spacers. (b) and (c) shows the electron concentration in OFF state (V_{DD} = 1V and V_{GS} = 0). (d) and (e) shows the electron concentration in ON state (V_{DD} = 1V and V_{GS} = 1V). L_g=20nm, T_{Si} = 6nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, ϕ_m = 5.0eV, L_{sp} = 15nm. Electron concentrations were computed by self consistently solving Poisson, drift-diffusion and electron continuity equations.

current, which is also explained.

3.2 Device Structure and Operation

Fig. 3.1(a) shows the proposed device architecture for n-channel operation. A gate stack with a gate metal workfunction of 5.0eV is formed on top of a thin n-doped device layer of the silicon on insulator (SOI) wafer. Device parameters used in this investigation are listed in Table 3.1. The large difference in the workfunction of the gate and the device layer depletes the device layer when the gate bias is zero, i. e. OFF state. The device layer is around flat band in the ON state (i. e., when V_{GS}=V_{DD}). As the source, channel and the drain regions are doped equally with donor atoms, JLTs do not have any source/drain extensions. This is unlike the case of conventional MOSFETs and hence a spacer may not be needed in a JLTs from this perspective. However a salicide contact to source and drain would necessitate a spacer in JLTs. We propose that the spacer be made of high-k material for improving the JLTs electrostatics.

Similar to the case of conventional MOSFETs, JLT suffer from SCEs, scaling the gate oxide thickness and reducing the device layer thickness are some of the methods to supress SCEs [46]. But, as the gate oxide thickness needed is already about 1nm and the SOI thickness control over large diameter wafers would be a challenge in the range of interest, an altranative scheme for controlling SCEs would be welcome.

It has been shown that the JLT has high vertical electric field (because of volume depletion) in OFF state and zero electric field (being in flat band) in ON state, which is converse to that of the case of conventional MOSFET [16, 17]. We can make use of this interesting phenomenon to reduce the SCEs. Introducing high-κ spacer on either sides of the gate can enhance the fringing electric fields through the spacer and deplete the device layer beyond the gate edges in the OFF state. This would result in an effective increase in the length of the depleted silicon region (effective channel length) and hence improve subthreshold characteristics. However, in the ON state, having zero electric field can leave the ON state current unaffected with the use of high-κ spacers. Any increase in gate voltage beyond the flat-band, would drive the channel into accumulation, and this can be further enhanced by the presence of high-κ spacers to augment the drain current.

To prove the concept, we have simulated the structure shown in Fig. 3.1(a) with the parameters listed in Table 3.1, for a κ_{sp} of 21 (HfO_2) and 1 (air). Electron concentrations in both ON and OFF states of these structures are shown in Fig. 3.1 (b)-(e). It can be clearly observed that the depletion layer is extended beyond the gate edges in the case of HfO_2 spacers

Table 3.1: Device parameters used for evaluating the JLT with high-κ spacers

Parameter	**Value**
Channel length (L_g)	20nm
Device layer thickness (T_{Si})	6 nm
Donor doping in device layer (N_d)	2x10^{19} cm^{-3}
EOT of gate dielectric (EOT_{ox})	1 nm
Gate Oxide Material	SiO_2 (3.9), Al_2O_3 (9.6)
and dielectric constant (κ_{ox})	and HfO_2 (21)
Gate work function (ϕ_m)	5.0 eV [49, 50]
Dielectric constant of spacer (κ_{sp})	1 to 34
Spacer length (L_{sp})	15nm
Drain Supply Voltage (V_{DD})	1 V

in OFF state compared to air spacer. Whereas in the ON state the electron concentrations are similar irrespective of κ_{sp}.

3.3 Results and Discussion

Simulations of the JLT with spacers were carried out using the SENTAURUS device simulator [43]. The models used for device simulation are well calibrated with experimental JLT data from [2] as explained in the previous chapter.

Fig. 3.2 shows the conduction band edge along the lateral direction at the mid of the device layer for OFF state operation. It can be understood from the band diagram that the enhanced depletion due to the fringing electric field through the spacer can cause the following: 1) higher barrier at source/channel interface (it should be noted that the barrier at source/channel interface is due to the depleted channel of JLT - and is due to a p-n junction in the case of a conventional MOSFET), and 2) higher effective gate length than that of the physical gate length. The consequences of these are shown in Fig. 3.3, where the device with high-κ spacers show a reduced OFF state leakage current. The inset of Fig. 3.3 shows the drain current in linear

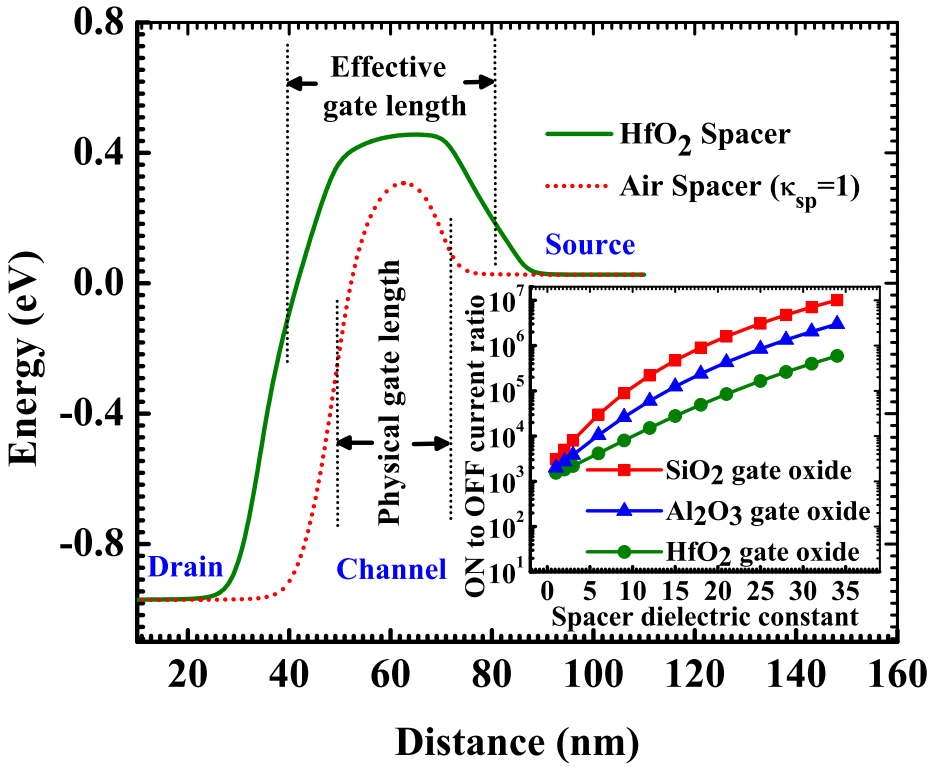


Figure 3.2: Conduction band-egde along the lateral direction for a JLT with HfO_2 and air spacers in OFF state. SiO_2 is used as gate dielectric for these simulations. Inset shows the effect of κ_{sp} on the ON current to OFF current ratio. κ_{ox} is varied from 3.9 to 21 in these simulations.

scale. As the κ_{sp} increases, the slope of the I_D - V_{GS} increases. This indicates a reduction in parasitic resistance from the region under the spacers with increasing κ_{sp}, due to stronger accumulation. By using an appropriate gate metal workfunction, the improvements gained in the leakage current can be traded for a higher ON current (this in-turn reduces the threshold voltage) for the device using high-κ spacers.

The cross-over of Id-Vg at a constant bias-condition (Vg) for the 3 curves (around 1.1V) of Fig. 3.3 can be explained is further explored. In Fig. 3.4, we show the Id-Vg for both high and low Vd, where we observe this cross over to occur even at lower gate bias. The reason for this can be better explained for the case of low drain bias (i.e., when only gate is controlling the electrostatics of the channel).

The Si doping of the device layer of JLT is an N-type with magnitude of $2x10^{19}$ cm-3. The workfunction for such high doping is expected around 4.1 eV. The gate workfunction chosen is 5.0eV and this requires 0.9V of gate bias to bring the channel into flat-band.

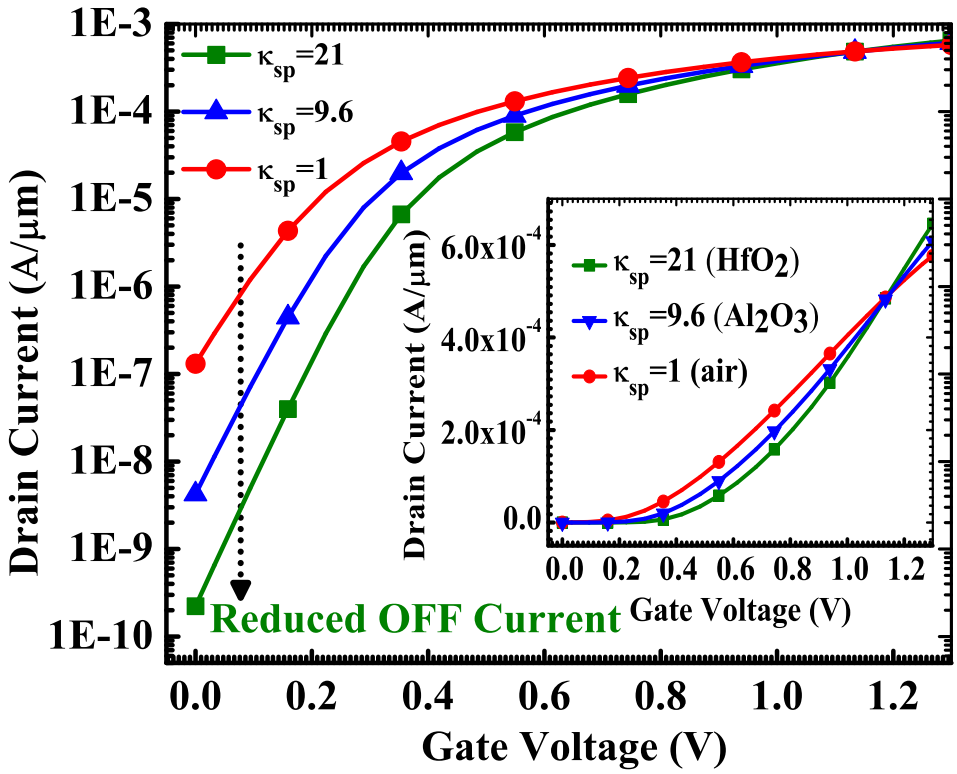


Figure 3.3: I_D - V_{GS} characteristics of 20nm gate length junctionless transistor for κ_{sp} varying from 1 to 21. κ_{ox}=3.9 and V_{DD} = 1V.

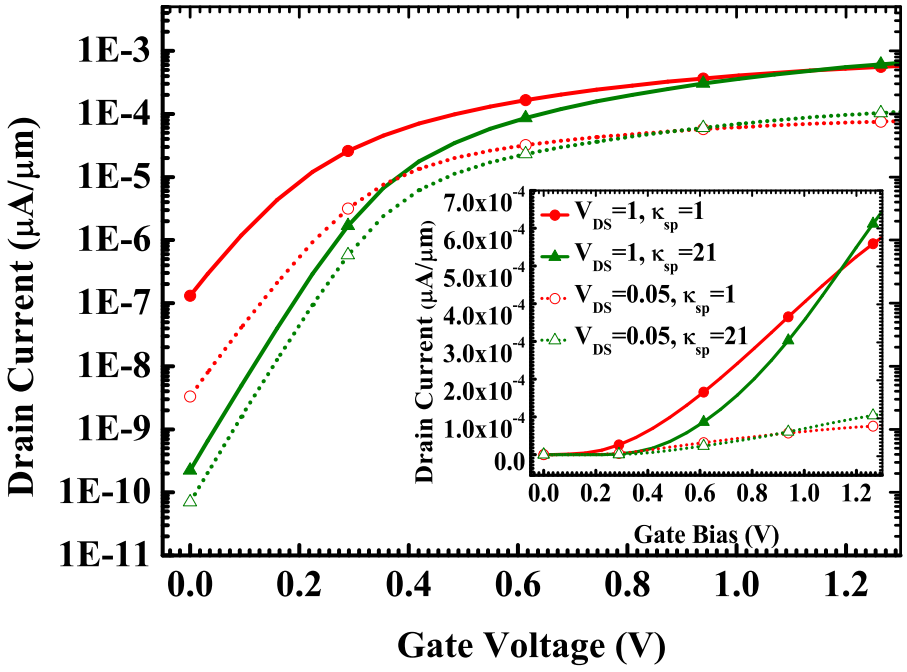


Figure 3.4: I_D - V_{GS} of 20nm channel length JLT, for a drain bias of 1V and 0.05V. L_g=20nm, T_{Si} = 6nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, κ_{sp}=1 and 21, ϕ_m = 5.0eV, L_{sp} = 15nm.

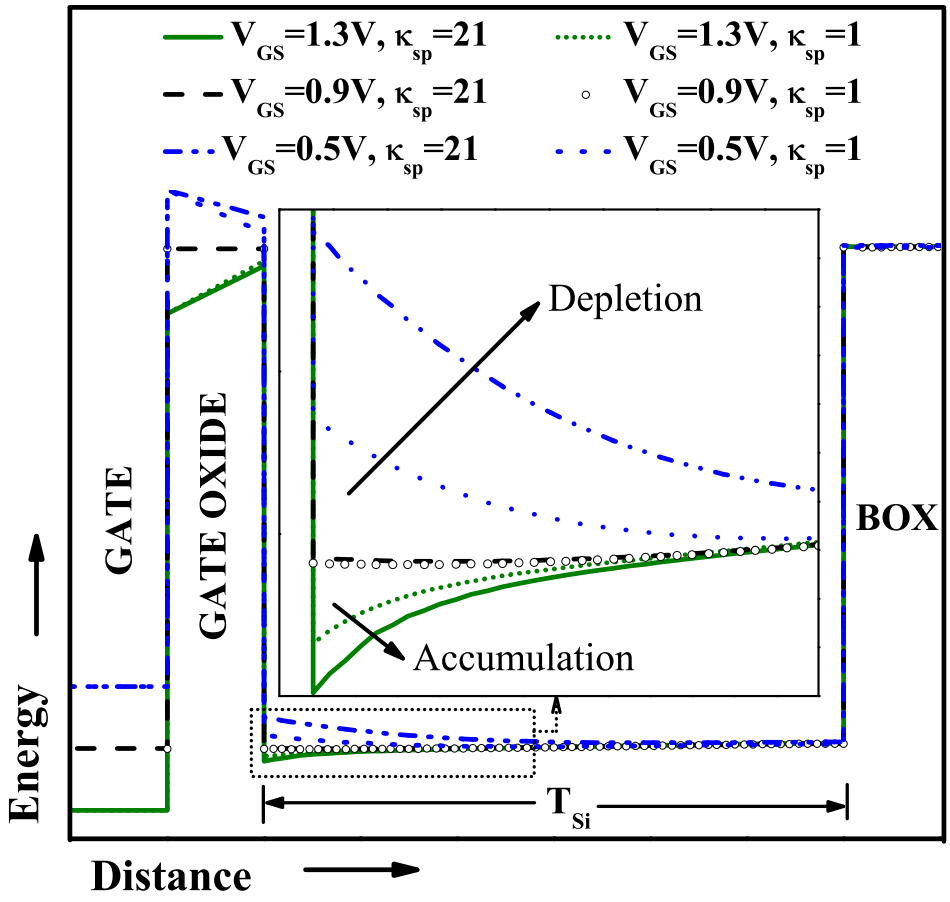


Figure 3.5: Band diagram in the vertical direction of the channel, 0.5 nm away from the channel/drain interface. L_g=20nm, T_{Si} = 6nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, κ_{sp}=1 and 21, V_{GS} = 0.5V, 0.9V and 1.3V, ϕ_m = 5.0eV, L_{sp} = 15nm.

Fig. 3.5 shows the band diagram in the vertical direction of the channel, at 0.5 nm away from the drain/channel interface. It can be observed from the figure that, at 0.9V of gate bias, i.e., in flat-band, fringing fields through the spacer are absent irrespective of κ_{sp} - this makes the drain current independent of κ_{sp}. However, when there is a band-bending in the channel, i.e., in the presence of gate electric field, there is a significant amount of fringing fields through the high-κ spacers. For example, at 0.5V of gate bias the channel is in mild depletion and this will be enhanced by the high-k spacers, resulting in a lower current. At 1.3V of gate bias, the channel is in mild accumulation and this will be enhanced by high-k spacers, resulting in increased drain current. However, when the drain bias is high, the accumulation starts to dominate at a slightly higher gate bias, as the positive drain bias will tend to deplete the channel. Hence, the cross-over occurs at 1.1V of gate bias for a 1V of drain bias. If we can sacrifice some of the OFF current of JLT, by using a lower workfunction metal at gate, we can make the accumulation to dominate at a much lower gate bias to have the advantage of increased ON current.

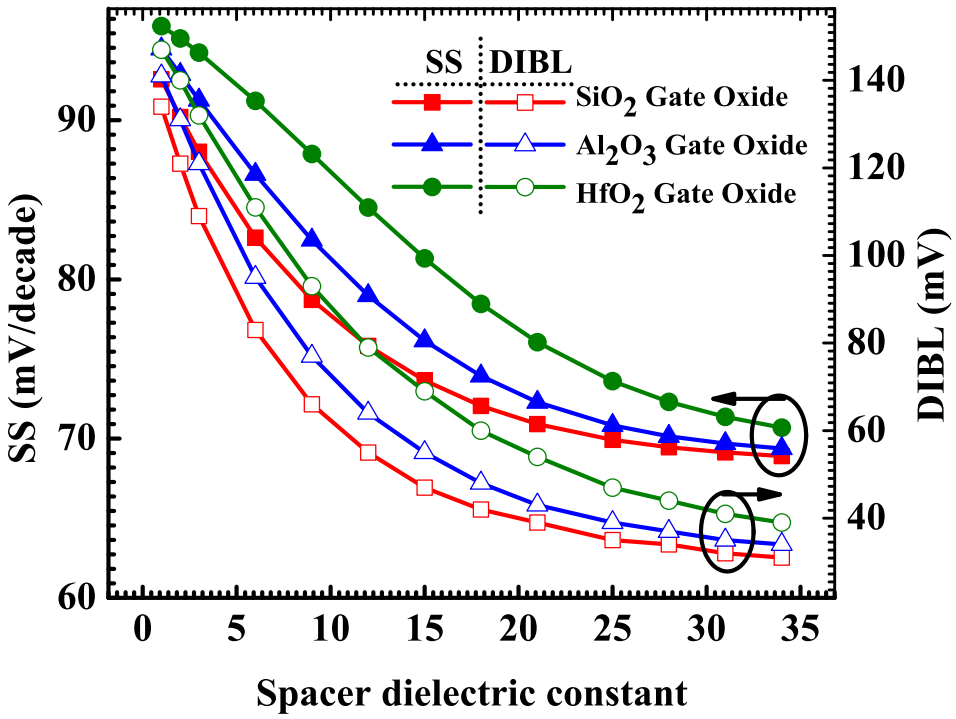


Figure 3.6: Effect of κ_{sp} on subthreshold swing and drain induced barrier lowering.

All the observations made in high-κ spacer device are still valid for devices using high-κ as gate dielectric. However, we observe that the advantage gained is at the maximum with SiO_2 as the gate dielectric and that the gain decreases as the gate dielectric constant is increased. In the inset of Fig. 3.2 we show the ON current to OFF current ratio as a function of κ_{sp} for devices using SiO_2, Al_2O_3 and HfO_2 as gate dielectric. In Fig. 3.6 the variation of DIBL and SS with κ_{sp} of the spacer are shown for three different gate dielectrics. It can be observed that a higher κ_{sp} can give a better electrostatic integrity for the reasons that were already explained. Near ideal SS is obtained with κ_{sp} of 34, whereas the DIBL has dropped to one fourth as the κ_{sp} is increased from 1 to 34.

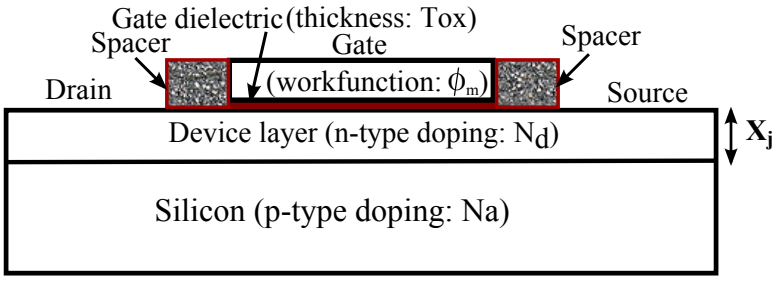


Figure 3.7: Device structure of BPJLT with spacers.

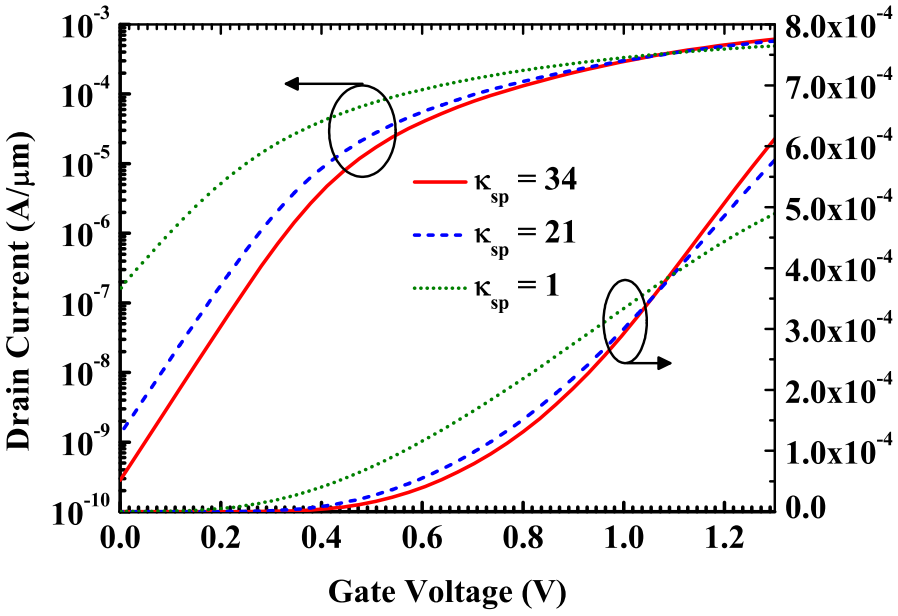


Figure 3.8: I_D - V_{GS} of 20nm channel length BPJLT with high-k spacers. L_g=20nm, X_j = 11nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, κ_{sp}=1, 21 and 34, ϕ_m = 5.0eV, L_{sp} = 15nm.

We evaluate the effect of high-κ spacers for our earlier device proposal, the BPJLT. The structure and I_D - V_{GS} of BPJLT with spacers is shown in Fig. 3.7 and 3.8. It is observed that, while the spacer with κ_{sp}=21 results in a 3 order decrease in the OFF current for SOI-JLT, it is only about 2 orders for BPJLT. The reason for this is the following:

In a SOI-JLT the full control on the channel is from the top gate as there is no bottom gate. Though the BPJLT also have also have a gate only at the top, the substrate of the BPJLT depletes a part of the device layer (as explained in Chapter 3), and acts as a pseudo gate. The spacers were provided only at the top gate and there is no field enhancement due to spacers at the bottom pseudo gate. Hence, we see a reduced effect of high-κ spacers in the BPJLT compared to its SOI counterpart.

We also evaluate the static and dynamic performance of SOI and Bulk junctionless transistors. For this purpose we take the static power consumption, static noise margin of a 6T SRAM cell, average dynamic power and delay as metrics. PMOS transistors were designed for both SOI-JLT and BPJLT to match the characteristics to that of the NMOS counterparts. I_D - V_{GS} of NMOS and PMOS for both for SOI and BPJLT with matched characteristics is shown in Fig. 3.9.

In Fig. 3.10 and 3.11 we show the static power consumptions and butterfly curves of

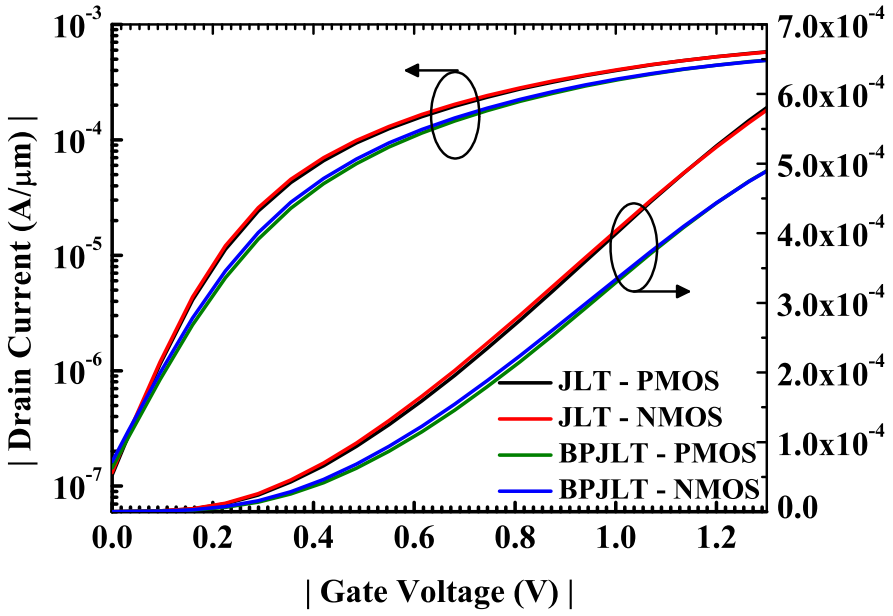


Figure 3.9: I_D - V_{GS} of 20nm channel length NMOS and PMOS of JLT and BPJLT. L_g=20nm, T_{Si} = 6nm, X_j = 11nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, κ_{sp}=1, ϕ_m = 5.0eV (4.26eV) for JLT(BPJLT), L_{sp} = 15nm.

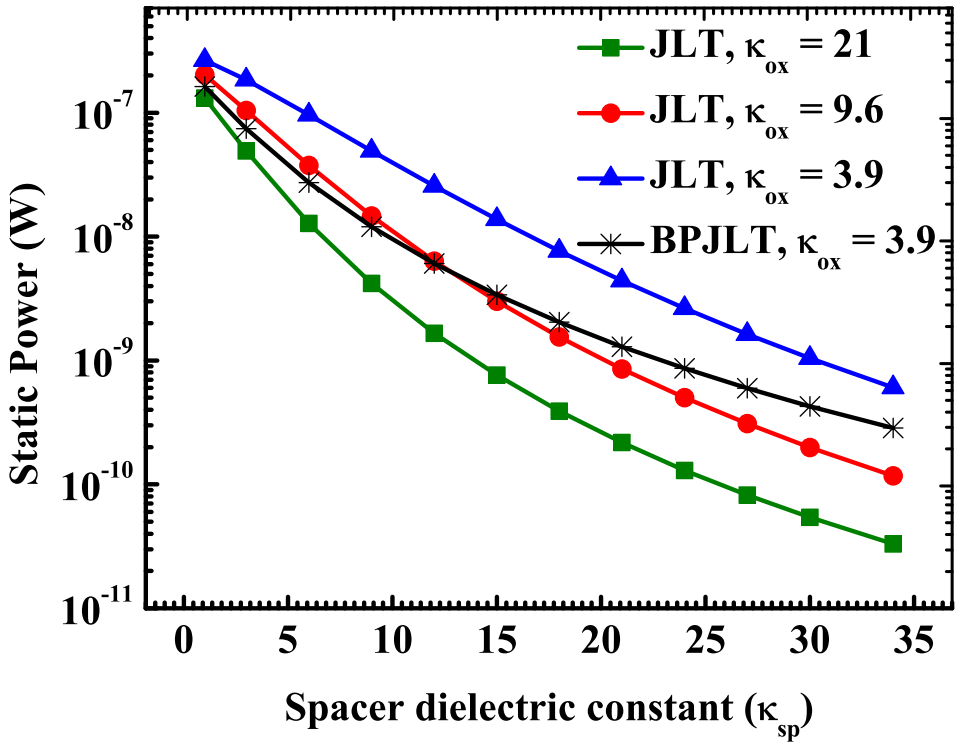


Figure 3.10: Static power consumption Vs. κ_{sp} of JLT and BPJLT with spacers. L_g=20nm, T_{Si} = 6nm, X_j = 11nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, 9.6 and 21, κ_{sp}=1, ϕ_m = 5.0eV (4.26eV) for JLT(BPJLT), L_{sp} = 15nm.

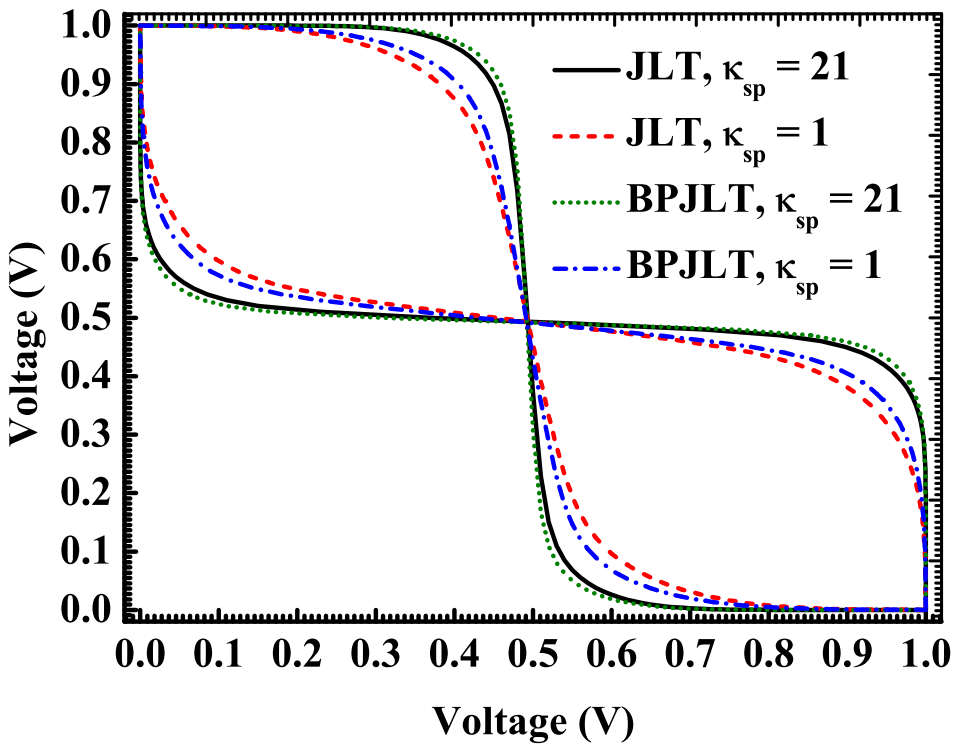


Figure 3.11: Comparison of butterfly curves of 6T SRAM cells using JLT and BPJLT with κ_{sp}=1 and 21. L_g=20nm, T_{Si} = 6nm, X_j = 11nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, κ_{sp}=1 and 21, ϕ_m = 5.0eV (4.26eV) for JLT(BPJLT), L_{sp} = 15nm.

6T SRAM cells using junctionless transistors with spacers. A lower OFF current in a device with high-κ spacers, results in orders of magnitude lower static power consumption. Also, a lower OFF current for a similar ON current comes with an increased threshold voltage and reduced subthreshold slope. An increased threshold voltage will be reflected as an increased noise margin of an 6T SRAM cell. This concludes that the junctionless transistors with high-κ spacers have excellent static behaviour. However, one have to trade the dynamic behaviour to gain the advantage, as explained below.

It is seen from Fig. 3.12 the time period of oscillations of a 3-stage ring oscillator is more for transistors with high-κ spacers. The reason for this is the increased capacitance due to the spacers with high dielectric constant. In Fig. 3.13 we see a gate capacitance with κ_{sp}=21 to be increased by 2.5 times compared to κ_{sp}=1. The increase in gate capacitance reflected as an increase in delay of similar magnitude. In Fig. 3.14 we plot the average power consumption Vs. delay in a 3-stage ring oscillator circuit.

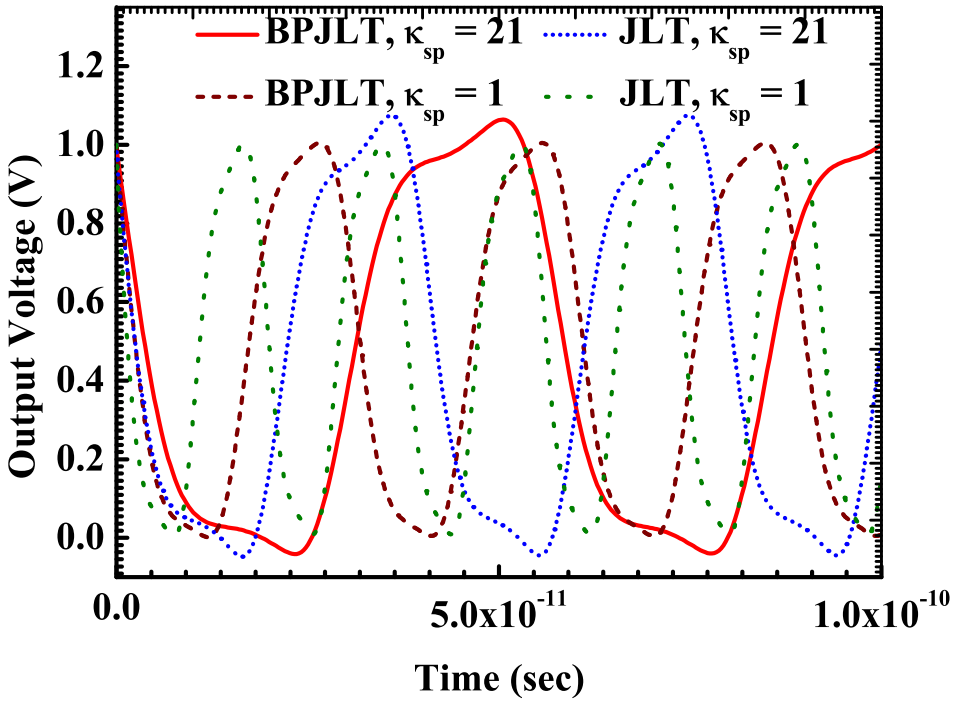


Figure 3.12: Oscillations of a 3-stage ring oscillator using JLT and BPJLT with κ_{sp}=1 and 21. L_g=20nm, T_{Si} = 6nm, X_j = 11nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, κ_{sp}=1 and 21, ϕ_m = 5.0eV (4.26eV) for JLT(BPJLT), L_{sp} = 15nm.

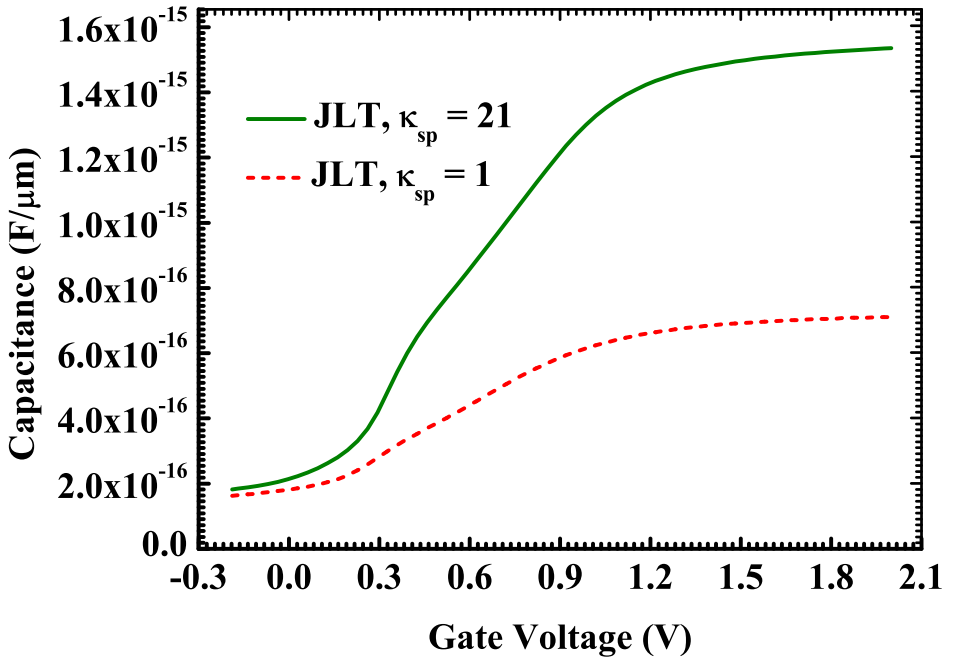


Figure 3.13: C - V_{GS} for a 20nm channel length JLT, with source and drain tied to substrate. L_g=20nm, T_{Si} = 6nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, κ_{sp}=1 and 21, ϕ_m = 5.0eV, L_{sp} = 15nm.

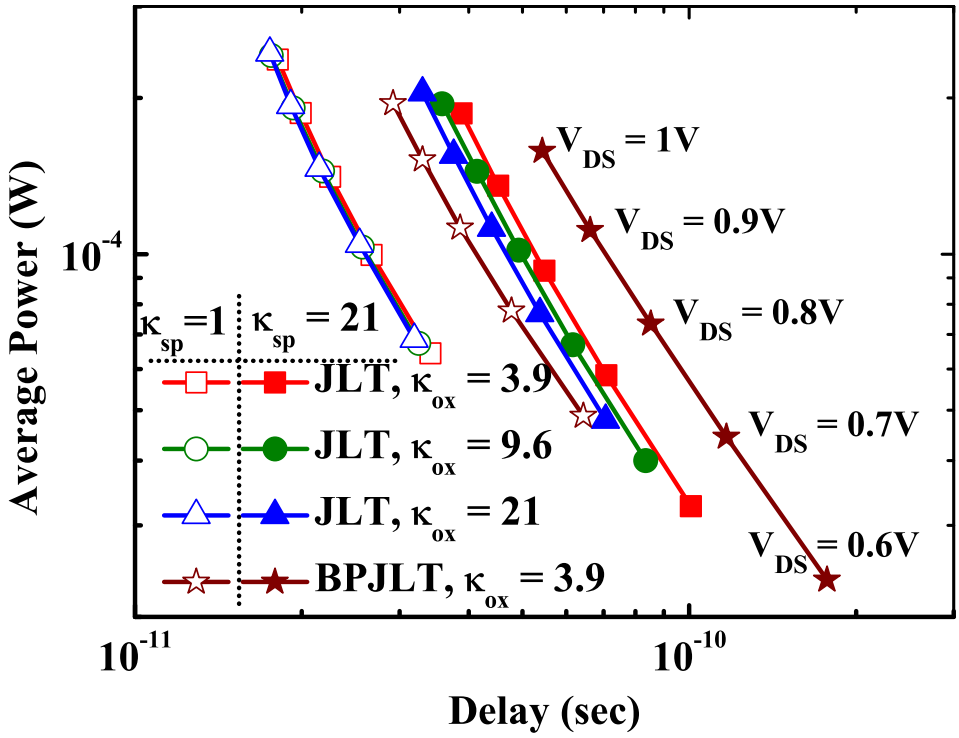


Figure 3.14: Average power consumption in a ring oscillator Vs. Stage delay of JLT and BPJLT with spacers. L_g=20nm, T_{Si} = 6nm, X_j = 11nm, N_d = 2 x 10^{19} cm^{-3}, EOT_{ox} = 1 nm, κ_{ox}=3.9, 9.6 and 21, κ_{sp}=1 and 21, ϕ_m = 5.0eV (4.26eV) for JLT(BPJLT), L_{sp} = 15nm.

3.4 Summary

We have proposed a novel concept of JLT transistors with high-κ spacers, which can improve the electrostatic integrity of the device to a great extent, potentially making the device scalable to extremely short channel lengths. While the OFF state leakage current and static power consumption is reduced by orders of magnitude, its delay need to be traded to gain the advantage. However, as the junctionless transistors are potential devices for low power and low standby power applications, the JLTs with high-κ spacers could be potentially used.

Chapter 4

Effect of quantum confinement on the ON state behaviour of JLT

4.1 Introduction

Although the JLT and the conventional MOSFET are two variants of MOS devices, there is a significant difference in their operating principle, the former operates in flat band and the later in inversion mode during the ON state [2]. The MOSFET, both the single gate and double gate versions, turns ON with the formation of a thin layer of inverted channel (under the gate oxide) between the source-drain, when a positive bias is applied to the gate for n-channel MOSFETs. Continued scaling of the MOSFETs to short channel lengths have forced device designers to use a higher channel doping in order to overcome the short channel effects (SCEs) like drain induced barrier lowering. Increased channel doping of MOSFET results in an increased vertical electric field that translates to sharp band-bending in the semiconductor close to the oxide interface, giving rise to a nearly triangular quantum well there. This leads to a shift of the charge centroid away from the interface, degrading the gate capacitance, inversion charge and thereby the performance of the MOSFETs [17, 36]. The fully depleted double gate MOSFET (FDDG-MOSFET) uses an extremely thin silicon layer for controlling short channel effects. The whole of the silicon film sandwiched between gate dielectrics acts as a quantum well when the film thickness is in the range of 10nm. This leads to similar performance issues as in conventional bulk MOSFETs.

As the JLT operates at flatband in ON state, most of the earlier works on JLT assumed that energy quantization would be insignificant and hence, the classical models without any quan-

tum correction in confinement direction, were used to predict the JLT performance [2, 13, 14, 16, 35]. Here we show that for a MOS capacitor representing the JLT in ON state and operating in flatband, quantization needs to be considered to accurately predict the carrier distribution and gate capacitance [51, 52]. This leads to a reduction in gate capacitance. The ON state current of a long n-channel (p-channel) field effect transistor is proportional to the total integrated electron (hole) concentration in the surface channel. Based on the total integrated carrier density in the vertical direction of the device, our analyses predict that the error in the ON state current depends on the doping and the device layer thickness of the JLT. We also compare the performance degradation of JLT with that of FDDG-MOSFETs, arising from quantum confinement effects. Even though the performance of JLT could degrade due to quantum confinement effects, it is seen that the performance degradation could be significantly smaller than in double gate MOSFETs.

4.2 Results and Discussion

Fig. 4.1(a) shows the typical structure of a double gated n-channel device that is used for computing the capacitance and charge in both the JLT and the MOSFET. It should be noted that the channel of the n-channel MOSFET is p-doped, whereas that of the n-channel JLT is n-doped.

Fig. 4.1 (b) shows the capacitance-voltage plot for a double gate MOS capacitor, with N-type Si doping. In such a MOS structure, the flat-band voltage is +1V and a negative voltage at gate will make the Si body inverted. Computations were carried out for the one dimensional device structure shown in Fig. 4.1 (a) using the SCHRED simulator which solves the Schrödinger and Poisson equations self consistently [53]. The wafer orientation of $\langle 100 \rangle$, two primed and four un-primed sub-bands, longitudinal electron mass of 0.916 m_o and transverse electron mass of 0.196 m_o were assumed in the calculation. Partial ionization and exchange interactions were assumed not to be present. We refer to the Schrödinger-Poisson solution with these parameters as the quantum solution and the Poisson solution as classical. Device structure parameters used are typical of JLTs and are given in the caption to the figure. The large workfunction difference between the channel and gate is required to keep the channel depleted during the OFF state [35]. From Fig. 4.1 (b) it can be observed that the capacitance degrades in the quantum calculation compared to classical calculations when the capacitor is operated in strong inversion, strong

accumulation and also when it operates in flat band.

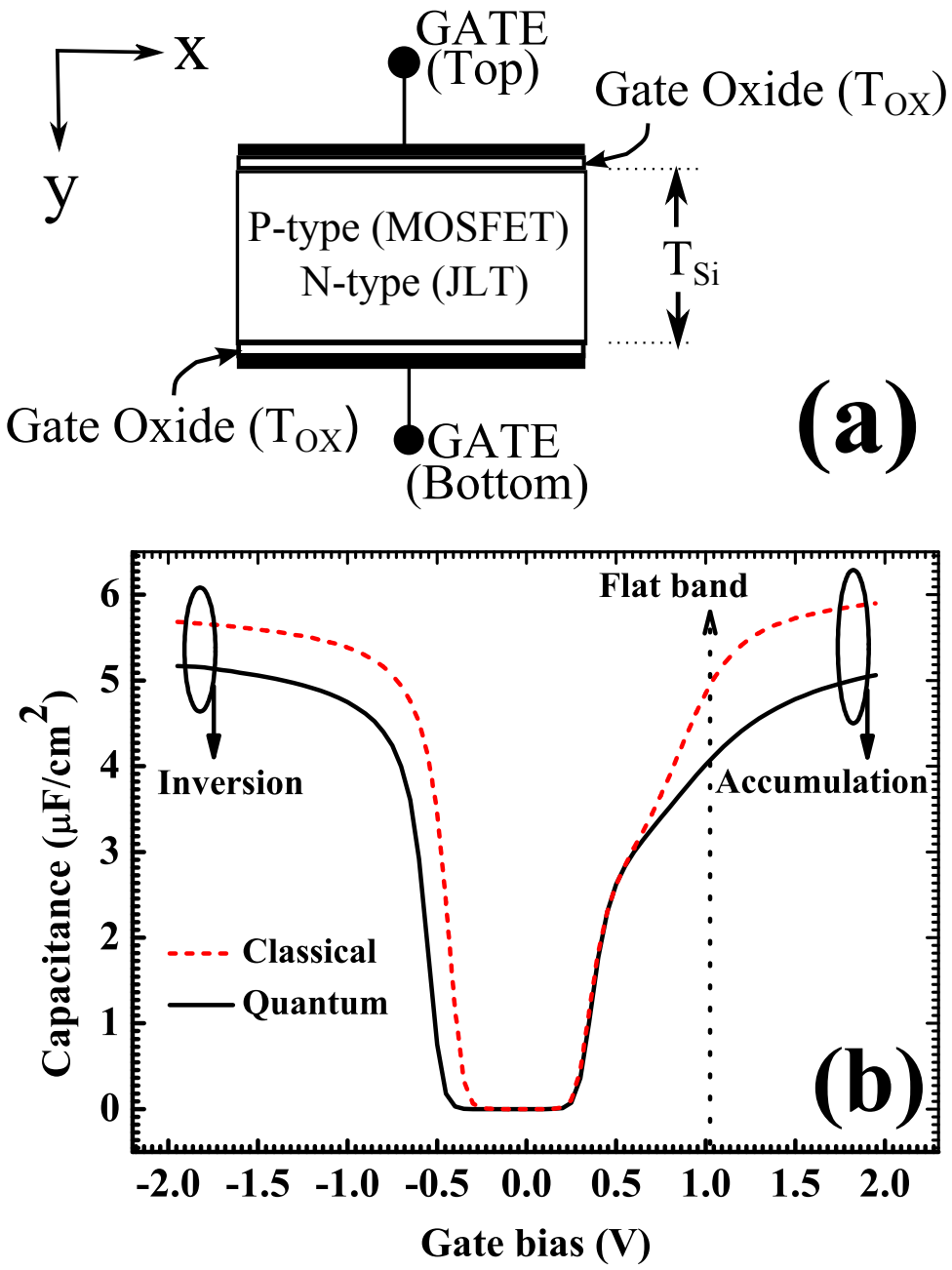


Figure 4.1: (a) Schematic representation of the device cross-section in confinement direction for FDDG-MOSFET and JLT. (b) Capacitance - Voltage characteristics with classical and quantum models for the schematic shown in (a). T_{Si} = 10nm, N_d = 1.5 x 10^{19} cm^{-3}, gate workfunction ϕ_m = 5.1eV, T_{ox} = 1 nm.

Fig. 4.2 shows the electron densities along the confinement direction for a MOS capacitor operating in inversion and flatband. The channel doping chosen here is 1.5 x 10^{19} cm^{-3}, typical

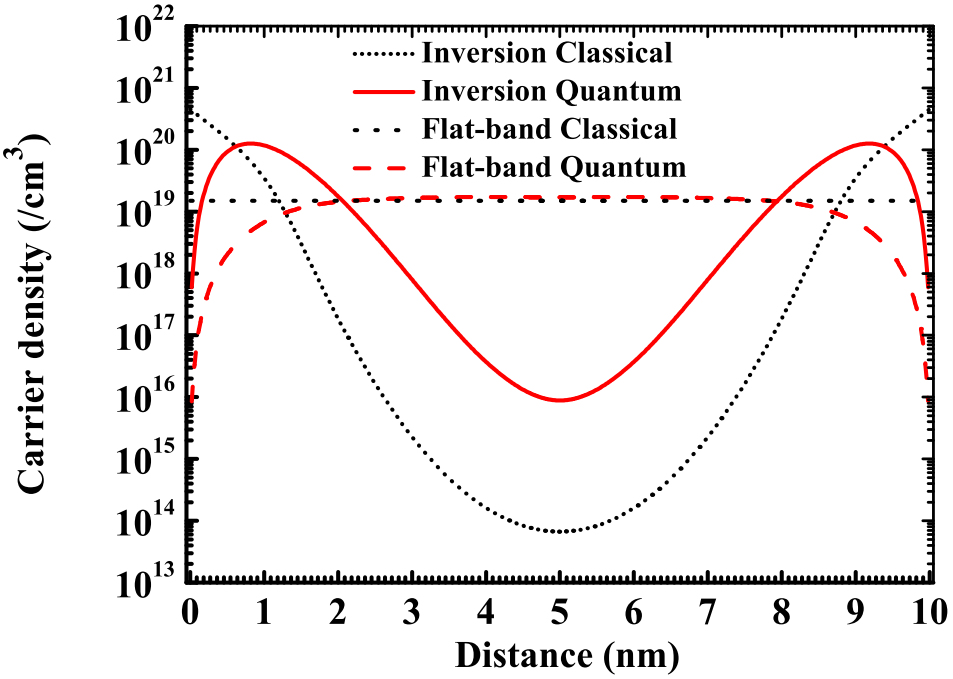


Figure 4.2: Carrier densities along the confinement direction for MOS capacitor operating in inversion and flat-band. T_{Si} = 10nm, N_d = 1.5 x 10^{19} cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm.

doping expected in a 20nm channel length JLT [35]. As expected the peak of the electron density in inversion is shifted away from the surface with a reduced peak density in quantum calculations, when the quantum solution is compared with that of the classical solution obtained from the same simulator. Fig. 4.2 also shows that the electron density profiles that come from classical and quantum calculations differ close to the interface, even in the flat-band condition. This can be attributed to the boundary condition on either side of the device layer (at Si/SiO_2 interfaces) that forces the wavefunction to become very small and this results in the decrease of density of states near the Si/SiO_2 interface.

Since the total integrated electron density in the y-direction of a long channel transistor can be taken as a proxy to the drive current performance of the transistor, the percentage reduction in the integrated electron density from classical to quantum calculations can be considered as a measure of the degradation of the device performance. It can be seen from the flat-band case of Fig. 4.2 that the electron density is lower over a distance of approximately 1nm adjacent to the top and bottom oxide interfaces when quantum confinement effects are considered. This distance amounts to a significant percentage (~ 20%) of total device layer thickness and hence, we observe a degradation in the performance of JLT.

Figure 4.3 (a) shows the percentage reduction in the total integrated electron density in

the channel at ON state for JLT as the doping in the silicon layer is varied for three values of T_{Si}. T_{ox} = 1nm and ϕ_m = 5.1eV. It can be seen that the percentage of degradation is smaller for thicker device layer. The reason is that the relative distance over which the density of electrons decreases is small compared to the device layer thickness for thicker device layer. i.e., the distance over which the states degrade is approximately 2nm, and this amounts to a dominant percentage of T_{Si} for T_{Si} = 5nm than for T_{Si} = 10nm and 15nm. But, at the same time thicker device layer results in increased OFF state current [35]. Hence, there exists a trade-off between the ON current degradation and the OFF state current in JLTs.

The performance degradation in JLT is compared to that in FDDG-MOSFET for various values of T_{Si}. For this purpose the threshold voltages and the subthreshold characteristics of the JLT and FDDG-MOSFET were matched for the classical case by tuning the doping in the JLT for each T_{Si}. T_{ox} = 1nm, ϕ_m = 5.1 eV for JLT and 4.5 eV for FDDG-MOSFET, and FDDG-MOSFET channel doping of 10^{17} cm^{-3} were used. The matching required channel doping values of 3.8 x 10^{19} cm^{-3}, 1.5 x 10^{19} cm^{-3} and 8.1 x ^{17} cm^{-3} for T_{Si} of 5 nm, 10 nm and 15 nm respectively for JLT.

Fig. 4.3 (b) shows the integrated electron density in the vertical direction versus gate voltage for the JLT and FDDG-MOSFET and illustrate the matching for T_{Si} = 5 nm. Fig. 4.4 shows the comparison in the percentage degradation in the total integrated electron density in the ON state for JLT and FDDG-MOSFET as a function of T_{Si}. As the FDDG-MOSFET is operated in inversion, the degradation is found to be independent of T_{Si} in the range of comparison. The JLT shows a significantly lower degradation for matched characteristics. Also the degradation is seen to be sensitive to the device layer thickness in this case. However, the shift in threshold voltage from classical to quantum calculations is similar in both JLT and FD-MOSFET (as seen in Fig. 4.4), this can be attributed to similar degradation in the subthreshold region from classical to quantum calculations (as seen in Fig. 4.3 (b))

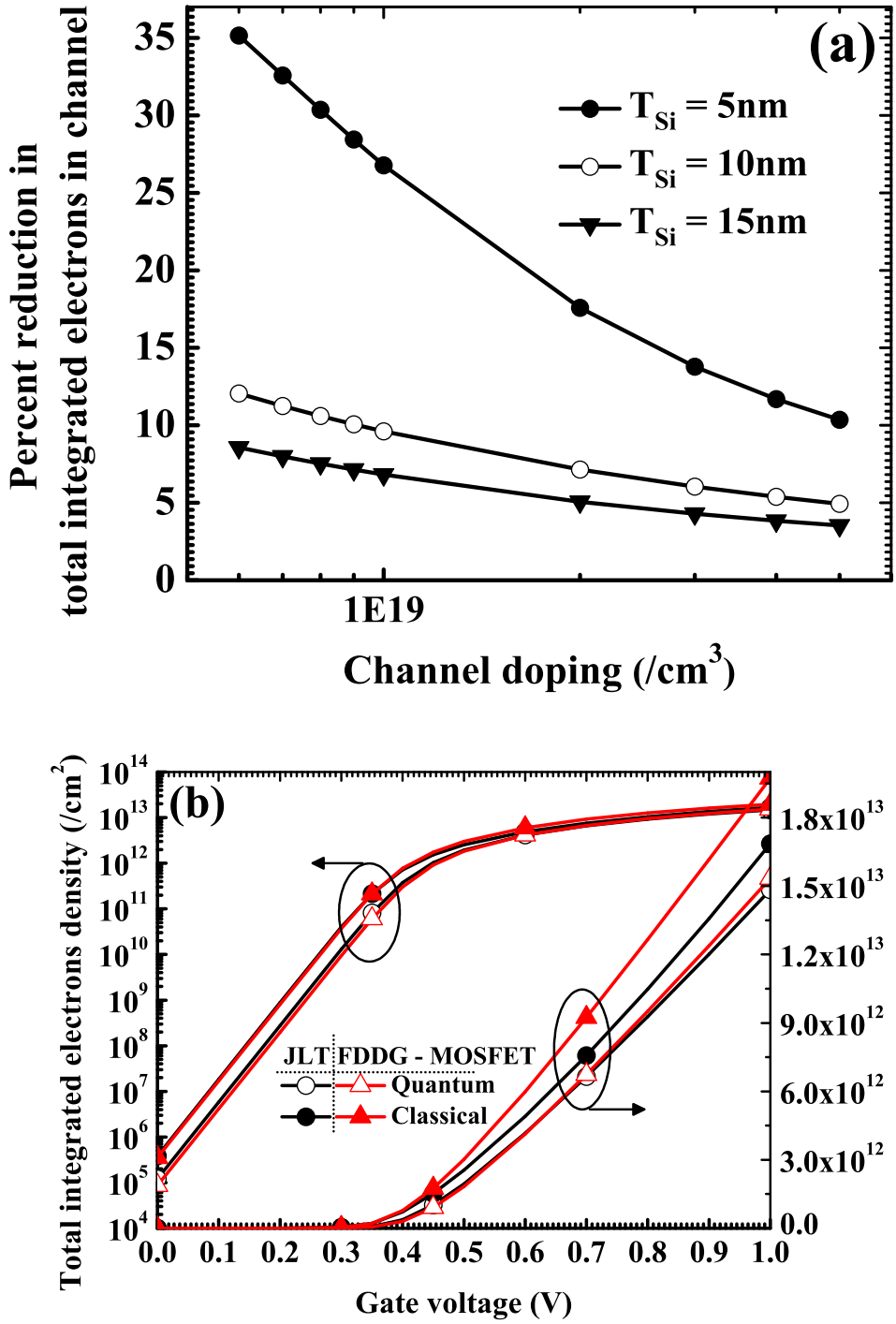


Figure 4.3: (a) Percent degradation of total integrated number of electrons in the confinement direction versus channel doping for JLT. (b) Integrated carrier density along the confinement direction versus gate voltage of JLT and FDDG-MOSFET from classical and quantum calculations, T_{Si} = 5nm, ϕ_m = 5.1eV (4.5eV) for JLT (FDDG-MOSFET), channel doping = 3.8 x 10^{19} cm^{-3} (1 x 10^{17} cm^{-3}) for JLT (FDDG-MOSFET).

Summary

We have shown that similar to the inversion mode FETs, junctionless transistors also suffer from quantization effects despite it being operated in the flat band region during ON state. How-

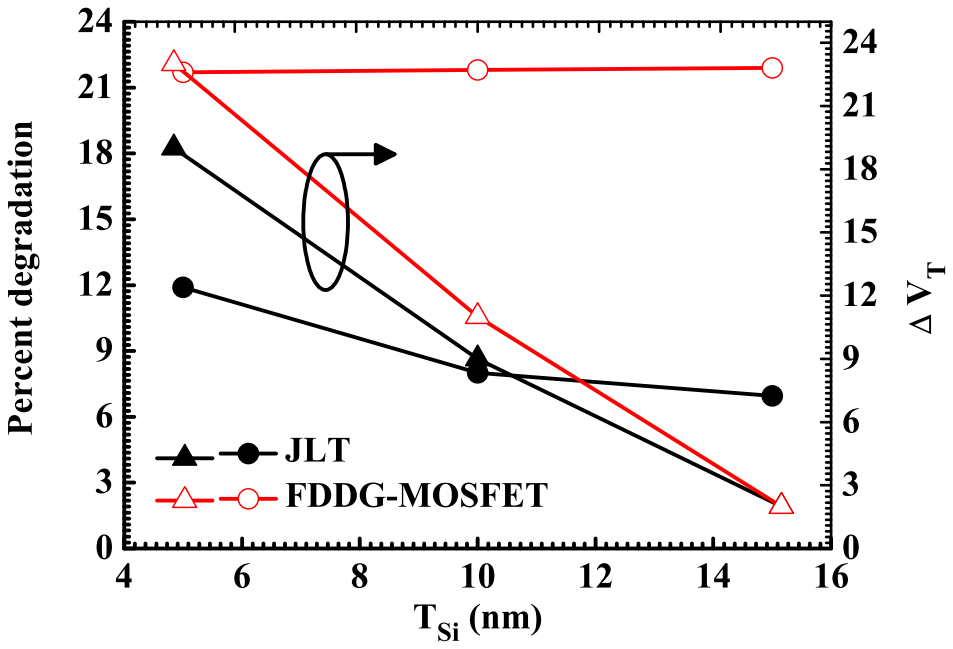


Figure 4.4: Comparison of percent degradation in total integrated electron density in the confinement direction and the shift in threshold voltage versus T_{Si} for JLT and FDDG-MOSFET.

ever, the degradation is smaller in JLTs compared to the conventional FETs. Also, the amount of degradation in JLTs reduces as device layer thickness increases, a requirement contrary to that required for controlling short channel effects.

Chapter 5

Effect of band-to-band tunneling on the OFF state behaviour

5.1 Introduction

Though there are many studies that explore the physics of JLTs [2, 14, 35], the effect of band-to-band tunneling on its characteristics is yet to be explored. It is well known that the gate overlap over the drain increases the valence to conduction band overlap in the direction perpendicular to the channel in a conventional MOSFET, especially in short channel devices with thin gate dielectric, results in a significant BTBT for low gate voltages [54, 55]. The tunneling current in the OFF state of a thin body SOI-MOSFET is known to turn ON the parasitic bipolar junction transistor (BJT) formed by the source, channel and the drain [55–57]. While the band to band tunneling and parasitic transistor actions in MOSFETs are well known, these are yet to be explored in JLTs.

We study in detail the OFF state behaviour of JLTs[58]. We show that the JLT operating in volume depletion in OFF state has a significant overlap between the valence and conduction bands. As the doping of the source-channel-drain regions of JLT is high, the band overlap during OFF state triggers tunneling of electrons from the valence band of the channel to the conduction band of the drain (for n-channel JLT operation). Improperly designed JLT with a thicker device layer (or nanowire diameter of a gate all around JLT) makes the OFF state band-to-band tunneling (BTBT) current very high. We also show that the OFF state leakage current is significantly lower in the bulk planar junctionless transistor (BPJLT). We further carefully investigate the current components in the OFF state and report the constraints on a proper design

Table 5.1: Device parameters used for evaluating the OFF state behaviour

Parameter	**Value**
channel length (L_g)	20nm to 100nm
device layer thickness (T_{Si})	3nm to 8 nm
junction depth (X_j) for BPJTL	12nm
doping (N_d)	10^{19} cm^{-3} to 1.5x10^{19} cm^{-3}
substrate doping for BPJLT (N_a)	5x10^{18} cm^{-3}
EOT of gate dielectric (T_{ox})	1 nm
gate work function (ϕ_m)	5.1 eV
drain bias (V_D)	0.05V to 1.2 V
gate bias (V_G)	-1 V to 1 V

of JLT. Our analysis could explain the OFF state leakage trends observed experimentally [18].

5.2 Device Structure and Simulation set-up

Device structures of the JLT and BPJLT used in the simulations are shown in Fig. 5.1. Parameters used for device simulation of the structures shown in Fig. 5.1 are listed in Table 5.1. The models used for the simulations are calibrated against a long channel, experimentally demonstrated JLT as described in Chapter 2 and also in [17]. We use a non-local band-to-band tunneling (BTBT) model in Sentaurus release E-2010.12 [43] that is well calibrated to the experimental data and this model is being used in the literature to predict the performance of the tunnel FETs [44]. The non-local BTBT model is included in the simulation to take into account the tunneling along the lateral direction (i.e., tunneling of carriers between the source, channel and drain regions) and in the vertical direction (i.e., tunneling of carriers between the n-type device layer and the substrate). The direct tunneling model for gate leakage calculations is turned OFF assuming the high-κ metal gate stack. For thin device layers used in this work, significant quantization can be expected. This can be modeled as an effective increase in the bandgap. The effective bandgap for the ultrathin-body SOI devices simulated here is obtained from [59].

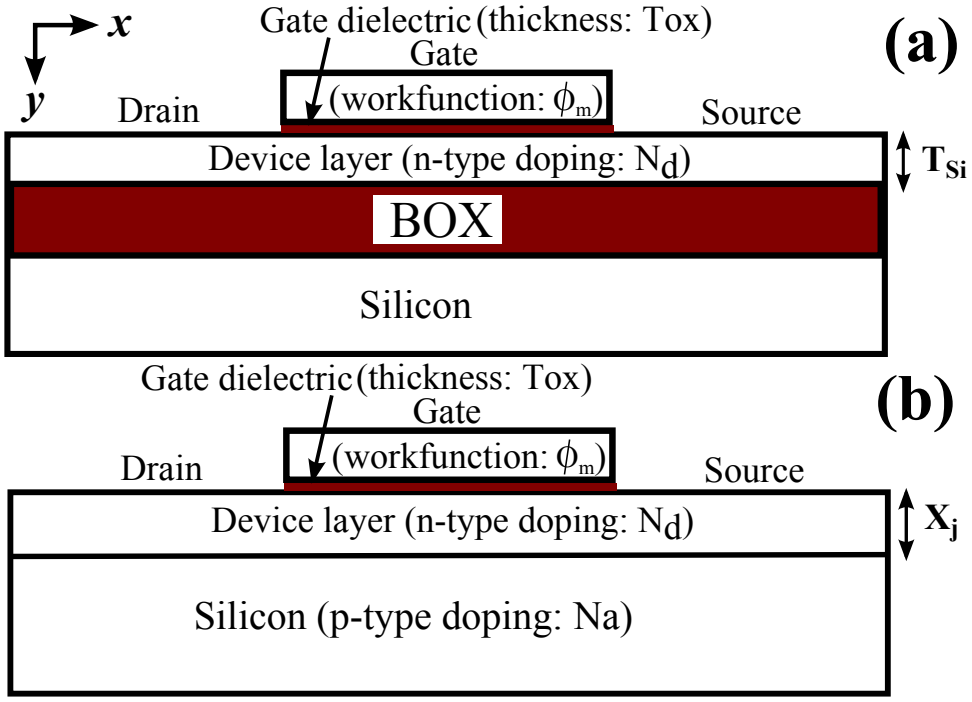


Figure 5.1: Structure of n-channel (a) junctionless transistor (JLT), (b) bulk planar junctionless transistor (BPJLT).

5.3 OFF state behaviour of JLT

The inversion of the channel in conventional MOSFETs, keeps the channel series resistance low during the ON state and hence does not demand for heavy channel doping. As the JLT operates around flatband during the ON state, JLTs have a high channel doping of the order of 10^{19} cm^{-3}, to ensure that the series resistance of the channel is low. While the flat band operation in the ON state of JLTs has several advantages [39], the heavily doped channel need to be volume depleted in the OFF state. The bands in the channel are pulled up for the volume depletion to happen. On the other hand, the gate overlap over the drain extension of inversion mode MOSFETs have a band bending in vertical direction, resulting in band to band tunneling current, well known as a gate induced drain leakage (GIDL) [55]. However, we show the existence of band to band tunneling current in the lateral direction for JLTs, i.e., due to the band overlap between the channel and drain.

Fig. 5.2 shows the typical I_D-V_G characteristics of a 20nm gate length JLT. We can see that the OFF state current computed by taking the band to band tunneling (BTBT) into account, is several orders higher compared to the OFF state current when the BTBT model is absent. Lateral band diagram of the JLT at different gate voltages (Fig. 5.3 (a)), shows a significant band

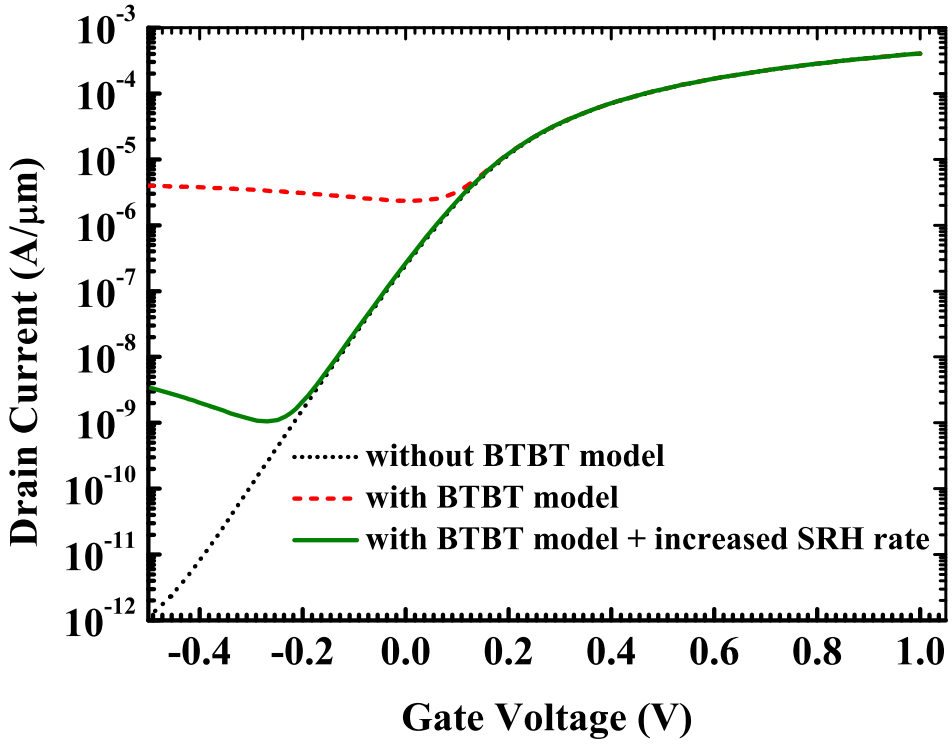


Figure 5.2: I_D-V_G plot for a junctionless transistor (JLT), with and without band to band tunneling model. Also shown is the I_D-V_G when Shockley-Read-Hall (SRH) recombination rate is made high, so as to keep the diffusion length of the carriers less than the channel length. L_g=20nm, T_{Si} = 6nm, $N_d = 10^{19}$ cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, V_D = 1V, carrier life times are set to 10^{-7} sec, this is corresponding to the life times at a doping of $\sim 10^{19}$ cm^{-3} [60] and are set to 10^{-15} sec for the high SRH recombination case.

overlap between the channel and drain regions for gate voltages less than 0V. The minimum tunneling width between the channel and the drain regions at V_G = 0 V, is measured to be approximately 7nm. This initiates tunneling of electrons from the valence band of the channel to the conduction band of the drain leaving behind holes in the channel region. However, from the band diagram in the y-direction (Fig. 5.3 (b)), at the point of maximum tunneling rate (5Å away from the drain and into the channel), show no band overlap in the vertical direction. This suggests that the BTBT is in the lateral direction. This is unlike the GIDL current of inversion mode MOSFETs - where the tunneling is in the vertical direction [55].

Holes generated in the channel because of electrons tunneling from channel to drain, are seen to be accumulated in the channel, as there exists a barrier for holes to flow from channel to the source. The hole accumulation in the channel is illustrated in Fig. 5.4, where we show the hole concentration in the channel region of JLT when simulated with (Fig. 5.4 (a)) and without (Fig. 5.4 (b)) the BTBT model at a gate bias of 0V. We observe a huge difference in

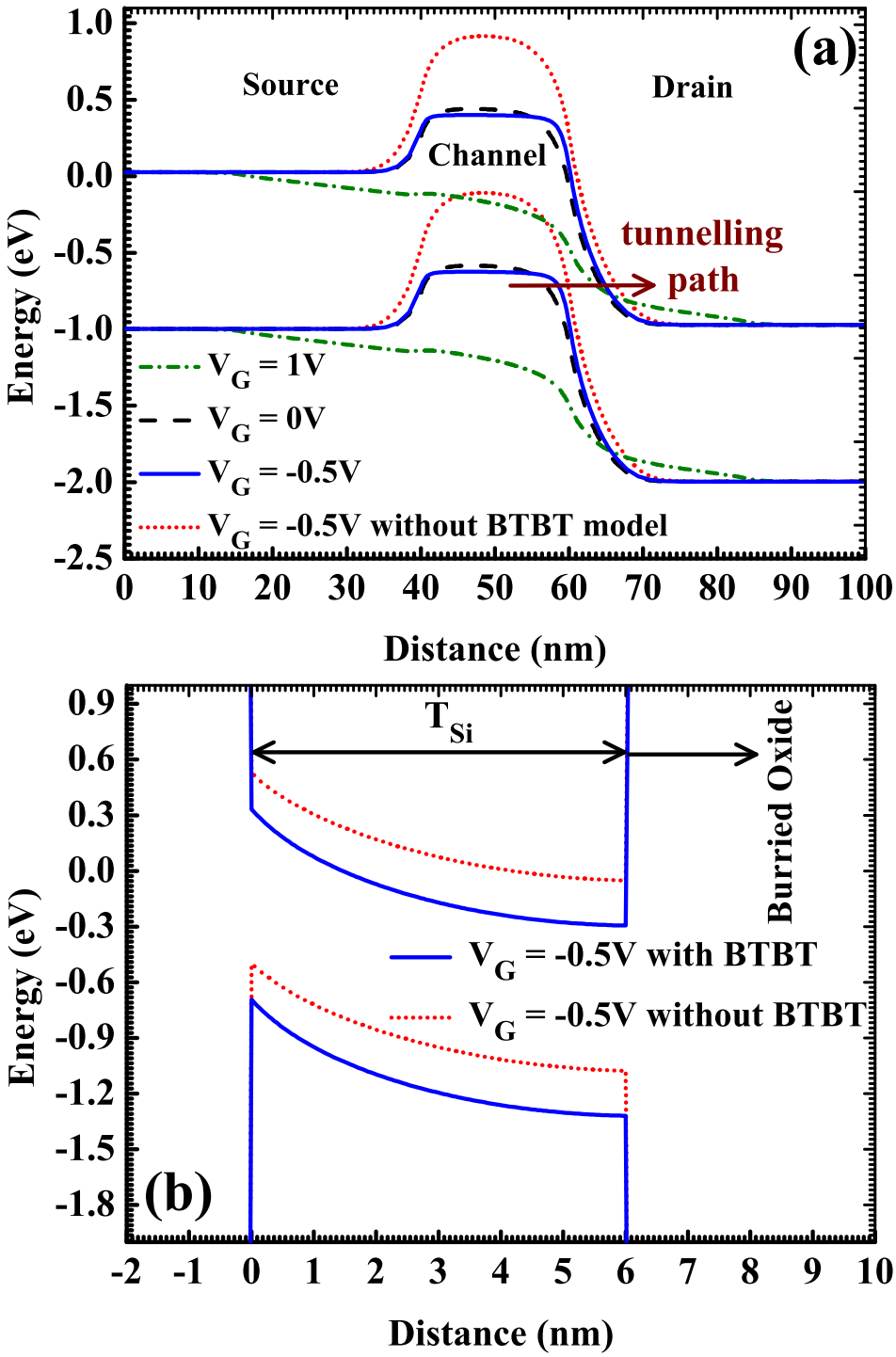


Figure 5.3: (a) Band diagram in the lateral direction for a junctionless transistor (JLT) at several gate voltages, with band to band tunnel model included in the simulation. We have included the band diagram at V_G = -0.5V when the band to band tunnel model is not included. (b) vertical band diagram (in the y-direction), at the point of maximum tunneling rate (5Å away from the drain and into the channel). L_g=20nm, T_{Si} = 6nm, N_d = 10^{19} cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, V_D = 1V.

the hole concentration in the channel, due to the tunneling of electrons from the channel to drain. The band diagram of the n-type source, depleted channel and n-type drain regions look similar to that of a n-p-n BJT. Hence, we expect a parasitic BJT action taking place in the lateral direction. The schematic of the parasitic n-p-n BJT is chown in Fig. 5.4 (c). Holes accumulated in the floating body channel of the JLT, forward biases the source-channel junction which is the emitter-base of the lateral parasitic n-p-n BJT. The forward biased source-channel junction eventually turns ON the parasitic n-p-n BJT, resulting in a heavy drain current (collector current of the BJT). Once the BJT is triggered, any further decrease in gate bias will increase hole concentration and thereby increases the floating body potential (observed as a downward shift of bands of Fig. 5.3(b), when BTBT is included). This saturates the source to channel barrier height. It is observed from the lateral band diagram in Fig. 5.3, that the BJT is triggered ON at 0V of gate bias due to the small tunneling width and further decrease in gate bias to -0.5V does not increase the source to channel barrier height. This is reflected in the I_D-V_G (Fig. 5.2) as a saturating drain current at a gate bias of 0V and lower. On the other hand, in simulations without the BTBT model, decreasing the gate voltage from 0V to -0.5V would increase the barrier by $\sim$0.5V supporting the hole build up and parasitic BJT model described above, resulting in a $\sim$5 order decrease in drain current.

To further explore the parasitic transistor action, the gain of the lateral parasitic BJT is reduced by reducing the diffusion length of carriers in silicon i.e., by increasing the Shockley-Read-Hall (SRH) recombination rate. Lifetime engineering is widely used to obtain fast switching performance in bipolar power devices [61]. In practice, the carrier lifetime is lowered by introducing deep levels in silicon, this include, adding noble metal impurities like gold or platinum and low-dose irradiation of electron, proton or helium in silicon [61]. In our simulations, the lifetime of carriers is reduced to 10^{-15} seconds to shorten the diffusion length of carriers to $\sim$2nm, i.e., $\sim$10 times shorter than the gate length of the simulated device. We notice from Fig. 5.2 that the OFF state leakage current is lower by orders of magnitude when the SRH recombination rate is high, i.e., the OFF state tunneling is lower when the diffusion length is shorter than the channel length of JLT.

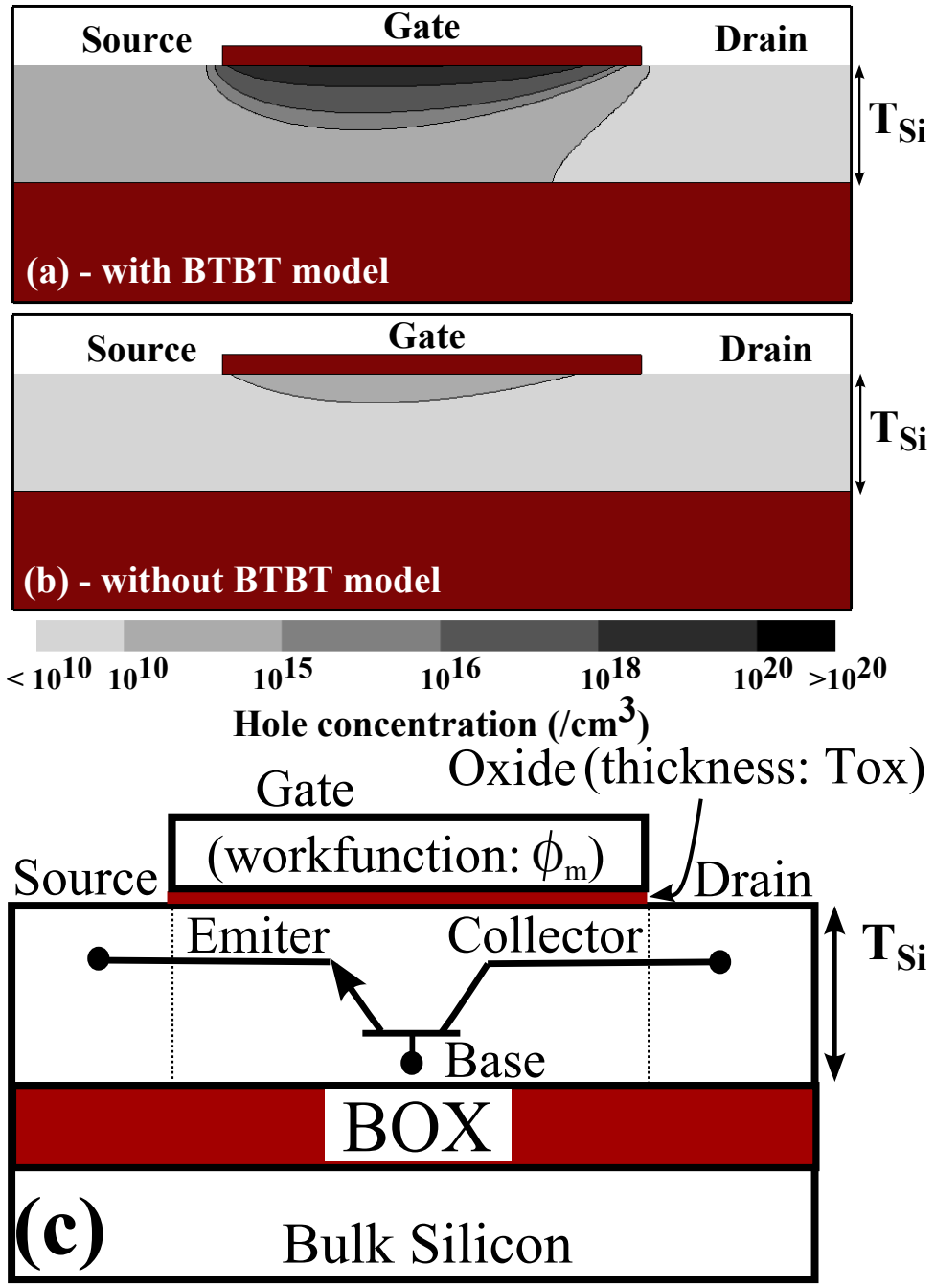


Figure 5.4: 2-dimensional contour plot for hole concentration in the channel region when band-to-band tunneling model is (a) included (b) not included. (c) schematic representing the parasitic bipolar junction transistor (BJT) formed in the lateral direction. L_g=20nm, T_{Si} = 6nm JLT, N_d = 10^{19} cm^{-3}, ϕ_m = 4.6eV (5.1eV) for JLT (FD-MOSFET), T_{ox} = 1 nm, V_G = 0V, V_D = 1V.

5.4 Optimization of the OFF state behaviour of JLT

As established in the previous section, band to band tunneling has a large impact on the OFF state current for a JLT. A careful design is essential to achieve a reasonable I_{ON} to I_{OFF}

ratio. In this section we discuss various options for reducing the effect of BTBT current in the OFF state characteristics.

5.4.1 Dependence of OFF state current on device layer thickness

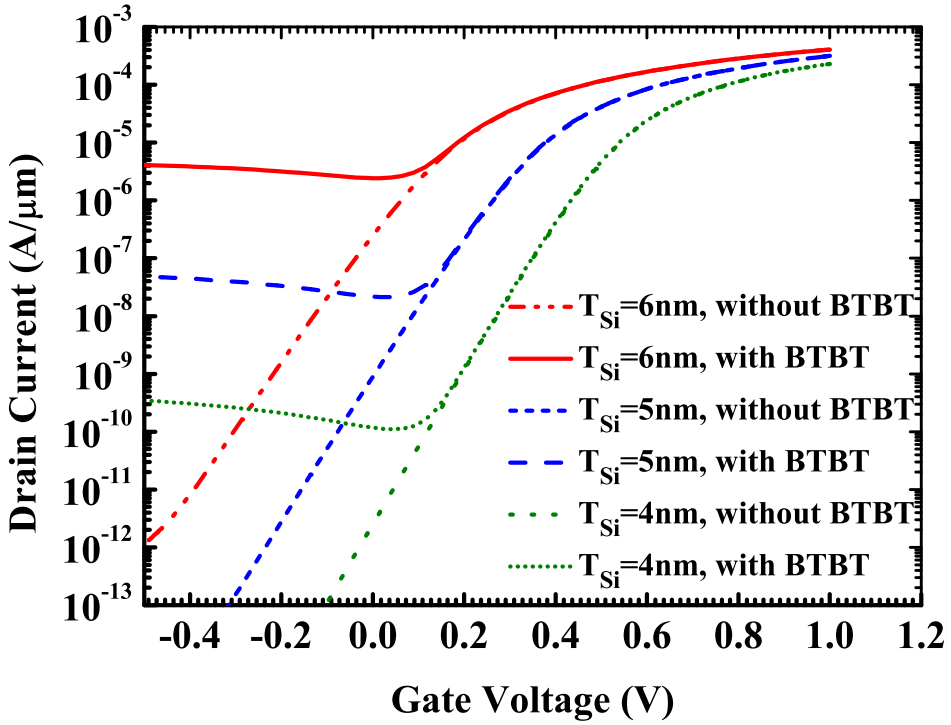


Figure 5.5: I_D-V_G plot for a JLT with several device layer thicknesses. L_g=20nm, T_{Si} = 4nm, 5nm and 6nm, $N_d = 10^{19}$ cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, V_D = 1V.

In Fig. 5.5 we show the I_D-V_G of JLT for device layer thicknesses (T_{Si}) = 4nm, 5nm and 6nm. It is observed that the JLT with thin device layer (T_{Si}) has a higher threshold voltage and a lower OFF current compared to the device with thicker T_{Si}. Reduction in OFF current with decreased T_{Si} is due to the fact that the lateral band to band tunneling from the channel to the drain is lower for JLT with thin device layer. This can be further explained as follows:

1. The device with a thick T_{Si} has a higher drain induced barrier lowering (DIBL) at the source/channel edge. It is observed in Fig. 5.6 (a) that the source to channel barrier height at 0V is lower for the JLT with thicker T_{Si}. This is reflected as a high OFF state leakage current, even with out tunneling. Also, triggering of the parasitic BJT would become easier with a lower barrier between the source and channel.

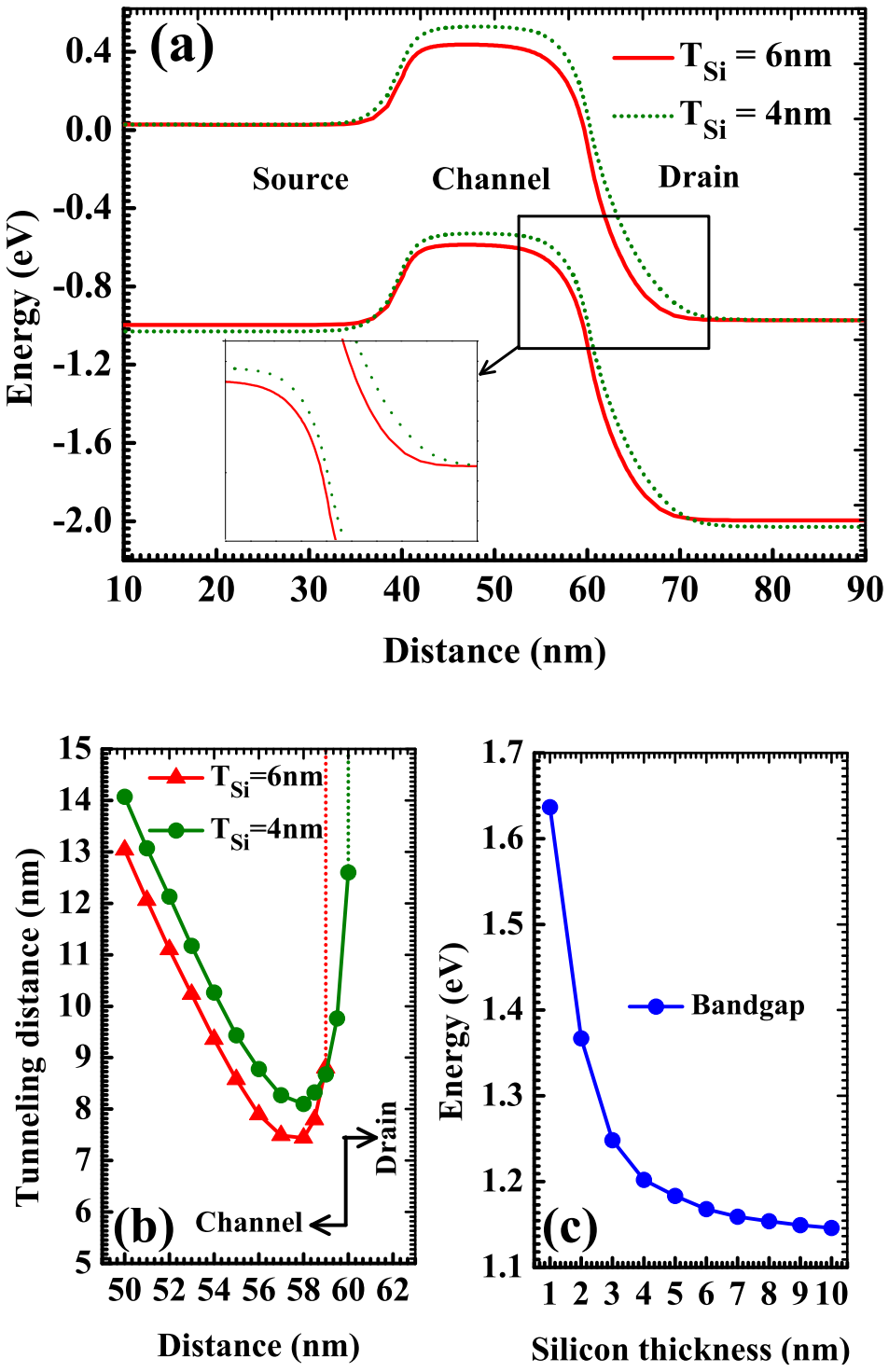


Figure 5.6: (a) Band diagram along the lateral direction (x-direction, source-channel-drain) of the device taken 5$\AA$ away from the gate dielectric, with BTBT model included in the simulation (b) tunneling width versus the distance along the channel for devices with T_{Si} = 4nm and 6nm (c) bandgap Vs. silicon body thickness obtained from [59]. L_g=20nm, T_{Si} = 4nm, 5nm and 6nm, $N_d = 10^{19}$ cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, V_D = 1V, V_G = 0V

2. As the JLT with thick T_{Si} suffer higher drain control over the channel, the tunneling barrier width observed between the channel and drain would be slightly lower in comparison to devices with thin T_{Si}. Tunneling width is measured as a minimum distance between the valence band maxima at a given point in the channel to the conduction band minima in the drain. In Fig. 5.6 (b), we plot the tunneling width versus the distance along the channel for devices with T_{Si} = 4nm and 6nm. We observe the tunneling width to be lower by $\sim$1nm at all points along the channel, for device with T_{Si} = 6nm compared to device with T_{Si} = 4nm.

3. The higher effective bandgap of silicon for extremely thin silicon films (as shown in Fig. 5.6 (c)), due to energy quantization, results in the reduced tunneling current. Though this effect is nominal in the range of T_{Si} shown in Fig. 5.6 (a) ($\sim$60 meV increase in effective bandgap for T_{Si}=4nm), this will be very important while predicting the OFF state current of JLTs for $T_{Si} < 4$nm.

Our observations of the OFF state current leakage current dependence on the silicon body thickness could explain the trend reported from experiments [18], shown in Fig. 5.7 for reference. It can be observed that for a given channel doping, channel length and gate dielectric thickness, the OFF state currents are strongly dependant on the diameter of the nanowire.

5.4.2 Dependence of OFF state current on drain voltage

Though the JLT suffers heavy OFF state leakage, it can be brought into control if it can be operated at a lower drain voltage. In Fig. 5.8 (a), we show the I_D-V_G plot for a 20nm channel length JLT operated for several drain bias. The reason for this is as follows:

It is observed from Fig. 5.8 (b), a lower drain bias reduces the overlap between the channel valence band and the conduction band of the drain, this in turn lowers the OFF state leakage current. The required amount of band overlap for the BTBT current to dominate the thermal leakage current is attained at a lower gate voltage for a lower drain bias. It is also noted that for extremely low drain bias (say 0.05V), there is no channel to drain band overlap in the operating gate voltage range, making the drain current drift-diffusion dominated in the full gate voltage range.

This suggests that the JLT may be more useful device for low drain voltage/low power applications.

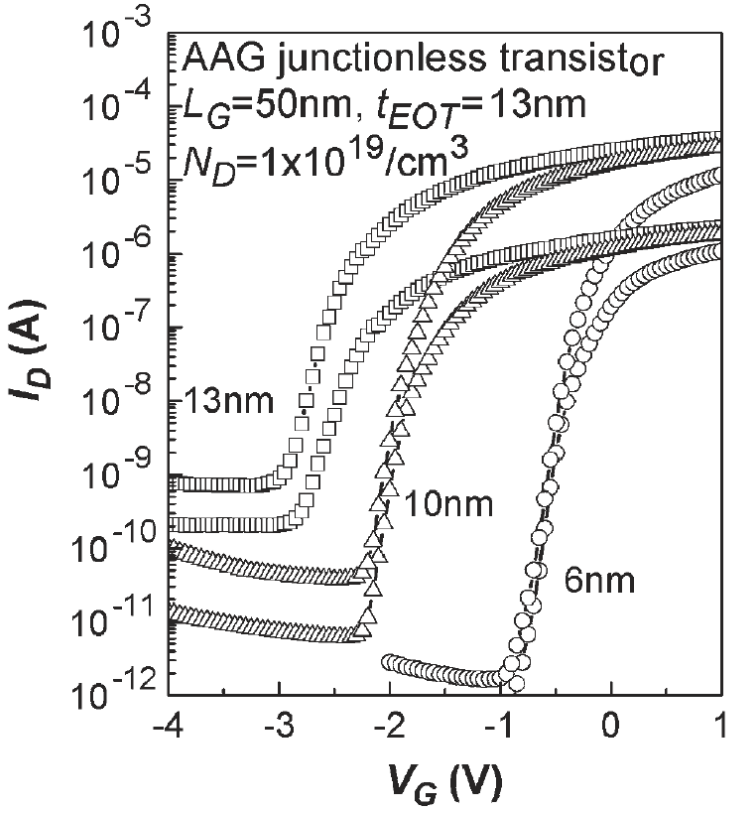


Figure 5.7: (a) I_D-V_G plot for a nanowire junctionless transistor with a varying nanowire diameter[18].

5.4.3 Dependence of OFF state current on channel length of JLT

In Fig. 5.9, we show the I_D-V_G plot for 20nm, 50nm and 100nm channel length JLT with T_{Si} = 6nm. We observe that the OFF current is higher for a 20nm channel length JLT when compared to that of 50nm and 100nm. The reasons for this are, as follows:

1. For a given T_{Si}, the device with shorter channel length suffers higher DIBL in comparison with a long channel JLT. As mentioned in Section 5.4.1, higher DIBL lowers the tunneling width and would facilitate easy turn ON of the parasitic BJT. Hence, a higher OFF current for a short channel JLT.

2. In addition to the DIBL effect, a base of the parasitic BJT is wider for a long channel JLT. A wider base has more recombinations happening in it, this results in a reduced gain of the BJT and hence, a lower OFF current.

For channel lengths as long as 1μm, the DIBL would be almost negligible and also, the diffusion length comes in comparison with the channel length. Hence, in a very long channel

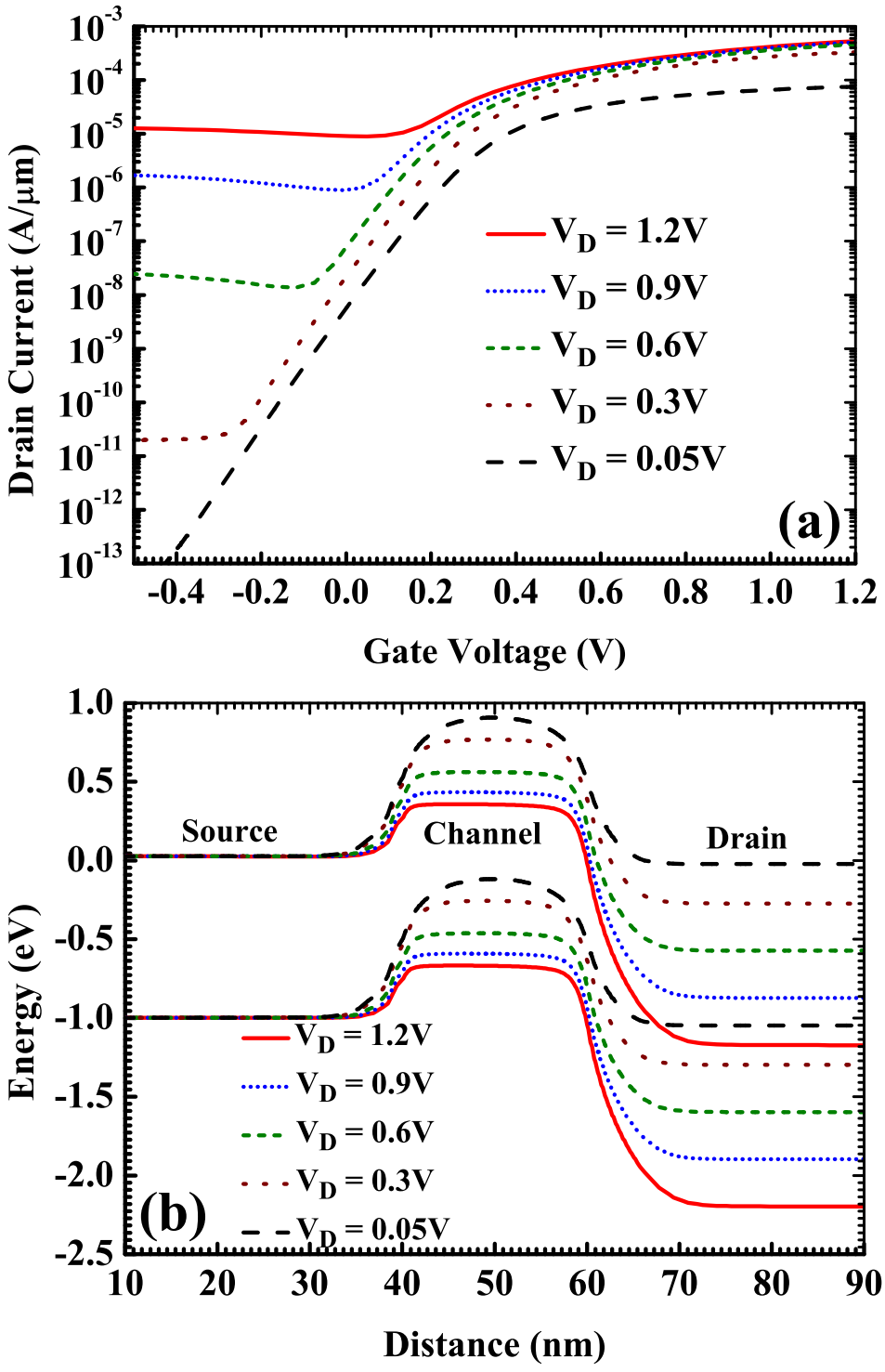


Figure 5.8: (a) I_D-V_G plot for a junctionless transistor at different drain voltages. (b) lateral band diagram at V_G=-0.4V for different drain voltages. T_{Si} = 6nm, N_d = 10^{19} cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, V_D = 0.05V to 1.2V.

length ($\sim 1\mu$m) device, we would not expect any parasitic BJT action taking place [2].

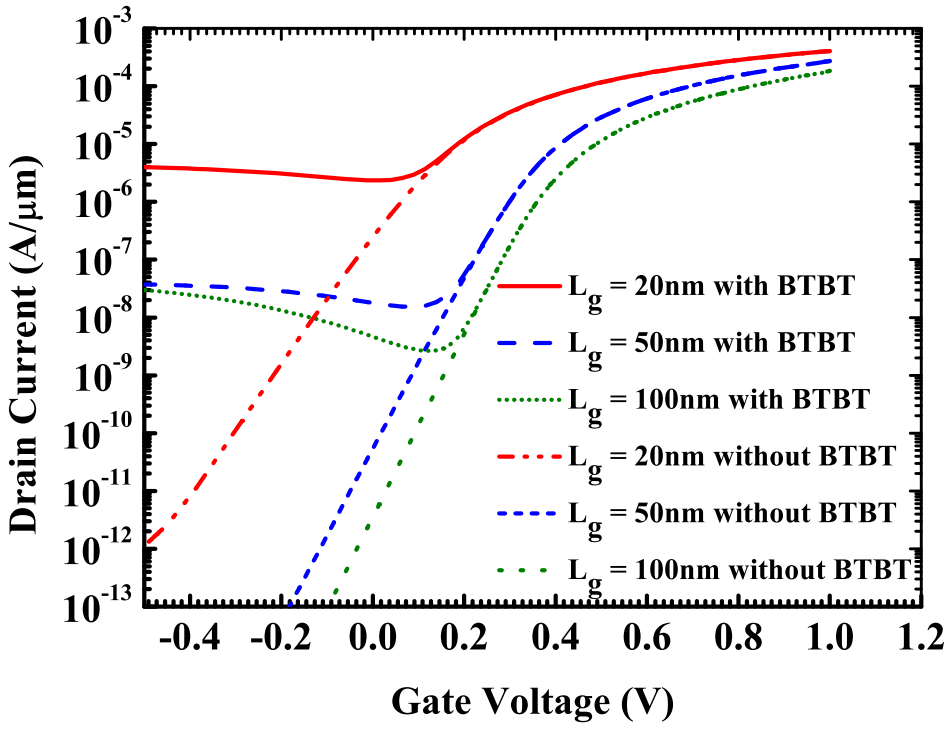


Figure 5.9: I_D-V_G plot for a junctionless transistor with channel lengths of 20nm, 50nm and 100nm. T_{Si} = 6nm, N_d = 10^{19} cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, V_D = 1V.

5.4.4 Dependence of OFF state current on the channel doping

Fig. 5.10 shows the OFF current and I_{ON}/I_{OFF} as a function of T_{Si} for several channel dopings. Fully depleting the channel would be difficult for a thick T_{Si} or for a high channel doping (N_d), hence, the DIBL and band-to-band tunneling are higher in these cases, leading to a high OFF state current (Fig. 5.10 (b)). A careful choice of T_{Si} and N_d should be made for an optimum value of ON current, OFF current and their ratio. In Fig. 5.10 (b), we show the ratio of ON to OFF current, as a function of T_{Si} and N_d. A reasonable ON to OFF ratio ($\sim 10^5$ to 10^6) can be achieved with N_d of $\sim 10^{19}$ cm^{-3} along with a T_{Si} of $\sim$5nm. Though we have shown the channel design space (Fig. 5.10 (b)) for a drain voltage of 1V with normal silicon carrier life times, reducing the life time of carriers or reducing the operating drain voltage can further increase the room for optimum JLT characteristics.

5.5 OFF state behaviour of BPJLT

In this section we evaluate the OFF state behaviour of the bulk device that we proposed in Chapter 2 . In Fig. 5.11, we show the I_D-V_G plot for a typical BPJLT, when simulated with

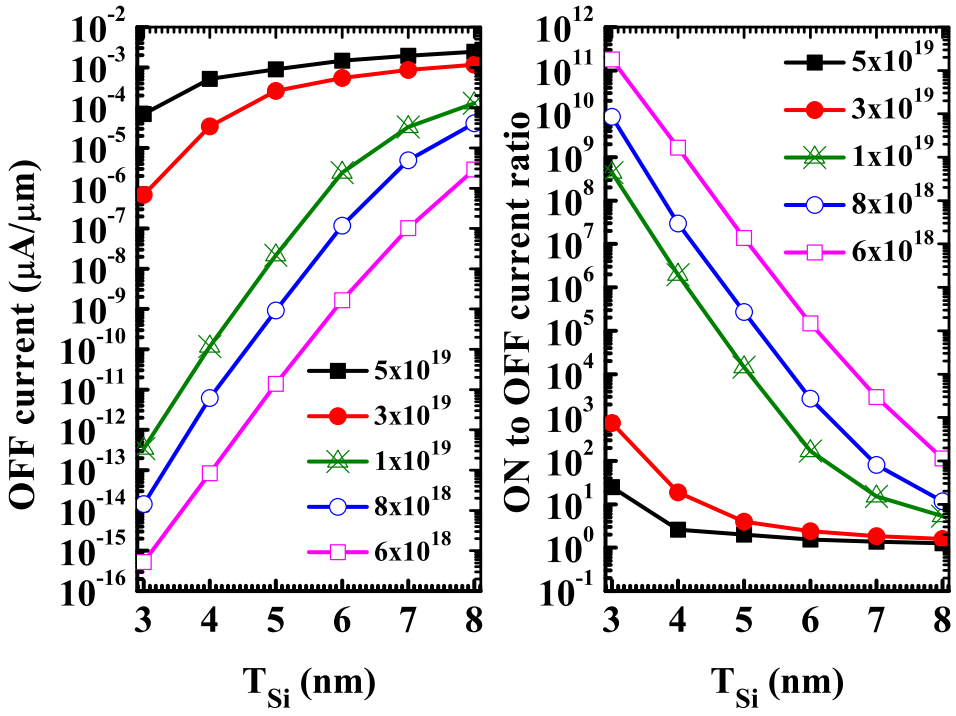


Figure 5.10: (a) OFF state current at V_G = 0V, (b) ON to OFF current ratio for a JLT. L_g=20nm, T_{Si} = 3nm to 8nm, N_d = 6x10^{18} cm^{-3} to 5x10^{19} cm^{-3}, ϕ_m = 5.1eV, T_{ox} = 1 nm, V_D = 1V, with BTBT model.

and without BTBT model included. The device is designed so that its OFF current is similar to that of the JLT with T_{Si} = 6nm (Fig. 5.2). We observe that the OFF state tunneling leakage dominates the drift - diffusion current approximately at -0.3V (this is 1.3V volts lower than the flatband voltage). On the other hand the BTBT current in the JLT with T_{Si} = 6nm starts to be dominant at +0.1V (this is 0.9V lower than the flatband voltage). This indicates that the tunneling current and hence the parasitic BJT action in the BPJLT are less dominant than in that of the JLT, i.e., the gain of the parasitic BJT is less in BPJLT. The reason for reduced parasitic BJT action in BPJLT compared to the JLT is explained as follows:

It was explained in section III that the hole accumulation in the channel of JLT, turns ON the parasitic BJT, increasing the leakage current. However in a BPJLT, the holes generated due to BTBT, are also near the depletion region of the substrate - channel junction. The built-in field of the vertical junction would sweep away the holes to the substrate. We observe from the schematic of parasitic BJT shown in Fig. 5.4 (c), that there is no such provision for the JLT. Hence there would be less accumulation of holes in the channel region and hence the reduced BJT action and reduced OFF state leakage in BPJLT. We show in Fig. 5.12 the 2-dimensional plot for hole concentration in the channel regions of JLT and BPJLT at a gate bias of 0V. As it

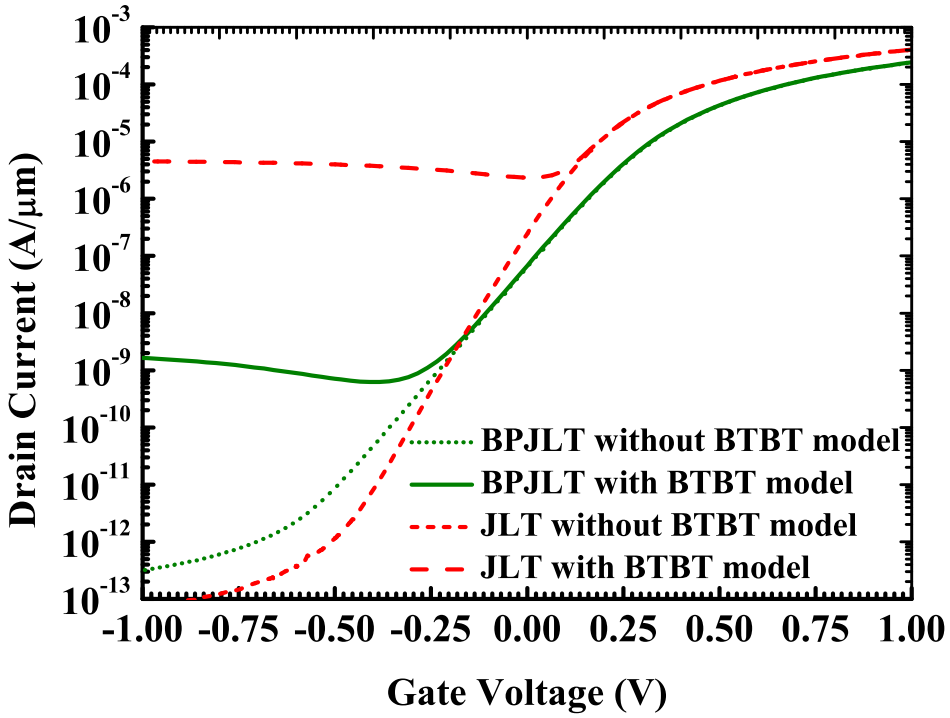


Figure 5.11: I_D-V_G plot for a bulk planar junctionless transistor (BPJLT) with and without tunnel model. L_g=20nm, X_j = 12nm, T_{Si} = 6nm, N_d = 10^{19}($1.5x10^{19}$) cm^{-3} - uniform doping (peak doping) for JLT (BPJLT), ϕ_m = 5.1eV, T_{ox} = 1 nm, V_D = 1V.

was explained, we see the hole accumulation in the channel of bulk device is much lower when compared to its SOI counter part. We also observe, the magnitude of current at 0V of gate bias for BPJLT being un-effected by the tunneling leakage. Hence, the design space for BPJLT we discussed in Chapter 2, is valid even when BTBT is taken into account.

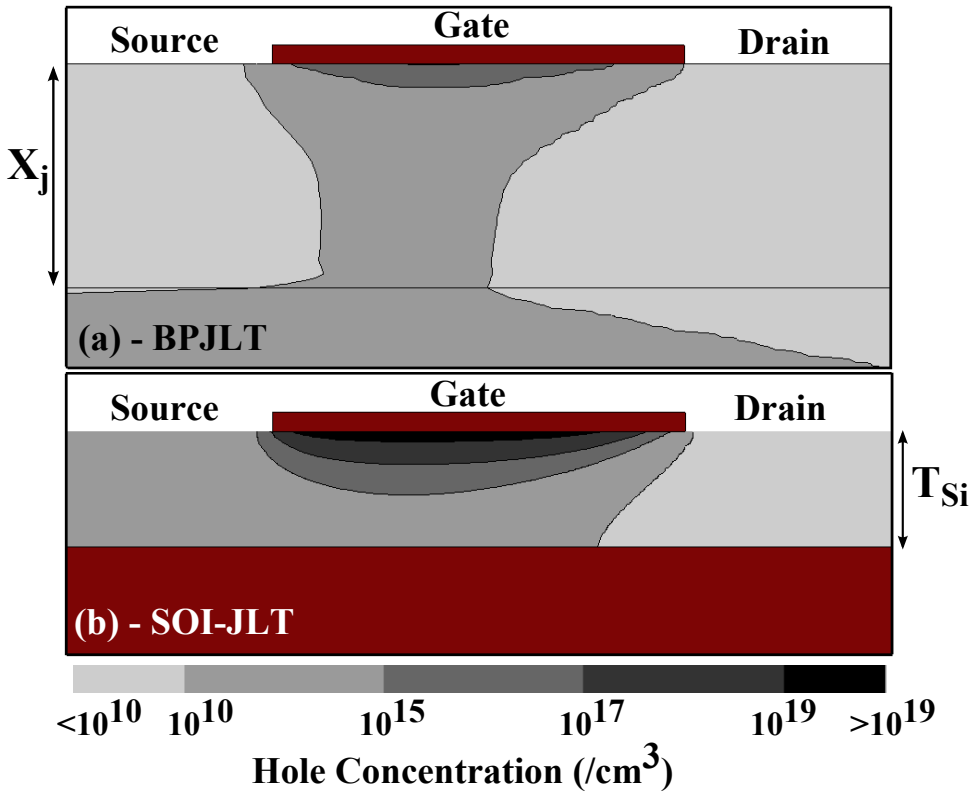


Figure 5.12: 2-dimensional contour plot for hole concentration in the channel region of (a) bulk planar junctionless transistor (BPJLT) and (b) junctionless transistor during OFF state. L_g=20nm, X_j = 12nm, T_{Si} = 6nm, N_d = 10^{19}(1.5x10^{19}) cm^{-3} - uniform doping (peak doping) for JLT (BPJLT), ϕ_m = 5.1eV, T_{ox} = 1 nm, V_D = 1V.

5.6 Summary

We have evaluated the impact of band-to-band tunneling on the OFF state behaviour of junctionless transistor (JLT) and bulk planar junctionless transistor (BPJLT). Band-to-band tunneling current is observed to be significant in the JLT, due to the high doping in the channel. A careful device design is necessary to keep the tunneling leakage current under control and to achieve a reasonable ON/OFF ratio of JLT. We show that the OFF stage tunneling leakage current is less in BPJLT compared to JLT, due to the reduced parasitic BJT action in the former.

Chapter 6

Fabrication of junctionless transistors

6.1 Introduction

Trigated, nanowire junctionless and thin film junctionless transistors were fabricated and reported in the literature [2, 18, 63] . Efforts were put in to fabricate the BPJLT, however, realizing an ultra shallow junction had been a challenging task [62]. Junctionless transistors for display applications have gained interest recently [63, 64]. JLTs on alternate substrates like paper were recently demonstrates with indium-tin-oxide (ITO)[64]. However, such devices, though use a transparent material like ITO, have several other limitations on the scalability and the speed of operation. Hence, a silicon based device with less absorption of light will be of interest to make the device faster and scalable. Silicon or poly-Si with thickness in the order of 10nm is known to show less absorption of light and this is our motivation to take up the fabrication of poly-Si junctionless transistors. The fabrication of these devices were carried out at the Centre of Excellence in Nanoelectronics (CEN) at IIT Bombay. The tools used in the process flow refers to those available at the CEN.

6.2 Process flow

The process flow planned for poli-Si thin film JLT is as follows:

Process flow

- 4 inch Silicon wafer

- Radio corporation of America (RCA) clean
- Pyrogenic oxide growth ($\sim$ 150nm) using atmospheric pressure furnace in Ultech furnace stack 2, tube 1 (details provided in Annexure A)
- Poly-Si thin film deposition ($\sim$ 10nm) using low pressure CVD (LPCVD) in AMAT Centura (details given in Annexure A)
- Active area patterning using optical lithography in double side aligner (DSA) EVG620 (details given in Annexure A)
- Low temperature oxide deposition ($\sim$ 5nm) using LPCVD in Ultech furnace stack 2, tube 2 (details given in Annexure A)
- Poly-Si deposition ($\sim$ 150nm) using LPCVD in AMAT Centura (details given in Annexure A)
- Dopant activation anneal using rapid thermal processing (RTP) in ANNEALSYS AS-ONE 150 (details given in Annexure A)
- Gate area patterning using optical lithography in DSA - EVG 620 (details given in Annexure A)
- Gate etch using reactive ion etching (RIE) in STS RIE 320 PC(details given in Annexure A)
- Characterization using Keithley 4200 parametric analyzer system.

We use the processes developed earlier in the nano-fabrication lab of IITB. The detailed information about the lithography techniques and masks used in our experiments are given in [65]. The information about the gate etch is documented in [66]. The CMOS process integration aspects are documented in [62, 66]. The mix and match lithography process for making the short channel devices is documented in [67]. The processes we developed and their integration issues are described in the sections that follow.

6.2.1 Gate stack optimization

The gate stack processes developed for standard CMOS flow developed [62, 66] uses a dry oxide grown at high temperature which have compatibility issues to be used on a 10nm

thick poly-Si channel. For example, the growth of 5nm gate oxide on Si consumes $\sim$ 2nm of Silicon (which is $\sim$ 40 $\%$) [68]. Gate oxide by thermal growth would make the thin poly-Si layer even thinner and may lead to cracks or physical deformations to the film. So, we have developed a process with low temperature oxide (SiO_2 by LPCVD in the Ultech furnace and Al_2O_3 by pulsed - DC sputtering in the Applied Materials (AMAT) Endura platform) with metal and poly-Si gates for our experiments.

6.2.1.1 Gate stack with TiN and Al gates

The process flow for the TiN/Al_2O_3/Si MOS capacitor (done jointly with [62]) is:

TiN/Al_2O_3/Si MOS capacitor process

- RCA clean
- Al_2O_3 deposition ($\sim$ 4.5nm) using physical vapour deposition (PVD) in AMAT endura (details given in Annexure A)
- TiN deposition ($\sim$ 80nm) PVD in using AMAT endura (details given in Annexure A)
- Oxide deposition ($\sim$ 300nm) using inductively coupled plasma chemical vapor deposition (ICPCVD) in Plasma lab system100 ICP 180 (details given in Annexure A)
- Gate area patterning using optical lithography in DSA EVG620 (details given in Annexure A)
- Oxide wet etch using 5:1 buffered hydrofluoric acid (BHF) (details given in Annexure A).
- TiN wet etch using NH_4OH + H_2O_2 + H_2O (details given in Annexure A).
- Resist strip using acetone + isopropyl alcohol (IPA)
- Oxide wet etch in 5:1 BHF (details given in Annexure A).

The gate stack processes as described above gave a reasonable MOS capacitor characteristics as shown in Fig. 6.1. Initially, we started with a $\sim$ 100nm of oxide hard mask deposited by ICPCVD and this is observed to have pin holes which subsequently etched out the protected TiN as well. Later, we tried using a thicker ($\sim$ 300nm of oxide), which was able to mask the TiN in the gate regions.

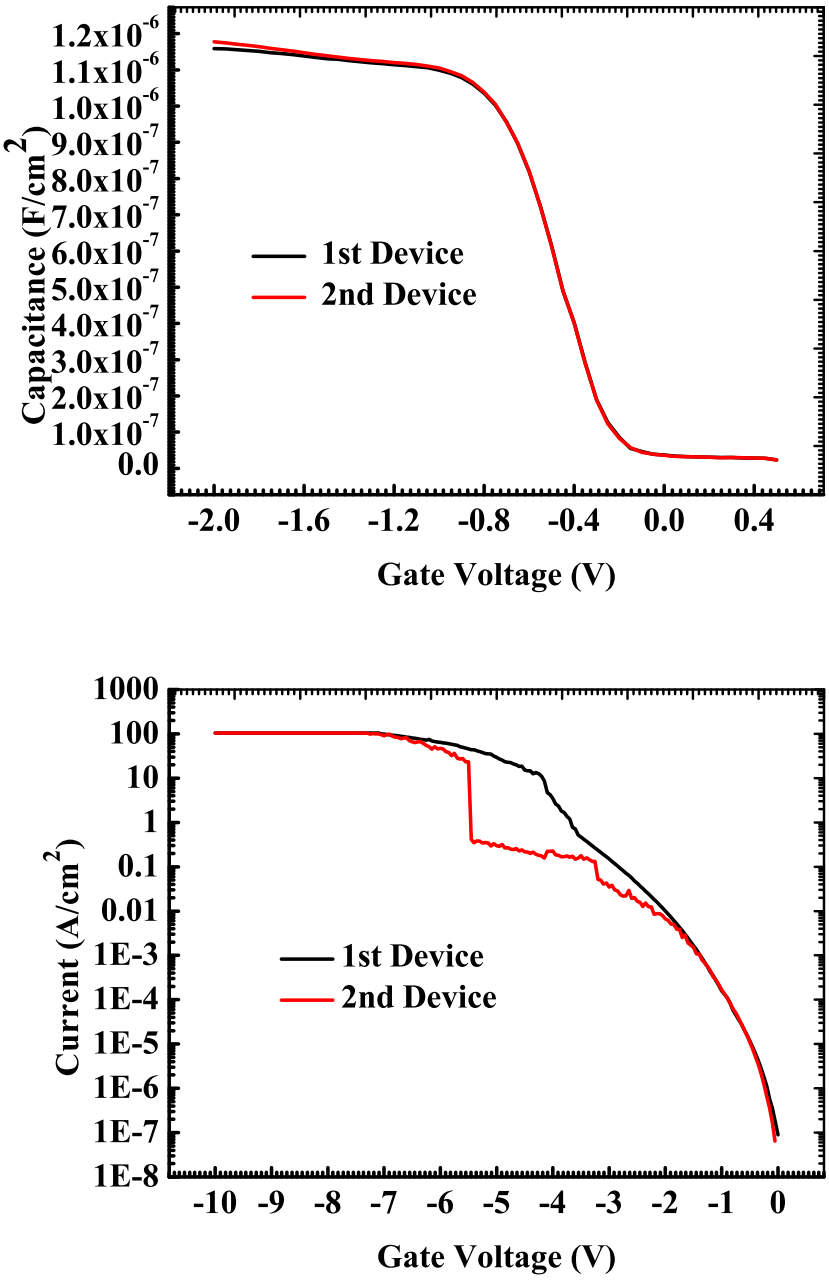


Figure 6.1: C-V, I-V (in accumulation only) of a TiN/Al_2O_3/Si MOSCAP with EOT = 2.95nm and substrate doping = 1 x 10^{15} – 1 x 10^{16} cm^{-3}. Note: This work is done jointly with [62]

However, when we later integrated, these into the actual process flow, where we need to have this gate gate stack on a poly-Si material, we observed that the poly-Si present in the active area of the transistor is also etched while etching TiN, as shown in Fig. 6.2. This made us to think of an alternative gate material and we chose Al for this as it is known that the Al etchant will not effect the resist and can be wet etched without an oxide hard mask.

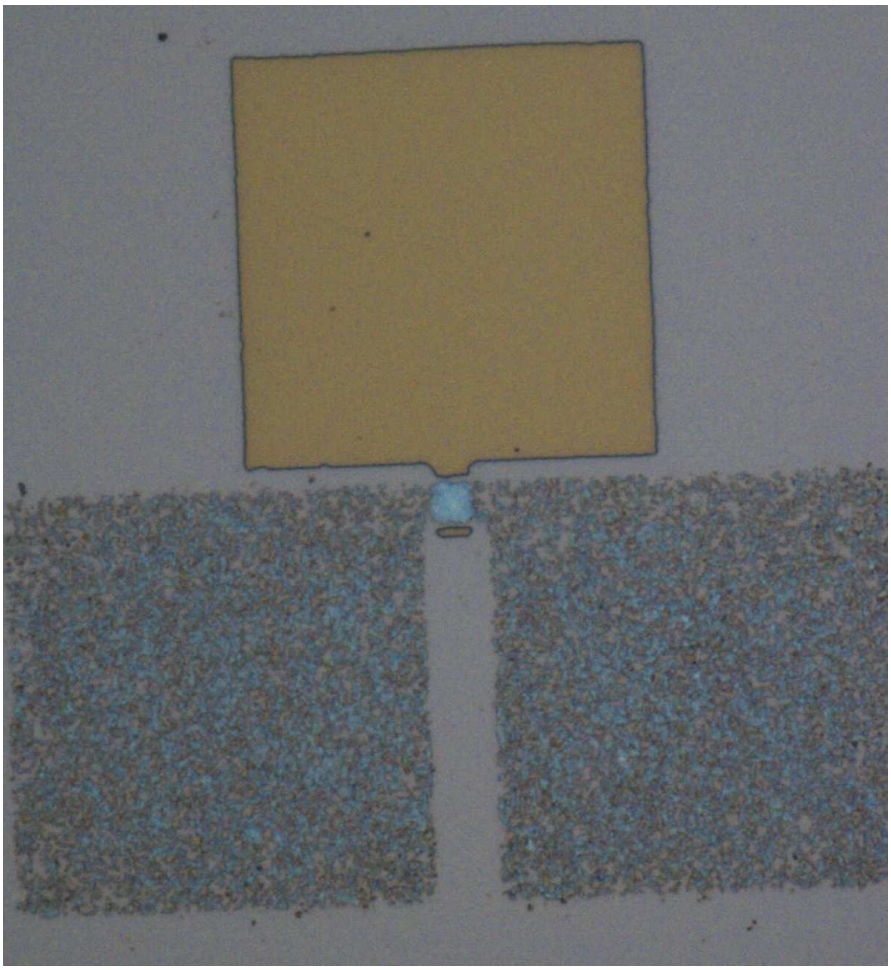


Figure 6.2: Optical microscopic image of poly-Si BPJLT with TiN-Al_2O_3 gate stack. Poly-Si pads are corroded by the wet etchant of TiN. Note: This work is done jointly with [62]

Al/LTO/Si MOS capacitor process

The process flow followed for making Al gated MOS capacitors is given below:

- 4 inch Silicon substrate
- RCA clean
- Low temperature oxide (LTO) deposition ($\sim$ 5nm) using LPCVD in Ultech furnace, stack 2, tube 2 (details given in Annexure A)
- Al deposition ($\sim$ 80nm) using PVD in AMAT endura (details given in Annexure A)
- Gate area patterning using optical lithography using DSA EVG620 (details given in Annexure A)

- Al wet etch using H_3PO_4 + CH_3COOH + HNO_3 + H_2O (details given in Annexure A)
- Resist strip using acetone + isopropyl alcohol (IPA)

The MOS capacitor C-V and I-V of these devices are shown in Fig. 6.3. However, this process also had similar process integration problems as that of with TiN gate. We observe the poly-Si film's resistivity to go down significantly after the full transistor flow. The wet etch of Al is one of the process that we suspect to be responsible for this. The exact detail of the process integration problems are explained in the sections that follow.

6.2.2 Poly-Si optimization for junctionless transistors

We started the poly-Si deposition experiments using LPCVD in AMAT gate stack cluster, chamber B (polygen for poly-Si) tool which has a very fast deposition rate. Junctionless transistors require a very thin layer of the semiconductor material. So, we chose to deposit poly-Si for a very short time. The deposition parameters of poly-Si thin films are listed in Annexure A. In Fig. 6.4 (a), we show the cross-sectional scanning electron microscope (SEM) image supporting the thickness of poly-Si as $\sim$ 12nm. Depositions are done for 5, 7, 10 and 15 sec and the approximate thickness obtained are listed in Table. 6.1. The donor doping in poly-Si deposited is estimated by sheet resistance measurements on a thick poly-Si film. However, as the contact probes are kept $\sim$ 50 μm apart during device characterization, the currents measured are significantly lower due to the increased series resistance. It can be observed from Fig. 6.4(b) that the current drives achieved for poly-Si deposited for time of 5 sec are very low and films deposited for longer time appear to be desirable for JLT applications. However, JLTs require a very thin device layer, failing which the channel region will not be fully depleted and this would result in a very low ON/OFF current ratio. Hence, we expect a better ON/OFF characteristics in devices where poly-Si is deposited for a shorter time.

6.2.2.1 Evaluation of LPCVD poly-Si deposition in AMAT gate stack cluster for JLT application

We have carried out several experiments to evaluate if the poly-Si deposited using LPCVD in AMAT gate stack cluster, chamber B (polygen for poly-Si) tool is suitable for JLT applications. Before going to a full process flow, we fabricated a back gated junctionless transistor with

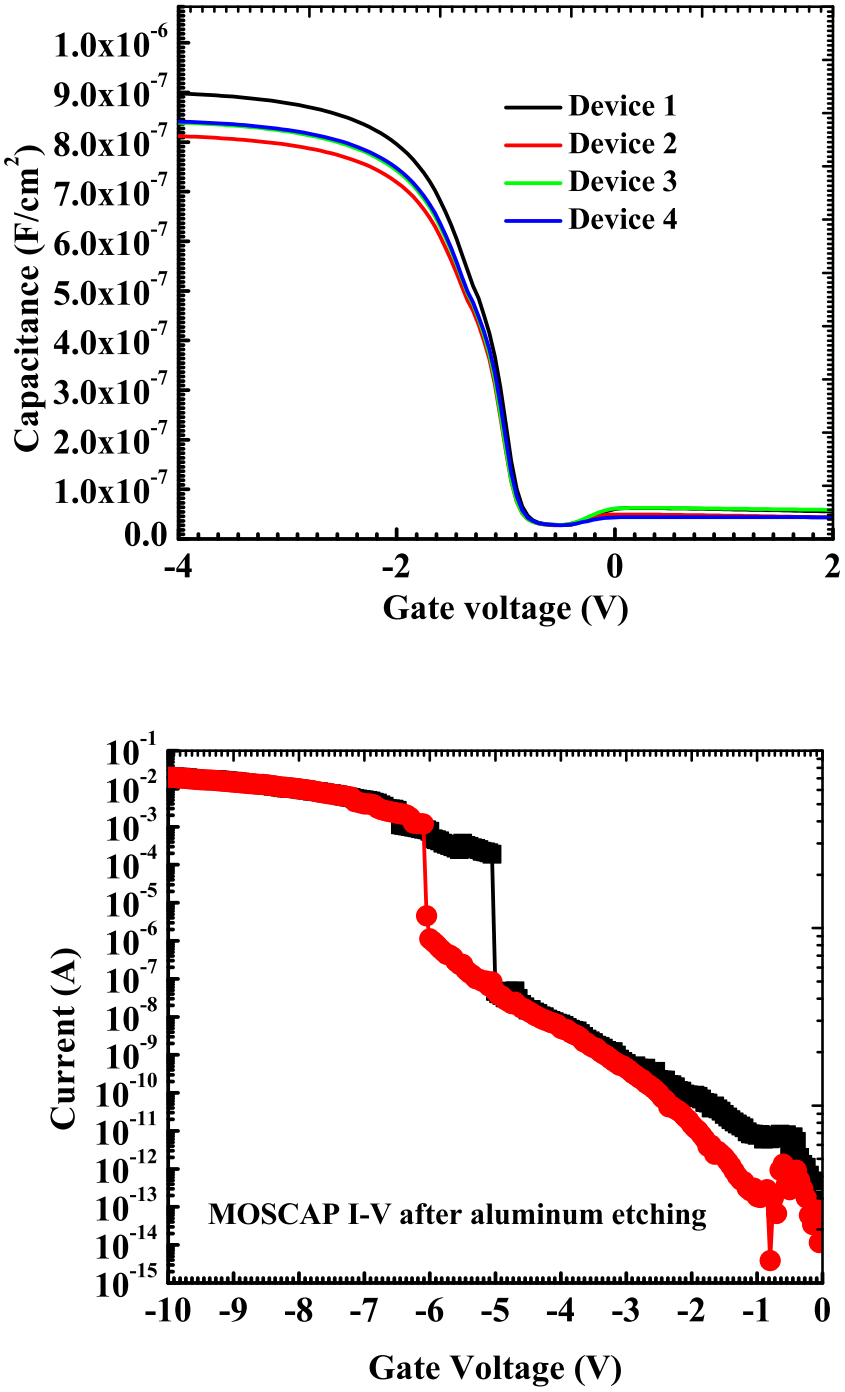


Figure 6.3: C-V and I-V (in accumulation only) of a Al/SiO_2/Si MOSCAP with EOT = 4nm and substrate doping = 1 x 10^{15} – 1 x 10^{16} cm^{-3}. Note: This work is done jointly with [62]

a heavily doped Si substrate as gate. We have chosen low resistivity (0.01 to 0.02 ohm-cm) Si wafers for these experiments. The process flow for these experiments is as below:

- RCA clean

Table 6.1: Poly-silicon deposition time (in sec) and their thicknesses (in nm) as seen in SEM. Note: This work is done jointly with [62]

poly-Si deposition time (sec.)	**poly-Si thickness (nm)**
5	10-14
7	15-18
10	23-27
15	38-44

- Oxide growth ($\sim$ 10nm) using dry oxidation in Ultech furnace, stack 1, tube 1 (details given in Annexure A)
- Poly-Si deposition (for deposition time of 5 and 7 sec) using LPCVD in AMAT gate stack cluster, chamber B (polygen for poly-Si) (details given in Annexure A)
- Activation anneal using RTP in ANNEALSYS AS-ONE 150 (details given in Annexure A)
- Active area patterning using optical lithography in DSA EVG620 (details given in Annexure A)
- Resist strip using acetone + isopropyl alcohol (IPA)
- Back side Al metallization ($\sim$ 200nm) using thermal evaporation in Al thermal evaporator (details given in Annexure A)

The schematic of the device structure at the time of probing is shown in Fig. 6.5. We probe the pads on the active area for source and drain - and the substrate as the gate. We observe a resistor like linear I-V characteristics (as shown in Fig. 6.4(b)) between the source and drain with substrate floating. However, the doping of the poly-Si film is estimated by depositing a thick ($\sim$ 135nm) film, followed by a sheet resistance measurement. The mean thickness and sheet resistance measured are 135nm and 151.17 ohm/square respectively. The mobility of electrons in Si at 300^{o}K at a doping of 10^{19} cm^{-3} is $\sim$ 100 cm^2/V-s. The doping estimate turned out to be 3.06x10^{19} cm^{-3}, based on the sheet resistance data of thick poly-Si film and

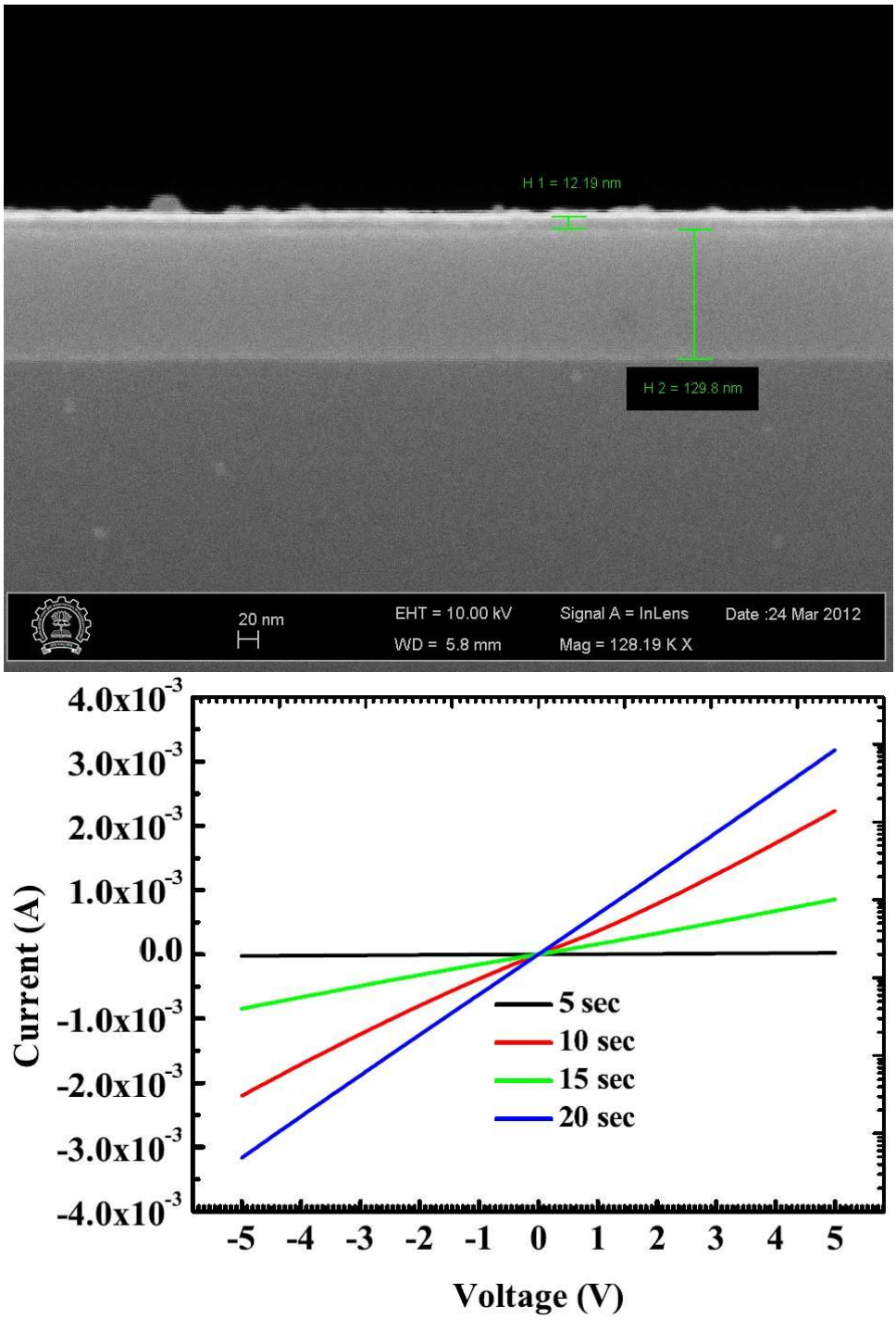


Figure 6.4: (a)Cross-section SEM of poly-Si deposited for 5 sec on 130nm SiO_2 (b)Resistor behaviour on a linear scale for poly-Si deposition time – 5 sec, 10 sec, 15 sec and 20 sec. Note: This work is done jointly with [62]

mobility data from literature. However, given the fact that the carrier mobility is lower in poly-Si compared to bulk-Si, we estimate the doping of the poly-Si film deposited to be slightly lower than 3.06x10^{19} cm^{-3}, but, will be in the order of 10^{19} cm^{-3}.

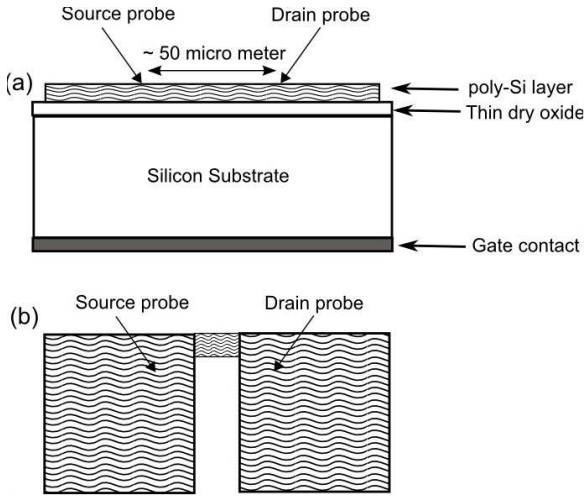


Figure 6.5: (a)Schematic of the cross-sectional view of the device at the time of probing and (b) Schematic of the top view of the device at the time of probing

The transistor I-V characteristics of the back gated JLTs are shown in Fig. 6.6 and 6.7 respectively for 5 sec and 7 sec deposition of poly-Si. It is clearly seen that the device offer switching characteristics and as can be observed from Fig. 6.8, the switching action tend to decrease for a thicker poly-Si as channel material. However we observe a very small ON/OFF ratio even for 10nm poly-Si (5 sec deposition) and this is attributed to a weak gate control as the gate oxide thickness is comparatively thick ($\sim$ 10nm). A thinner gate oxide and even thinner poly-Si as channel is expected to improve the switching behaviour. The capacitance - voltage and current -voltage characteristics of the MOS capacitor formed by the poly-Si in the active area and the substrate are shown in Fig. 6.9. The gate leakage is reasonably low, as we have a thick gate oxide for these devices. However, the C-V characteristics does not appear to be usual as we are probing directly on the 10nm poly-Si.

With an idea to improve the switching behaviour of the back gated JLT, we took forward another run with poly-Si deposition for 4 sec (expected to give semiconductor layer less than 10nm) and with 5nm of thin dry oxide. As expected, we observe the improved I-V characteristics as shown in Fig. 6.10. We observe $\sim$ 6 orders of ON to OFF current ratio. The gate leakage is an issue in this process and this is in line with the thin gate dielectric and large area MOS structure. However, we were successful in demonstrating the junctionless transistor action with this process. Our next step is to integrated this in to the full top gated process flow, where we can reduce the MOS capacitor area and can improve the gate leakage.

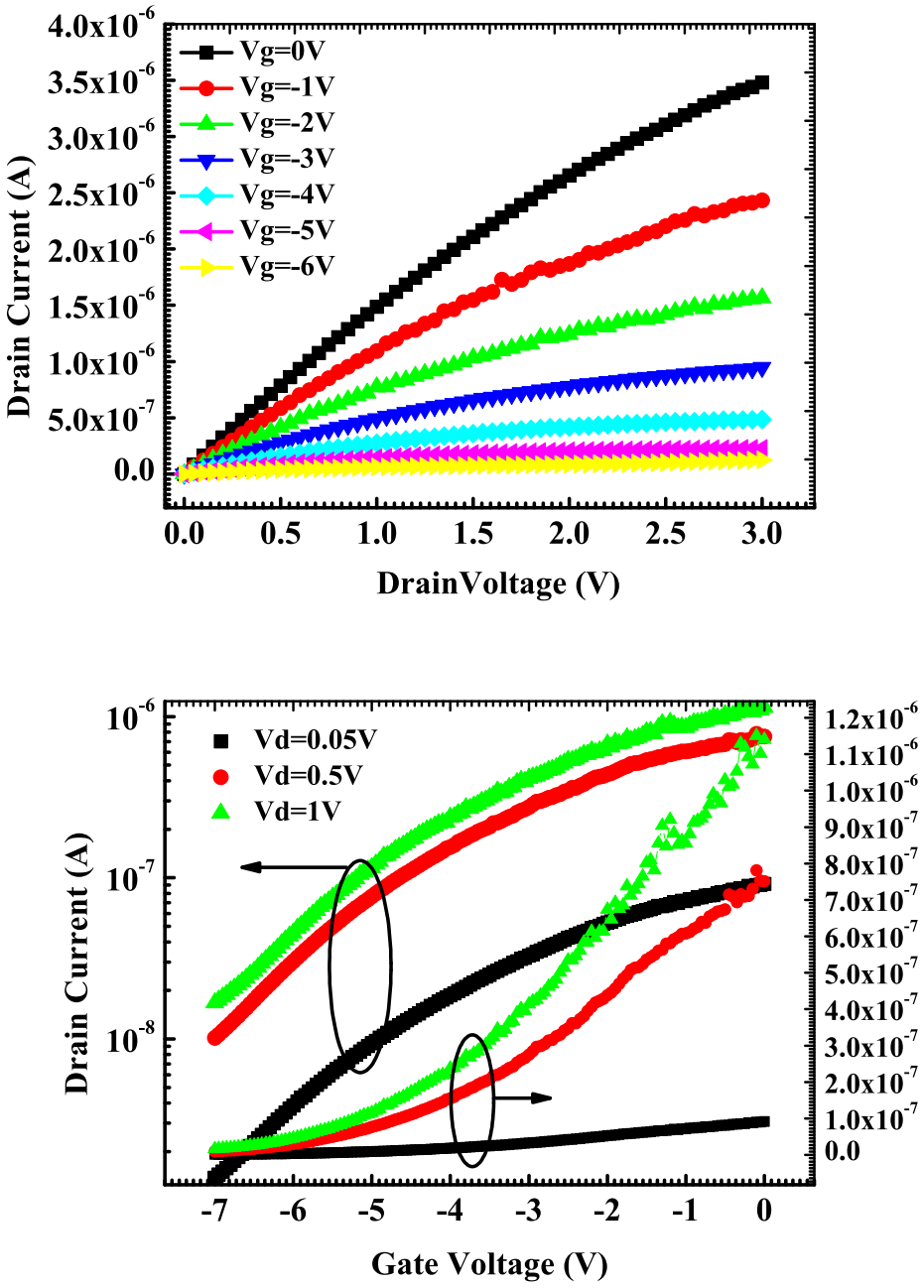


Figure 6.6: $I_D - V_{GS}$ and $I_D - V_{DS}$ of back-gated JLT with poly-Si deposition time as 5 sec. Note: This work is done jointly with [62]

6.2.2.2 Metal Oxide poly-Si capacitor structure

Having had the poly-Si film thickness optimized for junctionless transistors (which is evaluated by a back gated transistor), our next step was to get a working MOS capacitor on poly-Si layers. For this, we have followed the same process flow described earlier, except that we deposit a thick oxide and thick poly-Si on the Si substrate before making the MOS structure.

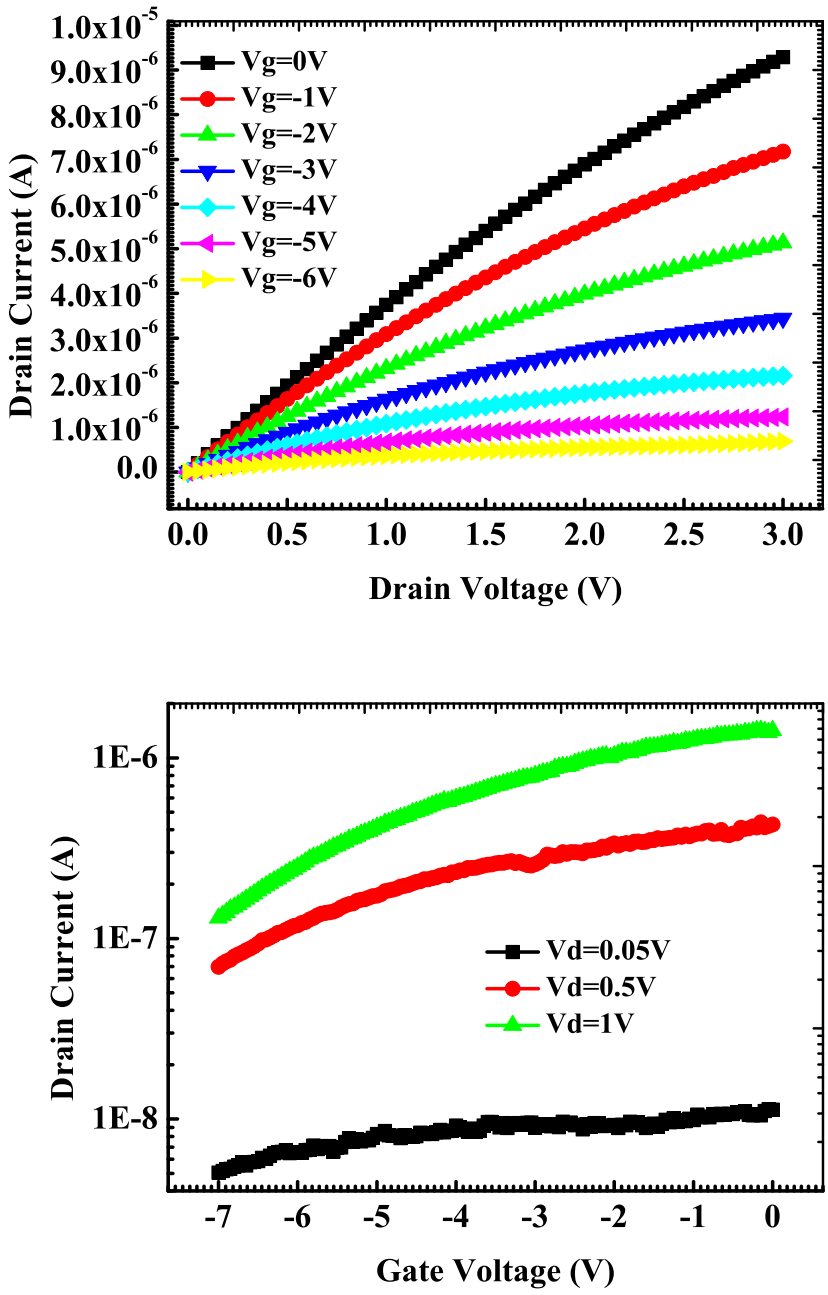


Figure 6.7: $I_D - V_{GS}$ and $I_D - V_{DS}$ of back-gated JLT with poly-Si deposition time as 7 sec. Note: This work is done jointly with [62]

Unexpectedly, we observe a heavy leakage in these capacitors as shown in Fig. 6.11.

Several unsuccessful attempts (like changing the gate material and gate oxide thickness) were made in order to improve the leakage behaviour of these devices. However, proper MOS structures on bare Si wafers and leaky behaviour of the same when made on top of poly-Si driven us to inspect the surface roughness of the poly-Si deposited using LPCVD in AMAT gate stack

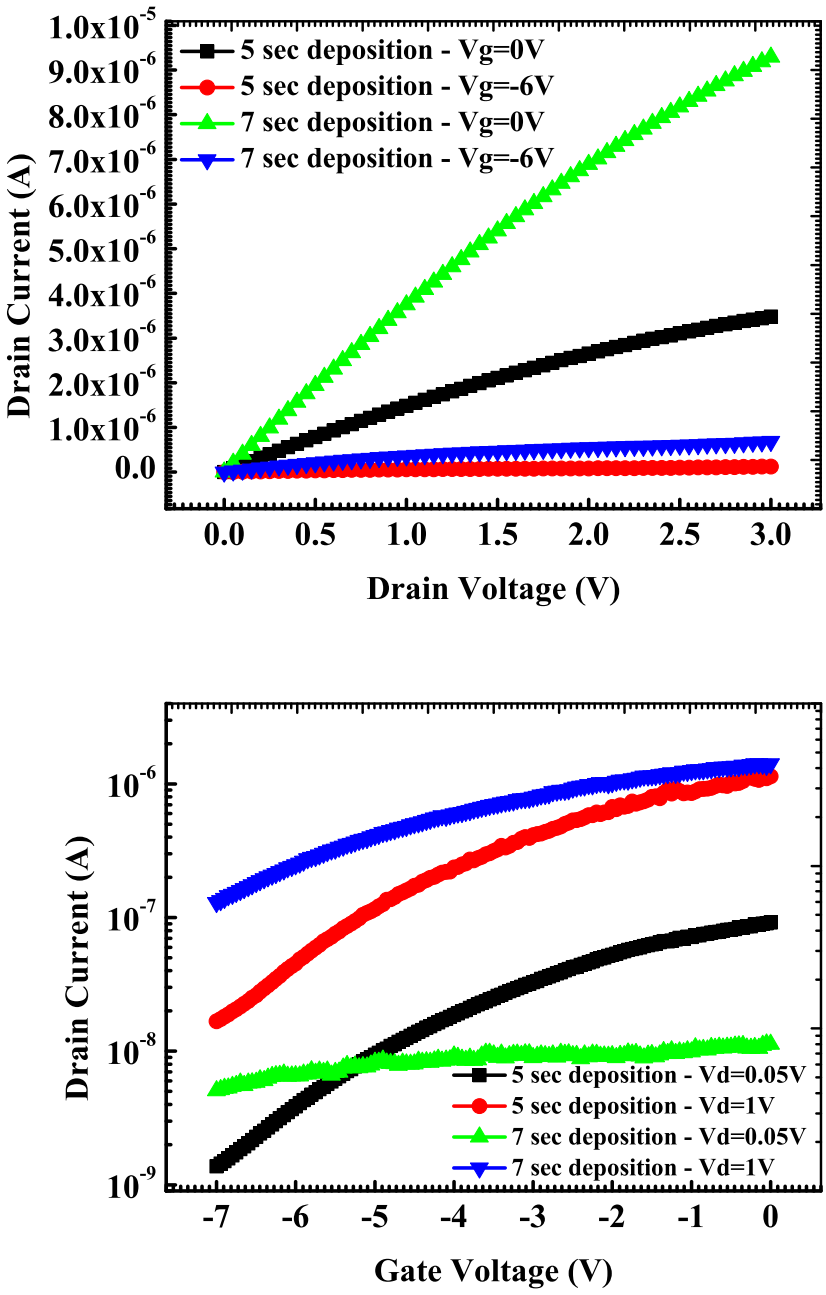


Figure 6.8: Comparison of I-V characteristics of back-gated JLTs with poly-Si deposition time as 5 sec and 7 sec. Note: This work is done jointly with [62]

cluster, chamber B (polygen for poly-Si). As shown in Fig. 6.12, the poly-Si deposited by AMAT gate stack cluster is very rough with the average surface roughness on $\sim$ 120nm poly-Si turned out to be 50nm. To achieve a smoother surface, we planned to deposit amorphous Si at low temperatures followed by an anneal at high temperatures to make it poly-crystalline. However, when tried with the same AMAT gate stack cluster tool at 500^o, we observed no

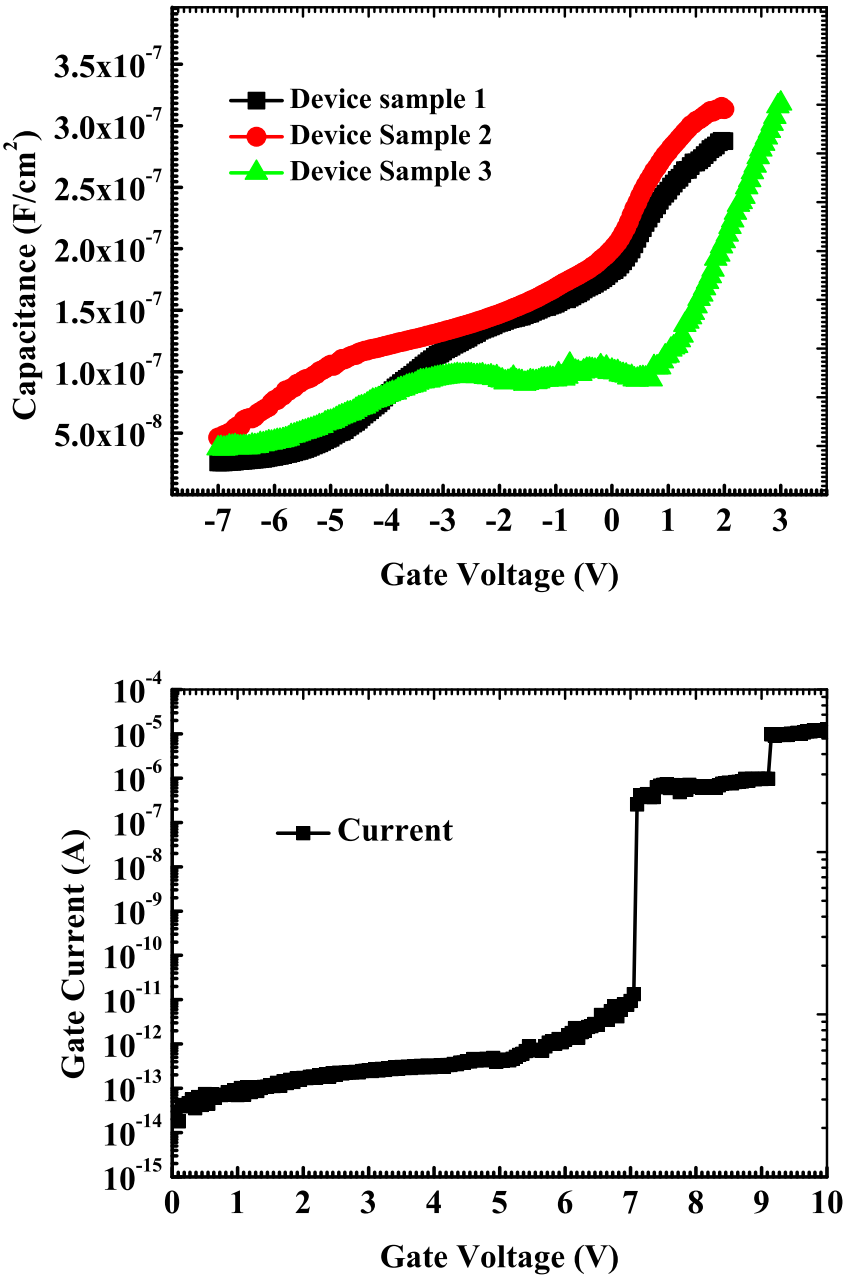


Figure 6.9: C-V and I-V measurements of back-gated poly-Si MOS capacitor. Note: This work is done jointly with [62]

deposition to happen. This made us to think of a different tool for amorphous Si deposition.

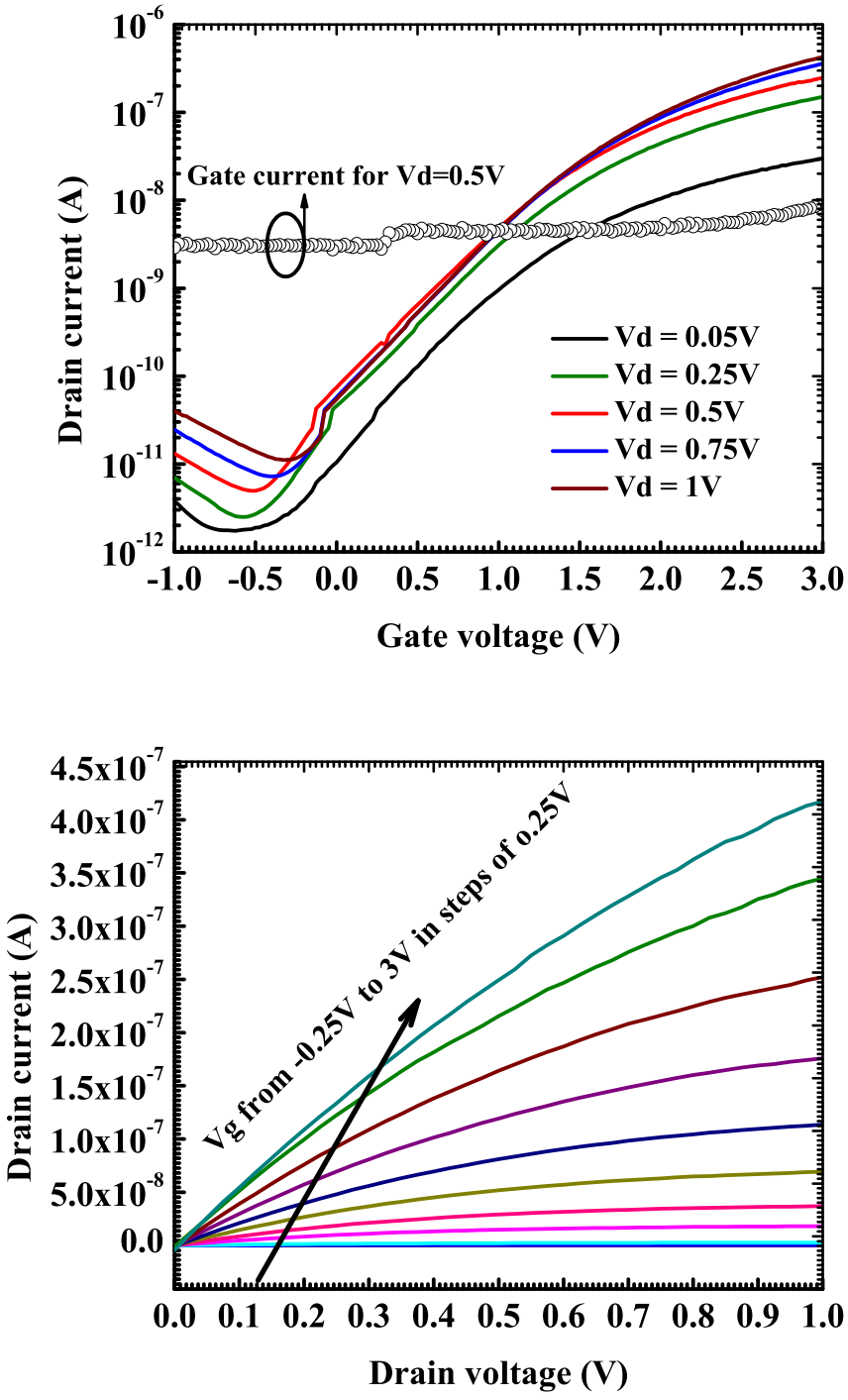


Figure 6.10: Comparison of I-V characteristics of back-gated JLTs with poly-Si deposition time as 4 sec and gate oxide as 4nm. Note: This work is done jointly with [62]

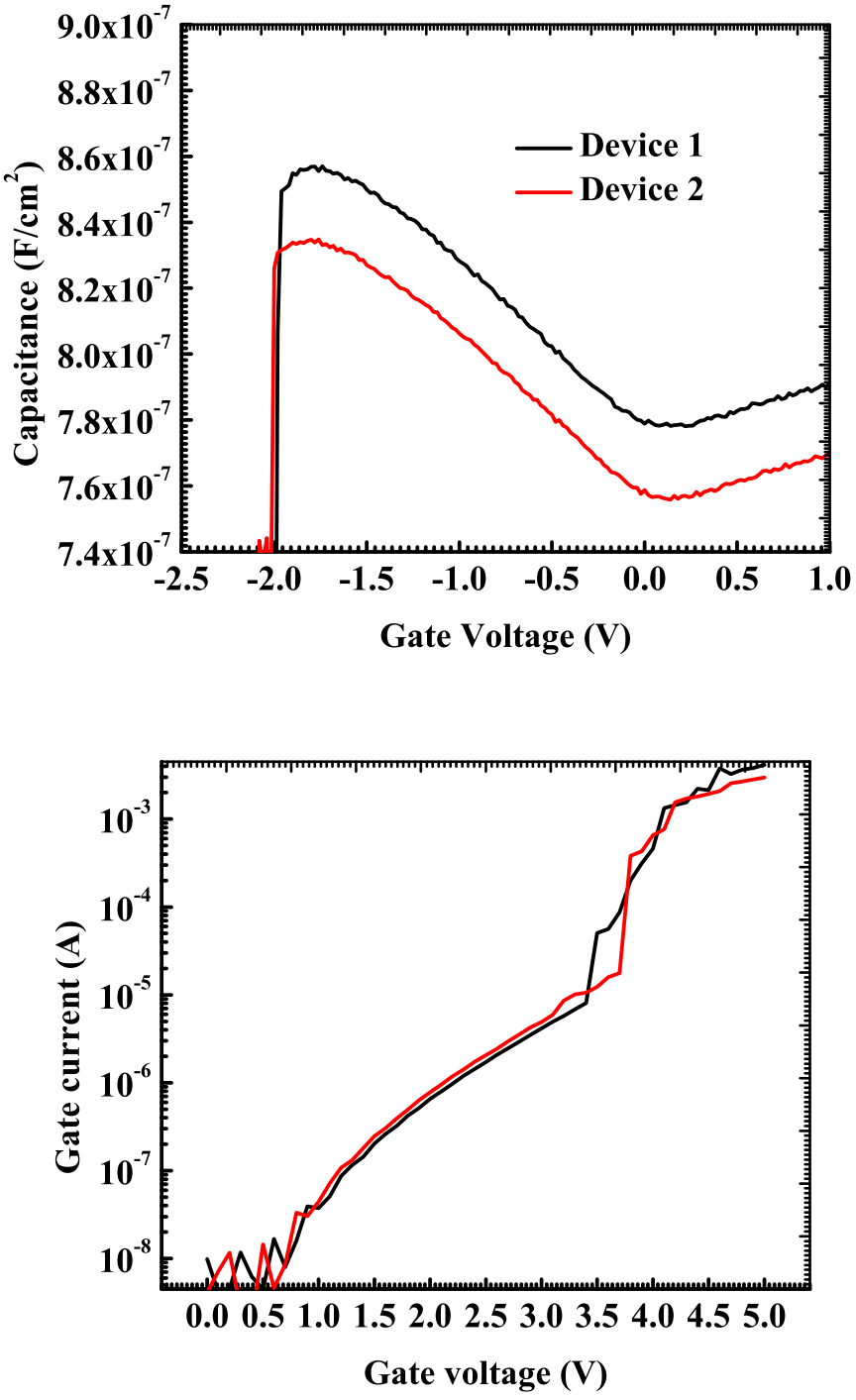
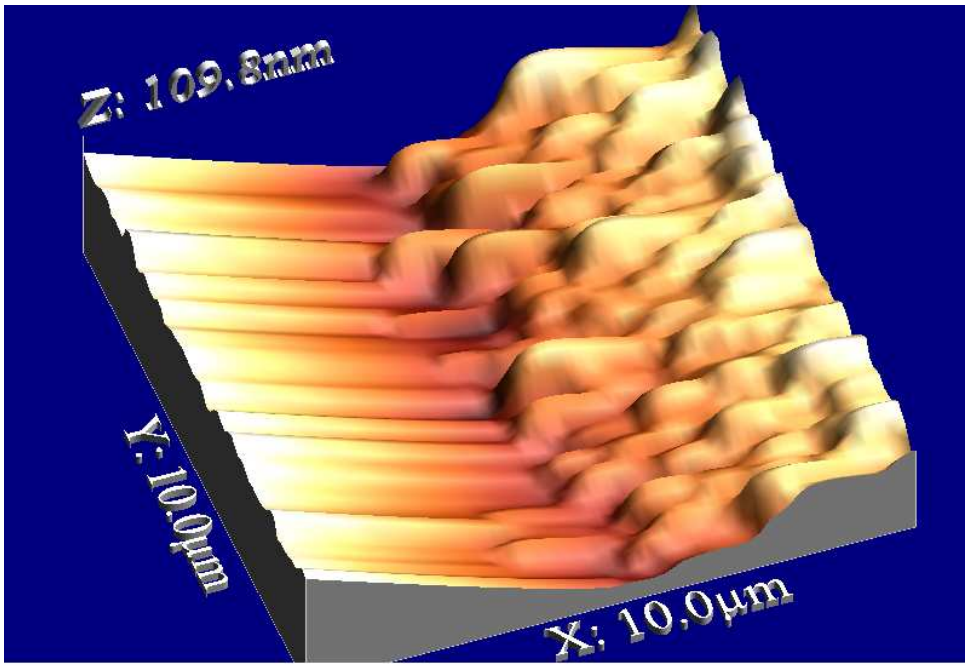


Figure 6.11: C-V and I-V (in accumulation only) of a Al/SiO_2/poly-Si MOS capacitor. Note: This work is done jointly with [62]



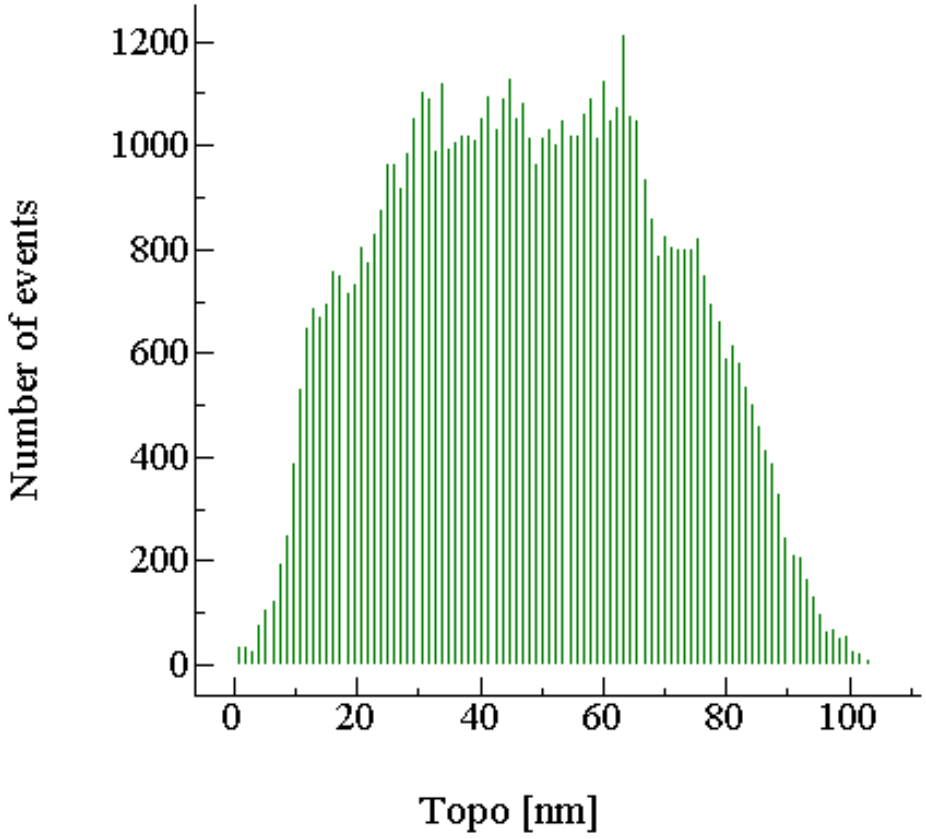


Figure 6.12: (a) 3D AFM image of poly-Si in a 10μm x 10μm area b) Histogram of no. of sample points vs. peak roughness in a 10μm x 10μm area. Note: This work is done jointly with [62]

6.2.2.3 Poly-Si deposition by LPCVD in furnace

Amorphous silicon was deposited using LPCVD in Ultech furnace - stack 2 tube 2, at a very slow deposition rate at 500^{o}C for one hour and subsequently annealed at 650^{o}C for another one hour. Fig. 6.13 shows the cross section SEM image of the deposited poly-Si after the re-crystallization anneal. It can be observed that the thickness of these films is $\sim$ 10nm. In Fig. 6.14 we show that the current drive of these films when probed at 50 micron apart is few micro Ampere, which is suitable for junctionless transistor applications. However, the non-linear characteristics observed in few of these plots is due to improper probing (note that we have probed directly on the thin poly Si).

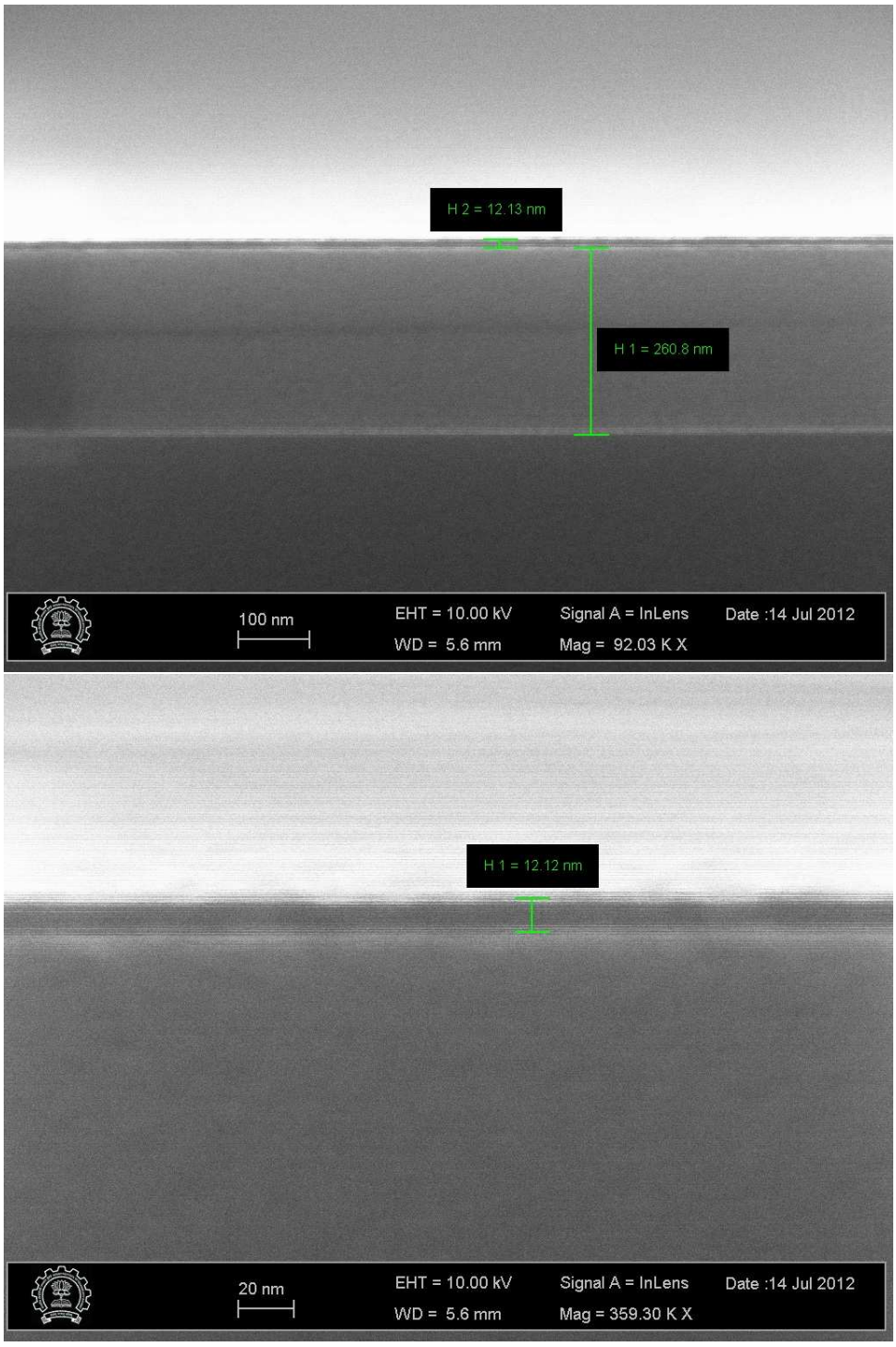


Figure 6.13: (a) and (b) Cross sectional SEM image of poly-Si deposited in Ultech furnace.

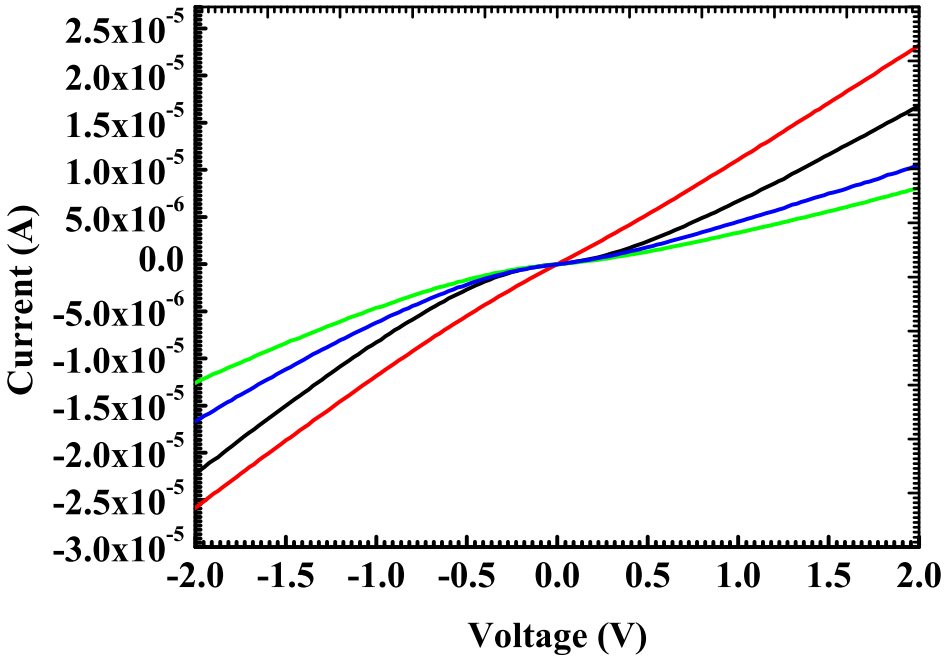


Figure 6.14: Current vs. voltage characteristics of poly-Si film probed at 50 micron apart.

6.2.3 Process integration of poly-Si thin film transistor

Using the process described in the previous section, we have fabricated the full device with process flow described in the beginning of this chapter. Initially we have made the devices with Al gate material. However, we observe that after the whole process the current between the source and drain pads is very low, which is at least two orders less when compared to the measurements made immediately after the poly-Si deposition. Though not clearly visible in the microscopic inspections, we believe that this is the problem similar to the one we faced while making the TiN gated devices. Keeping these integration aspects in mind we have carried out another run with phosphorous doped poly-Si as gate material. The top down SEM image of the final device fabricated with poly-Si gate are shown in Fig. 6.15. As it can be seen from the figure, we were able to achieve channel lengths down to 2 micron.

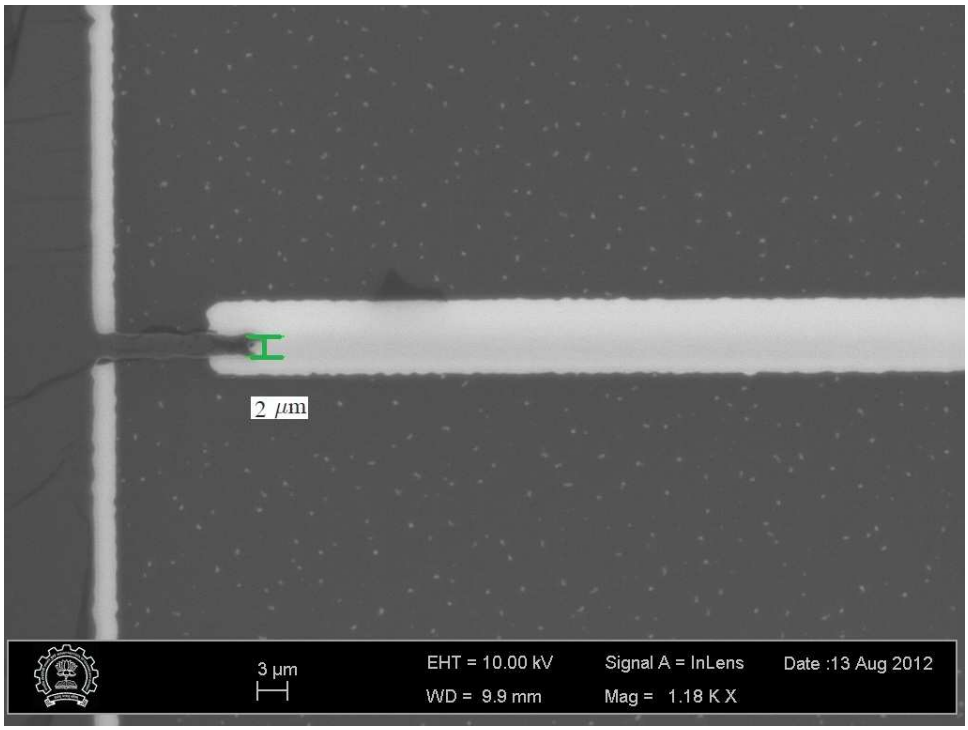


Figure 6.15: Top down SEM image of poly-Si junctionless transistor.

In Fig. 6.16, we show the I_D vs. V_G characteristics of the poly-Si channel and poly-Si gate thin film junctionless transistor with channel lengths ranging from 2 micron to 10 micron. As it can be observed from the figure, the device shows switching behaviour, but, with a low ON current (at least two orders lower than expected) and a high drain induced barrier lowering (DIBL). We attribute the low ON current to the high contact resistance (as we are probing

directly on the thin poly-Si film). Also, a higher DIBL in junctionless transistors can cause even when the thickness of poly-Si is more than it is supposed to be OR due to a weak gate control due to a thick gate oxide (the gate oxide thickness in this device is $\sim$ 5nm).

While we face an issue with the ON current and the DIBL in the fabricated devices, we observed an undesirable characteristics when the same devices are measured after 48 hours. The I_D vs. V_G and I_D vs. V_D characteristics of these measurements are shown in Fig. 6.17. It can be observed that the ON current had degraded by two orders in a time period of 48 hours. We expect that this is due to the defective thin poly-Si film which is not stable. As the dimensions we talk about are $\sim$ 10nm, it could be possible that the poly-Si can go defective even due to the native oxide. Further top down SEM imaging (as shown in Fig. 6.18) aid to support our argument. It can be observed in Fig. 6.18(a), that there appears some particle like features in the active regions and not on either on the gate pad or on the field oxide. Small strains we observe on the gate pad are the strains of acetone and IPA (this is because we did not do the piranha clean before imaging). A close inspection of the source/drain pads as shown in Fig. 6.18(b) indicates that these regions have particles of size of a micron. Further closer inspection shows that (in Fig. 6.18(c)-(d)) these regions seems to be porous as well. This supports our argument that the poly-Si device layer seems to be defective and unstable.

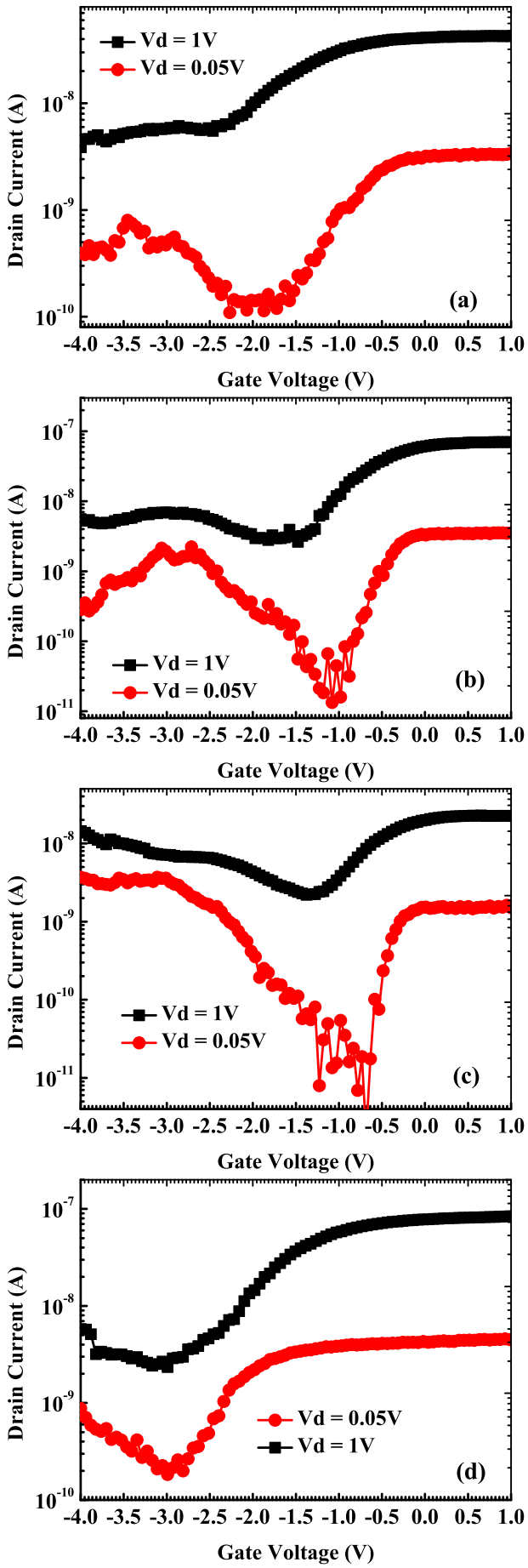


Figure 6.16: I_D vs. V_G characteristics of poly-Si junctionless transistors of channel length (a) 2 μm (b) 3 μm (c) 5 μm (d) 10 μm

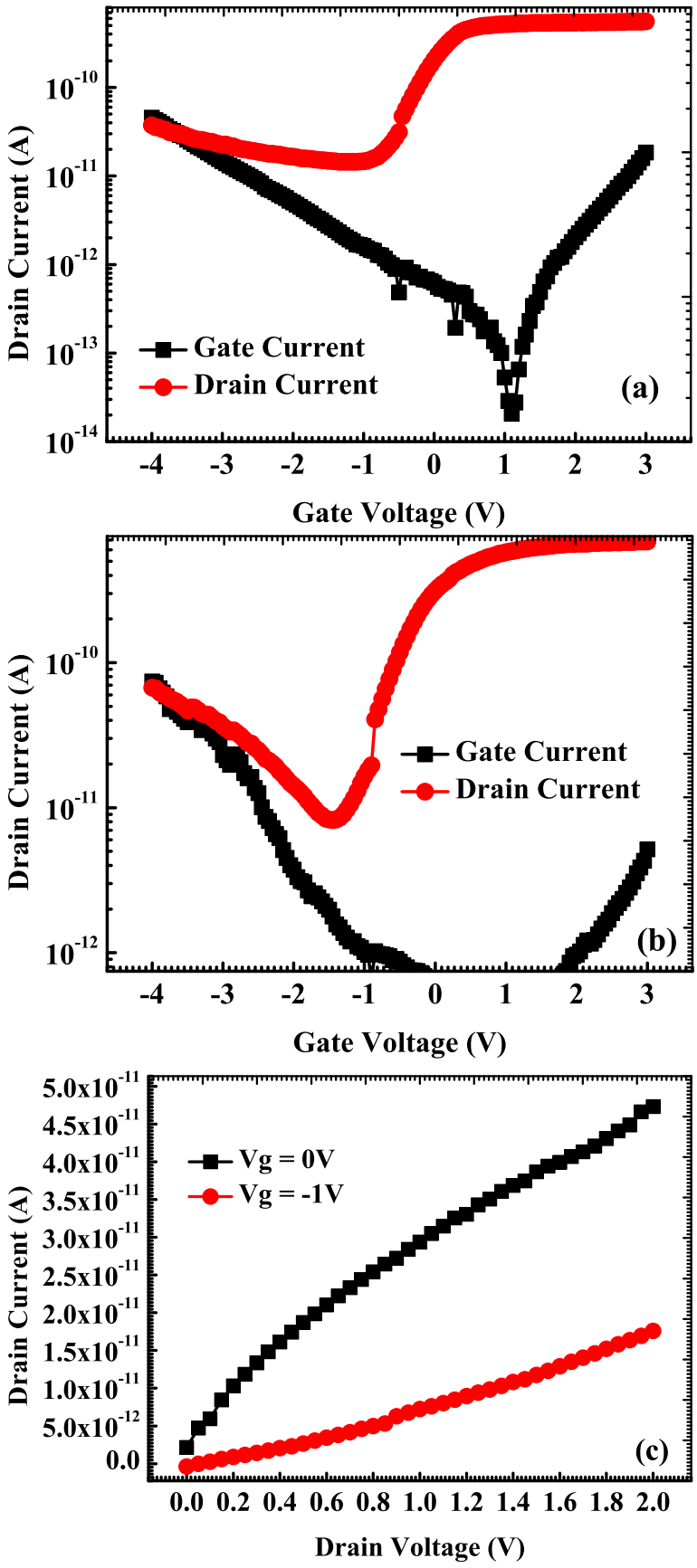


Figure 6.17: I_D vs. V_G characteristics of poly-Si junctionless transistors of (a) 2 μm channel length (b) 3 μm channel length measured after 48 hours after the first measurements (c) I_D vs. V_D characteristics of poly-Si junctionless transistors of channel length 5 μm measured after 48 hours after the first measurements.

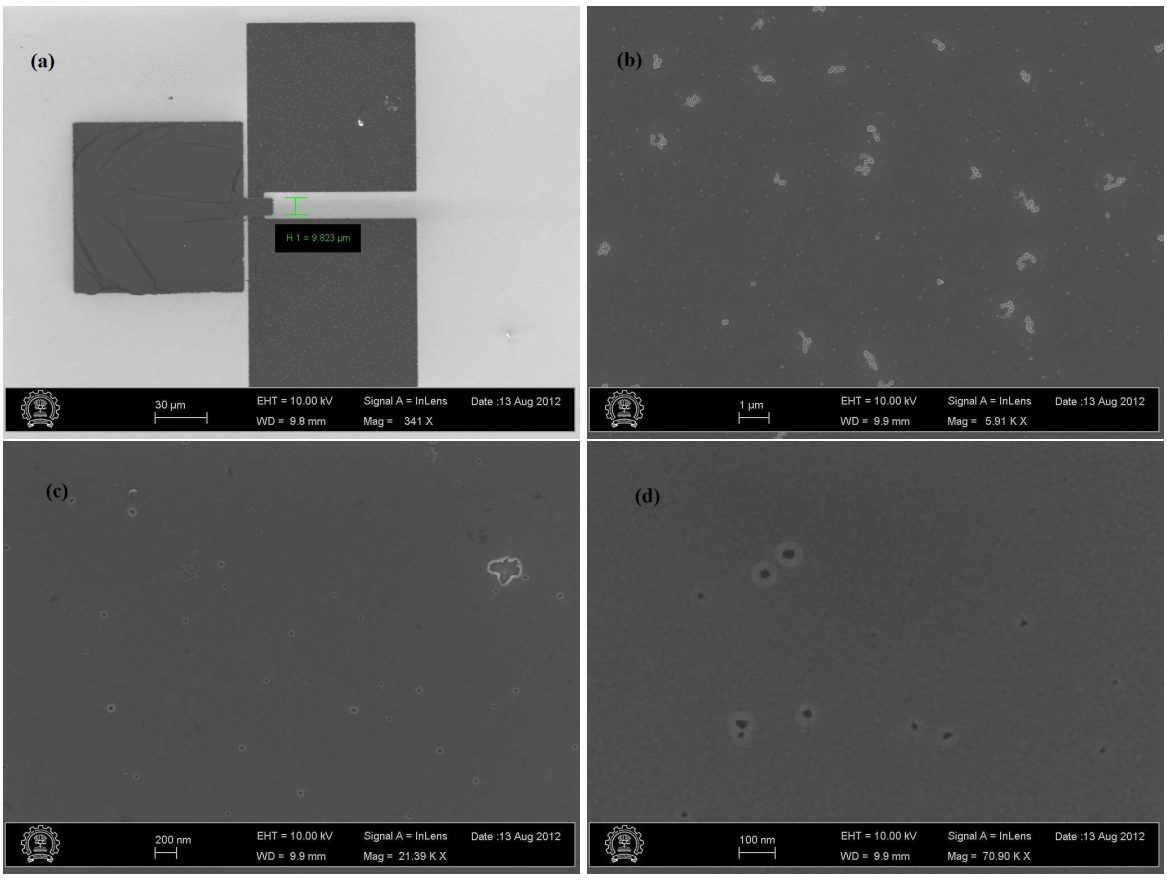


Figure 6.18: Top down SEM image of the 10 micron channel length (b) - (c) Zoomed view of the device shown in (a)

6.3 Conclusions

Poly-Si thin film junctionless transistors were fabricated with channel length varying from 2 micron to 10 micron. However, we observe that the current between the source and drain regions is as expected immediately after poly-Si deposition and drops by about two orders when measured immediately after the gate stack integration. Further, we observe that the source to drain current reduces with the duration of time the samples were exposed to ambient. We attribute this degradation of current with time of ambient exposure as an instability in poly-Si film. This instability could possibly be due to the native oxide developed on poly-Si, when exposed to ambient. This problem could be addressed by an immediate SiO_2 passivation post the gate stack process. However, this require a process development for metallization through the passivation layers (i.e., to optimize the via region etch process, via fill, metal contact deposition and etch processes). A possible further problem to investigate is to fabricate short channel length devices with the mix-and-match process developed in [67]

Chapter 7

Conclusions and Future Work

In this work we have presented a detailed study of JunctionsLess Transistors (JLTs) as possible alternatives for conventional MOSFETs, where we have a detailed study of ON and OFF behaviour of the device and we have also suggested two different architectures to improve the electrostatic integrity of JLTs. We have studied the effect of band-to-band tunneling (BTBT) on the OFF state behaviour of both SOI and BPJLT. We also have attempted to fabricate thin film planar JLTs with poly-Si.

First we propose a bulk FET architecture which we call as a bulk planar junctionless transistor (BPJLT), where we propose to make JLTs on bulk substrates instead of silicon on insulator (SOI) substrates. This would substantially reduce the fabrication cost of the device as the bulk substrates are cheap compared to the SOI. The BPJLT architecture has a junction isolation instead of dielectric isolation as in the case of SOI-JLTs. Though we have a junction in the device, we have shown that this device still works on the principle of JLT, as there are no junctions in the transport direction and we still have the advantage of not having ultra steep source/channel and channel/drain doping profiles. We have an extra advantage of have the channel region being depleted, due p-n junction in the direction normal to the transport direction. As the channel of the JLT needs to be fully depleted in the OFF state, the choice of the SOI thickness in the case SOI-JLT is very limited and any variation in the specification would result in a large variation in the device characteristics. On the other hand, in BPJLT, as we have an additional contribution to the channel depletion, other than the one due to the channel to gate workfunction difference. This enabled us to use a thicker device layer (this is the junction depth in BPJLT and thickness of SOI in SOI-JLT) in BPJLT. Added to these, as the substrate conditions can control the amount of depletion in the channel, we have proposed to use the substrate doping and substrate bias as

knobs for tuning the device characteristics.

We also propose to use high-κ spacers in JLTs. This could be applied both to SOI and BPJLTs. Having high-κ spacers on either sides of the gate could enhance the gate fringing fields to the channel and can lead to an increased gate action on the channel. We show that this can be applied to reduce the OFF current by several orders of magnitude for a similar ON state current. In the ON state, as we have the channel in the flat band condition, the κ of the spacers does not make much of a difference to the source to drain current. However, as the device goes into accumulation, we see an increased source to drain current, again, this is due to the increased gate action because of the gate fringing fields through the high-κ spacers. We have shown that the effective gate length of the JLT is increased when the field is fringed through the high-κ spacers, however, in the ON state of JLT, i.e., around flat-band, the effective gate length is equal to the physical gate length. We find that the high-κ spacers will increase the parasitic capacitance of the device, which in turn effects the dynamic performance of JLT. In this context we mention that this proposal is only for application where the designer is concerned about the operating power than the speed of operation, i.e., low operating power (LOP) applications.

In addition to these proposals, we have studied the effect of quantum confinement on the JLT characteristics in the ON state. We observe that the quantum confinement in JLT is not due to the usual triangular well as in the case of conventional MOSFET, but is due to the rectangular quantum well formed in the direction normal to the transport direction. However, as the JLTs operate on the bulk conduction mechanism in contrary to surface conduction in conventional MOSFETs, the reduction in ON current due to quantum confinement is relatively less in JLTs. However, we have carried out this work by solving only a 1D Schrodinger-Poisson as our device designs are with an SOI thickness of 5nm and greater. Device designs with thickness less than this dimension would require a full quantum simulation which included the size quantization.

We also study the OFF state behaviour of JLTs in detail. As it is fully depleted in the OFF state, a large source to channel barrier is created and we observe that for a high drain bias, this results in a band overlap between the valance band of the channel and the conduction band of the drain. Hence, we observe a high probability of band-to-band tunneling to happen between the channel and drain for a high drain to source bias. In the SOI JLT, the minority carriers generated in the channel due to BTBT in the OFF state will remain accumulated in the channel it self. Hence, the accumulated carrier tend to increase the channel potential, which in turn decreases the source to channel barrier. We tried to relate this to a parasitic bipolar junction

transistor (BJT) action in the lateral direction, as the band diagram in the OFF state of JLT looks like a BJT. If we talk in terms of BJT, the carriers accumulated in the channel increases the bias at the base of the BJT which in turn forward biases the emitter to base junction and this would lead to triggering of parasitic BJT - and this action leads to a heavy source to drain leakage. The ways we suggest to improve this are (1) by changing the device architecture that can purge the carriers accumulated in the channel and we observe that this can be done by the BPJLT, where the carriers can be swept off to the substrate, reducing the BJT action (2) the other way could be to reduce the life time of the carriers in the channel so that the carriers accumulated in the channel recombine in the channel itself, before they trigger the parasitic BJT. However, all this analysis is for planar device architectures and the study of non-planar devices like a tri-gated or a gate all around JLT would require more robust band to band tunneling models.

Finally, we attempted to fabricate a thin film junctionless transistor with poly-Si as a channel material. Though we were able to see the transistor action, in devices, they suffer from poly-Si instability issues. That is, we see a degradation of conductivity of poly-Si during the fabrication process and this could possibly due to the native oxide that forms on top of poly-Si when exposed to ambient. There is a scope for further experiments in this direction, with an immediate passivation of poly-Si after the gate stack formation. However, there needs a further optimization of metallization through a via (i.e., the optimization of via etch, via metal fill, contact metal deposition and etch).

The findings presented in this work are mostly based on the simulation results obtained from a drift-diffusion solved by including appropriate models. This helped us to arrive at a qualitative understanding of the device operation. More rigorous information can be obtained by full quantum simulations using either non-equilibrium green's function (NEGF) approach [69] or Wigner-function approach [70]. There is good scope for research in investigating alternate materials in the device. For example, Germanium is a potential material to study for JLT applications as its higher mobility can further improve the ON state behaviour of the device. There is also a lot of scope to improve the process of thin film transistor fabrication by further improvements in processes developed (in Chapter 6) and by introducing additional processing steps like contact formation by a via through a passivation oxide layer.

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Annexure A: Process recipes for TFT fabrication

RCA Clean

Tool : Wet process bench.

- 2% HF dip: 1152ml DI water + 48ml(49%HF) for 30sec;
- RCA1: NH_4OH:H_2O_2:DI water in the ratio 125ml:250ml:875ml @75^{o}C, duration: 1200 sec.;
- 2% HF dip: 1152ml DI water + 48ml(49%HF) for 30sec;
- RCA2: HCl:H_2O_2:DI water in the ratio 125ml:250ml:875ml @75^{o}C, duration: 1200 sec.;
- 2% HF dip: 1152ml DI water + 48ml(49%HF) for 30 sec;

Thin dry oxide

Tool : Ultech furnace, stack 1, tube 1 - Dry oxidation.

- Pre-growth step: Temperature = 850^{o}C, O_2 gas flow = 50 sccm, N_2 gas = ON, duration = 120 sec
- Growth step: Temperature = 850^{o}C, O_2 gas flow = 5000 sccm, N_2 gas = OFF, duration = 1800 sec
- Expected thickness $\sim$ 10nm

Silicon Nitride deposition

Tool : Ultech furnace, stack 2, tube 3 - LPCVD.

- Ramp up step = 300 sec, temperature Stabilization step: 120 sec, pressure Stabilization step : 300sec
- Deposition step : SiH_4 gas flow: 80 sccm, NH_3 gas flow: 100sccm, N_2 gas flow: 1000sccm, temperature: 780^{o}C, pressure: 0.3 torr, duration: 3900 sec
- Expected-thickness = 60nm, stoichiometric

Pyrogenic oxide growth

Tool : Ultech furnace, stack 2, tube 1 - Pyrogenic oxidation.

- Growth step: H_2 gas flow = 8000 sccm, O_2 gas flow = 6000sccm, temperature = 1000^{o}C, torch temperature: 735^{o}C, time: 2400 sec
- Expected-thickness $\sim$ 300nm, across the wafer variation of 30nm

Poly-Si deposition by LPCVD of AMAT gate stack cluster

Tool : AMAT gate stack cluster, Chamber B (polygen) - LPCVD

- temperature = 700^{o}C, SiH_4 gas flow: 85 sccm, PH_3 gas flow = 120 sccm, Chamber Pressure = 275 Torr, time = 5sec.
- Expected -hickness = 10nm,
- Doping 10^{19} cm $^{-3}$

Poly-Si deposition by LPCVD in furnace

Tool : Ultech furnace, stack 3, tube 3 - LPCVD.

- temperature = 650^{o}C, SiH_4 gas flow = 80 sccm, PH_3 gas flow = 8 sccm, N_2 gas flow: 0 sccm, chamber Pressure: 170 mTorr, time : 6600 sec
- Expected thickness $\sim$ 150nm
- sheet resistance $\sim$ 150 ohm / square.

Thin Poly-Si deposition by LPCVD in furnace

Tool : Ultech furnace, stack 3, tube 3 - LPCVD.

- Deposition step : temperature = 500^{o}C, SiH_4 gas flow = 80 sccm, PH_3 gas flow = 8 sccm, N_2 gas flow: 0 sccm, chamber Pressure: 170 mTorr, time : 3600 sec
- Anneal step : temperature = 650^{o}C, SiH_4 gas flow = 0 sccm, PH_3 gas flow = 0 sccm, N_2 gas flow: 0 sccm, chamber Pressure: 45 mTorr, time : 3600 sec

- Expected thickness $\sim$ 10nm
- Doping $\sim 10^{19}$ cm $^{-3}$

Active area lithography

Tool : Double side aligner (EVG 620)

- Dehydration : 130^{o}C, 300sec on hotplate
- HMDS spin : 7000 rpm,45sec
- Bake : 120^{o}C, 3600sec
- Resist spin: Shipley 1813, 6000rpm, 45 sec(Program E)
- Prebake: 90^{o}C,120sec
- Exposure : 64mJ/cm^2, (V+H)contact, 1um separation
- Development : MF 319(vertical), 25sec
- Post development bake : 90C, 60sec

Gate area lithography

Tool : Double side aligner (EVG 620)

- Dehydration : 130^{o}C, 300sec on hotplate
- HMDS spin : 7000 rpm,45sec
- Bake : 120^{o}C, 3600sec
- Resist spin: Shipley 1813, 6000rpm, 45 sec(Program E)
- Prebake: 90^{o}C,120sec
- Exposure : 50mJ/cm^2, soft contact, 1um separation
- Development : MF 319(vertical), 25sec
- Post development bake : 90C, 60sec

Silicon Nitride etch

Tool : STS RIE

- CF_4 gas flow : 40sccm, O_2 gas flow : 4sccm, RF Power for Selective Etch (SE) = 50W, Chamber pressure(SE) = 110 mTorr,
- Etch rate of Si3N4 (SE) = 31 (nm/min)
- Etch rate of SiO2 (SE) = 9 (nm/min)
- Selectivity obtained : 3.5

Poly-Si etch

Tool : STS RIE

- CF_4 gas flow = 40sccm, O2 gas flow = 5sccm, RF Power for Selective Etch (SE) = 350W, Chamber pressure(SE) : 20mTorr
- Etch rate of poly-Si (SE) (nm/min) : 210
- Selectivity obtained with SiO2 : 2.5

Piranha clean

Tool : Micro 1 wet bench

- H_2SO_4:H_2O_2 in the ratio 910ml:390ml for 3600sec

Activation anneal

Tool : Annealsys RTP

- Temperature = 950^{o}C, time = 5 sec, N_2 gas flow = 1000sccm

TiN deposition

Tool : AMAT endura - PVD

- Power: 300W, argon gas flow : 20sccm, N_2 gas flow : 20sccm, time : 900sec

- Expected thickness $\sim$ 80nm

TiN wet etch

Tool : Micro-1 wet bench

- NH_4OH:H_2O_2:H_2O in the ratio 1:2:7 @60^{o}C for 60sec

Al deposition

Tool : Al thermal evaporator

- Pressure : 2x10 $^{-6}$ mbar
- Expected thickness: Al pellet has chosen to give a approximate thickness of 100nm

Al wet etch

Tool : Micro-1 wet bench

- H_3PO_4:CH_3COOH:HNO_3:H_2O in the ratio 16:1:1:2 @ 25^{o}C for 150 sec

Oxide etch in BHF

Tool : Micro-1 wet bench

- 5:1 BHF
- Etch rate: 110nm/min.

Annexure B: Proposed process flow for BPJLT

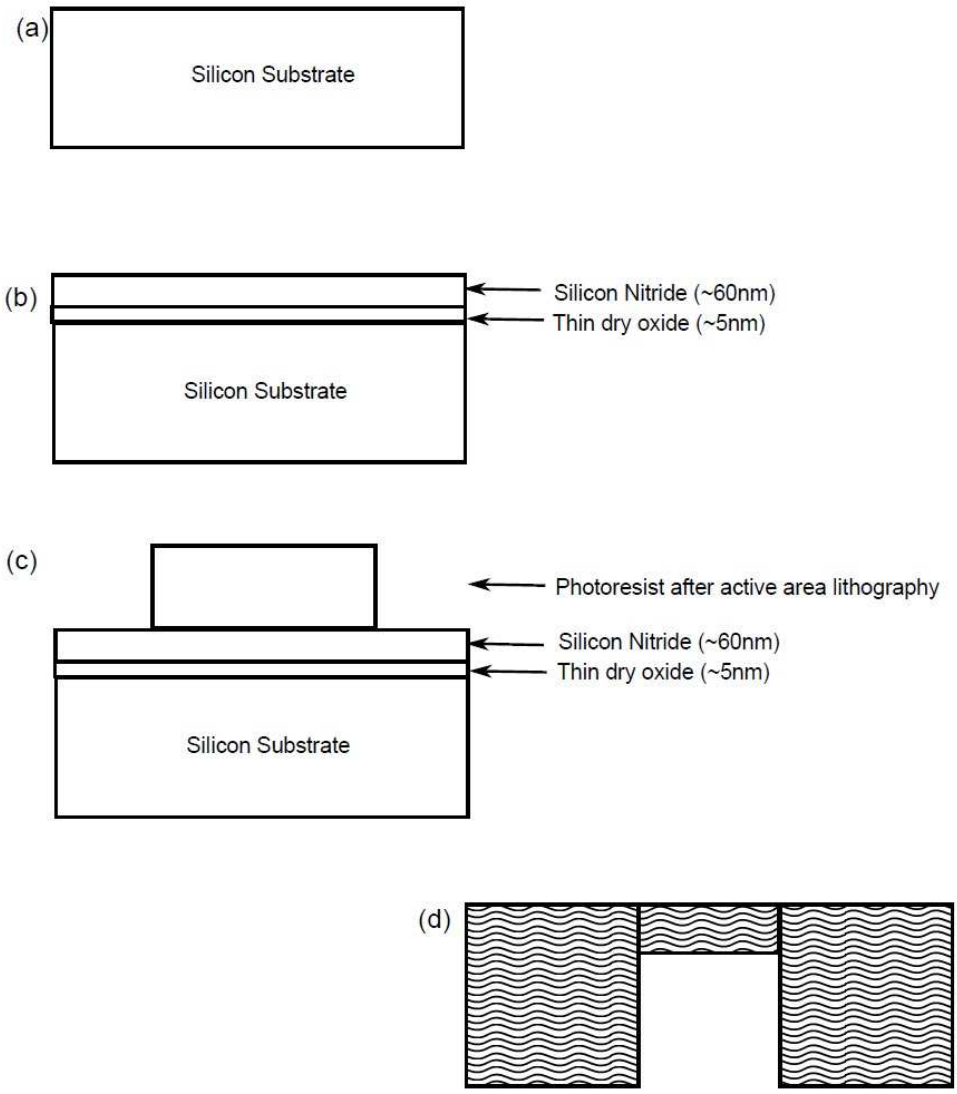

Figure A: Process flow for BPJLT (part 1)

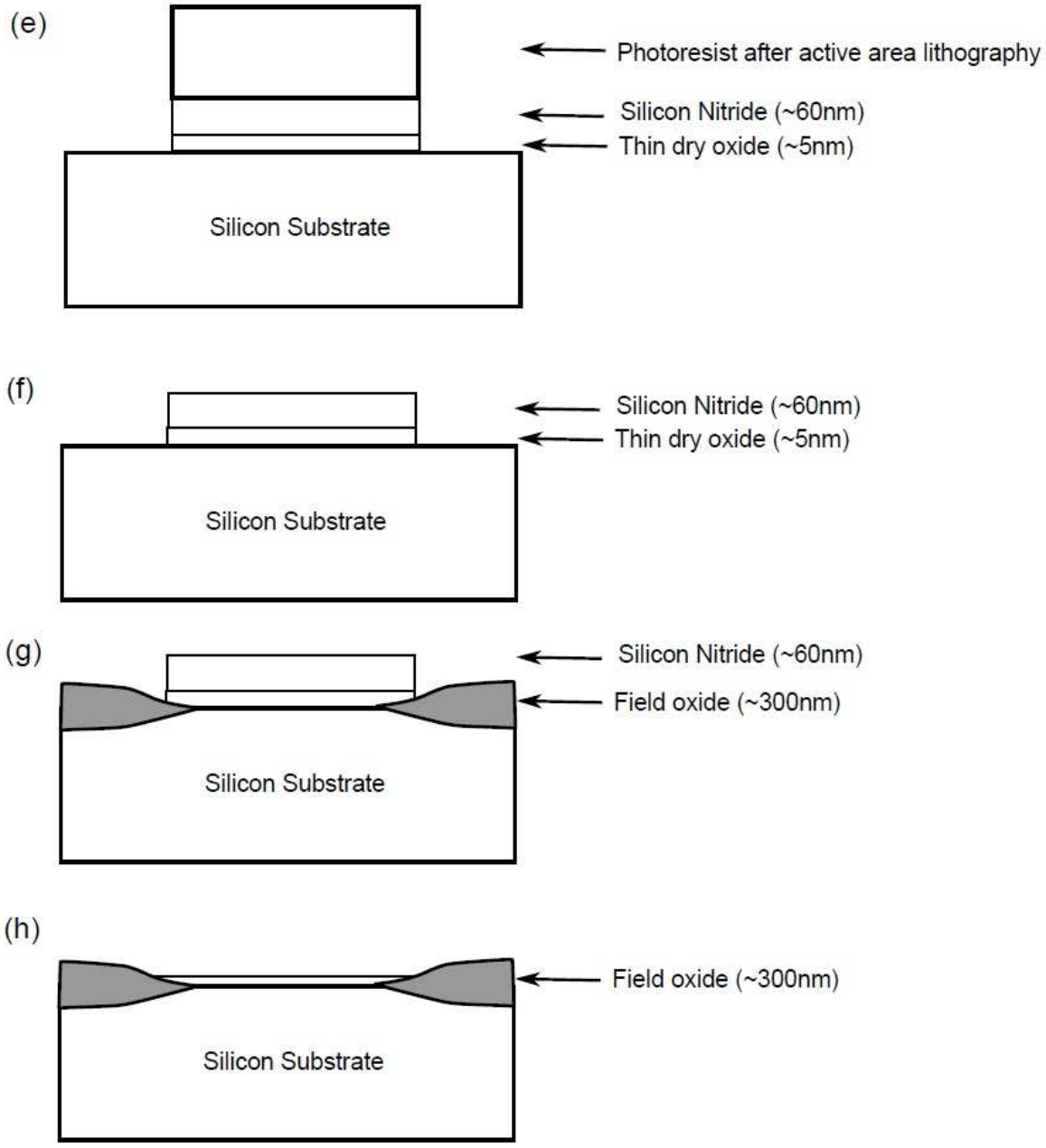

Figure B: Process flow for BPJLT (part 2)

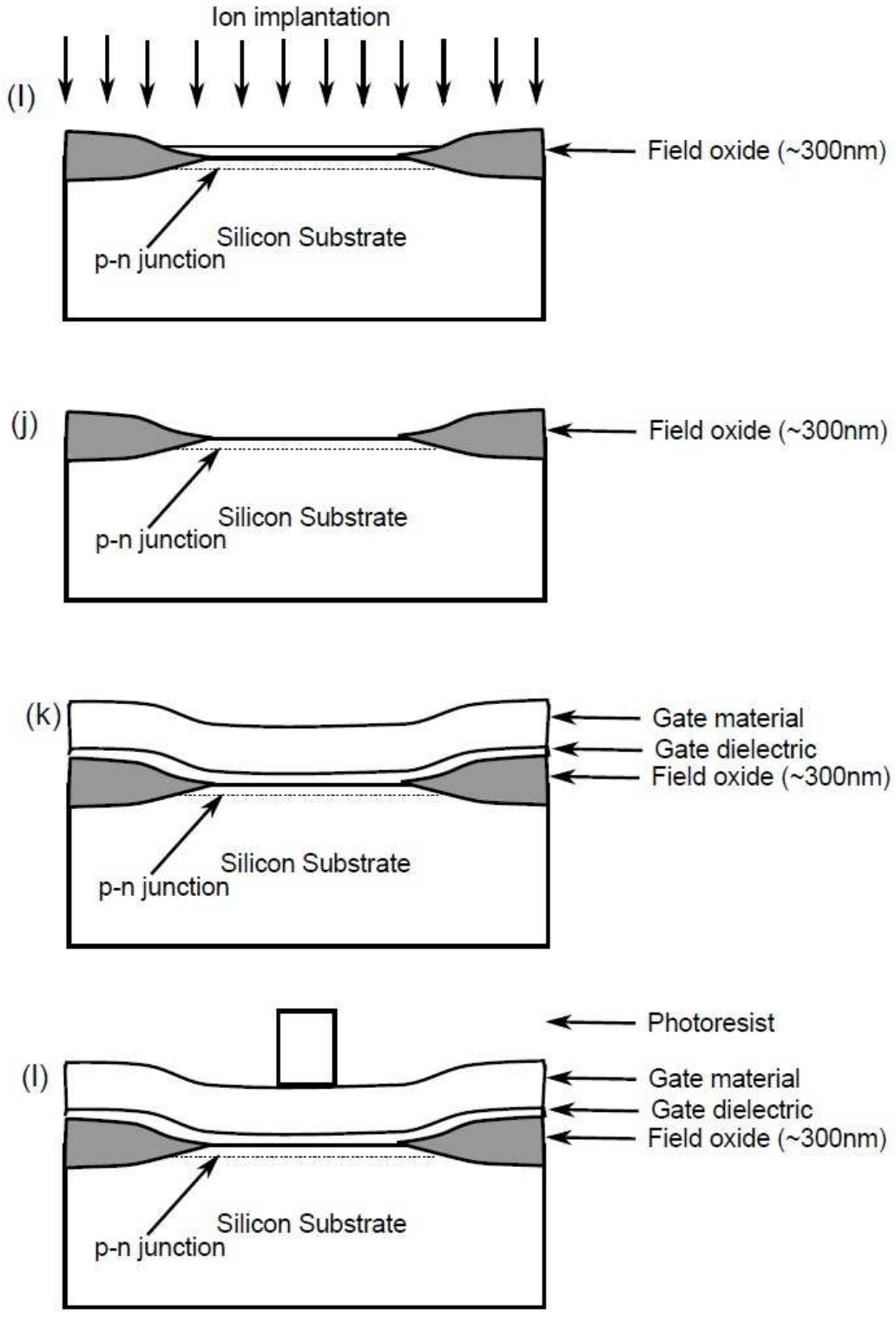

Figure C: Process flow for BPJLT (part 3)

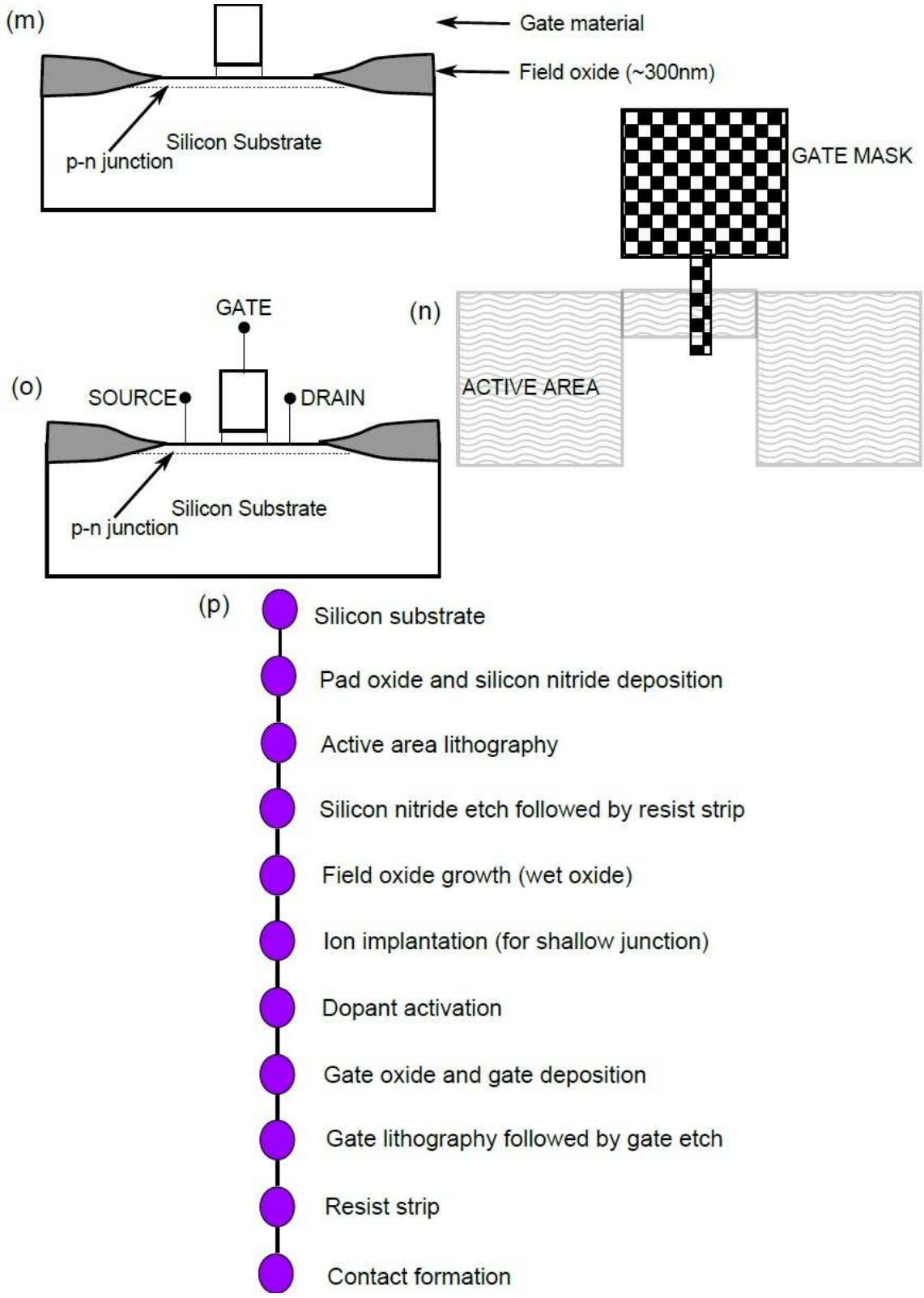

Figure D: Process flow for BPJLT (part 4)

Annexure C: Sentaraus simulation decks

A: Models used

The calibration of the SOI JLT is done against the published experimental data of tri-gated SOI JLT [2]. In the structure we created using SDE, while we keep all geometrical dimensions similar to the cross-sectional TEM images and the descriptions provided in [2], we have made process assumptions in the Si doping and the dielectric constant of the gate dielectric. We keep the Si doping as $1.5x10^{19}$ and the gate dielectric constant as 21. Models included in the simulation are:

(a) Philips unified mobility model - as this takes care of the mobility degradation of both due to impurity scattering and due to carrier-carrier scattering.
This is enabled by keyword `Mobility{PhuMob}` in the physics section of Sdevice.

(b) Mobility saturation due to high electric field is taken into account.
This is enabled by keyword `Mobility{HighFieldSat}` in the physics section of Sdevice.

(c) Mobility dependence on transverse electric field is taken into account.
This is enabled by keyword `Mobility{Enormal}` in the physics section of Sdevice.

(d) Bandgap narrowing due to high Si doping is taken into account by the "oldSlotboom" model.
This is enabled by keyword `EffectiveIntrinsicDensity(BandGapNarrowing (oldSlotboom))` in Sdevice.

(e) SRH and Auger recombination models are included in the simulation deck. However, we do not turn ON the doping dependant SRH model, rather we use a constant carrier life time as 10^{-7} and this corresponds to Si when the doping is 10^{19} [60]
This is enabled by keyword `Recombination( SRH Auger)` in Sdevice.

(f) As the doping of Si is only $\sim 10^{19}$ we use a distributed contact resistance in the electrode section of Sdevice

This is included by

```
Electrode { { Name="s" Voltage=0.0 DistResistance=1.5e-6}
{ Name="d" Voltage=0.0 DistResistance=1.5e-6}
{ Name="g" Voltage=0.0 workfunction=5.1}}
{ Name="sub" Voltage=0.0 Barrier=0}}
```

Where, the term `DistResistance=1.5e-6` corresponds to the distributed resistance and we have included this both at the source and drain contacts. The substrate contact is assumed to be ohmic. The gate workfunction is chosen to be 5.1eV for n-channel transistor, unless it is explicitly mentioned.

(g) In Chapter 5 of the thesis we have included the WKB approximation of non-local band-to-band tunneling model. This is calibrated against the experimental data as mentioned in [44]

This is enabled by keyword

```
Recombination(eBarrierTunneling(Band2Band TwoBand Transmission)
hBarrierTunneling(Band2Band TwoBand
Transmission))
```

The electron and hole mass values in the `BarrierTunneling` part of the parameter file are set to 0.65 as mentioned in [44]. However, a proper non-local mesh needs to be specified specified between regions of the device. For example, in our BPJLT simulations in Chapter 5, we have specified the mesh between the substrate and the device layer (i.e., source, drain and channel) as well as between the channel and drain. We observed that this model is strongly dependant on the mesh spacing, the length of tunneling distance we specify and the position of the tunneling interface. So, for the simulations in Chapter 5, we have made sure that these parameters are properly fixed so that the results are consistent with variations in mesh spacing etc. for a given structure.

B: SDE script for BPJLT

We here provide the SDE script for the BPJLT simulations carried out in Chapter 5.

```
(define contlen 0.015)
(define gapmar 0.025)
(define gatlen 0.02)
(define tox 0.001)
(define strulen (+ (+ (* contlen 2) gatlen) (* 2 gapmar)))
(define bashit -0.15)
(define wirhit 0.012)
(sdegeo:create-rectangle (position 0 0 0) (position strulen \
bashit 0) "Silicon" "region_1" )
(sdegeo:create-rectangle (position 0 (+ bashit wirhit) 0) \
(position (+ gatlen (+ contlen gapmar)) bashit 0) "Silicon" \
"region_Epi1" )
(sdegeo:create-rectangle (position (+ gatlen (+ contlen \
gapmar)) (+ bashit wirhit) 0) (position strulen \
bashit 0) "Silicon" "region_Epi2" )
(sdedr:define-refeval-window "Wire" "Rectangle" (position 0 \
(+ bashit (+ wirhit 0.003)) 0) (position strulen \
bashit 0))
(sdedr:define-refeval-window "Tunn" "Rectangle" \
(position (- (+ gatlen (+ contlen gapmar)) 0.04) \
(+ bashit (+ wirhit 0.005)) 0) (position (+ (+ gatlen \
(+ contlen gapmar)) 0.04) bashit 0))
(sdegeo:set-default-boolean "BAB")
(sdegeo:create-rectangle (position (+ contlen gapmar)\
bashit 0)
(position (+ gatlen (+ contlen gapmar)) (- bashit \
tox) 0) "SiO2" "region_3" )
(sdegeo:create-rectangle (position 0 bashit 0) (position \
contlen (- bashit 0.0005) 0) "Silicon" "region_5" )
(sdegeo:create-rectangle (position (- strulen contlen)\
```

```
bashit 0) (position strulen (- bashit 0.0005) 0) \
"Silicon" "region_6" )
(sdegeo:define-contact-set "d" 4 (color:rgb 1 0 0 ) "##" )
(sdegeo:define-contact-set "s" 4 (color:rgb 1 0 0 ) "##"" )
(sdegeo:define-contact-set "g" 4 (color:rgb 1 0 0 ) "##"" )
(sdegeo:define-contact-set "sub" 4 \
(color:rgb 1 0 0 ) "##"" )
(sdegeo:define-2d-contact (list (car (find-edge-id \
(position (/ contlen 2) (- bashit 0.0005) 0)))) "s")
(sdegeo:define-2d-contact (list (car (find-edge-id \
(position (- strulen (/ contlen 2)) (- bashit \
0.0005) 0)))) "d")
(sdegeo:define-2d-contact (list (car (find-edge-id \
(position (+ (+ contlen gapmar) (/ gatlen 2)) (- \
bashit tox) 0 )))) "g")
(sdegeo:define-2d-contact (list (car \
(find-edge-id (position (+ (+ contlen gapmar) \
(/ gatlen 2)) 0 0)))) "sub")
(sdedr:define-refinement-size "RefinementDefinition_1" \
0.0004 0.0004 0.0004 0.0004 0.0004 0.0004 )
(sdedr:define-refinement-region "RefinementPlacement_1" \
"RefinementDefinition_1" "region_Epi1" )
(sdedr:define-refinement-region "RefinementPlacement_1a" \
"RefinementDefinition_1" "region_Epi2" )
(sdedr:define-refinement-size "RefinementDefinition_2" \
0.001 0.0003 0.001 0.001 0.0003 0.001 )
(sdedr:define-refinement-region "RefinementPlacement_2" \
"RefinementDefinition_2" "region_3" )
(sdedr:define-refinement-size "RefinementDefinition_9" \
0.002 0.002 0.002 0.002 0.002 0.002 )
(sdedr:define-refinement-region "RefinementPlacement_9" \
"RefinementDefinition_9" "region_1" )
```

```
(sedr:define-refinement-region "RefinementPlacement_soi" \
"RefinementDefinition_9" "region_soi" )
(sedr:define-refeval-window "RefEvalWin_1" "Rectangle" \
(position (+ 0.05 gapmar) (- bashit wirhit) 0) (position \
(+ 0.15 gapmar) bashit 0) )
(sedr:define-refeval-window "RefEvalWin_2" "Rectangle" \
(position (+ gatlen (+ 0.05 gapmar)) (- bashit wirhit) 0) \
(position (+ gatlen (+ 0.15 gapmar)) bashit 0) )
(sedr:define-refinement-size "RefinementDefinition_3" \
0.001 0.001 0.001 0.001 0.001 0.001 )
(sedr:define-refinement-region "RefinementPlacement_con1" \
"RefinementDefinition_3" "region_5" )
(sedr:define-refinement-region "RefinementPlacement_con2" \
"RefinementDefinition_3" "region_6" )
(sedr:define-refinement-placement "RefinementPlacement_3" \
"RefinementDefinition_3" "RefEvalWin_1" )
(sedr:define-refinement-placement "RefinementPlacement_4" \
"RefinementDefinition_3" "RefEvalWin_2" )
(sedr:define-constant-profile \
"ConstantProfileDefinition_1" \
"BoronActiveConcentration" 5000000000000000000)
(sedr:define-constant-profile-material \
"ConstantProfilePlacement_1" \
"ConstantProfileDefinition_1" "Silicon")
(sedr:define-refeval-window "RefEvalWin_3" "Line" \
(position 0 bashit 0) (position strulen \
bashit 0))
(sedr:define-gaussian-profile \
"AnalyticalProfileDefinition_2"
"PhosphorusActiveConcentration" "PeakPos" 0 \
"PeakVal" 2e19 "ValueAtDepth" 5e18 "Depth" \
wirhit "Gauss" "Factor" 0.5)
```

```
(sdedr:define-analytical-profile-placement \
"AnalyticalProfilePlacement_3" \
"AnalyticalProfileDefinition_2" \
"RefEvalWin_3" "Both" "NoReplace" "Eval")
(sde:build-mesh "mesh" "-t -F tdr " "20nm-BJLT-Gauss-TED")
```

C: Sdevice script for BPJLT

We here provide the Sdevice script for the BPJLT simulations carried out in Chapter 5.

```
File{ Grid = "20nm-BJLT-Gauss-TED_msh.tdr"
Current = "IdVg_Vg=1Vguess-20nmLg-BulkGauss-TED-SRH-BTB.plt"
Plot = "PlotOUT_20nmLg_msh.tdr"
Output = "SOI-20nmLg_msh1_des.log"
Parameter = "ntfet2.par"}
Electrode {{ Name="s" Voltage=0.0 DistResistance=1.5e-6}
{ Name="d" Voltage=0.0 DistResistance=1.5e-6}
{ Name="g" Voltage=0 workfunction=5.1}
{ Name="sub" Voltage=0.0 Barrier=0.0 }}
Physics {Mobility( PhuMob HighFieldSat Enormal )
EffectiveIntrinsicDensity(BandGapNarrowing (oldSlotboom))
Recombination(SRH Auger
eBarrierTunneling(Band2Band TwoBand Transmission)
hBarrierTunneling(Band2Band TwoBand Transmission) )}
Plot{eDensity hDensity eCurrent hCurrent equasiFermi
hquasiFermi AvalancheGeneration eGradQuasiFermi
ConductionBandEnergy ValenceBandEnergy ConductionCurrent
DisplacementCurrent eAlphaAvalanche hAlphaAvalanche
EffectiveBandGap EquilibriumPotential eQuasiFermi
EffectiveBandGap hGradQuasiFermi hQuasiFermi IntrinsicDensity
EffectiveIntrinsicDensity eTemperature eIonIntegral Auger
ElectricField eEparallel hEparallel Potential Doping
SpaceCharge SRHRecombination eMobility hMobility
eVelocity hVelocity DonorConcentration
```

```
AcceptorConcentration
eIonIntegral hIonIntegral
MeanIonIntegral BuiltinPotential
eDriftVelocity Band2Band BandGap
HotElectronInjection HotHoleInjection
eBarrierTunneling hBarrierTunneling }
Math {Extrapolate
Derivatives
RelErrcontrol
Iterations=10
NewDiscretization
Method=Blocked SubMethod=ParDiso
number_of_threads = 4
stacksize = 2000000
wallclock }
Math(regionInterface="region_Epi1/region_Epi2"){
NonLocal(Length=2.5e-6 Permeable Permeation=2.5e-6)
Digits(NonLocal)=3
EnergyResolution(NonLocal)=0.001 }
Math(regionInterface="region_Epi1/region_1"){
NonLocal(Length=2e-6 Permeable Permeation=2e-6)
Digits(NonLocal)=3
EnergyResolution(NonLocal)=0.001}
Math(regionInterface="region_1/region_Epi2"){
NonLocal(Length=2e-6 Permeable Permeation=2e-6)
Digits(NonLocal)=3
EnergyResolution(NonLocal)=0.001}
Solve { Poisson
Coupled { Poisson Electron hole}
Quasistationary (
Initialstep = 0.025 Maxstep = 0.05 Minstep = 1e-6
Goal{ name="sub" voltage=0 })
```

```
{ Coupled { Poisson Electron Hole } }
Quasistationary (
Initialstep = 0.0125 Maxstep = 0.05 Minstep = 1e-6
Goal{ name="d" voltage=1.0 })
{ Coupled { Poisson Electron Hole } }
Quasistationary
(InitialStep=0.025 Maxstep=0.05 MinStep=1e-6
Goal{ name="g" voltage=0 })
{ Coupled {Poisson Electron Hole }}
plot ( FilePrefix = \
"Vg=1Vguess-20nm-BulkGauss_vg=0-BTB")
Quasistationary
(InitialStep=0.025 Maxstep=0.025 MinStep=1e-6
Goal{ name="g" voltage=-1 })
{ Coupled {Poisson Electron Hole }}
```

D: SDE script for SOI-JLT

We here provide the SDE script for the SOI-JLT simulations carried out in Chapter 5.

```
(define contlen 0.015)
(define gapmar 0.025)
(define gatlen 0.02)
(define tox 0.001)
(define strulen (+ (+ (* contlen 2) gatlen) \
(* 2 gapmar)))
(define bashit -0.15)
(define wirhit (/ 6 1000))
(sdegeo:create-rectangle (position 0 0 0) (position \
strulen bashit 0) "Silicon" "region_1" )
(sdegeo:create-rectangle (position 0 (+ bashit wirhit)\
0) (position (+ gatlen (+ contlen gapmar)) bashit 0)\
"Silicon" "region_Epi1" )
(sdegeo:create-rectangle (position (+ gatlen (+ contlen\
```

```
gapmar)) (+ bashit wirhit) 0) (position strulen bashit \
0) "Silicon" "region_Epi2" )
(sdegeo:create-rectangle (position 0 (+ bashit (+ wirhit \
0.1)) 0) (position strulen (+ bashit wirhit) 0) "SiO2" \
"region_soi" )
(sdedr:define-refeval-window "Wire" "Rectangle" (position\
0 (+ bashit (+ wirhit 0.003)) 0) (position\
strulen bashit 0))
(sdedr:define-refeval-window "Tunn" "Rectangle" \
(position (- (+ 0 (+ contlen gapmar)) 0.00) (+ bashit \
(+ wirhit 0.005)) 0) (position (+ (+ gatlen (+ contlen \
gapmar)) 0.005) bashit 0))
(sdegeo:set-default-boolean "BAB")
(sdegeo:create-rectangle (position (+ contlen gapmar) \
bashit 0) (position (+ gatlen (+ contlen gapmar)) (- bashit \
tox) 0) "SiO2" "region_3" ) (sdegeo:create-rectangle (position 0
bashit 0) (position\
contlen (- bashit 0.0005) 0) "Silicon" "region_5" )
(sdegeo:create-rectangle (position (- strulen contlen) \
bashit 0) (position strulen (- bashit 0.0005) 0)\
"Silicon" "region_6" )
(sdegeo:define-contact-set "d" 4 (color:rgb 1 0 0 ) "##" )
(sdegeo:define-contact-set "s" 4 (color:rgb 1 0 0 ) "##" )
(sdegeo:define-contact-set "g" 4 (color:rgb 1 0 0 ) "##" )
(sdegeo:define-contact-set "sub" 4 \
(color:rgb 1 0 0 ) "##" )
(sdegeo:define-2d-contact (list (car (find-edge-id \
(position (/ contlen 2) (- bashit 0.0005) 0)))) "s")
(sdegeo:define-2d-contact (list (car (find-edge-id \
(position (- strulen (/ contlen 2)) (- bashit 0.0005) 0)))) "d")
(sdegeo:define-2d-contact (list (car (find-edge-id \
(position (+ (+ contlen gapmar) (/ gatlen 2)) (- bashit tox) 0 ))))
```

```
"g") (sdegeo:define-2d-contact (list (car (find-edge-id \
(position (+ (+ contlen gapmar) (/ gatlen 2)) 0 0)))) "sub")
(sdedr:define-refinement-size "RefinementDefinition_1"\
0.001 0.0005 0.0005 0.001 0.0005 0.0005 )
(sdedr:define-refinement-region "RefinementPlacement_1"\
"RefinementDefinition_1" "region_Epi1" )
(sdedr:define-refinement-region "RefinementPlacement_1a"\
"RefinementDefinition_1" "region_Epi2" )
(sdedr:define-refinement-size "RefinementDefinition_2"\
0.0002 0.00005 0.00005 0.0002 0.00005 0.00005 )
(sdedr:define-refinement-region "RefinementPlacement_2"\
"RefinementDefinition_2" "region_3" )
(sdedr:define-refinement-size "RefinementDefinition_9"\
0.002 0.0005 0.0005 0.002 0.0005 0.0005 )
(sdedr:define-refinement-region "RefinementPlacement_9"\
"RefinementDefinition_9" "region_1" )
(sdedr:define-refinement-region "RefinementPlacement_soi"\
"RefinementDefinition_9" "region_soi" )
(sdedr:define-refeval-window "RefEvalWin_1" "Rectangle"\
(position (+ 0.05 gapmar) (- bashit wirhit) 0) \
(position (+ 0.15 gapmar) bashit 0) )
sdedr:define-refeval-window "RefEvalWin_2" "Rectangle" \
(position (+ gatlen (+ 0.05 gapmar)) (- bashit wirhit) 0)\

(position (+ gatlen (+ 0.15 gapmar)) bashit 0) )
(sdedr:define-refinement-size "RefinementDefinition_3"\
0.001 0.001 0.001 0.001 0.001 0.001 )
sdedr:define-refinement-region "RefinementPlacement_con1"\
"RefinementDefinition_3" "region_5" )
(sdedr:define-refinement-region "RefinementPlacement_con2"\
"RefinementDefinition_3" "region_6" )
(sdedr:define-refinement-placement "RefinementPlacement_3"\
```

```
"RefinementDefinition_3" "RefEvalWin_1" )
(sedr:define-refinement-placement "RefinementPlacement_4"\
"RefinementDefinition_3" "RefEvalWin_2" )
(sedr:define-refeval-window "RefEvalWin_top" "Rectangle"\
(position 0 (- bashit wirhit) 0) (position strulen bashit 0))
(sedr:define-refinement-size "RefinementDefinition_top"\
0.001 0.001 0.001 0.001 0.001 0.001 )
(sedr:define-refinement-placement "RefinementPlacement_top"\
"RefinementDefinition_top" "RefEvalWin_top" )
(sedr:define-refinement-size "RefinementDefinition_tunn"\
0.0002 0.00005 0.00005 0.0002 0.00005 0.00005 )
(sedr:define-refinement-placement "RefinementPlacement_ttunn"\
"RefinementDefinition_tunn" "Tunn" )
(sedr:define-constant-profile "ConstantProfileDefinition_1"\
"PhosphorusActiveConcentration" 50000000000000000)
(sedr:define-constant-profile-region "ConstantProfilePlacement_1"\
"ConstantProfileDefinition_1" "region_1")
(sedr:define-constant-profile "ConstantProfileDefinition_1a"\
"PhosphorusActiveConcentration" wirdop_val)
(sedr:define-constant-profile-region "ConstantProfilePlacement_1aa"\
"ConstantProfileDefinition_1a" "region_Epi1")
(sedr:define-constant-profile-region "ConstantProfilePlacement_1ab"\
"ConstantProfileDefinition_1a" "region_Epi2")
(sedr:define-constant-profile-region "ConstantProfilePlacement_1b"\
"ConstantProfileDefinition_1a" "region_5")
(sedr:define-constant-profile-region "ConstantProfilePlacement_1c"\
"ConstantProfileDefinition_1a" "region_6")
(sde:build-mesh "mesh" "-t -F tdr " "SOI-JLT")
```

E: Sdevice script for SOI-JLT

We here provide the Sdevice script for the SOI-JLT simulations carried out in Chapter 5.

```
File {Grid = "SOI-JLT_msh.tdr"
```

```
Current = "IdVg-BTB.plt"
Plot = "PlotOUT_msh.tdr"
Output = "Logoutput_des.log"
Parameter = "ntfet2.par"}
Electrode {{ Name="s" Voltage=0.0 DistResistance=1.5e-6}
{ Name="d" Voltage=0.0 DistResistance=1.5e-6}
{ Name="g" Voltage=0 workfunction=5.1}
{ Name="sub" Voltage=0.0 Barrier=0.0 }}
Physics { Mobility( PhuMob HighFieldSat Enormal)
EffectiveIntrinsicDensity(BandGapNarrowing (oldSlotboom))
Recombination( SRH Auger
eBarrierTunneling(Band2Band TwoBand Transmission)
hBarrierTunneling(Band2Band TwoBand Transmission))}
Plot{eDensity hDensity eCurrent hCurrent equasiFermi
hquasiFermi AvalancheGeneration eGradQuasiFermi
ConductionBandEnergy ValenceBandEnergy ConductionCurrent
DisplacementCurrent eAlphaAvalanche hAlphaAvalanche
EffectiveBandGap EquilibriumPotential eQuasiFermi
EffectiveBandGap hGradQuasiFermi
hQuasiFermi IntrinsicDensity
EffectiveIntrinsicDensity eTemperature eIonIntegral Auger
ElectricField eEparallel hEparallel Potential Doping
SpaceCharge SRHRecombination eMobility hMobility
eVelocity hVelocity
DonorConcentration AcceptorConcentration
eIonIntegral hIonIntegral
MeanIonIntegral BuiltinPotential
eDriftVelocity Band2Band BandGap
HotElectronInjection HotHoleInjection
eBarrierTunneling hBarrierTunneling}
Math {Extrapolate
Derivatives
```

```
RelErrcontrol
Iterations=20
NewDiscretization
Method=Blocked SubMethod=ParDiso
number_of_threads = 2
stacksize = 2000000
wallclock}
Math(regionInterface="region_Epi1/region_Epi2"){
NonLocal(Length=2.5e-6 Permeable Permeation=2.5e-6)
Digits(NonLocal)=3
EnergyResolution(NonLocal)=0.001}
Solve {Poisson
Coupled { Poisson Electron hole}
Quasistationary (
Initialstep = 0.025 Maxstep = 0.05 Minstep = 1e-6
Goal{ name="sub" voltage=0 })
{ Coupled { Poisson Electron Hole } }
Quasistationary (
Initialstep = 0.0125 Maxstep = 0.05 Minstep = 1e-6
Goal{ name="d" voltage=1.0 })
{ Coupled { Poisson Electron Hole } }
Quasistationary
(InitialStep=0.025 Maxstep=0.05 MinStep=1e-6
Goal{ name="g" voltage=0 })
{ Coupled {Poisson Electron Hole }}
NewCurrent="OUT_Vd=1V"
plot ( FilePrefix = "vg=0-BTB")
Quasistationary
(InitialStep=0.025 Maxstep=0.05 MinStep=1e-6
Goal{ name="g" voltage=0.5 })
{ Coupled {Poisson Electron Hole }}
plot ( FilePrefix = "vg=0.5-BTB")
```

```
Quasistationary
(InitialStep=0.025 Maxstep=0.05 MinStep=1e-6
Goal{ name="g" voltage=0 })
{ Coupled {Poisson Electron Hole }}
plot ( FilePrefix = "vg=0-BTB")
Quasistationary
(InitialStep=0.025 Maxstep=0.05 MinStep=1e-6
Goal{ name="g" voltage=-0.5 })
{ Coupled {Poisson Electron Hole }}
plot ( FilePrefix = "vg=-0.5-BTB")
Quasistationary
(InitialStep=0.025 Maxstep=0.05 MinStep=1e-6
Goal{ name="g" voltage=-1 })
{ Coupled {Poisson Electron Hole }}
plot ( FilePrefix = "vg=-1-BTB")}
```

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List of Publications

[1] M. Golve, **S. Gundapaneni**, A. Kottantharayil, "Novel Architectures for Zinc-Oxide Junctionless Transistor", to appear in IEEE Xplore, *International Conference on Emerging Electronics (ICEE)*, December, 2012.

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