Anwesha Mukhopadhyay

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RESEARCH INTEREST

High Power-density traction inverter for EVs, EMI filter design for EV applications, GaN Power Module Fabrication, harmonic filtering, active power decoupling, grid-connected converter for renewable and storage, wireless power transfer: inductive and capacitive.

EDUCATION

Indian Institute of Science, Bangalore, India Aug., 2017 - Aug., 2023
Ph.D. in Electrical Engineering (Thesis Submission)
CGPA: 8.9/10 March, 2024 (Defence)
Advisor: Prof. Vinod John

Indian Institute of Technology, Kanpur, India Jul., 2014 - Jul., 2016
M.Tech in Electrical Engineering
CGPA: 10/10 (Ranked 1st in M.Tech Batch, EE Dept.)

Jadavpur University, Kolkata, India Jul., 2005 - Jun., 2009
B.E., Electrical Engineering
CGPA: 9.03/10 (Ranked 6th among 131 students in EE Dept.)

West Bengal Council of Higher Secondary Education 2005
Higher Secondary (Class XII) 92.6%

West Bengal Board of Secondary Education 2003
Secondary (Class X) 95%
(First in the state among female students)

WORK EXPERIENCE

Academic:
Post-doc researcher at Univ. of Tennessee, Knoxville, USA Oct., 2023 - Till date

- Managing 3 projects funded by Department of Energy (DoE), USA, Army Research Lab (ARL), USA, and Texas Instruments, USA.
- Leading efforts in innovative and power-dense EMI filter design, resulting in 200 kW/L inverter design, GaN-based power module design for 3-level EV traction inverter.
- Leading innovation activities for Wireless Power Transfer for Drones requiring high volumetric power density.
- Mentoring and technical training of team members in hardware and firmware development, debugging, and testing.
- Interdisciplinary collaboration with Thermal and Motor Design teams.

Junior Research Fellow in IIT Kanpur, India Jul., 2016-May, 2017

Industry:
National Thermal Power Corporation (NTPC) Limited, Farakka, India.
Deputy Manager (E3), Electrical Maintenance (Generator and Aux.) Oct., 2013 - Jun., 2014
Engineer (E2A), Electrical Maintenance (Generator and Aux.) Oct., 2009 - Oct., 2013

ACADEMIC RECOGNITIONS

- **IEEE Industry Application Society (IAS) CMD Student Thesis Contest 2024, PhD category**, 3rd prize winner for the Ph.D dissertation, titled "Reduced Electrolytic Capacitor-Based Single-Phase Converters: Topologies, Control, and Stability"
- **Prof. D. J. Badkas Medal** for the best Ph.D thesis in the Department of Electrical Engineering for the year 2024-25, IISc, Bangalore.
- **Grid India Power Systems Award (GIPSA, previously POSOCO), 2024-25** for Ph.D thesis.

- **Academic Excellence Award** for securing the highest CGPA (10/10) in M.Tech in IIT Kanpur, 2016.
- **Academic Excellence Scholarship**, State Electrical Engineers' Association, West Bengal, 2008 for excellence in Bachelor of Electrical Engineering studies.
- **Ranked 79 in Engineering** Entrance Examination (Total No. of candidates 50,263) and **291 in Medical** Entrance Examination (Total No. of candidates 36,322) in West Bengal Joint Entrance Examination 2005 (WBJEE-2005).
- **West Bengal Board of Secondary Education Merit Award** and **Gold medal from All Bengal Teachers' Association (ABTA)** for **securing 1st position in the state among female students** in the secondary examination (class X), 2003.
- **Governor's Certificate for First position among the female students in the district** in the secondary examination (class X), 2003.

PROFESSIONAL RECOGNITIONS

- Invited tutorial talk on "Active Impedance DC Filter for Single-Phase Power Conversion" in **IEEE Energy Conversion Congress and Exposition (ECCE) Asia 2025**, Bangalore, India, May 11-14, 2025.
- Among 10% selected out of 221 posters for **Dialog Preview Session** in **IEEE Applied Power Electronics Conference (APEC), 2025**, Atlanta, Georgia, USA, Mar 15-20, 2025.
- **IEEE IAS Annual Meeting Travel Grant Program, AMTGP 2024** for attending IEEE IAS Annual Meeting, 2024, held at Phoenix, Arizona, USA.
- **WIE Travel Grant Award** (not availed) for IEEE Energy Conversion Congress and Exposition (ECCE), 2024, awarded by IEEE Women in Engineering.
- **Student Attendance Grant** for IEEE Energy Conversion Congress and Exposition (ECCE), 2022, awarded by IEEE PELS and IAS.
- **Student Attendance Support** for IEEE Applied Power Electronics Conference (APEC), 2022, awarded by Power Sources Manufacturers Association (PSMA).

TEACHING EXPERIENCE

- Tutorial class in **ECE202: Circuits II** for Sophomore on Circuits at the University of Tennessee, Knoxville.
- Lab course **ECE 482/582: Power Electronic Circuits** at the University of Tennessee, Knoxville.
- Laboratory classes in **Power Electronics (E6 201)** in 2018 in IISc. Bangalore.
- Teaching Assistant in **Advanced Power Systems Analysis (E4 234)** in 2019 in IISc, Bangalore.
- Tutored and Teaching Assistantship in **Switched Mode Power Conversion (E6 221)** 2020, 2022, 2023 in IISc, Bangalore.
- Teaching Assistant in **Topics in Power Electronics and Distributed Generation (E6 224)** in 2021 in IISc., Bangalore.
- Conducted tutorial classes in **Introduction to Electrical Engineering (ESO 203A)** in 2016 in IIT Kanpur.
- Teaching Assistant in **Special Topics in Power Electronics (EE698)** in 2015 in IIT Kanpur.
- Teaching Assistant in **Control Techniques in Power Electronics (EE662)** in 2015 in IIT Kanpur.

RESEARCH EXPERIENCE

POSTDOCTORAL RESEARCH

I. Wireless Battery Charger for High Gravimetric Power Density Receiver in Drones
The project aims at designing an ultra lightweight onboard receiver for the Drones to maximize flight time. High output power to reduce charging time and achieve maximum uptime is an essential requirement. The present design of 200 W prototype achieves a gravimetric power density of 7.1 W/gm. Apart from the design of the power stage of the receiver, the control of the receiver, independent of the transmitter, is a major control challenge. I am involved in development and implementation of the synchronization and control for the receiver to achieve ZVS turn on and required power-flow for CC and CV mode charging of battery.

II. EMI Filter Design for 200 kW Integrated Motor Drives for EV Applications
The project aims to develop a high power density GaN-based three-level inverter for motor drive that can be integrated into a 200 kW motor for EV applications. My work involves designing DC and AC side common mode filters to meet the CISPR25 standard and keep the bearing current within a limit. The work plans to evolve with integrated common and differential mode filters to limit the dv/dt at the motor.

III. Discrete-Time Modelling for Power Converters
Switching-cycle averaged modelling technique is adopted for DC-DC converter. Small-signal perturbations around the steady-state operating point is applied to obtain the linear plant model. In DC-AC, isolated DAB, resonant converters, where state variables are of AC nature and have large excursions in magnitude, an average model becomes inaccurate. The inaccuracies are more of a concern for high-frequency switched resonant converters targeting a high bandwidth. Discrete-time modelling is an approach that addresses this issue by considering sub-switching-cycle intervals and corresponding states in the circuit. This research revisits the discrete-time modelling approach and explores on the intuitive way of accurately predicting the major dynamics of the converter even without the rigorous modelling effort.

IV. Micro-Magnetics Modelling for Magnetic Loss Estimation in Power Converters
For high-frequency power converters, magnetic design poses challenges due to the complex nonlinear behaviour of magnetic materials. Accurate estimation of magnetic losses and understanding of the loss mechanisms are essential for high power-density converter designs in which magnetics are often the largest component. A physics-based equivalent circuit model is developed based on the Landau-Lifshitz-Gilbert (LLG) equation to accurately model different micromagnetic behaviours that decide the area of the BH-loop. The developed equivalent circuit model aims to act as a bridge between the dynamic magnetization phenomenon and nonlinear characteristics such as core loss and permeability.

DOCTORAL RESEARCH

I. Solid State Tuning Restorer (SSTR) for Second-Harmonic LC-tuned Filter
LC-tuned shunt filters are used for second-harmonic current filtering in PV inverters, locomotive traction converters, etc. Due to parameter drift or frequency variations, the filter can get detuned, resulting in poor current THD, imperfect tracking of maximum power point, and generation of beat frequencies in traction drives. In this work, a solid state tuning restorer is proposed to augment the LC filter to achieve flexibility of adjustable impedance characteristics. The proposed configuration facilitates a low-power converter, with only about 2% of the main converter rating to be utilized as SSTR.

II. Modelling and Stability Analysis of Series Stacked Buffer (SSB) for Second-Harmonic Power Decoupling
Series-capacitor stacked buffer (SSB) is a promising active power decoupling circuit for handling the second-harmonic ripple in single-phase systems. The absence of a model that considers the loading effect of the main converter DC bus elements on the buffer converter necessitates either hysteresis control or open-loop control as the only control mechanism. This work develops a reduced-order model of the buffer converter that aids in implementing a fixed frequency PWM

control technique and finds the stability limits of the dc-bus voltage with respect to the controller gain. The effect of active damping to achieve a wider bandwidth and better stability is explored.

III. Synthesis of Minimum Switch Low Power Buffer Converter with Series Capacitor (SC) Stack for Second-harmonic Power Decoupling
Series-capacitor Stacked Buffer (SSB), despite being a low-power converter-based active power decoupling (APD) solution, employs an H-bridge auxiliary converter. As the driving circuits and controller burden increase with the switch count, it is preferable to achieve the second-harmonic power decoupling utilizing the minimum number of active devices. In this work, a series-capacitor stacked active power decoupling circuit with minimum switch realization is proposed. Using three-terminal cells as a basic building block, different possible configurations are synthesized and compared in terms of device rating and control challenges. The reduced voltage stress is one of the major advantages of the devised configurations compared to the existing minimum switch-count-based APD circuits.

IV. DC Capacitor-less Unified Active Capacitor and Inductor (UACI)
Two-terminal active capacitors and inductors are effective in achieving configurable impedance characteristics. H-bridge converter, usually employed to emulate a two-terminal capacitance or inductance, requires a sizeable DC capacitor. The literature discusses reduced or no DC capacitance-based solid-state variable capacitors (SSVC), which can not emulate inductive characteristics. Hence, they are unsuitable for applications requiring impedance characteristics to migrate from capacitive to inductive or vice-versa. This work incorporates the inductive emulation feature in DC capacitor-less SSVC to obtain a two-terminal unified active capacitor inductor (UACI). The proposed topology allows a smooth transition from capacitive to inductive characteristics and vice-versa without any current overshoot.

V. Impact of Reduced Capacitance DC Bus on Control and Stability of Three-Phase STATCOM and Active Front-End Converter In a balanced three-phase system, the DC bus capacitance requirement is predominantly decided by the switching ripple limit, or hold-up time, demanded by the downstream converters or loads. In the STATCOM application, where the DC bus is neither connected to any DC source nor any DC load, the switching ripple constraint can be relaxed as long as the input current THD remains within permissible limits. Therefore, the capacitance across the DC bus can be minimal. In this work, an analytical limit of capacitance is found below which the decoupled control of the AC current loop and DC bus voltage loop is lost, reducing the voltage-loop bandwidth from the designed value. For an Active Front End converter (AFEC) feeding a constant power-type load, the reduced capacitance effect is more severe, leading to an unstable operation.

MASTER'S RESEARCH

I. Series Input PFC Rectifier with Dual Output Channels

This work develops an input series connected Boost PFC rectifier, consisting of two units. The DC outputs are regulated at equal voltage levels, irrespective of their load mismatch. The developed topology targets medium voltage applications where an 'N' number of such PFC units can be incorporated to provide 'N' outputs.

II. Non-isolated Dual Output PFC Rectifier with Simultaneous Boost and Buck Outputs

This work develops a dual-output AC-DC converter with unidirectional power flow capability. The front end consists of a diode-bridge rectifier, the input current of which is maintained at the unity power factor by controlling the subsequent switching network. The DC outputs are regulated such that one of the output voltages is higher and the other is lower with respect to the amplitude of AC input voltage. The developed topology targets to provide DC distribution of 380 V and 24 V from a single-phase 230 V AC supply.

LEADERSHIP/ MENTORSHIP

- Women in Engineering Committee Member and activity manager for IEEE COMPEL, 2025 conference, held in Knoxville, Tennessee, USA, from 22-26 June, 2025.
- Technical Programming Committee Chair for IEEE COMPEL, 2025 conference.
- Mentoring two PhD students at the University of Tennessee, Knoxville.

RESEARCH GUIDANCE

Mentored undergraduate student under NSF 'Research Experience for Undergraduates (REU)' program to execute the project "Developing a Coordinated Solution for Power Negotiations in a High Density Integrated USB-C Battery Charger" during May-July, 2024 at the University of Tennessee, Knoxville.

HARDWARE EXPERIENCE

- GaN-based converter prototype for Inductive Wireless Power Transfer for drone battery charging: assembly, testing and debugging.
- GaN half-bridge module for EV motor drive: packaging assembly and testing.
- Two-level H-bridge voltage source converter for active power decoupling: design, development, and testing.
- A synchronous buck converter-based point of load converter using EPC 2015 GaN: development and testing.
- Reconfigurable capacitive DC-link: design, development, and testing.
- Boost PFC: design, development, and testing
- Dual output boost PFC with simultaneous boost and buck output: design, development, and testing

RESEARCH PUBLICATIONS

J1. **A. Mukhopadhyay** and V. John, "Synthesis of Minimum Switch Count Second-Harmonic Hybrid Filters, " in IEEE Transactions on Industry Applications, vol. 61, no. 2, pp. 3279-3292, March-April 2025, doi: 10.1109/TIA.2025.3529809.

J2. **A. Mukhopadhyay** and V. John, "Solid-State Tuning Restorer for Second-Harmonic LC Filter in Single-Phase Converters, " in IEEE Transactions on Industry Applications, vol. 60, no. 1, pp. 658-671, Jan.-Feb. 2024, doi: 10.1109/TIA.2023.3320109

J3. **A. Mukhopadhyay**, M. Palmal and V. John, "DC Capacitor-Less Two-Terminal Unified Active Capacitor and Inductor," in IEEE Transactions on Industry Applications, vol. 59, no. 4, pp. 4441-4453, July-Aug. 2023, doi: 10.1109/TIA.2023.3267025.

J4. **A. Mukhopadhyay** and V. John, "Fixed-Frequency PWM Control and Stability of Series-Stacked Buffer for 2ω-Power Decoupling," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 11, no. 2, pp. 1555-1567, April 2023, doi: 10.1109/JESTPE.2022.3220494.

C1. **A. Mukhopadhyay** and D. Costinett, "Wireless Battery Charger with Reverse Power Flow Blocking and Cell Over-Voltage Protection", **Presented** 2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), 22-26 June, 2025. Knoxville, Tennessee, US.

C2. **A. Mukhopadhyay**, A. Basu, and D. Costinett, "Double-Frequency Sampling Impact on Dynamic Model of Half-Wave Symmetric Converters", **Presented** 2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), 22-26 June, 2025. Knoxville, Tennessee, US.

C3. A. Basu, **A. Mukhopadhyay** and D. Costinett, "Practical Design of Synchronization Control for a Wireless Battery Charger", **Presented** 2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), to be held in Knoxville, Tennessee, US, from 22-26 June, 2025.

C4. X. Liu, Y. Jhang, **A. Mukhopadhyay**, S. Fan, D. Costinett, H. Bai and L. Tolbert, "Crosstalk Mitigation and Switching Speed Enhancement of GaN HEMT with Adaptive Gate Resistance under Wide Temperature Variation", **Presented** 2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), to be held in Knoxville, Tennessee, US, from 22-26 June, 2025.

C5. X. Liu, Y. Zhang, N. Jia, **A. Mukhopadhyay**, D. Costinett, H. Bai and L. Tolbert, "Packaging a 650V/400A GaN Half-bridge Power Module with Ultra-Low Parasitics for Electric Vehicle Drive Applications", 2025 IEEE International Workshop on Integrated Power Packaging (IWIPP), Tuscaloosa, AL, USA, 2025, pp. 1-5, doi: 10.1109/IWIPP61784.2025.10971623.

C6. **A. Mukhopadhyay** and D. Costinett, "Unveiling Aliasing Effect on Resonant Pole Locations in Wireless Battery Chargers", 2025 IEEE Applied Power Electronics Conference and Exposition (APEC), Atlanta, GA, USA, 2025, pp. 3267-3274, doi: 10.1109/APEC48143.2025.10977200.

C7. **A. Mukhopadhyay**, K. Froehle, A. Basu, and D. Costinett, "CC-CV Control of Wireless Battery Charger Based on Discrete-Time Small-Signal Model, " 2024 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), Lahore, Pakistan, 2024, pp. 1-8, doi: 10.1109/COMPEL57542.2024.10613941.

C8. S.B. Sohid, **A. Mukhopadhyay**, C. Harmon, D. Costinett, G. Gu and L. Tolbert "A Generalized Physics-Based Circuit Model for Predicting Nonlinear Properties of Magnetic Materials", 2024 IEEE Energy Conversion Congress and Exposition (ECCE), Phoenix, AZ, USA, 2024, pp. 7159-7166, doi: 10.1109/ECCE55643.2024.10860826.

C9. **A. Mukhopadhyay** and V. John, "Low Voltage, Minimum Switch Count Second-Harmonic Filter for Single-Phase Converters," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), 2022, pp. 1-7, doi: 10.1109/ECCE50734.2022.9947864.

C10. **A. Mukhopadhyay** and V. John, "DC-Link Current Sensor-Less Average Current Mode Control for Series Stacked Buffer," 2022 IEEE Energy Conversion Congress and Exposition (ECCE), 2022, pp. 1-8, doi: 10.1109/ECCE50734.2022.9947883.

C11. **A. Mukhopadhyay**, M. Palmal and V. John, "A DC Capacitor-Less Two-Terminal Unified Active Capacitor and Inductor," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), 2022, pp. 436-442, doi: 10.1109/APEC43599.2022.9773513.

C12. **A. Mukhopadhyay** and V. John, "DC Bus Second Harmonic LC Filter with Solid-State Tuning Restorer," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), 2022, pp. 1-7, doi: 10.1109/APEC43599.2022.9773433.

C13. **A. Mukhopadhyay** and V. John, "Constraints Based Design of DC side LC Filter for Single-Phase Voltage Source Converter," 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), 2020, pp. 1-6, doi:10.1109/PEDES49360.2020.9379380.

C14. **A. Mukhopadhyay** and V. John, "Minimum DC Bus Capacitance Limit for STATCOM," 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), 2020, pp. 1-6, doi: 10.1109/PEDES49360.2020.9379515.

C15. **A. Mukhopadhyay** and S. Mishra, "Dual Output PFC Rectifier with Simultaneous Boost and Buck Output," IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, 2017, pp. 1113-1118, doi: 10.1109/IECON.2017.8216191.

C16. **A. Mukhopadhyay** and S. Mishra, "FPGA based novel voltage balancing technique for series input boost pre-regulator," IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, 2017, pp. 1160-1165, doi: 10.1109/IECON.2017.8216198.

PATENT

P1. **A. Mukhopadhyay** and V. John, "HARMONIC RIPPLE COMPENSATOR FOR POWER ELECTRONICS," Indian Patent Application number: IN202341070546.

SOCIETY MEMBERSHIP AND SERVICES

- Technical Track Chair for IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), 2025
- Women in Engineering Committee member and event organizer, IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), 2025
- Reviewer of IEEE Transactions on Power Electronics
- Reviewer of IEEE Journal of Selected and Special Topics in Power Electronics
- Reviewer of IEEE Access
- Reviewer of IET Electric Power Applications
- Reviewer of IEEE-sponsored international conferences: APEC, ECCE, PEDES, INTELEC
- Member of IEEE Industry Applications Society (IAS)
- Member of IEEE Power Electronics Society (PELS)
- Member of IEEE Women in Engineering (WIE)