Madhu N. Belur
Control and Computing group, EE, IITB
www.ee.iitb.ac.in/~belur/

Quick Review of PD/PI controller design

Lead (cascade) compensator ← PD

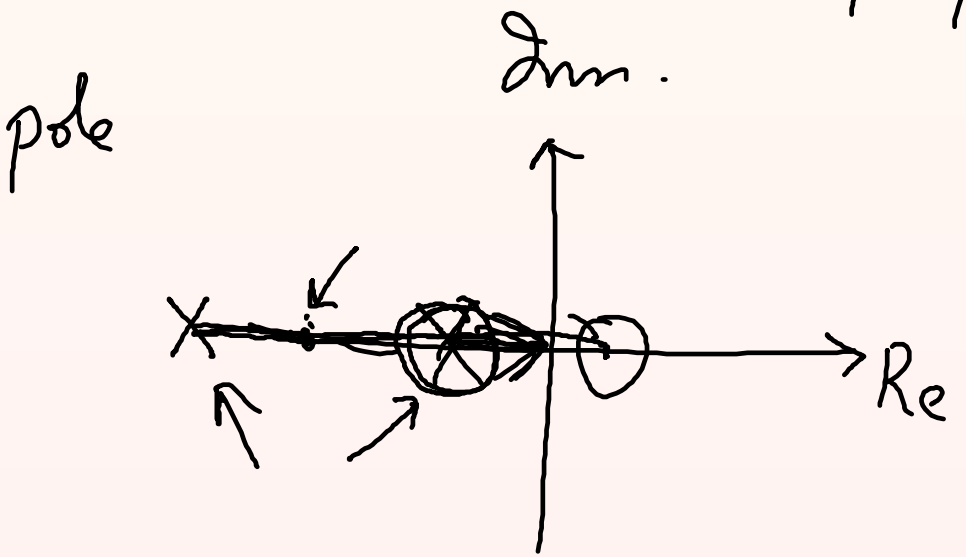
Lag (cascade) compensator ← PI

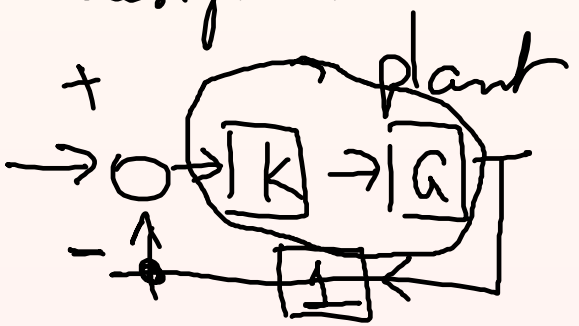
This lecture – lead-lag compensator

(using Root locus methods) – review of PD, PI controller.

– cascade/feedback compensator

– pole/zero cancellation ("by design")





Pole/Zero cancellations

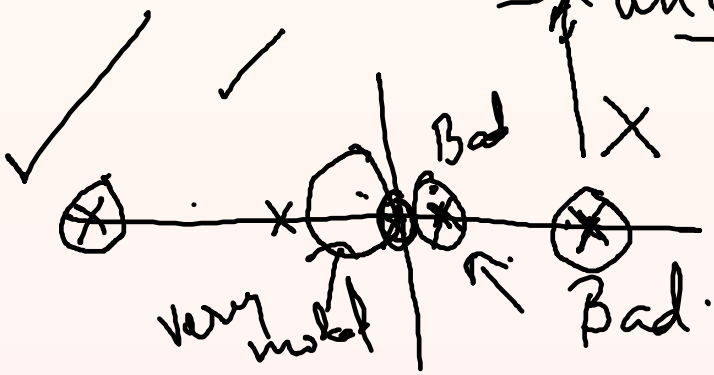
- does not show-up in input to output map

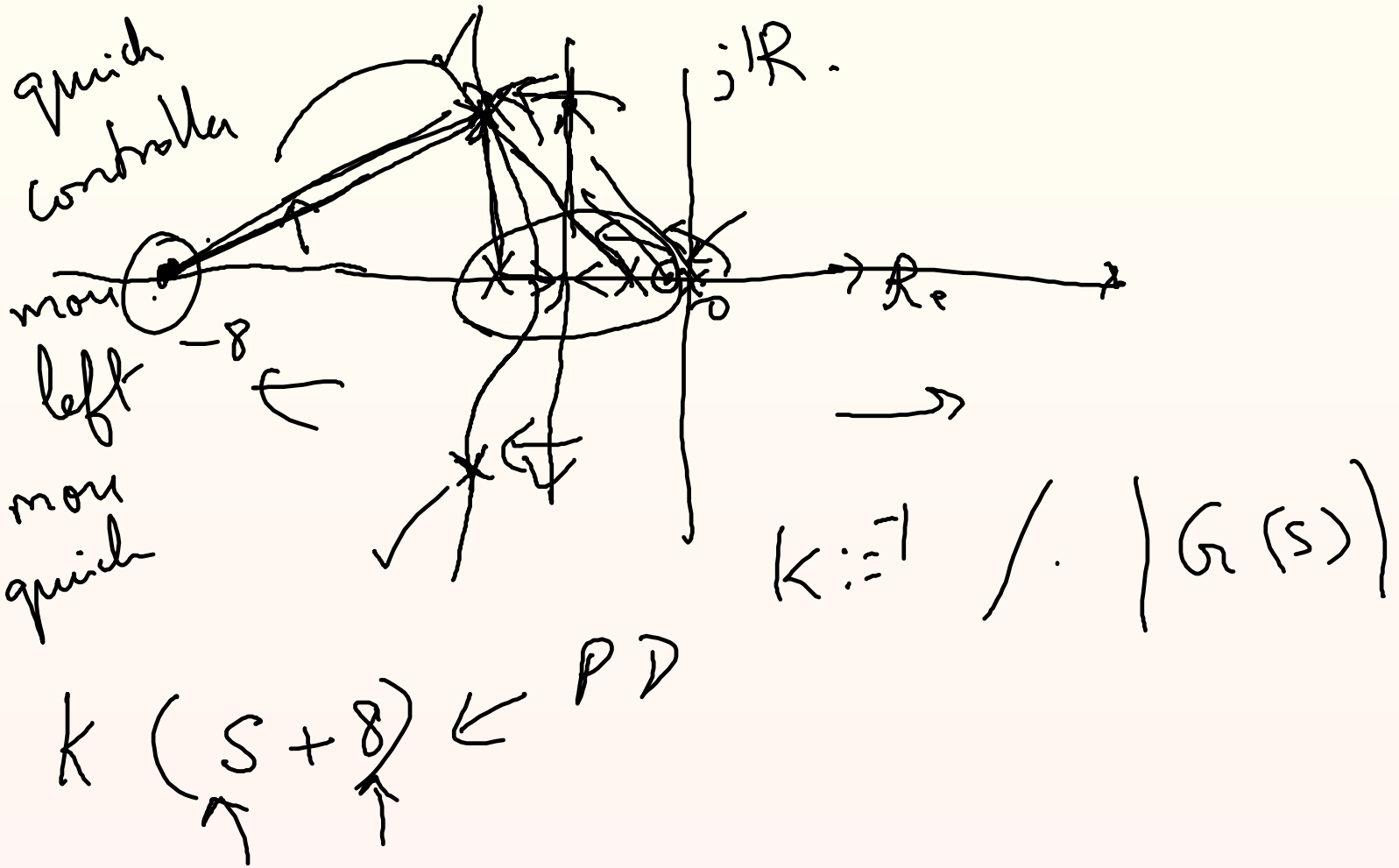
Defn. transfer fn: initial condition $\equiv 0$

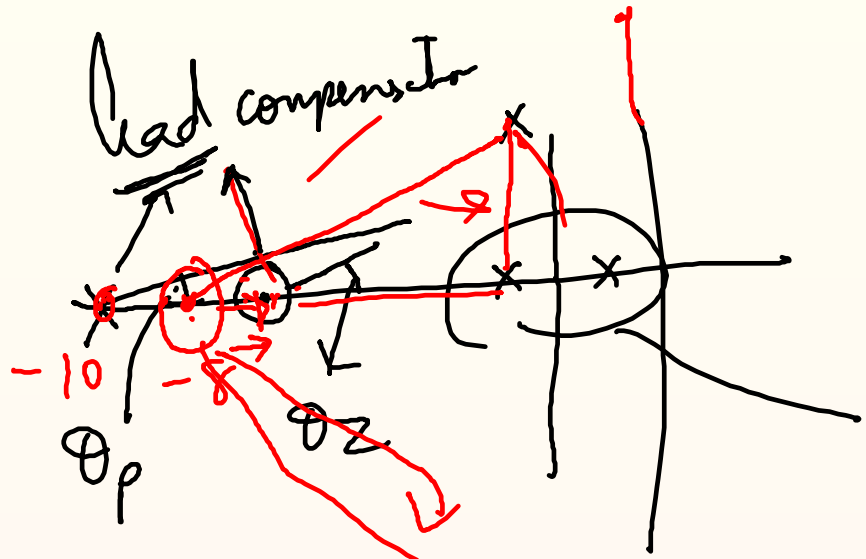
- does show due to nonzero initial conditions

↳ uncontrollable/unobservable "modes"

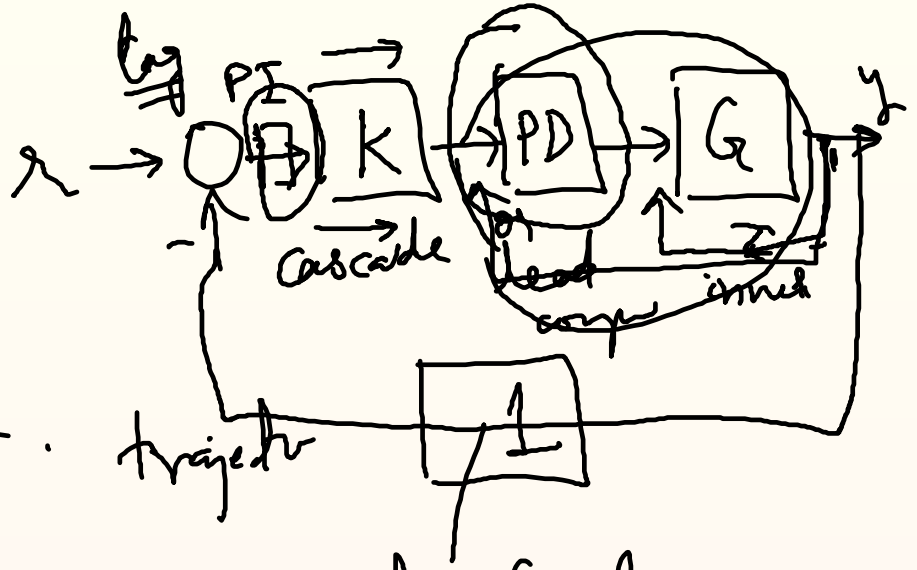
and/or




quick
controller
mov
left
mov
quick
$j\mathbb{R}$.
-8
0
$\mathbb{R}_e$
$k := \frac{1}{|G(s)|}$
$k(s+8)$ ← PD



plant · trajectr



feedback compensator

$\theta_z > \theta_p$

controller.

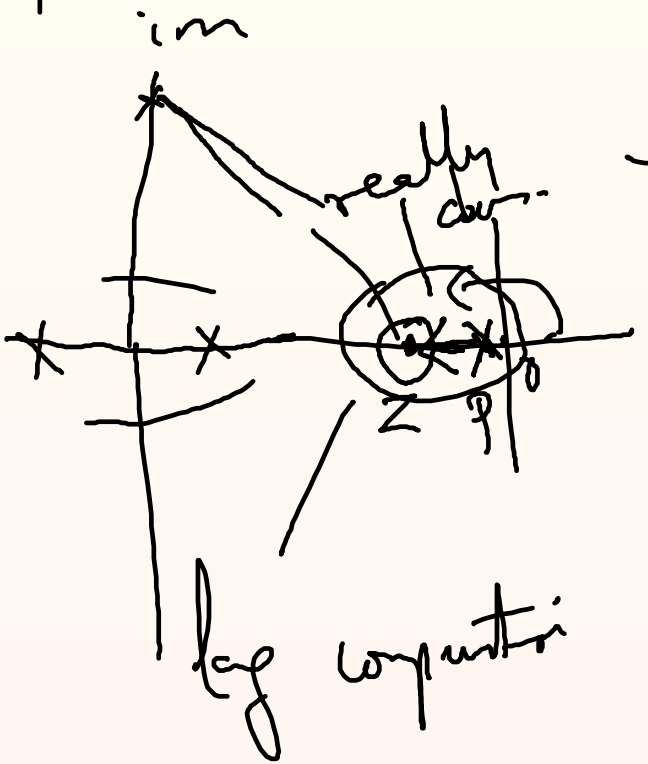
lone zero

PD

$\theta_z - \theta_p > 0$

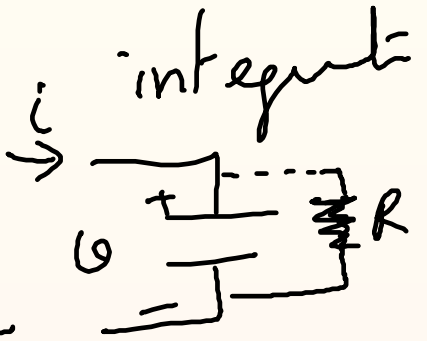
lag compensator

realistic practical



PI controller

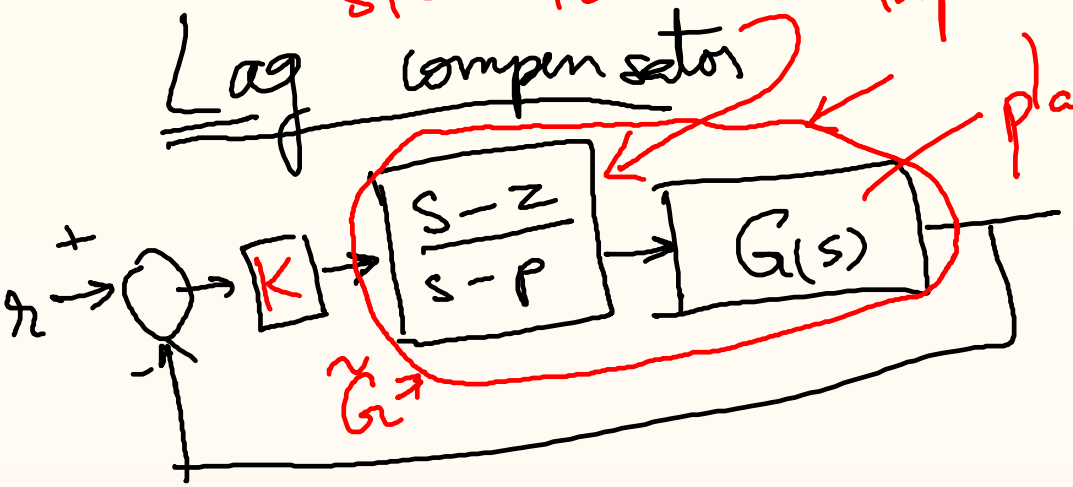
integrator

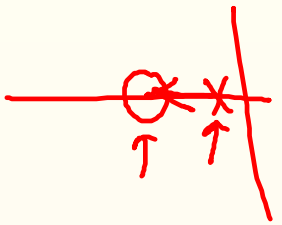


$v \propto \int i$

steady state error input.

Lag compensator





$z < 0$

$p < 0$

$-z$: zero

$-p$: pole

$$\frac{s+z}{s+p}$$

$G(s)$ – type 0.

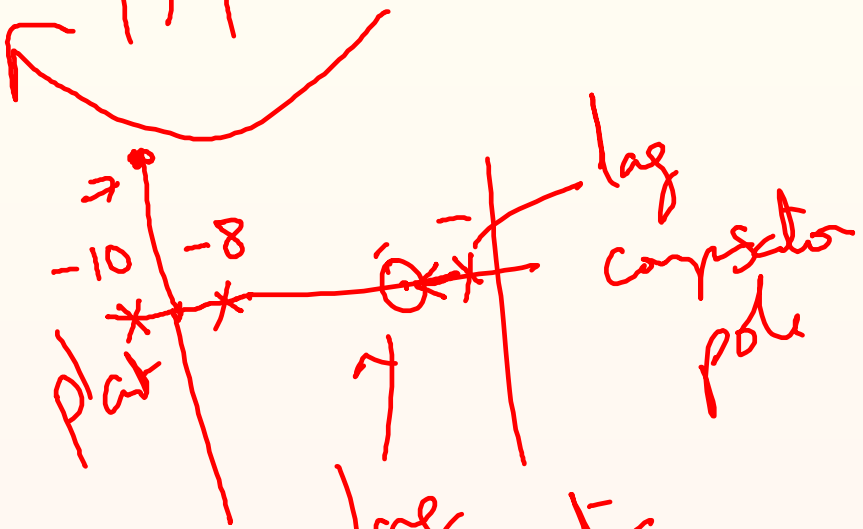
r – step input.

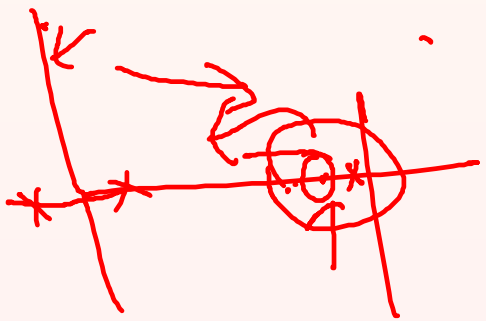
$$\text{s.s. error} = \frac{1}{1+kG(0)}$$

$G(0)$: DC gain.

closed loop is stable

$$\tilde{G}(0) = \frac{|z|}{|p|} \cdot G(0)$$

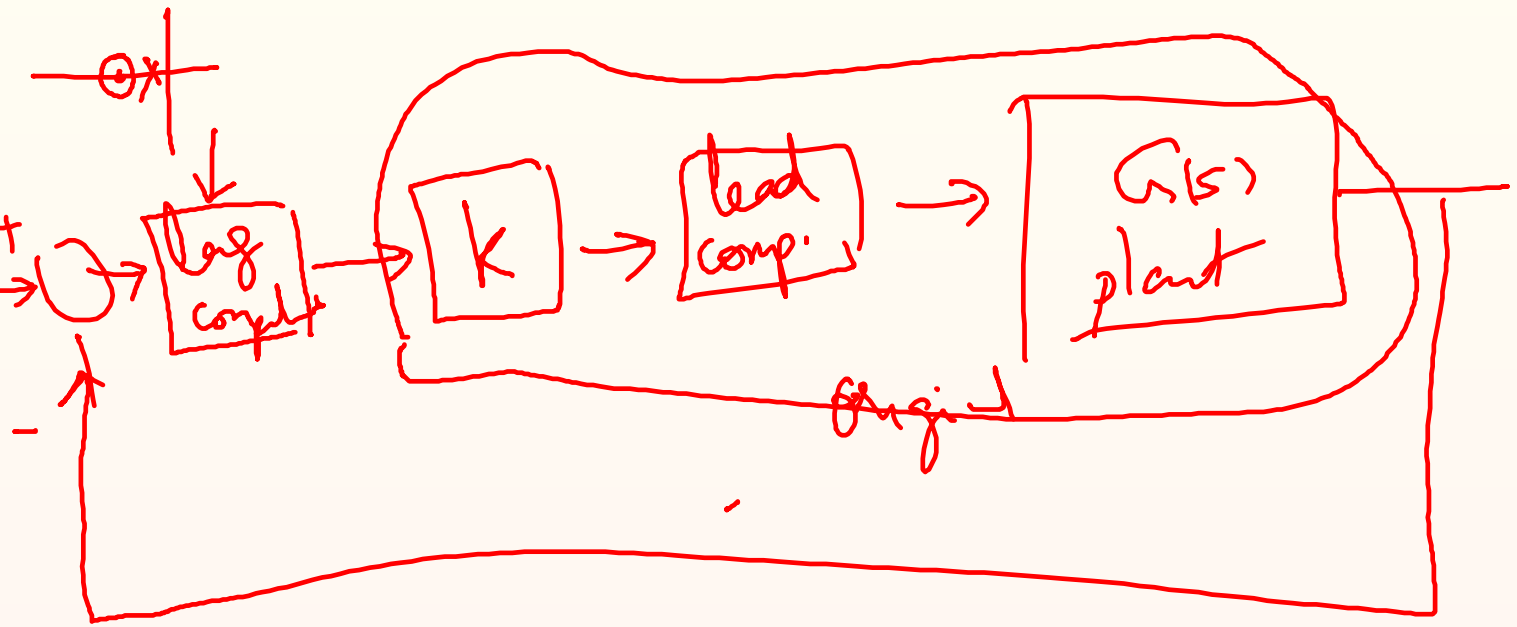




for small steady state error

then $\frac{|z|}{|p|} \to 1$

also need pole/zero close to the origin.



lag compensator's effect is for very frequencies (DC gain) term wise "much later" after transients have died.

- Pure simulation

- HIL simulation