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DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, BOMBAY

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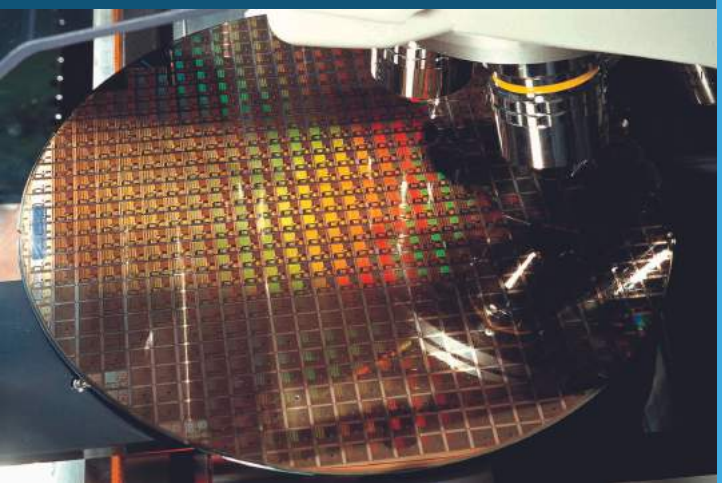

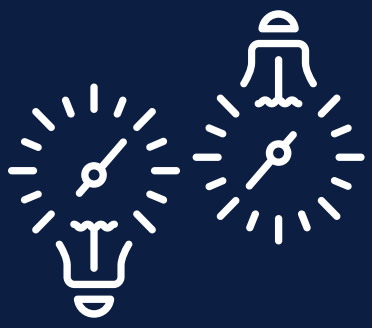

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Tête-à-Tête with
Prof. Kishore Chatterjee


SHEEL SHAH


AMOL SHAH


ADIL KHAN

Professor Kishore Chatterjee is currently serving as the Head of the Electrical Engineering Department and has been associated with our department for the past 23 years. In the past, he has served as the Organizing Vice Chairman, Joint Entrance Examination, the Associate Dean (IPS) and Chairman for GATE (2017), and is presently also the convener of the institute committee looking into undergraduate curriculum revision. We decided to have an informal conversation with him on his life experiences and also his work as the head of the department. Read on to know more…

Q. You are now the head of one of the largest departments in the top institute of the country. How has your life journey been - could you describe the major milestones in your journey till date?

I am originally from Kolkata, and after my higher secondary education, I went to REC Bhopal for my undergraduate studies. Those days, they were called RECs (Regional Engineering colleges), now they are named as NITs. In a given REC, there used to be seats distributed for all the states and Union territories of the country. I got exposed to real India this way once I moved to the REC. I am sure you also had the same experience once you joined IIT Bombay. I did my BTech from there and subsequently I went to one of the oldest colleges in India, the Bengal Engineering College, Howrah, later renamed as the Indian Institute of Engineering, Science and Technology (IIEST), which is again an institute of national importance similar to the IITs and NITs. There I did my ME in Power Electronics and Machines and immediately after that I joined IIT Kanpur for my PhD. There I spent around 5-6 years and soon afterwards I got an offer from IITB and joined as a faculty member here in December 1998.

Q. Having been a professor in our department, is there any difference in your life after becoming its head?

Not really, as far as our department, and the culture of IITB is concerned, there is hardly any difference. Between a professor, an associate and an assistant professor, there is absolutely no hierarchy. The standing of an assistant professor, a full professor or an HOD are all at the same platform. The process of the selection of the HOD is such that the faculty members give their preferences for who they want to be the head for this cycle. The Director of the Institute gets an impression of the faculty members who are being preferred, and based on that the head is selected by him. So what I want to stress over here is that the process is very democratic, and the brief answer to your question is that there is hardly any difference between being a faculty and the HOD, as far as my interaction with other faculty members is concerned.

Q. So, how has your typical working day changed after becoming the department head?

Yes, that has changed certainly because I have to do several routine things from the morning to the evening which the department requires. So my professional life has changed somewhat and I have two duties to perform - first as the chair of the department, and second as the regular faculty member of the Institute. The function as an HOD includes the routine things pertaining to issues concerning students and faculty, academic and non-academic matters etc. The other function of the HOD, not just for me, but for anyone who is heading any academic unit, is to give a vision to the progress of the department, such as how the faculty members would like to see the department to grow, and in which direction in 5 to 10 years down the line. Hence I am giving utmost importance in understanding the aspirations of the faculty colleagues and the students of our department, and more importantly how to realize them.

Q. Can you describe your vision for the department and its future to us?

If you see the evolution of the department from the past to the present, when I joined in 1998 we used to have not more than 15 to 20 PhD students, and the MTech students also used to be around hundred, and the number of undergraduate students used to be around 200-300. Now, our total student strength is around 1100 and out of this 400 are undergraduate students while the rest 700 are postgraduate students. As you can see from the '90s to 2021, the complexion of the department has changed primarily from an undergraduate teaching institute, to an undergraduate teaching as well as a research institute. Not only that, 20 years back, the number of faculty members used to be around 30, now it is 70. And the increase in the number of faculty members has happened in the last 10 years or so. And we took that bold step, because we firmly believed that if we kept on recruiting young minds the department would grow in the right direction. I can now definitely say that we took the right decision. As far as research is concerned we have been doing extremely well. Now our mandate is that not only we should involve ourselves in blue sky research but also we need to engage in research which has an immediate impact on society. By society, I mean the society at large and also the industry, so that the industry can take our innovation and make a product out of it. IIT Bombay is trying to enable such an ecosystem, if you know there is a centre called SINE. SINE is that entity where IITB faculty as well as students can establish their own startup. It will help you out as far as infrastructure is concerned for 2-3 years and then you can take off on your feet. SINE is not a part of the EE department but it shows that the focus of the institute has changed over the years towards doing meaningful research.

Q. What do you think are the most important issues you face while working as the HOD, especially about the department or its students?

As far as the last two years are concerned, quite a few students had problems, especially because of online learning, being at home, and moreover the absence of peer learning. However, if you remove the issues due to Covid, I don't think there is any major problem as far as the student body is concerned. However, as far as the aspirations of the department are concerned, a major issue is about

the infrastructural requirements. If we want to grow, we need to invest in infrastructure development. If we hire a new faculty, we have to give him/ her space to carry on with their work - research activities. As far as Mumbai and IIT Bombay is concerned, space is an issue, but still we are working hard to get more facilities developed. Having said that, we can see the phenomenal growth we have achieved in the past 8 to 9 years, in the number of faculty members, number of labs and other facilities which we have built. Yes, there may have been some delays here and there, but ultimately we have realized what we wanted. In the coming future, if we want to grow more, we need to develop the right infrastructure, and so this is the main issue of concern, which we are working hard to resolve. One source we are vigorously exploring for support on this is our alumni, and the initial response from the alumni community has been very encouraging.

Q. How has the pandemic affected the teaching activities of the department in the last couple of years?

The thing is that when you are delivering a lecture in an online mode, you never know how receptive the students are to your teaching, or how much content of your delivery they are able to absorb. In a live lecture, you can look at the faces of students, understand and immediately change track if needed - it is not possible in an online setting. It is easy to say that it is always possible for students to respond online, but in front of 150 students in the meeting, everyone cannot speak out together as it will inevitably lead to chaos, and hence the result is that everyone keeps quiet. This means that the faculty cannot understand if the material being taught is being assimilated by the students or not, and hence there is a disconnect that happens. In any case, we have now learnt how to go about teaching in an online mode, we know how to conduct courses online, but still it slows down the pace. Technology definitely helps, but ultimately one-on-one human interaction cannot be replaced.

Q. Going forward along the lines of the previous question, how have the research activities of our doctoral students been impacted due to the pandemic?

In the first lockdown, we got really affected, especially those students whose research is experimental in nature and dependent on building hardware prototypes or requiring usage of instruments. They really suffered and lost at least six to seven months of their time. Even others also suffered a lot. In an online mode, you cannot have that kind of an interaction with your guide, which you can have in an in-person setting. But not only the interaction with your guide, for a PhD scholar, peer learning is very important. During my PhD days, in my day to day work, I learned a lot from my peers and seniors. The nitty gritty of problems being faced during experimentations, small issues that you face in your work - these are the things that you need to learn from your peers, and this got lost completely during the lockdown. Now that almost all our PhD students are back, this problem no longer exists, but yes, they lost quite a bit of their valuable time.

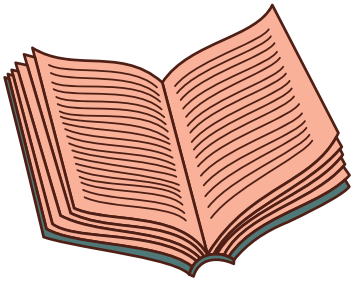
Q. How much has your research been affected due to the increased workload after becoming the department head?

Earlier I mentioned that I am still a regular faculty member of our department, I am still teaching and I also have to guide PhD students. I would put it this way, that my students have been affected due to my work as the HOD, research is still going on as my students are doing the research. But I feel sorry for them, as earlier I could attend to them whenever they wanted, but now I cannot spend that much amount of time with them. For example, if they give me a paper to read, earlier my turnaround time used to be a week or so, now it has increased substantially. But they have been accommodative and cooperative, I have tried to have discussions with them and continue my work with them after regular office hours.

Q. We noticed that you had completed your PhD under Professor BGF, how does it feel now that you are his successor as the department head?

Interestingly, Prof. BGF was a PhD student at IIT Bombay, and later joined IIT Kanpur as a faculty member while I was a research scholar over there. Although he was my PhD supervisor as well as teacher, our relationship was more of a friend. The first time when I met him, I still remember – a misty cold morning in Kanpur, he said to me, "Don't address me with a 'Sir". Once I joined IIT Bombay, BGF had also joined back here by then, and our relationship has remained to be that of a friend. It's an honor to take over charge from BGF who led the department from the front for two terms as the HOD.

Q. Lastly, would you like to give any message to the students?



A friendly suggestion is that, of late, students are getting more and more worried about their future, material things like - what will I do after graduation?, what will be my salary? - and similar things right from their first or second year. I think this is not the right attitude. During your stay over here you should enjoy your academic life – every bit of it, and not waste your precious time in thinking about material gains. The curriculum and pedagogy that you are getting here is remarkable, and you will not be able to realise the importance and worth of what you are getting unless you step into your professional career. You should involve yourself and engage yourself in various extracurricular activities like debates, drama, sports, seeing good movies, reading good books. Reading a book in isolation and reading a book in a campus environment is completely different. After reading a book, you can go and tell your friends about it and discuss your views on the book with them. So take maximum advantage of the environment that IIT Bombay provides. You are not only living on a good campus but also living in the company of good peers as well as experienced faculty members. You tend to approach faculty members only for academic problems or for functional problems. The faculty members of the department are eager to engage with you in all possible ways – be it personal, cultural or in whatever ways social beings interact with each other. Earlier we used to have a film club, and the students and faculty members used to watch films together, but now we are living in silos, we have our own mechanisms of seeing movies. Let us try to break this barrier and let us live as a closely knit community – and take the maximum benefit of living together in a campus.

Global Chip Shortage

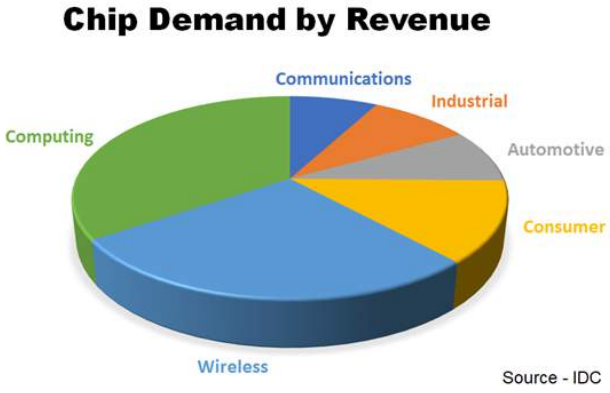

MIHIR KAVISHWAR


ADIL KHAN


AMOL SHAH

November 2020 was supposed to be an exciting month for gamers. Sony's PlayStation 5 and Microsoft's Xbox Series X and Series S consoles were released just a few days apart. However, both PS5 and Xbox went out of stock almost immediately after their respective launches, disappointing thousands of users who were eagerly waiting to buy these products. Strangely enough, it's December 2021, and a large number of users are still waiting. With online retail stores greeting customers with "product unavailable" and "out of stock" messages, desperate gamers are turning to websites like eBay, where scalpers are selling at more than triple the retail price. One must ask that despite being amongst the biggest technology companies globally, why haven't Sony or Microsoft boosted their production even a year after the launch? It turns out gaming consoles are just the tip of the iceberg. Almost every industry that uses electronic components, be it something as simple as an amplifier, is bearing the brunt of a significant ongoing global chip shortage.

The most brutally hit are the auto manufacturers. Earlier this year, car companies found themselves in a predicament. While an average car comprises about thirty thousand individual components, they were missing one or two, worth perhaps only a couple of dollars. It didn't matter. For just a few missing parts, the entire production had to stop. In the United States, companies like Ford, Honda, Volkswagen, Audi and General Motors shut down many of their factories and sent workers home. We saw a similar trend in India with Maruti Suzuki, Tata Motors, Toyota and Mahindra & Mahindra announcing closures of some of their manufacturing plants. Although it is hard to estimate the exact economic implications, AlixPartners, a global consulting firm, has projected mammoth losses of up to $110 billion for the entire automotive sector, with nearly 3.9 million vehicles of production being lost to the chip shortage this year alone. Despite several new launches keeping consumer interest high, auto sales seemed to decline by about 3% in November 2021, largely attributed to the paucity of critical electronic parts that continues to impact production.



The consumer electronics sector has also been suffering massively in the last few months. During the pandemic, the demand for mobile phones, laptops and PCs shot up. Although the shortage did not severely impact the high end processors, supply of lower value silicon such as chips that are used to derive displays and audio functions has been impacted. Apple executives have already warned that the shortage could impact production of the latest iPhones and Mac devices. Apart from big companies, small scale start-ups and research centers are also severely affected since the manufacturers typically prioritise bulk orders from big clients over smaller orders. The shortage was felt even in our department – it posed some challenges when we needed to get boards made at WEL last semester for our online lab courses.

How does the global supply chain work?

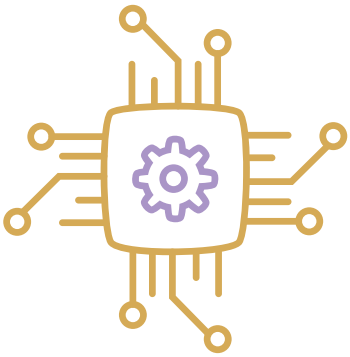
The supply chain for semiconductors is highly globalized with even individual companies having manufacturing and design facilities in multiple countries around the world. At a high level, it comprises three broad steps, namely Integrated Circuit Design, Wafer Fabrication and Assembly & Testing. The industry today operates majorly in a foundry model, with fabless semiconductor companies involved in the design of ICs, and these in turn outsource the manufacturing to pure play foundries, which only manufacture devices for other companies. A few companies operate in both areas and are known as integrated device manufacturers. Adding to these, there is a large supporting ecosystem of specialised equipment manufacturers, raw material suppliers and EDA and core IP vendors. Back-end processing is typically carried out by OSAT (Outsourced Semiconductor Assembly and Testing) firms where the multiple chips on a single silicon wafer produced by fabs are converted and packaged into individual chips that can be readily assembled into actual electronic devices.

What led to the shortage?

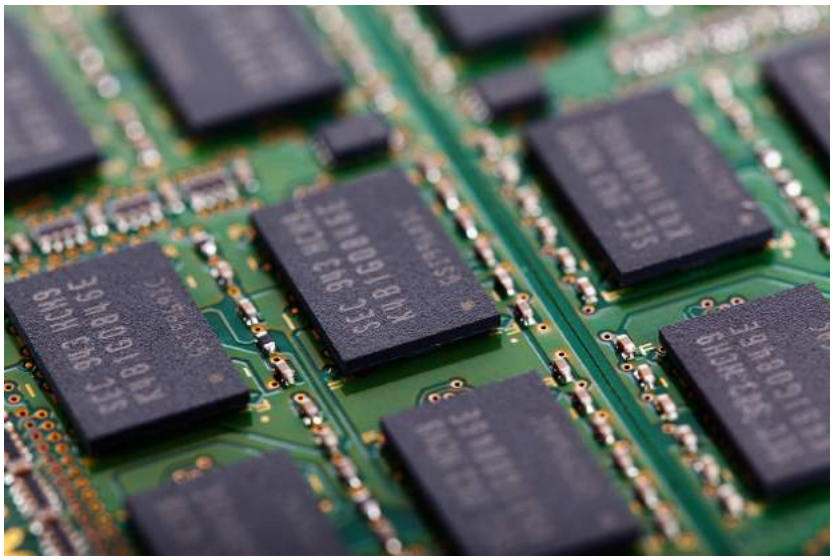
A wide array of reasons have been given for one of the most widespread chip shortages in history, ranging from the classical economic problem of supply and demand mismatch to a recent drought in Taiwan. The cause which is most often cited is the industry wide miscalculation of semiconductor demand, especially going into the COVID-19 pandemic. But the roots for the crisis had taken place well before the pandemic and the imposition of widespread lockdowns. In 2018, a full-blown trade war started between the United States and China, leading to cascading effects in the semiconductor production line starting from the shortage of raw materials. A year later, the United States began a series of gradual restrictions on Chinese tech giant Huawei cutting it off from the global semiconductor ecosystem. This resulted in Huawei racing against deadlines and stockpiling semiconductors before each new ban came into effect. Meanwhile, another trade war erupted, albeit on a smaller scale, between Japan and Korea. Japan, one of the largest producers of fluorinated polyimide, resist and hydrogen fluoride, all three crucial chemicals for semiconductor production, announced in July 2019, that it would restrict sales of these materials to South Korea.

Enter the COVID pandemic, and the chip manufacturing companies were suddenly faced with lockdowns and disruptions in production and also the possibility of subdued demand due to

lower consumer spending. However, this turned out not to be the case as within a few months, orders from consumer electronics companies and cloud service providers skyrocketed. As work home became the norm, the demand for devices like laptops, smartphones and routers surged. On the other hand, companies in the automotive and industrial sectors, faced with a rather gloomy outlook, began cutting back on chip orders. However, this was short lived as demand for cars recovered faster than expected in many parts of the world, ostensibly due to people avoiding public transportation. Already overloaded with orders from consumer electronics firms, the automotive industry orders were pushed to the back of the queue and this resulted in increased lead times for supply. As the effects of the shortage were felt more and more, companies started stockpiling orders in anticipation, sending ripples up the supply chain and causing more and more shortages due to the bullwhip effect.



Isolated events like fire at a PCB substrate manufacturer in Japan and the closure of several fabs including those of Samsung, NXP and Infineon in Texas due to a winter storm further exacerbated the shortages. In 2021, Taiwan faced one of its most severe droughts in more than half a century. Semiconductor production requires high amounts of ultra pure water, and Taiwan even decided to prioritize water for chip manufacturing over rice farming in its national and global interest. However, all of these events threw the supply-demand equilibrium into complete disarray, with the demand far outpacing the supply.



Companies and governments around the world announced huge investments in fabrication plants to get over the chip shortage, however these measures can only have an effect in the long term as setting up a new fab takes around three years. Moreover, the shortage is spread across the spectrum, including in 40 nm and larger nodes whose chips are widely used in the automotive industry. There is insufficient incentive for setting up new fabs at these older nodes, even at the peak of the chip shortage, due to huge capital costs and insufficient profitability on legacy node technologies in the long run. In the current scenario, the chip shortage is estimated to last well into 2022 and possibly beyond that, however with newer fab capacity coming into operation by then, there is hope of some light at the end of the tunnel.

Solutions and India's role for the future

The shortage was an eye-opener for many countries around the world to work towards curbing the growing gap between supply and demand for semiconductor chips, and also to reduce the global reliance on a multitude of countries to create even a basic single chip. Many countries and multinational blocs like the European Union have started working on plans to set up indigenous fabs to reduce reliance on foreign countries. Long-term solutions include increasing the production facilities; however, setting up new fabs typically takes many years.

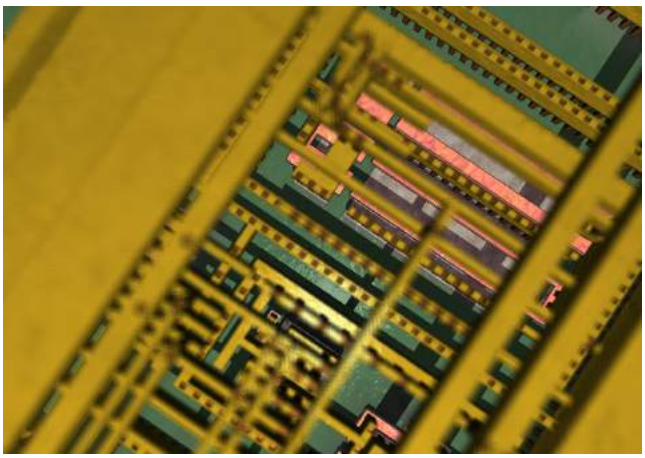
The Government of India floated an expression of interest (EoI) in December 2020 to set up a commercial semiconductor fab in India, with the government being open to negotiating new incentives for fabs apart from the already fixed ones. It was reported by the Business Line that over 20 semiconductor manufacturing and designing companies submitted their expression of interest proposals. Tata Sons recently stated that they are looking at the possibility of entering into semiconductor manufacturing in India. It was reported in various media outlets that they are currently in talks with three state governments and scouting for land to set up an outsourced semiconductor assembly and test (OSAT) plant by late 2022.

On 15th December 2021, almost a year after floating the EoI, the Union Cabinet approved a ₹76,000 crore (> $10 billion) program for the development of semiconductor and display manufacturing ecosystem in India. It promises to usher in a new era in electronics manufacturing by providing a globally competitive incentive package to companies in semiconductors and display manufacturing as well as design.

As per the statement released by the Ministry of Electronics and Information Technology (MeitY), the program aims to provide attractive incentive support to companies / consortia that are engaged in silicon semiconductor fabs, display fabs, compound semiconductors / silicon photonics / sensor (including MEMS) fabs, semiconductor packaging (ATMP / OSAT) and semiconductor design. The government promised to extend fiscal support of up to 50% of the project cost to eligible applicants for setting up commercial semiconductor and display fabs in India. It also announced that MeitY would take requisite steps for the modernization and commercialization of the Semi-conductor Laboratory (SCL). In order to drive the long-term strategies for developing a sustainable semiconductor and display ecosystem, a specialized and independent nodal agency, "India Semiconductor Mission (ISM)" will be set up. With several incentive-based schemes as a part of the program, the Government of India committed support of ~₹2,30,000 crore ($30 billion) in total to position India as a global hub for electronics manufacturing with semiconductors as the foundational building block.

We talked to Prof. Udayan Ganguly, who is part of a team from IIT Bombay commissioned by the government to prepare a detailed project report on the setting up of an RnD semiconductor foundry in India. He emphasized on the need of a semiconductor ecosystem as a precursor for commercial fabs. As per him, the talent and human resources in India are the key reasons why any company would want to invest and build fabs in India. There is a thriving and well established fabless design ecosystem in our country, however the same is not true for chip manufacturing.

He specified that setting up a fab ecosystem is not a short term project, but is akin to a 30 year long space program. As companies usually work on a shorter time horizon, government incentives are necessary in order to incubate such an ecosystem. However, once a fab ecosystem is developed, it can be extremely beneficial for the country; in terms of being talent intensive, providing high quality employment, being highly profitable and also being at the cutting edge of technology. Prof. Udayan listed the lack of a market for semiconductor chips in India as being one of the key challenges. As of now, the Indian industry has been mostly limited to purchasing pre-finished goods like printed circuit boards which come later in the value chain instead of individual semiconductor chips. He suggested that one of the ways to get around this is inviting foreign semiconductor manufacturers who already have a well established market to come and set up fabs in India. We need to prepare the field for semiconductor fabrication companies to come here and provide them an edge over other competing countries. He said that the sweet spot right now for India might be in more mature technology nodes like 28 nm and above instead of leading edge nodes like 14 nm and below, as the 28 nm node requires a comparatively lower capital investment while still covering about 60% of the market.



All in all, with the ubiquitousness of semiconductors and the growing demand for electronic devices in India and globally, it becomes all the more important to have a thriving semiconductor manufacturing ecosystem in India that can compete with the world. We hope that the recent initiatives of the government in this regard bear fruit and emerge successful.

References - Strengthening the Global Semiconductor Supply Chain in an Uncertain Era, Report by BCG and SIA, April 2021
Image Credits: TSMC, David Carron

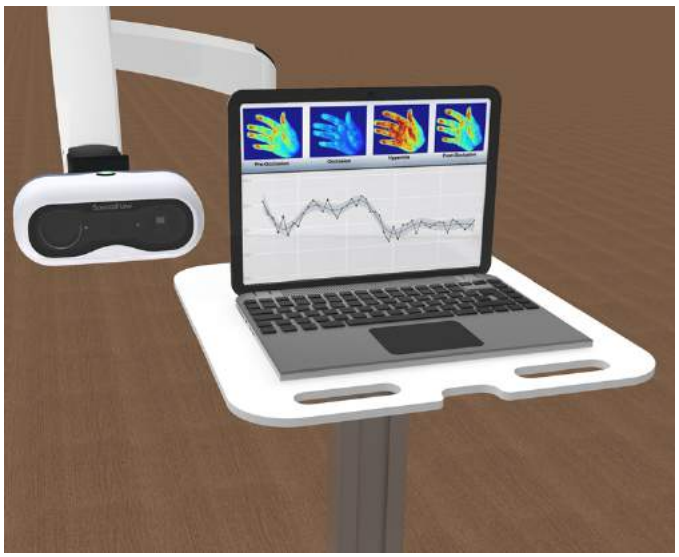
Interview with Mr. Amaldev

In the second part of our coverage on the global chip shortage, we talk with Mr. Amaldev on various aspects of his work and how it has been affected by the ongoing chip shortage. Mr. Amaldev Venugopal is a senior engineering project manager at the Tata Center for Technology and Design, IIT Bombay. He currently leads a health-tech research group that aims to develop affordable point-of-use diagnostic solutions for deployment in primary and secondary-care contexts. He is also a technology consultant at several startups and large companies: he offers them guidance in product development and technology interventions for their product roadmaps.

Tata Centre for Technology and Design
IIT Bombay

Additionally, he is the co-founder of an early-stage deep-tech medical imaging startup called Epocare. In 2015, he co-founded APCAD Instruments, a successful music-tech hardware startup based in Berlin and Mumbai. Mr. Venugopal received an MTech degree in Electrical Engineering from IIT Bombay in 2015.

Q. Can you tell us about the different kinds of projects that you work on at the Tata Center?



I lead a health-tech group that primarily focuses on making affordable point-of-care devices. For example, we have developed a handheld imaging device that enables a rural health worker to screen women for cervical cancer. It has an AI-based learning approach that can help diagnose based on the severity of legions found. It enables a remote consultation sort of arrangement. Another major project we work on is a Digital Pathology device. Typically, if you have some growth in some part of your body, you get a biopsy surgery done. That tissue gets sliced into very thin sections, and that gets placed on a glass slide. A pathologist looks at this slide under the microscope and creates a report. The problem in rural areas is that there are no pathologists, so the slides have to be sent to a tier 1 city where good pathologists are present. They create a report and send it back. This process has a 2 to 3 weeks turnaround time. We are trying to cut down on that with a digital pathology scanner. Once you put in a glass slide in the scanner, it's like an automated microscope - it goes at multiple spots, scans the entire slide, digitizes it, and uploads it.

To give you a scale of complexity, a 15mm x 15mm slide corresponds to around 3000 images at a very high resolution. We have our own algorithms for stitching and our own cloud platform also for the reporting process. Currently, the cost of a commercial digital pathology scanner is around one crore or so. We want to do it under five lakhs sort of price point.

There are multiple other projects which Tata center handles across several verticals such as energy, housing, pollution, waste management, etc.

Q. When did the global chip shortage start affecting you, and what challenges are you currently facing?

I regularly have to place orders for various electronic components. Around late December last year, I started to see that lead times were getting longer. By January, everyone had begun hoarding the few available components in anticipation of a shortage, further worsening the situation. You can't buy anything these days. Usually, you base your design on a circuit and have some idea of the integrated circuits (ICs) you would like to use. In the current scenario, all of that goes for a toss. Let's say I'm using some IC, and I'm writing my entire firmware stack. Now you find that you have enough for prototyping, but you can't buy if you want more. There isn't much we can do because the lead times for many of these components are currently more than a year, optimistically speaking.

There is a particular microcontroller that we wanted to use. Around 1500 were available with the vendor. However, from the moment I thought of putting it into the cart and checking out, the entire 1500 was bought by someone. When I contacted the vendor, he said that some other clients already booked the order. The lead time for that microcontroller is Dec 2022, so I can't use that controller in my board and have to redesign and redo my firmware. If I am trying to prototype something with my clients, I first try to figure out which ICs are available and do a rough sketch. Then I purchase a sufficient number of the available ICs so that we at least have enough for prototyping. This is not an ideal way to design, but that's a hit you have to take; there is no alternative till this entire thing eases off.

Q. Are there any specific components or chips of some particular technology node that are short in supply?

The most cutting edge, sub-10nm devices are not affected much because dedicated fabs are running full time to cater to that market. Mobile phones and laptops are prime hot king selling devices. The older nodes and stable designs are most affected.

All the fast-moving ICs and components which were popular in the market are getting exhausted quickly. At the moment, we have to rely on less popular parts to use in our designs. It is not necessarily the case that these parts are less reliable or inferior in quality, but to switch from a familiar component to an unknown one takes a lot of effort. Say we are used to working with a particular IC, and our development and firmware teams know the entire toolchain. Now we need to write in a different firmware and alternative development toolchain altogether, and this causes several issues.

Q. Are there alternative ways of procuring components? How are companies dealing with the shortage?

There is nothing much that we can do other than wait for the crisis to mitigate. Earlier, you could find some components in the grey market and use that for prototyping (but not for the final product). Usually, big companies buy ICs in a reel format because they can be easily fed into a pick-place machine to assemble a PCB. If some company is making a product X, and say they buy a reel of 2500, but their requirement is only 2000. Then the rest is useless and is sold by the manufacturer in the grey market. If you know the right vendors, you can get your hands on these. But the quality of these components is not guaranteed.

You can reach out to the manufacturer and ask them for the lead time. But if your order quantities are significantly less, they wouldn't care about you because they have bigger clients to cater to their first batch of ICs. Then the only solution is to redo your design.

Auto manufacturers are being forced to scale down or shut down production because they can't get a particular IC. They need to use that specific IC because that's a stable design. They have spent months developing the PCB, writing the firmware, and everything. Once a product is made, it goes through an immense amount of certification cycles. In the automotive industry, crores of rupees are spent on EMC compliance, product testing, etc. If there is some part in the critical chain that you need to replace, you need to go through the same certification route to ensure the product is compliant. You can't say that I just replaced X product with Y. In hardware, the primary issue is that your entire hardware production cycle is dependent on the slowest component in the chain. Even if one capacitor is missing in the product chain, you can't ship that product.

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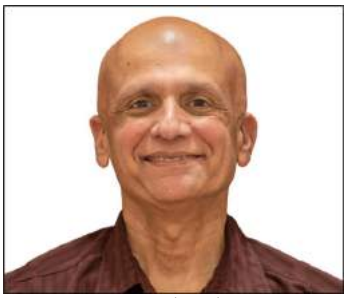
JANEEL PATEL


SHEEL SHAH

A lot is known and talked about how to make the most of the IIT Bombay journey, getting good internships and placements, building a network and gaining soft skills. The Electrical Engineering Department's cell for Alumni and Corporate Relations, recently conducted fireside chats with two of our distinguished alumni, Mr. Sunil Shenoy and Mr. Sharad Sanghi in September and November 2021 respectively. We decided to talk with them to understand the challenges that life after IITB holds. They also throw light upon how they navigated the challenges themselves and give tips on how we can be better prepared for the future.

Mr. Shenoy graduated from IIT Bombay with a BTech in electrical engineering in 1980. Currently, he is the Senior Vice President and General Manager of Intel's Design Engineering Group. He has been at the forefront of microprocessor design in the industry, helping Intel build many generations of laptops and server chips.


Mr. Sunil Shenoy


Mr. Sharad Sanghi

Mr. Sanghi graduated from the electrical engineering department, IIT Bombay in 1989. He founded Netmagic in July 1998, which is now a subsidiary of NTT Communications. He is a pioneer in the Indian cloud computing space and has been featured on the "Top 25 Indian Tech business persons who have completed 25 years of service" list by Economic Times.

Q. What was the biggest shock that you experienced after graduating from IIT Bombay? How can one be better prepared to tackle unexpected situations better?

Sunil Shenoy:

Well, we went abroad for our graduate studies, and so the shock, if you will, was associated with moving to a different country, culture and environment. As I recall it, some of the significant elements of the difference were the informality between students and faculty and between employees, supervisors, and the management. We grew up in a society where at least then there was a large "power difference". In particular, compared to IIT there was less rigorousness and less emphasis on regular quizzes and exams. The assignments and projects were more open-ended.
I am sure that a lot of this has changed over the years at IIT Bombay and India.

Sharad Sanghi:
I have been very fortunate to have gone with the flow, and things just worked out. I got admission to Columbia University and met my wife in the first month there.Therefore, I did not experience any shock. I also received a research assistantship for the NSFNet project, which helped in funding my education. Later, I was recruited from college at AT&T Bell Labs and became financially independent. I have been fortunate to not experience any rejection. However, there are many students who often do not know what they want. Many also experience job rejection after college, leading to post-graduation anxiety/ depression. The best way to tackle such situations is to have a goal, believe in yourself and work hard. It is also essential to have a great set of friends and support from the family so that you don't waver while striving to achieve your goals. Approach things one step at a time.

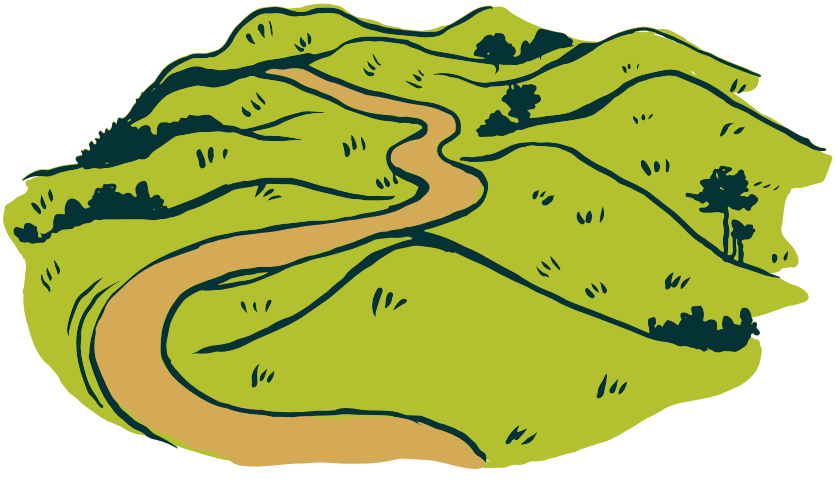
Q. How did you familiarise yourself with taxation, personal finance etc, important things in daily life but aren't taught in the IIT B classroom?

Sunil Shenoy:
Not for a very long time until you do have the income or wealth to worry about all this! Today, of course, with the Internet, this question is moot because Google can help you find anything you need to know! But in those days, the sources were trusted friends and relatives who maybe did not turn out to be so knowledgeable and trustworthy after all. There were also a lot of scams where agents were offering advice with their own interests in mind.

Sharad Sanghi:
In New York, I used the H&R Block. Now, in India, I have outsourced these aspects to experts. I have always ensured that I do not go against the law when I do this on my own. In fact, I still rely on my 85-year-old father to manage my investments and taxes.

Q. How did your experiences and non-academic learnings from IIT Bombay help you in your career and life?

Sunil Shenoy:
As I had mentioned before, I was initiated into hiking and trekking at IIT. This has remained a lifelong passion, and I am grateful for this. The other thing was the friendships cultivated at a crucial period in our lives, and many of these have persisted.



Sharad Sanghi:
When I received admission to IIT Bombay, it was the first time I stayed away from home. This made me independent and also helped me when I went abroad. I participated in a lot of sports and other team activities, which inculcated the 'team spirit' in me. I was also involved in fundraising for Mood Indigo which gave me a lot of confidence to take initiative and organise events.

Q. Could you please illustrate how the IIT Bombay network and peer group help you throughout your career?

Sunil Shenoy:
Very much so. As I said, these friendships developed at a critical phase, beyond childhood friendships. Students got to know each other well and choose who they wanted to be with, their strengths and weaknesses. Hostel, sports, faculty experiences create solid and memorable bonds. I have tried to leverage these for fundraising for IIT several times over the years. In professional life, it is quite common to run into IIT alumni who introduce themselves and identify mutually beneficial enterprises.

Just last month, I came to know that a key technologist in one of my company's partner companies was a junior who lived in our hostel wing at IIT Bombay and who we would ceaselessly tease and "rag".

Sharad Sanghi:
The fact that I graduated from IIT Bombay is enough to validate my credentials even today. My peer group, including Ashish Chauhan (BSE) and Haresh Chawla (TV18), has helped in enhancing my career.

Q. Would you like to give any suggestions to juniors and current students of the institute to be better prepared for life after college?

Sunil Shenoy:
It would be very presumptive for me to do this to students over a couple of generations later.
I think the key advice would be to learn about your strengths, figure out what motivates you and follow that passion and path. I wish you the best!

Sharad Sanghi:
Set a goal, follow your dream, and never give up. Do not be afraid to fail and learn from your mistakes so that you do not make the same mistake twice. Remember that there are no shortcuts to success, and it takes hard work and determination. Always try to look at the positive side of things rather than finding weaknesses and faults.

Internship Diaries


JANEEL PATEL


SAMYAK SHAH

Millen Kanabar is a fourth-year dual degree student specialising in Communications and Signal Processing. He is also a member of the Student Satellite Team, currently working as an electrical and controls engineer. Being academia and research oriented, he spent his third-year summer break working on a research project at the National University of Singapore (NUS), and in this article he walks us through his internship experience.

MY RESEARCH JOURNEY

I had really liked the proof-based methods taught in MA 105, so I knew I wanted to do something that used similar mathematics, but I also didn't want to do maths for the sake of doing it. I didn't really have any idea about what exactly I would like to do until I took the Data Analysis and Interpretation course (EE 223) in the third semester. I liked what I studied in that course, so I got in touch with Prof. Jayakrishnan Nair in the winter of 2019 and did a project that relied on methods in applied probability to deal with a real-world problem. The major part of my work in this project was done within a little more than a year. I had also read up about information theory and the questions it sought to answer, and I found them very interesting. I had a lot of time on my hands in the summer break of 2020, so I did a course on Coursera (taken by Prof. Raymond Yeung, one of the top experts in this field) covering the basics of information theory. I quickly fell in love with the subject, so I followed it up with a course in the department to fortify my basic concepts.

HOW I GOT MY INTERNSHIP OFFER

I was very certain about the kind of internships I wanted to take in the summer of my third year, so I decided to be very selective about the IAFs I signed in the internship season and only spend time on apping/ preparing for internships that had profiles I was interested in: Information Theory and Random Processes. I ended up not signing a single IAF because none of the ones I saw matched with what I wanted to do in the summer. I made a database of professors I wanted to intern with, read a little bit from a few of their papers and made sure I would like the work. I prioritised getting a guide for the DAAD-WISE scholarship, so most of the initial emails I sent were to professors in German universities. Out of all those, I got one positive reply, but the professor was not willing to do a remote internship if restrictions didn't allow me to physically

come to Germany. I asked him if he was okay with filling the scholarship proposal while I continued looking for other opportunities that offered more flexibility in that regard. He happily agreed, so I continued emailing professors (and sending a reminder to ones who hadn't responded). Thankfully, before the submission deadline for the DAAD scholarship, I got another email from Prof. Scarlett from NUS telling me he was willing to offer me an intern. We had a short meeting at the end of which he confirmed the offer. The selection process involved an "interview" (if we can call it that) which was mostly about my future plans, what sort of problems I'd like to work on and ended with him asking me to go through one of his recent papers.

MY WORK

I worked on mismatched encoding in rate-distortion theory. Rate-distortion theory is the study of encoding a sequence of random variables using a pre-defined codebook while incurring the minimum possible distortion. I worked on the limits of encoding when the distortion measured by the encoder can be different from the actual distortion (which might lead to a suboptimal codeword being selected) using already existing codebook construction techniques from a different setting.

MY WFH EXPERIENCE

As far as the WFH experience goes, it was quite relaxed. I used to work according to my own schedule, and communication used to happen over email. We had meetings over Zoom once every two weeks. I used to send over handwritten notes via email whenever I wanted an opinion on some of my work, and when I was confident about a result, I added it to my progress report that I had shared via Dropbox. What made me enthusiastic about the internship was the fact that I really wanted to work on a problem in applied probability, so I went for interns aligned with the same. It turned out quite well!

SKILLS I ACQUIRED

One of the most important skills I learned was working collaboratively on a theoretical problem. The apping process taught me how to write good emails. I also learned a few new techniques from information theory (and in general from applied probability) that will help me in future research.

ADVICE TO JUNIORS

Set your goals, and work towards them. Be confident in your abilities. The responses I got made me realise that as an undergraduate, not much is expected in terms of previous knowledge. You should be enthusiastic about what you want to do, most professors really appreciate that. It is also important to be honest about your expectations and abilities, an exaggeration either way will almost always be counterproductive. WFH is a very subpar experience as compared to being there in person, but it is, in my opinion, still better than being stuck doing something you have no interest in, so make sure you have your preferences straight before you make any decisions. Everything said and done, internships are just a small part of your development as a student, engineer and/ or researcher, so don't lose sleep over the process, spend time on yourself and good things will happen to you. Cheers!

Widening Absorber Bandwidth

KARAN RANE

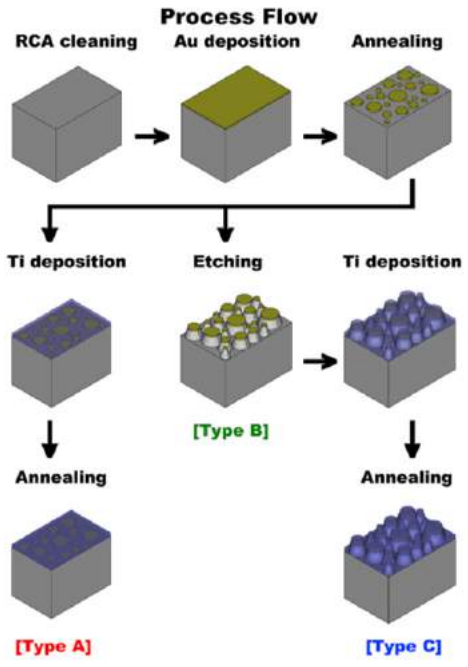
Discussing research work done on Silicon-based absorber bandwidth broadening with bulk processes by Ankitha Bangera, Prof. Kumar Appaiah

MATERIAL-LIGHT INTERACTION

Natural light spectrum can be described as a composition of individual components graphed against a continuum of wavelengths. A spectrometer is used by scientists and engineers to describe the nature of molecules in matter, using the spectrum of light emitted by them. A photodetector is a part of the spectrometer, which converts optical energy into electrical energy. Light falling on a photodetector is either reflected or transmitted or absorbed. The intensity of the reflected, transmitted and absorbed light depends upon the wavelength of the incident light and the material, silicon surfaces in this article. Characterization is the process employed to measure this dependence on wavelength. Typical silicon based photodetectors have a limited wavelength range (bandwidth). Hence, a complex system consisting of multiple detectors is constructed to sense (or detect) a broad range of frequencies.

IDEA FOR WIDER BANDWIDTH

Ms Ankitha E. Bangera, a researcher at IITB has implemented a process flow for modification of the silicon surface to expand the bandwidth of silicon based photodetectors. These devices absorb photons belonging to a wide spectrum; finding applications in spectrometers, optical noise absorbers and photovoltaic cells. The processes used in the study allow industry-standard bulk manufacturing. “I was a system owner (incharge of a lab facility) of a spectrometer that used multiple sensors to capture a wider spectrum of light. The requirement of multiple sensors increased the system complexity. This is where the idea to build a wideband device occurred to me.”, said Ankitha.



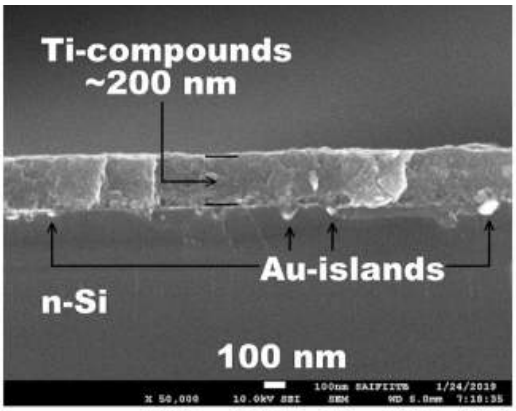
Process flow for three biocompatible configurations is illustrated in the diagram. Type A depicts nanocoating of Ti-compounds formed on Au-islands/n-Si, type B shows Au-island assisted textured n-Si, type C corresponds to nanocoating of Ti-compounds formed on Au-islands/ textured n-Si.

The silicon surface was textured in type B and type C samples because texturing reduces surface reflections.

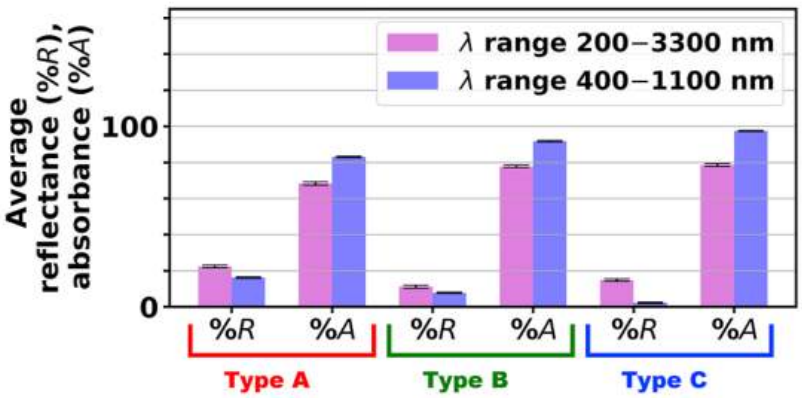
The titanium deposition (Ti of thickness ~200 nm), on annealing, forms Ti-Si schottky barrier at the interface and Ti-O and Ti-O-Si hydrophobic surface on the outer surface. The schottky barrier improves radiation absorption in the IR region. Hydrophobic surfaces prevent gumming by biological materials. An antireflective coating (such as oxides of Ti formed on the surface) or a textured (textured-Si) surface reduces the noise which fortifies the configurations against multiple types of degradation.

POTENTIAL APPLICATIONS

The three biocompatible configurations reduce surface reflections and improve the absorbance for silicon surfaces over an ultra-wideband region of wavelength ranging from UV to IR. These configurations can find applications in broadband absorbers, anti-reflective surfaces and optical detectors or sensors for spectroscopy. The fabrication steps are non-lithographic, which can lead to cost effective bulk manufacturing in industries. The surface hydrophobicity of type A and type C configurations allow integration with biological devices.



Cross sectional SEM image confirms thickness of Ti-compounds and presence of Au-islands. The XPS wide scan confirms the surface chemical composition, which comprises Ti–O on the surface of the samples



Bar graph depicting the average reflectance and average absorbance for the type A, B and C. Type A involves blanket deposition and annealing processes whereas type B and type C involve an additional process for surface texturing. Type C provides least average reflectance ~2% and highest average absorbance ~97%, for wavelengths ranging from 400 nm to 1100 nm.

CHALLENGES ENCOUNTERED AND OVERCOME

Timing is a key requirement of the modification process. When exposed to air, silicon surfaces form native oxide. Hence, the deposition steps need to be done quickly, say, within a day or two. Storing the samples in a vacuum desiccator before the deposition avoids silicon surface oxidation. After the final samples are prepared, the modified surfaces, that consist of nanocoatings of Ti-compounds, act as a passivation, even though the samples are not stored in a vacuum desiccator. A similar challenge related to timing lies in the process of etching, which requires careful monitoring. All facilities required for fabrication were available on campus. However, the pace of study is limited by the availability of target elements.

CONCLUSION

The proposed configurations reduce surface reflections and enhance absorbance for silicon surfaces over an ultra-wideband region. The processes used in fabrication allow cost-effective bulk manufacturing in industries. All the materials used are biocompatible, eco-friendly and non-toxic. Schottky and quantum effects due to Au islands are demonstrated. Surface hydrophobicity in Ti coated surfaces can benefit in integration with biological devices for human implants.

Research Paper: Bangera, A. E., & Appaiah, K. (2021). Quantum-confined ultra-wideband Si-based absorbers by a non-lithographic approach. Solar Energy Materials and Solar Cells, 230, 111161.

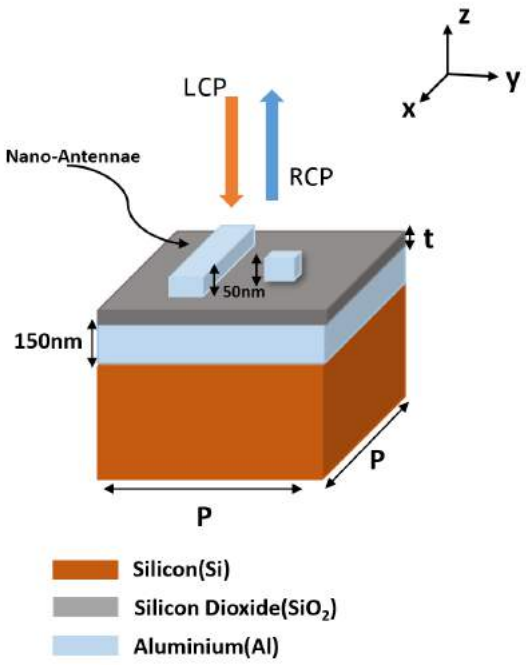
AI enabled designing of next generation photonic devices

SHRUSHTI TAPAR

I am a researcher working in the domain of nano-electronics within the electrical engineering department at IIT Bombay. The research in this domain mainly contributes to designing, scaling, and thereby enhancing the performance and competence of an electronic chip. In today's digital era, devices, gadgets, and the internet are the most integral part of our daily routines. World-leading semiconductor companies like TSMC, Intel, Samsung, and GlobalFoundries invest billions of dollars every year on research to keep pace with advancing chip designs for ever-growing data operation speeds. The current chip technology is reaching its limit of possible advancement. I am always curious to know what would be the next paradigm in technology, and this motivated me to look at photonics, which is regarded as an upcoming technology in integrated circuits.

CHALLENGES IN DEVELOPING A NEW TECHNOLOGICAL PARADIGM: ELECTRONICS VERSUS PHOTONICS

Present computing technology relies on electrons as the fundamental particle carrying information in integrated circuits. Electrons are charged particles, hence their control and manipulation is achieved by the application of different electric and magnetic fields. However, improvement in speed and size of electron-based devices is reaching its limit. Knowing that 'Light has an ultimate speed', researchers are trying to achieve data transmission at the speed of light at the level of integrated circuits. So, the idea of using a quanta of light (called photon) for information transfer at the chip-level is referred to as Photonics. The field of photonics is in its infancy. Photons are chargeless entities, thus their confinement, control, and manipulation at spatial and phase level on-chip is challenging.



A schematic illustration of unit cell of gap-plasmon based half-wave plate

BACKGROUND AND INTRODUCTION

The starting point for photonic chips is to bring light on-chip and attain its maneuvering at the nanoscale. Among the possible ways of confining light on the nanoscale, using surface plasmons is an effective technique. Surface plasmons are quanta of oscillations confined at surfaces and have the unique capacity to confine light to very small dimensions. At the nanoscale, the lens, mirrors for manipulating light are replaced by a metasurface. The metasurface is a cleverly engineered dense array of ultra-thin planar nanostructures. Thus, surface plasmons confine light to the chip, and a metasurface attains desired optical response.

Before going for actual device fabrication, optimizing the metasurface design parameters for the desired response using simulations is a common practice. In simulations, the way of optimizing nanostructure geometry and parameters is by calculating optical response for each possible combination of design and size and finalizing the nanostructure that is having the closest possible optical response to desired ones. Solving Maxwell's equations for light-matter interaction for incident light and metasurface using FEM (finite element method) in simulation tools is very expensive in terms of computational resources and time.

In a recent study by a team led by **Prof. Amit Sethi** from the electrical engineering department and **Prof. Anshuman Kumar** from the physics department, researchers have tried to acquire the maximum efficiency of polarization of light by designing a surface plasmon-based metasurface. Polarization efficiency is defined as the percentage of incident light that changes its polarization state (i.e. from right circularly polarized RCP to left circularly polarized LCP and vice versa) on interacting with metasurface at the reflected side. As said before, numerical simulations are an expensive and cumbersome method of obtaining optimized parameters, which the authors tried to overcome by using an AI-based framework.

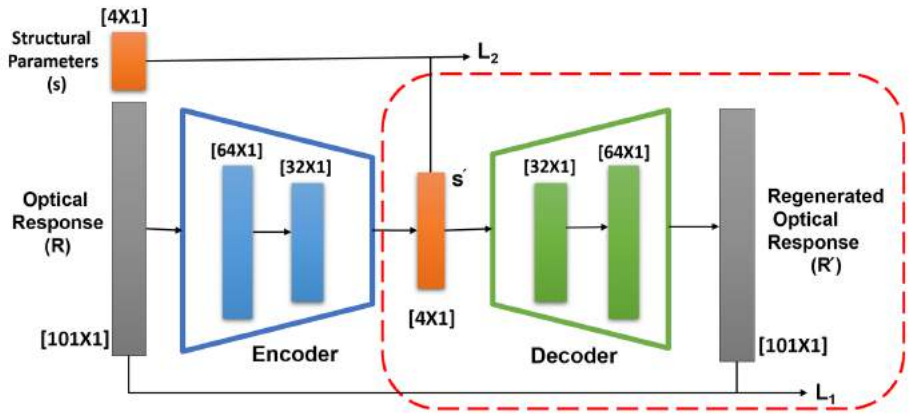
IN TO DEPTHS

The framework uses Deep Learning (DL) algorithms, which are the subsets of supervised learning. In DL, Neural networks (NN) are trained using data sets (inputs and corresponding outputs) to obtain the output response for new input data without actually solving equations numerically.

The AI algorithm framework discussed can be broken down into three stages:

Bidirectional Autoencoder (BiAE)

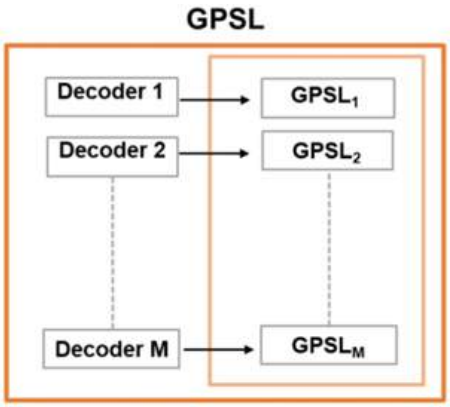
Bidirectional Autoencoder combines the two training stages of NN, the first is encoding, and the second is the decoding stage. The encoding stage is trained for inverse mapping, i.e. generating structural parameters for desired optical response and the decoding stage is trained for forward mapping i.e. for generating optical response for given structural geometry and parameters. The biAE is simultaneously trained for forward and reverse mapping, which improves the performance concerning individually trained networks.



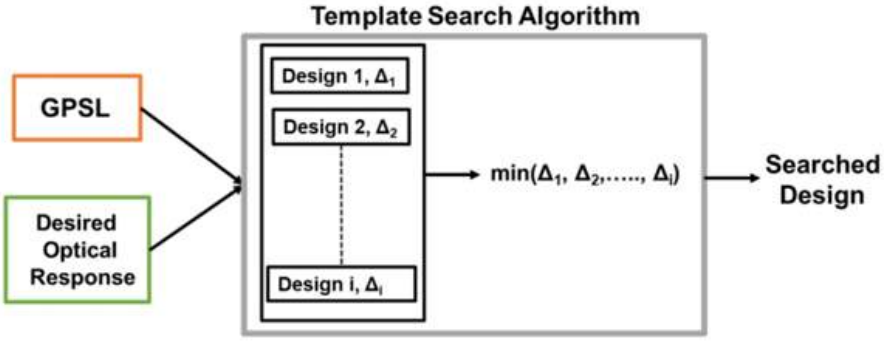
(a)

In the training process, the encoder accepts the optical response and produces structural parameters as latent vectors. The decoder then regenerates the optical response from structural parameters.

The validation of trained NN is the next stage, where BiAE is validated by comparing the output responses from trained NN with calculated simulation results for randomly picked geometric parameters for each design class, which were not shown during training. The output and calculated response are compared and it was observed that the average mean absolute error is ≤ 5% for 97-100% of the dataset samples.



(b)



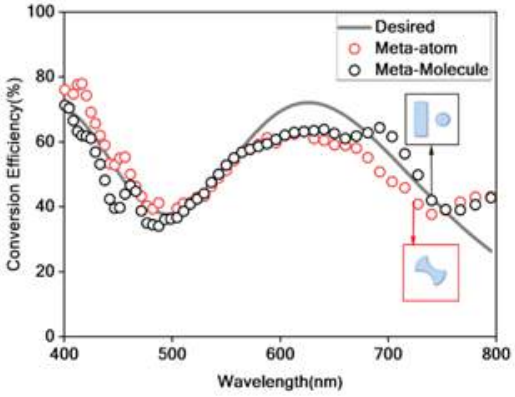
(c)

Global library (GPSL)

The Global library is formed by combining many sub-libraries. Each sub-library (GPSL1, GPSL2, GPSLM) corresponds to a particular design class, containing optical responses generated by the decoder for each possible combination of parameters for the provided optical spectrum (Figure b).

Template search algorithm

Finally, a template search algorithm is used to obtain the optimized design parameters for the closest optical response to the desired response for maximum polarization. Usually, the deep NN faces an issue while working with inverse design mapping, that is having multiple outputs (designs and parameters) for the desired optical response. The proposed template search algorithm addresses this issue and provides the solution in form of local and global optimized design parameters while working at sub-libraries and GPSL levels respectively (Figure c). The template search algorithm provides non-unique output, multiple designs, and parameter configuration for a desired optical response, that too in duration of milliseconds (Figure d).



(d)

The implemented AI-based algorithm demonstrates that the developed DL architecture accurately and rapidly identifies the optimized structural design and parameters in the space of different metasurface topologies and it can be used for applications needing one to many mapping for inverse design problems.

Research Paper: Abhishek Mall, Abhijeet Patil, Dipesh Tamboli, Amit Sethi, and Anshuman Kumar. "Fast design of plasmonic metasurfaces enabled by deep learning." Journal of Physics D: Applied Physics 53, no. 49 (2020): 49LT01.

Demystifying the PhD Program


MIHIR KAVISHWAR


PUDI SESHASAINADH


SHEEL SHAH

The Doctor of Philosophy (PhD) program offered by the Department of Electrical Engineering is widely known for nurturing talented research scholars who play leadership roles in research and development, either in industry or academia. Of the 1100+ students in our department, we have over 400 PhD students who devote around five years of their lives to the department's research activities. The research contributions made by our PhD students have been crucial for advancing the state of knowledge in various specializations of Electrical Engineering. However, despite having such significant representation among students and an impressive research reputation, the daily struggles of the PhD community largely remain a mystery to the undergraduates who seldom get to interact with them. Therefore, through this article, we seek to demystify the PhD program of our department, and subsequently, we also highlight some key challenges our research scholars face. We hope that such discussions lead to more positive interactions among all students and a greater appreciation for our research scholars who push the boundaries of human knowledge.

What do we mean by a PhD, and when has a student earned a Doctoral qualification?

It is not an easy question to answer and requires intense deliberation. In 2014, a document titled "Goals and Roadmap of PhD Program - A Desiderata" was prepared within the department after thoughtful discussions among multiple professors and incorporation of feedback from research scholars. We encourage our readers to go through the entire document to gain interesting insights into the motivations behind the current structure of our doctoral program.

To quote from this document, "the degree of Doctor of Philosophy recognizes a clearly discernible advancement in the state of knowledge in a particular branch of learning, clearly attributable in the large, to the recipient of this degree and acknowledged by representatives of the peer community in that field. At the end of the PhD program, a student should be an independent researcher. He/she should be able to stand alone and work in some area of choice. He/she should be a creative thinker and should be able to analyze and assess research work. The PhD program should have instilled enough confidence in the student so that he/she has the courage to venture out to some new frontiers of knowledge."

Admission Categories

PhD students in the department are majorly admitted under the teaching assistant or research assistant categories. A limited number of teaching assistant (TA) positions are available which are funded by the Ministry of Education. Teaching assistant positions through sponsored projects may also be open sometimes and these are called teaching assistantship through project (TAP). All teaching assistants (whether TA or TAP) are required to assist course instructors in grading, conducting tutorials and tests for the prescribed hours in a week. They may also be assigned any other academic or administrative duties related to the department such as admissions and examinations. PhD students under the research assistantship through project (RAP) categories are usually funded by sponsored research projects being undertaken by faculty members of the department. In such cases, research work leading to a PhD, is in general, closely related to the objectives of the respective project. There are various other categories of admission as well, such as those who are sponsored by their employing organisations (SW), quality improvement program for teachers of other engineering institutes (QIP), external candidates (EX), project staff of the institute (PS), institute staff (IS) and fellowship awardees from external organisations (FA). Admissions to the PhD program are usually conducted twice a year around May and December respectively. Additionally, admission into a dual degree program combining MTech and PhD is offered as well; and existing MTech students are also given an option to convert into this dual degree program.

Stages in the PhD program

The IITB PhD process as described in the Desiderata document is given below. An approximate duration for each stage of the process is also given, however the exact exit point depends upon successful completion of the exams and evaluations at each stage.

Stage 1: Preparation to begin thesis (1-1.5 years)

a. Completion of minimum course work
b. PhD Qualifiers: Tests comprehension and critical thinking based on course work and research paper review

Stage 2: Thesis Development (2 - 5 years)

a. Gradually defining a thesis: Four skills need to be essentially developed during a PhD process
    i. Analysis Capability
    ii. Lab work/ Tools Capability
    iii. Context Development
    iv. Technical Communication
b. Annual Progress Seminar (APS): Updates on progress made by the PhD candidate
c. Pre-Synopsys Exam: Test for completion of research

Stage 3: Thesis Defense (0.5-1 year)

a. Every PhD candidate has to defend his/her final thesis in front of a Research Progress Committee (RPC) which certifies the completion of a PhD if it finds that all the learning objectives were adequately met

Challenges faced by PhD students

During the pandemic, shutting down of labs hindered the progress of scholars who were involved in experimental work. The relatively sudden closing down of the institute also meant that ongoing experiments and their setups had to be left midway. The inconsistency of the 2020 semesters had a negative impact on the Annual Progress Seminars as well. Peer learning, an instrumental part of research, plummeted during the virtual semesters. Even after returning to campus, physical interaction with guides and other faculty did not start immediately, slowing the research progress of scholars.

Apart from problems caused by the pandemic, issues related to funding persist even during normal times. It is pretty evident from the data that the average stipend for research scholars at IITs is significantly less than what many foreign universities or industry jobs can offer for the same amount of work. The problem is exacerbated for PhD students from the TAP category who face a lot of uncertainty concerning their stipends. These students are already overburdened as they are required to work on their sponsored project and perform teaching assistantship duties in addition to carrying out independent research. The latter often becomes necessary since industry projects usually have restrictions on publishing the results.

Land is scarce in Mumbai, and with IIT Bombay being constrained by space as well, accommodation is an important issue for PhD students. The institute doesn't have sufficient rooms to accommodate all research scholars. Hostel allocations often get delayed, sometimes by a couple of years, and the rent in Mumbai is very high to be a viable alternative. Married research scholars find it especially difficult to get accommodation on campus.

PhD advisors play a very crucial role in the academic development of their students. Lack of understanding between a professor and a student can be detrimental to both and negatively hamper research progress. Other than this, the research scholar community in our department is highly diverse and scattered, with students coming from widely different backgrounds. Unlike undergraduates, research scholars have less common courses and instead have to work on independent research topics. Therefore, informal interaction among scholars often gets limited to their research groups.

Conclusion

Despite such challenges, our research output has increased considerably in the last few years, thanks to immense efforts from both students and faculty. We hope that the concerns raised by our postgraduate student representatives, some of which we highlighted here, are addressed in due course of time so that a further boost can be given to research activities. We thank Vishakha Pandey, Surya Varchasvi and Parth Mehta for their valuable inputs in this article.

SCAN THIS QR CODE TO VIEW THE DESIDERATA DOCUMENT ON OUR DEPARTMENT'S PHD PROGRAM

Aspire: IITB Research Park

In the current day global practices, financial growth as well as societal development need to be integrated closely to ensure security and sustainability of the planet. To develop a deep understanding of the issues involved, industry and academia need to work together to innovate, evolve and translate technology solutions for the society. While discovery, innovation and development of various technologies have been in the domain of academia, the industry has been the prime mover for translation of these technologies into practice. Therefore, a strong need for tight engagement of the industry and academia is felt. And there emerges the role of a Research Park – a place that connects knowledge, ideas, technology, and resources all under one roof. Research Park is a space where leading-edge anchor institutions and companies cluster and collaborate to complement each other's strengths. While the practice of having a university research park has been existent for decades internationally, India has tapped its potential only in recent years.

IIT BOMBAY RESEARCH PARK
aspire

The IIT Bombay Research Park, also called ASPIRE, celebrated its 5th anniversary in June 2021. This article looks back at the role of the Research Park in shaping industry-academia collaborations at IIT Bombay and its promising plans ahead.

Overview of the Research Park

The Ministry of Education, Government of India, commissioned IIT Bombay to build a Research Park on its campus. Subsequently, in 2016, the IIT Bombay Research Park Foundation (IITBRPF) was incorporated. The Research Parks' vision is to promote innovation, entrepreneurship, and research excellence through industry-academia collaboration. Modeled on the learnings from successful national and global research parks, ASPIRE is envisioned to become the nerve-center linking knowledge, expertise, and resources to boost industry-academia collaboration in India.

Companies are encouraged to set up working spaces, labs, and offices in the Research Park and benefit by leveraging the knowledge capital available at IIT Bombay. Not only this, the member companies get an opportunity to tap the growing talent of students, get access to state-of-the-art labs and the exhaustive collection of books at the IIT Bombay library. Companies can choose to collaborate with the institute through the following modes of engagement - *Fellowships & Scholarships, R&D Projects, Faculty Visiting Fellowship, Endowment for a Cause, Joint Project with Third Agency, Employment Opportunities, Joint Training/ CEP Courses, Adjunct Faculty, etc.*

The Journey So Far

At present, 21 companies namely, Applied Materials, Amar Chemistry, Atomberg, Bharat Forge, Ceremorphic, CTech, Everest, Google, ideaForge, igrenEnergi, Inventys, Jay Chemicals, MNST, MuRata, NanoSniff, NCIIPC, TATA Advanced Systems, Tejase Aerosense, Ubisoft, Viacom18, and Virenxia are the members of the Research Park. Of these, 12 companies have research labs set up on the campus, and nine other are Associates, wherein a company is virtually connected, need not co-locate itself, and can initiate collaborative activity with IITB. Though the Research Park is in its nascent stage, the temporary set-up at the IIT Bombay campus has resulted in several collaborations amongst the companies, the student community, and the faculty. The Park was able to initiate collaborations and garner funding of almost INR 10 crore generated through R&D collaborations in the last five years. There have been 25 joint publications, one patent registration, and 79 students have benefitted directly by getting internships and employment. While the Research Park offers many benefits for the companies, it equally helps the faculty and students in their academic pursuits. Start-ups like Nanosniff Technologies, ideaForge, Atomberg, igrenEnergi Services & CTech have graduated from SINE, faced the market, grown tremendously, and have set up R&D facilities in the Research Park. These success stories are a testament to the fact that IIT Bombay provides a complete ecosystem to shorten the time of innovation to mature and reach the market, by working parallelly with SINE, E-Cell, and the Research Park.

The Way Forward

The Research Park building is currently under construction and shall be operational by early 2022. This building will be a landmark structure cocooned in the flora and fauna-rich campus of IIT Bombay. It aims to be a green building on an area of 5 lakh sq. ft. About 50 companies are expected to set up their R&D labs/ centres in the Research Park in the coming two years. The structure provides all the utilities and facilities required by the industry.

The Research Park has helped establish R&D links in scientific domains that include, but are not limited to Semiconductors, Metals & Materials, Energy, Bio-technology, Chemical, Automobile, IT & Telecom. Some of the emerging technology domains that could be witnessed at the Park are Artificial Intelligence & Machine Learning, Healthcare, Energy, Robotics, Cyber Security, and e-mobility. Government schemes like ‘Make in India' and 'Startup India' provide funding opportunities with a vision to bolster research in the country. The existing R&D interaction between industries, institutes, and the various centres of excellence will only support the Research Park stand true to its commitment to connecting industry and academia.

To know more or to get associated with IITB Research Park, please visit www.iitbresearchpark.com or e-mail at info@iitbresearchpark.com.

Lab Tour - IITBNF


ADIL KHAN

PUDI SESHASAINADH

JANEEL PATEL

Those who have had a chance to walk along the never-ending pathways of the Infinite Corridor might have seen the tall and sleek nanoelectronics building which houses the IITB Nanofabrication Facility (IITBNF) on its lower levels. However, what many might not be aware of is the amazing research that goes on within the confines of the numerous labs within this facility. Through this article, we aim to take our readers on a quick tour of the IITBNF and provide them with a glimpse of the research work being undertaken inside this state-of-the-art facility.

As stated by IITBNF itself, its guiding mission is to provide a benchmark for state-of-the-art research, learning and outreach in the fields of semiconductor technology and nanotechnology. IITBNF consists of over 18 laboratories under its umbrella and has 60 faculty members associated with it spanning multiple research domains. Such is its importance that even Joe Biden (then the US Vice President) spent two hours touring this facility while on a visit to IIT Bombay in 2013. We would like to especially thank Prof. Udayan Ganguly, a key member and proponent of the IITBNF ecosystem, for sharing a lot of insights on its history and significance with us.

History of IITBNF

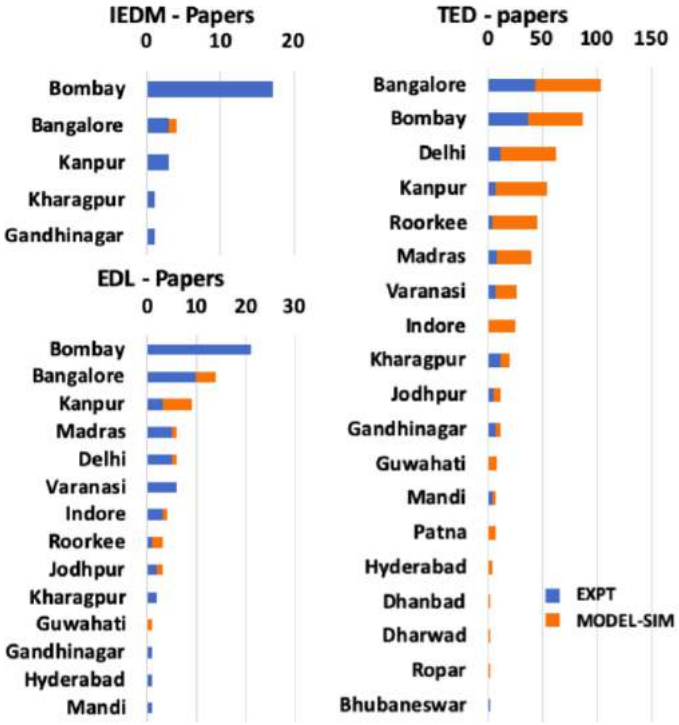
Nanofabrication is an integrative and complicated process, with a different set of tools required for each stage of the fabrication process. As Prof. Udayan points out, the culture at IIT Bombay is of setting up shared labs, which are open to researchers across different groups. This is driven by the fact that a large facility such as the IITBNF is beyond what any single faculty member can host alone, and the huge operational requirements for just running such a facility requires collaboration between multiple research groups. IITBNF, together with a similar facility (CeNSE) at IISc form the two earliest pioneers of nanoelectronics research in India.

IITB's journey with device fabrication goes back to 1985 when the first device fabrication lab with a Class 1000 cleanroom was set up through an MHRD funded project on the Centre for Microelectronics. This project was managed jointly by Prof. Juzer Vasi, Prof. A. N. Chandorkar and Prof. R. Lal; who together successfully built a 3 micron NMOS fabrication lab to promote research and teaching in microelectronics. The main boost towards setting up the present day IITBNF came in 2006 with an INR 500 million grant from the Government of India for a collaborative project between IITB and IISc to set up a Centre of Excellence in Nanoelectronics. Many of the cleanrooms, labs and instruments at IITBNF came up between 2006 and 2012 with support obtained from industrial collaborators as well. Back in 2006, no one expected IITBNF to be a huge success; rather it was more of an aspirational thing. However, fifteen years on, research data today shows that we have done extremely well in nanoelectronics research.

A recent article by Prof. Udayan, Sandip Lashkare and Prof. Swaroop published in IEEE Electronic Devices Society Newsletter (January 2021) details the rise of nanoelectronics research in India, led by IIT Bombay. Starting from only a few contributions to nanoelectronics engineering before 2011, we have become one of the top 10 nations in this field, as measured by the number of papers published in IEEE Electronic Devices Letters (EDL) and Transactions on Electronic Devices (TED).

India among the top 10 contributors to research in nanoelectronics in the year 2019

Research groups associated with the IITBNF have a large number of industrial collaborations including sponsored projects and fellowships from companies such as Intel, GlobalFoundries, Applied Materials, IMEC and Micron among numerous others. The establishment of the National Centre on Photovoltaic Research and Education (NCPRE) in 2010 has aided in the expansion of tools and equipment especially in the fields of solar cell research and applications. Through the INUP (Indian Nanoelectronics Users Program), the facilities at IITBNF are also thrown open to the rest of the country, with researchers from other universities and organisations coming here to work on their research proposals and projects.



IIT-B leads in nanoelectronics research as measured by the number of contributions to IEDM, EDL and TED

Areas of Expertise

Research at IITBNF spans numerous technology domains such as computing devices, communication devices and environmental sensors to name a few.

Computing Devices:

This has been the traditional area of strength with numerous publications in high-impact journals and conferences and tens of national and international patents. IITBNF houses clean rooms, equipment and process tools for all essential device fabrication processes. Additionally, IITBNF is well-equipped with state-of-the-art device simulation and characterisation facilities, including

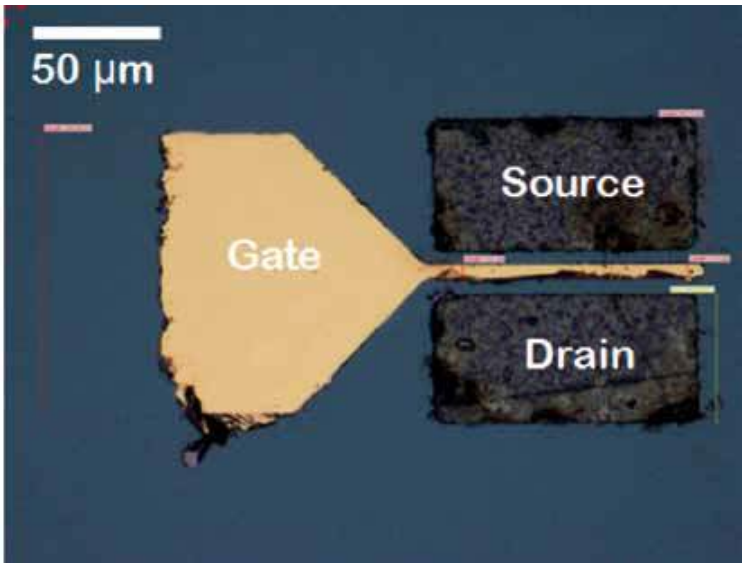
commercial process tools. Ongoing research in the lab focuses on contemporary topics such as CMOS-based device reliability, advanced CMOS logic devices, advanced memory devices and beyond-CMOS approaches.

Sensing & Actuator Devices:
This research domain at IITBNF encompasses a wide range of materials and device platforms that find applications in public health, homeland security and agriculture. Work done in this area is interdisciplinary bringing together groups from Electrical Engineering, Mechanical Engineering, Chemistry and Bio-sciences departments. The facility has full-fledged CAD setups, fabrication tools and characterization facilities for micro/nano electromechanical devices. Some technologies developed here include a point of care sensor for detecting cardiac markers, a handheld device for explosive detection, a wearable web-enabled ECG monitoring device and a soil moisture measurement unit. Prototypes of 320x256 Quantum Dot Infrared Photodetector based IRFPA (infrared photodetectors and focal plane arrays) thermal imagers were developed and demonstrated for the first time in India at IITBNF.

Energy-harvesting Devices:
This is a fast-growing, vital area of research attracting immense interest in recent times. IITBNF currently houses 7 laboratories (including a class 1000 cleanroom) exclusively dedicated to solar cell research, which work on modelling, fabrication and characterisation of crystalline, thin film, multi-junction and organic solar cells. Apart from solar energy, the research work at this facility also revolves around deep exploration and evaluation of various other widely available forms of energy to develop energy harvesting devices for numerous electronic applications. Work in this domain is multidisciplinary, bringing together researchers from Energy Science & Engineering, Chemistry and Electrical Engineering departments, among others.

A gallium nitride (GaN) based high electron mobility transistor (HEMT) was first successfully fabricated in India in 2009 at this facility.

Communication Devices:
This research area at IITBNF focuses on relatively new topics such as III-V semiconductors, which are increasingly being deployed for high-speed and high-power applications. IITBNF now possesses state-of-the-art facilities for simulation, characterisation and fabrication of III-V compound semiconductor-based high-speed switches and optoelectronic devices.



Micrograph of the first GaN HEMT fabricated in India

Recent Research

Recently, a 180 nm CMOS based memory technology developed at IITBNF got adopted for indigenous manufacturing by the Semi-Conductor Laboratory, Chandigarh. A team led by Prof. Udayan Ganguly developed this one-time programmable (OTP) memory based on ultra-thin deposited silicon dioxide (a few atoms thick) instead of the existing gate oxide-based OTP technology. In contrast to the high voltage required by current technologies, this new memory chip requires less power and chip-area as the need for boosted voltage supply is avoided. This invention was covered in the national media as well and is considered to be an important national milestone in semiconductor R&D for memory technologies. It enables secure memory and authentication for national products like e-passports and credit cards.

Details of the facilities

Clean Room:

It is imperative to have an extremely clean environment for semiconductor fabrication, as the presence of even a tiny dust particle can have a devastating influence on the operation of nanoscale devices. A class 1000 cleanroom, such as that present at IITBNF, has a maximum of 1,000 particles (≥ 0.5 μm in size) per cubic feet of air inside. By comparison, an ordinary room in a building may have more than a million such particles per cubic foot of air.

Lithography:

Lithography forms the backbone of a typical semiconductor device fabrication run. It enables one to 'draw' or 'write' micrometre or nanometre sized patterns, thereby defining the device dimensions. In optical lithography, a UV beam is used for writing, and the pattern sizes can be as small as a few micrometres. Even smaller, nanometre-sized patterns can be written via e-beam lithography which uses a beam of electrons to write. In both cases, 'writing' is done on special light-sensitive (or electron-sensitive) materials known as resists. These are chemically processed after exposure (to the light or electron beam) and reveal the written pattern according to the part that was exposed or left unexposed. IITBNF has multiple optical lithography tools with different pattern dimension limits. The best resolution at IITBNF (< 20 nm) is achieved through a state-of-the-art e-beam lithography tool: RAITH150 Two. For both optical & e-beam tools, mask aligners and resist spinners dedicated to different types of resists are available with capabilities to process 2", 4" and 8" wafers.

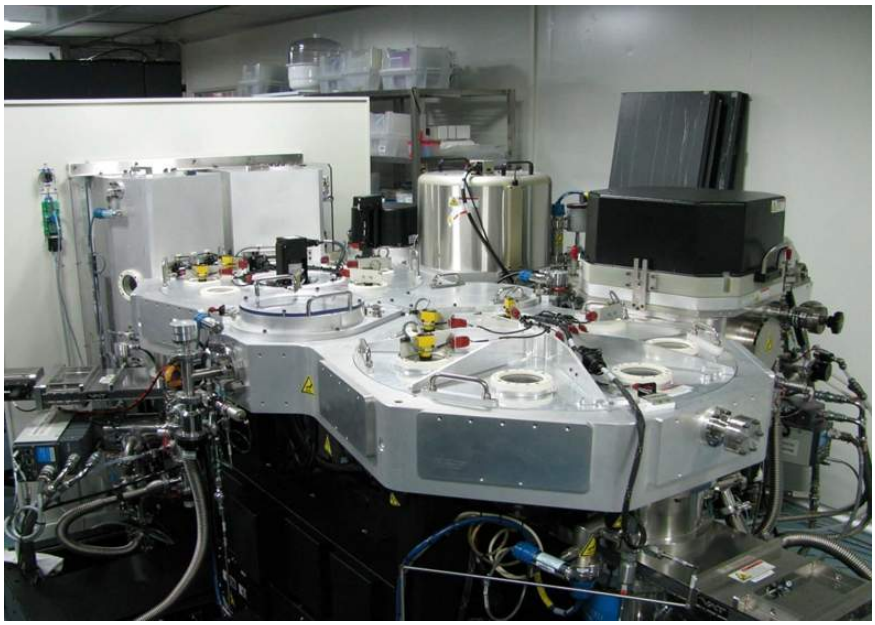
Karl Suss MJB4 Mask Aligner

Etching Tools:

While a lithography process is used to write patterns on a resist layer, a different technique is needed to transfer these patterns from the resist onto the main layer of the semiconductor wafer. Wet etching & dry etching are the most commonly used processes to achieve this goal. IITBNF has separate dry etch tools for silicon and III-V semiconductor samples to prevent material cross-contamination. A general-purpose ion miller is used to dry etch any sample using a purely physical ion bombardment process. Plasma asher tools are also available that are typically used to remove resist from a sample via a chemically reactive oxygen plasma.

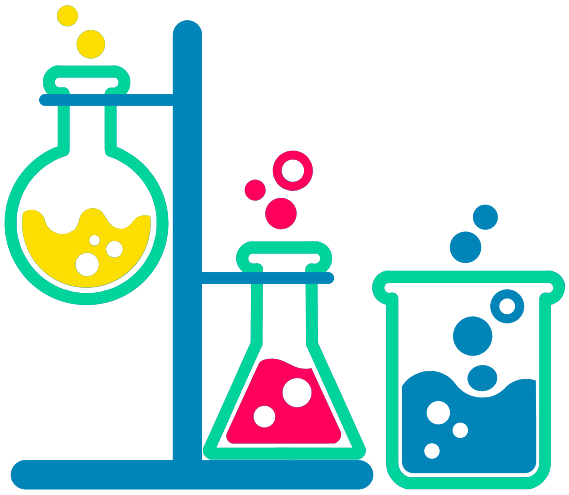
Deposition, Growth and Anneal Tools:

Thin film deposition of some materials is needed at various stages of the process – from the initial active semiconducting layers to the final metal contact layers. With new materials being explored for various applications today, dedicated systems and novel deposition techniques are required to integrate them into devices. Pulsed laser deposition (PLD) and atomic layer deposition (ALD) are two examples of such enabling capabilities available at IITBNF, along with other conventional silicon processing equipment. Apart from these, three molecular-beam epitaxy (MBE) growth systems are available at IITBNF, which can grow different kinds of samples (III-V compounds, III Nitrides, Si, Ge, Sn). Molecular-beam epitaxy (MBE) works in an ultra-high vacuum and it's slow deposition rate allows the films to grow epitaxially (in an ordered arrangement with respect to the underlying crystal structure). For annealing, there are rapid thermal processing (RTP) tools in use with the ability to do annealing, oxidation and nitridation of the substrates as and when required.



Physical vapor deposition (PVD) system at IITBNF

Molecular-beam epitaxy (MBE) system for GaN at IITBNF



Wet Chemistry Tools:
Use of chemical solutions is often needed at various stages of device fabrication; most commonly during wafer substrate cleaning and wet etching. In order to minimize cross-contamination and maintain process control, IITBNF has dedicated wet benches and clean stations for silicon placed away from general purpose stations. Complementary apparatus such as sonicators, spin coaters and hot plates are also provided at specific stations.

Characterisation Tools:
IITBNF has an array of physical and chemical characterization tools that enable in-line (during fabrication) and post-fabrication investigation into material structure and related properties. They include optical microscopes, profilometers, ellipsometers and multiple spectroscopy tools. Apart from these, there are extensive facilities for electrical characterisation of nanodevices. Dedicated instruments for detailed measurements and analysis of device capacitance, current, magnetism and lifetime are available. Additionally, instruments for specialized measurements on solar cells and quantum devices are also in place.

How to get involved with the work

Prof. Udayan tells us that there are three different kinds of work in which one can get involved at IITBNF. To start with is the simulation-modelling work such as the simulation of new device structures using TCAD software. This is the level of work which is the most accessible to undergraduate students due to their short time constraints. The second level is device characterisation, which includes measuring the electrical, material and structural properties of devices which have already been fabricated. This work is comparatively more time consuming but still feasible for everyone. Then comes the third level which is the actual fabrication of devices. Being a very long and multi stage process, device fabrication is usually carried out by 3-year Masters and PhD students.

The courses that one can do in order to get involved with research at IITBNF include EE735 (Microelectronics Simulation Lab), EE672 (Microelectronics Technology Lab), EE669 (VLSI Technology), EE728 (Growth and Characterization of Nano-electronic Materials) apart from various standard courses on device physics.

SCAN THIS QR CODE TO VISIT THE WEBSITE OF IIT BOMBAY NANOFABRICATION FACILITY (WWW.IITBNF.IITB.AC.IN) AND FIND OUT MORE ABOUT IT

Wellness is a Well-Trodden Path

Cornered


NEHA CHAUDHURI


MIHIKA DHOK

All things are difficult before they are easy. - Proverb

Depression, anxiety and performance related pressures at work or in student life are not new phenomena. Yet when people talk about mental health these days, they seem to imply that mental health is a precarious entity independent of a person's immediate environment, physical capacities or social relationships. That the resolution to mental health problems is to talk to experts.

But, what if you're not there yet.

You're not sure what is wrong. You're not even sure why you're unhappy.

And you have trouble expressing or pinpointing the matter.

What if all you know is that you keep looking for evidence of doing better but do not find it? You observe that you slip faster than before into a miasma of anger or frustration every time you face a failure.

How do you get out of having been cornered into silence? Where do you restart the process of expressing what seems difficult to put into words?

Where do you begin, so that ten or twenty-one days later, you are capable enough to express your situation or state of mind to a friend, a family member, or even an expert on mental health?

Starting Small – Reading the ABC's Yourself

A good book is like a pot of gold. – Proverb

People across generations have experienced loneliness, disconnection, doubt, desire, struggle and hardship. Pressures and forces beyond our control or power have always existed. Over the ages and in all religions, specific daily regimens have been used to combat such forces and develop resilience, self-sufficiency and integrity in individuals. These different daily regimens have led to diverse lives: of saints, warriors, householders, scientists, professionals, artists or tradesmen. Whether Eastern or Western, these systems are founded on a daily routine that follows the human body's biological rhythm in alignment with the natural regularity of sunlight and darkness or moonlight.

Our most common actions, across history, nationalities, races and genders linked to this natural rhythm are:

- Waking up
- Getting out of bed
- Going back to bed at night
- Sleeping

Since we wake up every day, we get out of bed every morning, we brush our teeth, and every night we fall into bed, these actions become the easiest to take for granted. But like the spine of a sturdy hardbound book, they hold the pages of our life together and can absorb a lot of wear-and-tear before we notice the need for mending.

The First Page – Action As Transformation

I ask not for a lighter burden, but for broader shoulders.
– Proverb

Each morning is a new opportunity, a blank page and each micro-action – from opening your eyes, making sense of your surroundings, swinging your feet off the bed, pulling your torso up and feeling the floor beneath your soles – is like preparing to flip a page, take a pen and start writing.

Noticing these micro-actions, paying attention to them while breathing normally, will cause your thoughts to slow down, and cultivate awareness. Slowing your mind is the best self-therapy. It builds silent awareness, which is the first step to enabling the understanding of one's own predicament.

Good sleep is essential to the cultivation of this silence. Reverse engineer your day, if need be, to ensure a watertight before-sleep routine.

Winding down at the end of the day requires something around two hours, since the measure of discipline that sleeping on time requires often conflicts with our ambitions.

There's enough information linking organ health, emotional stability, productivity etc. to visual charts of the bio-rhythm that you can look up if interested. This information essentially has roots in older non-written (i.e. oral), only practice-based Indian Knowledge Systems that emphasize the value of action, repetition and the body's capacity to overcome psycho-emotional states through action, fortifying mental, emotional and physical health.

Reaching out to others comes later, when we are able to generate expression.

Sanding Down the Edges
– Reading a Chapter

A bird does not sing because it has an answer. It sings because it has a song. - Proverb

Modern medicine has broken down the physical, emotional and psychological aspects into separate parts to be treated. Yet, a human being is the sum of all these. Hence, positive psychology, cognitive therapy, authenticity and engagement development, evolving the growth mindset, emotional resilience, and physical improvement have become separate things to pursue during the day. But the whole is greater than the sum of its parts. The day is one – its start is one and open to all, as is its end.

Latest self-help books like BF Fogg's Tiny Habits, Charles Duhigg's The Power of Habits and James Clear's Atomic Habits illustrate evidence from various scientific fields to support why habits and repetition of certain habits are transformative for your mental health, physical health and surrounding environment. What can be added from the vast Eastern pantheon of wisdom into this cauldron of eternally-produced knowledge is the ability to effect transformation through awareness. There is a basic narrative song we have about ourselves. It is a song we have acquired through history and culture; often patched up, received from others and added to our notes to make our own. We run it over and over in our heads when faced with exceptional decisions or choices, so that we can choose actions that 'someone like us' will undertake.

When we begin to practice observation of micro-actions around waking up, getting out of bed and getting back to sleep, that base level narrative is interrupted because these actions are organically repetitive, and equal to all. Everybody undertakes these actions.

Corners to Circles
– Conquering Sections

Pain is the best instructor but no one wants to go to his class. – Choi, Hong Hi

The psychophysical state has a base stable level and the ego tries to maintain that base level even if that stability means to repress, break off, numb down parts of us. So resistance is inevitable when change happens. With awareness, we can voluntarily bring about change.

Hence, it is essential to anticipate change – pleasant or unpleasant - when you face whatever you think you are, and accept before you can un-repress, ex-press, release and ultimately gain the flexibility to flip the base narrative currently inhabiting you. The way to begin this is to take an extra 30 minutes so you can wake up slowly, get out of bed with awareness and come back to bed on time.

Over time, you begin to sand down the edges of exaggerated perception and witness what is unique to you in these actions. Over time, repressed emotions, feelings, thinking patterns that define a person's psycho-emotional-physical state get disturbed since they are coming into view through awareness. This subtle change happens in silence, in your own company, without intervention from anyone.

Circles to Spirals – Your Own Book

Freedom is what we do with what is done to us. – Sartre

You're not sure what is wrong or why you're unhappy.
And you don't think this needs to be talked about just yet.

How do you gain self-sufficiency in setting right the balance for yourself, one day at a time?

Waking up early in the morning need not depend on your doubt, unhappiness, or lack of ability to express your anxiety. You do not need to wait until you are regularly burning with anger to set right your sleep routine.
Waking up and going to bed at the same time everyday need only be a decision you make to see what happens at the end of the next 10 – 21 days.
Set these up, pay attention to each micro-action for the first and last thirty minutes of your day. They're the only trigger you need to begin reaching out to others.

Ms. Neha Chaudhuri is part of a new Department Alumni and Corporate Relations Outreach Initiative. You can get in touch with her at eeacr.iitb@gmail.com.

Informal Section

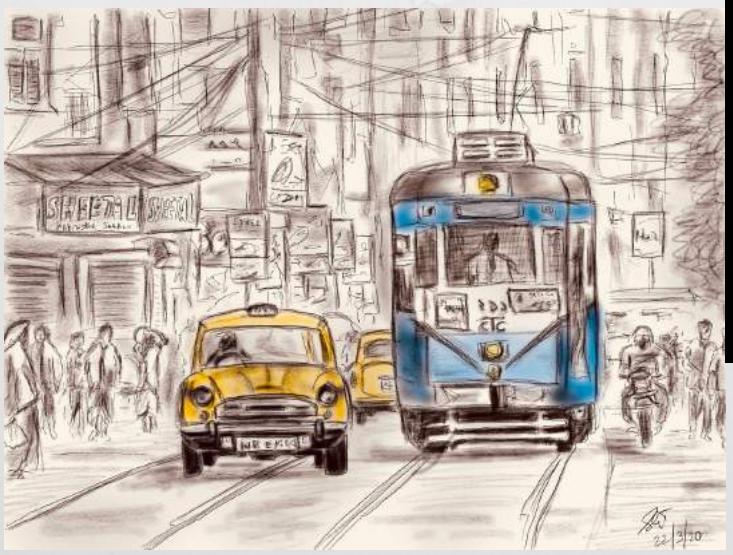

MIHIKA DHOK


PRASANN VISWANATHAN


SIDDHARTH ANAND

Road painting done by Elec students - Ali, Ravi Thakur, Sudesh, Akansha and others before closing of campus to raise awareness for wearing masks on 5th March 2020 at slope near gymkhana ground and library. Quote - "Wear a Mask"

Artwork by Prof Siddharth Tallur



Vemparala Lakshmi Pravallika

Sinkar Sharvaree Rajendra

Art is not what you see,
but what you make others see.

Presenting Artworks

Phansalkar Ishan Shrirang

Aakanksha Suresh Jain

Phansalkar Ishan Shrirang

Aakanksha Suresh Jain

Art is not what you see,
but what you make others see.

Presenting Artworks

Reet Jignesh Mehta

So,
Million are thoughts,
A million already fought.
When the heart ponders,
While the mind throbs.
And the vision hears,
What the breath speaks.
And uncanny is natural.

As I seek the truth,
While I pen the uncanny most,
Though I doubt,
Is it
The prose
Or the doubt himself.

- Hemo

The stars lie still,
strengthen your will.
You are a deep verse,
You are a whole universe;
Pull the Trails the way You Wish..!

The stars lie still,
waiting for you to,
strengthen your will.

- Tanmay Goyal

खुदा ने तो तकदीर ये अधूरी छोड़ी न होगी,
हार लिखी है तो क्या;
जीत लिखने से भी, कलम उसकी कतराई न होगी !

- Tanmay Goyal

WORDS SPEAK A LOT

Presenting Poetry

In the end we're all just stories.
Few of them sung by bards,
Some end up in books and speeches.
A lot, like most literary works,
Just get crushed,
Under the wheels of the chariot of time.

Our traces may fade away,
Just like the strides,
Rinsed off by the tides,
Just like the memories we washed off,
In the journey to heal our heart
And move on,
But in vain.
Time, yet has he to see
One more sinister,
Than himself.

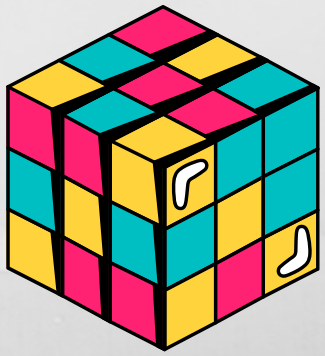
- Ram

PUZZLE UP

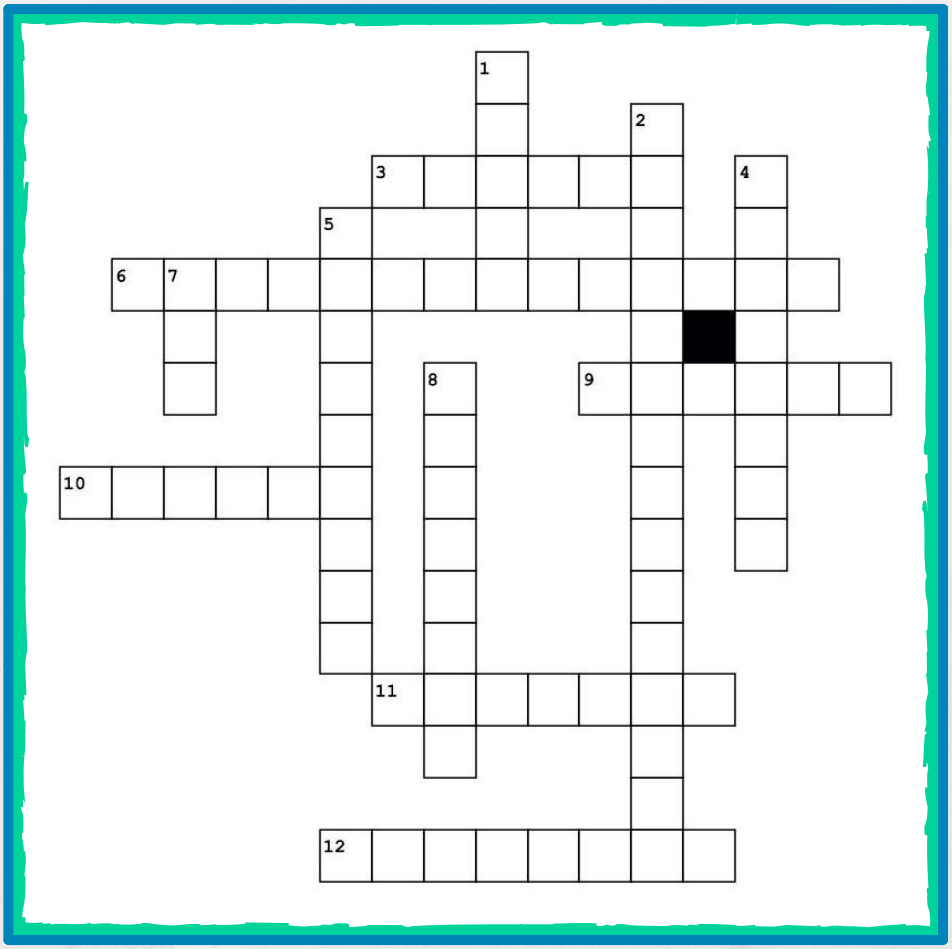
1) An enemy spy has poisoned one out of 1000 barrels of wine in a king's cellar. Even a sip of the poisoned wine has potency to kill. However, the effects of the poison show only in 30 days. The king asks the royal jailor to identify the poisoned barrel within 30 days. What is the least number of prisoners the jailor must employ to identify the poisoned barrel?

Solution at -
https://gurmeet.net/puzzles/poisoned-wine-barrels/

2) Design a 3-input 3-output logic circuit that negates the 3 signals. You have an infinite supply of AND and OR gates but only two NOT gates.



Solution at
https://gurmeet.net/puzzles/three-not-gates-from-two-not-gates/



Across

3. the navigation chip developed by our department, supervised by Prof Rajesh Zele

6. the department building where most of the classes are held

9. _____ Semiconductor Manufacturing Co. is the largest manufacturer of semiconductor chips in the world

10. the first ever department cultural night was held in 2019 in _____ (Hint: it is a venue)

11. department fest, conducted last in 2019

12. bilayer _____ becomes superconducting when twisted to the magic angle

Down

1. all the students belonging to the department wear traditional attire on _____ day

2. The US Vice president Joe Biden, in 2013, visited the _____ facility in our department

4. ___ Electronics Lab is where most of the UG lab courses are conducted (Hint: EE main building 3rd floor)

5. The first _____ was patented in 1892 by Jesse W. Reno

7. this technology has been proposed for wireless charging of electric vehicles

8. name of the restaurant nearest to our department

THIS CROSSWORD CAN BE SOLVED ONLINE AS WELL BY SCANNING THIS QR CODE OR USING THE LINK https://crosswordlabs.com/embed/electrical-320

A Letter from EESA

The Electrical Engineering Students' Association (EESA) is a student body within the Department of Electrical Engineering whose main objective is to keep students engaged through extracurricular and professional activities to bring the student community together. Having the blueprint already laid down by the EESA 2020-21 team, whose complete tenure had been online, the EESA 2021-22 team, composed of people with an online experience, carried forward the legacy of the department.

For the students of the EE department, EESA organized a weekend extravaganza during the summer vacation titled as the 'Midsummer w-EE-kend'. The event consisted of fun quizzes followed by intra departmental chess and Valorant tournaments, with the entire event witnessing a substantial footfall of more than 200 enthusiastic participants. The culmination of these festivities happened with the screening of the 2009 Morgan Freeman and Matt Damon starrer 'Invictus', which brought out the sweet nostalgic memories of the EESA movie screening that used to be an integral part of the life of an EE student before the pandemic. Speaking of memories and nostalgia, EESA organized the Valedictory Function for the Class of 2021 just before the day of their Convocation, with the goal of providing them with a farewell that they deserve. The function was filled with enthralling cultural performances, fun activities and Department Awards presented to the students of the graduating batch.

'Core Talks', conducted with the aid of SARC, saw two distinguished alumni as speakers and more than 250 students as attendees; the event covering aspects of pursuing higher education and job opportunities in the core Electrical Engineering sector, respectively. For the professors of the department, a Teacher's Day felicitation ceremony was conducted in order to express our gratitude to the respected professors. The ceremony saw an address from the HoD Prof Kishore Chatterjee followed by felicitation of professors from the department who had been bestowed upon the honour of Teaching Excellence by the institute.

Autumn 2021-22 concluded with the much awaited Department Orientation being conducted for Undergraduate Freshmen joining this year, with the aim of breaking the ice and helping them know more about our beloved department and various activities. The event was filled with students displaying their various talents in various genres of performing arts and was complemented by fun quizzes and activities that allowed them to further lighten up and interact freely with their peers and seniors. To facilitate cognizance among freshmen regarding the marvelous facilities that are present in the department, a video tour of the department building and the numerous labs present in it was conducted for them.

Through all these activities this semester, the council tried to provide avenues for students to enrich their experience of IIT life and culture, and facilitate interaction among everyone despite the pandemic forcing us to resort to the safety of our homes.

EESA Council 2021-2022


विद्युत अभियांत्रिकी विभाग
गिरीश गायतोंडे व्याख्यान कक्ष संकुल
DEPARTMENT OF ELECTRICAL ENGINEERING
GIRISH GAITONDE LECTURE HALL COMPLEX
G व्याख्यान कक्ष ००१, ००२, LECTURE ROOM 001, 002
1 व्याख्यान कक्ष १०१, १०२, १०३ LECTURE ROOM 101, 102, 103
2 विभाग कार्यालय
संमेलन कक्ष
DEPARTMENT OFFICE
CONFERENCE ROOM
3 व्याख्यान कक्ष ३०१, ३०२, ३०३
अभ्यागत संकाय कक्ष
LECTURE ROOM 301, 302, 303
VISITING FACULTY ROOM
4 ज्ञाता केंद्र
पुस्तकालय
LEARNING CENTRE
LIBRARY
5 भारती संचार केंद्र
वी एल एस आई लॅब
एम्बेडेड सिस्टम्स लॅब
BHARTI CENTRE FOR COMMUNICATION
VLSI LAB
EMBEDDED SYSTEMS LAB


विद्युत अभियांत्रिकी विभाग
ELECTRICAL ENGINEERING DEPARTMENT

We feel delighted to have brought forth a new edition of the department newsletter, Background Hum. Through this edition, we aimed to bring to you the fascinating stories of people who are or have been associated with the department and also provide you with unique perspectives on contemporary issues like the global chip shortage.

We would like to thank all the faculty members, students, and the EE ACR team, whose invaluable contributions have been instrumental in getting this edition ready.

We will appreciate your feedback and comments about the newsletter. Feel free to reach out to us at bh@ee.iitb.ac.in. Wish to contribute? Have an article idea? We're all ears!

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