Introduction to the PCI Interface

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Outline

1. Outline
2. Motivation
3. Bus Standards
4. PCI Technology Overview
5. PCI Local Bus
6. References
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- Motivation
- BUS standards
- PCI Technology Overview
- PCI Local Bus
- PCI protocol
- Special Cases
- Electrical and Mechanical Specifications
- Other Topics
- References
Introduction to the PCI Interface

Motivation

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- Motivation

Inside a Computer

- What is a BUS?
  - Components - Processor, Memory etc
  - Peripherals
  - Interconnection

- Motivation
  - Data flow
  - Speed
Local Bus

- A set of parallel conductors, which allow devices attached to it to communicate with the CPU.
- The bus consists of three main parts:
  - Control lines, Address lines, Data lines

Diagram shows how devices are attached to a generic bus.

Key
- Data Lines
- Address lines
- Control lines
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Bus Protocols

- Requirements of a BUS standard
  - Electrical, Mechanical requirements
  - Protocol requirements

- Common BUS standards
  - ISA and EISA
  - MCA (Micro Channel Bus)
  - VESA Local BUS (Video Electronic Standard Associations) : 1-2 devices can be connected.
  - PCI Local BUS
ISA (Industry Std Arch.)

- Has a clock speed limit of 8 MHz
- Has a word length of 8 or 16 bits (8 or 16 data lines)
- Requires two clock ticks to transfer data (16 bit-transfers)
- Very slow for high performance disk accesses and high performance video cards
EISA (Enhanced Std Arch)

- Has a clock speed of 8.33 MHz
- Maximum of a 32-bit wide word length (32 data lines)
- Can support lots of devices
- Supports older devices which have Slower or Smaller word lengths (ISA)
- Transfers data every clock tick.
MCA (Micro-channel Bus)

- Has a clock speed of 10 MHz
- Has a 32 bit word length (32 data lines)
- Transfers data every clock tick.
VESA (Video Electronic Std Arch.)

- Has a clock speed limit of 33 MHz.
- Limited to a 32-Bit wide word length (32 data lines).
- Cannot take advantage of the Pentium’s 64 bit architecture.
- Limited support for Burst Transfers, thereby limiting the achievable throughput
- Restricted on the number of devices which can be connected (1 or 2 devices).
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PCI General Block Diagram
PCI - technology Information

- PCI: Peripheral Component Interconnect
- Conventional PCI
- PCI-X
  - 1.0
  - 2.0
- PCI Express
- Other
PCI-SIG

- PCI Special Interest Group
- Industry organization formed in 1992
- Over 900 members
- Promotes PCI as an industry-wide standard
- Full ownership and management of the PCI specifications
- Maintains the PCI specifications and forward-compatibility of all PCI revisions
PCI Technology Overview

PCI Technology

- Conventional PCI
  - Initial PCI 1.0 proposal by Intel in 1991
  - Introduced by PCI-SIG as PCI 2.0 in 1993
  - Version 2.1 approved in 1995
  - Recent version 2.3 approved in March 2002

- PCI-X
  - Version 1.0 approved in September 1999
  - Version 2.0 approved in July 2002

- PCI Express
  - Formerly known as 3GIO
  - Version 1.0 approved in July 2002
Conventional PCI

- Plug-and-Play Functionality
- Standard PCI is 32 bit and operates at 33 MHz
  - Throughput 133 MB/sec
- PCI 2.1 introduced
  - Universal PCI cards supporting both 3.3V and 5V
  - 64 Bit slots and 66 MHz capability
    - 32-Bit throughput @ 66 MHz: 266 MB/sec
    - 64-Bit throughput @ 66 MHz: 532 MB/sec
- PCI 2.3 system no longer supports 5V-only adapters
  - 3.3V and Universal PCI products are still fully supported
PCI-X 1.0

- Based on existing PCI architecture
- 64-Bit slots with support for 3.3V and Universal PCI
  - No support for 5V-only boards!
- Fully backwards-compatible
  - Conventional 33/66 MHz PCI adapters can be used in PCI-X slots
  - PCI-X adapters can be used in conventional PCI slots
- Provides two speed grades: 66 MHz and 133 MHz
  - The slowest board dictates the maximum speed on a particular bus!
  - Targeted at high-end data networking and storage network applications
PCI-X 2.0

- Based on PCI-X 1.0
  - Still fully backwards-compatible
- Introduces ECC (Error Correction Codes mechanism to improve robustness and data integrity
- Provides two additional speed grades
  - PCI-X 266: 266 MHz (2.13 GB/sec)
  - PCI-X 533: 533 MHz (4.26 GB/sec)
- Bandwidth sufficient to support new breed of cutting-edge technologies
  - 10 Gigabit Ethernet / Fiber Channel
  - 4X/12X infiniBand
PCI-X Speed Limitations

- PCI-X supports point-to-point and multi-drop loads
- Highest speed grades are supported exclusively with point-to-point loads
  - PCI-X 133
  - PCI-X 266
  - PCI-X 533
- Two PCI-X 133 loads operate at 100 MHz
- Four loads operate at a maximum of 66 MHz
- OEMs can build connector-less systems with multiple loads utilizing high speed grades
**PCI Express**

- High-speed point-to-point architecture that is essentially a serialized, packetized version of PCI
- General purpose serial I/O bus for chip-to-chip communication, USB 2.0 / IEEE 1349b interconnects, and high-end graphics
  - Viable AGP replacement
- Bandwidth 4 Gigabit/second full duplex per lane
  - Up to 32 separate lanes 128 Gigabit/second
- Software-compatible with PCI device driver model
- Expected to coexist with and not displace technologies like PCI-X in the foreseeable future
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PCI Local Bus

- Bus Width: 32 or 64 bits
- Operating frequency: 0-66 MHz
- Can support many more devices than VESA
- 64 bit extension for Pentium proc.
- Greater Variety of Expansion cards available.
- Multiplexed Address and Data
- PCI SIG (Special Interest Group)
PCI Local Bus Revisions

- 2.0 - connector and expansion board specification
- 2.1 - 66MHz operation
- 2.2 - protocol, electrical and mechanical specs
### Overview of Speeds of buses

<table>
<thead>
<tr>
<th>Bus Type</th>
<th>Bus Width</th>
<th>Bus Speed</th>
<th>MB/sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISA</td>
<td>16 bits</td>
<td>8 MHz</td>
<td>16 MBps</td>
</tr>
<tr>
<td>EISA</td>
<td>32 bits</td>
<td>8 MHz</td>
<td>32 MBps</td>
</tr>
<tr>
<td>VL-bus</td>
<td>32 bits</td>
<td>25 MHz</td>
<td>100 MBps</td>
</tr>
<tr>
<td>VI-bus</td>
<td>32 bits</td>
<td>33 MHz</td>
<td>132 MBps</td>
</tr>
<tr>
<td>PCI</td>
<td>32 bits</td>
<td>33 MHz</td>
<td>132 MBps</td>
</tr>
<tr>
<td>PCI</td>
<td>64 bits</td>
<td>33 MHz</td>
<td>264 MBps</td>
</tr>
<tr>
<td>PCI</td>
<td>64 bits</td>
<td>66 MHz</td>
<td>512 MBps</td>
</tr>
<tr>
<td>PCI</td>
<td>64 bits</td>
<td>133 MHz</td>
<td>1 GBps</td>
</tr>
</tbody>
</table>
PCI Local Bus Features

- **Performance** -
  - Burst Transfer at 528 m bps peak (64 bit- 66 MHz)
  - Fully concurrent with Processor-Memory subsystem
  - Access time is as fast as 60ns.
  - Hidden central arbitration.

- **Low cost** - multiplexed
- **Low Pin count** - 47 pin for target; 49 pin as initiator.
- **Ease of Use** - full auto configuration
- **Flexibility** - processor independent, accommodates other protocols
- **Green Machine** ‘CMOS drivers → low power
Every device on the PCI bus is either
- PCI compliant - has the same signals as the PCI bus
- Connected via a PCI core - this piece of hardware does the interfacing

Common devices
- Audio/Video cards
- LAN cards
- SCSI controllers
PCI Interface Signals

**Required Pins**
- Address & Data:
  - AD[31::00]
  - C/BE[3::0]#
  - PAR
  - FRAME#
  - TRDY#
  - IRDY#
  - STOP#
  - DEVSEL#
  - IDSEL

**Interface Control**
- PERR#
- SERR#
- REQ#
- GNT#

**Error Reporting**
- CLK
- RST#

**System**

**Optional Pins**
- AD[63::32]
- C/BE[7::4]#
- PAR64
- REQ64#
- ACK64#
- LOCK#
- INTA#
- INTB#
- INTC#
- INTD#

- TDI
- TDO
- TCK
- TMS
- TRST#
Introduction to the PCI Interface

PCI Local Bus

PCI System Signals

- CLK: clean signal derived from the clock generator (33MHz, 66MHz)
- RST: Active Low Asynchronous reset
- PAR: Parity Signal to ensure the parity across the AD bus and C/BE.
PCI Bus Protocol - Signal Definition

- **AD** - Multiplexed address and data lines
- **C/BE** - Command and Byte Enables
- **FRAME** - Master indicating start/end of transfer
- **IRDY** - Master (initiator) ready
- **TRDY** - Target ready
- **DEVSEL** - Target device selected
- **REQ** - Request for bus
- **GNT** - Bus Grant
PCI control signals contd.

- **STOP [I/0]**: Target asserts to stop the transaction in Progress.
- **IDSEL [I]**: Used as chip select
- **LOCK [I/0]**: During semaphore currently accessed target locked by initiator
- **DEVSEL [I/0]**: Asserted by target when the target asserts has decoded its address. (If by 6 clk not asserted $\Rightarrow$ master abort.
PCI Configuration Register

- Device ID
- Vendor ID
- Status / Command reg
- Base Address \([0,1,2,3,4,5]\)
- Maximum Latency
- Minimum GNT
- Subsystem ID, Subsystem Vendor ID
PCI Command Types [C/BE]

- 0000 → INTR ack
- 0010 → I/O Read
- 0011 → I/O Write
- 0110 → Memory Read
- 0111 → Memory Write
- 1010 → Configuration read
- 1011 → Configuration write
JTAG boundary scan

- Test Access Port
  - Test Clock
  - Test Data in
  - Test Data out
  - Test Mode select
  - Test Reset
- IEEE standard 1149.1 compliant
Interrupts

- Asynchronous events
- 4 interrupt lines for multi-functional devices.
- Interrupt lines go to the interrupt controller to execute the ISR
PCI Bus Protocol-Transfer mechanism

- Configuration read/write
- IO read/write
- Burst
  - Basic form of data transfer
  - Includes one address phase
  - One or more data phase
Burst Transfer Mechanism

- Assert REQ
- GNT granted
- Wait for current transaction to end
- Assert FRAME
- Transfer data when both TRDY and IRDY are asserted
- De-assert FRAME during last data phase
Timing Diagram for a basic Read operation

CLK
FRAME#
AD
C/BE#
IRDY#
TRDY#
DEVSEL#

ADDRESS
DATA-
ADDRESS PHASE
DATA PHASE
DATA TRANSFER
DATA PHASE

WAIT
DATA TRANSFER
WAIT
DATA TRANSFER
WAIT
DATA TRANSFER

BUS TRANSACTION
Various read transaction

- Single cycle Read
- Burst data read
- Read with no wait states
- Byte Enables can be changed for every data cycle
- Data Cycle with NO byte enables.
Introduction to the PCI Interface

PCI Local Bus

Basic Write Operation
Transaction termination

- Last data phase completes when
  - !FRAME and TRDY (normal - master)
  - !FRAME and STOP (target termination)
  - !FRAME and Device Select Timer expires (Master abort)
  - !DEVSEL and STOP (Target abort)
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PCI Local Bus

Multiple bus

- PCI to PCI bridge
- Concept of LOCK
- All on one level
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