Ice Packs for Red Hot CMOS Power Amplifiers

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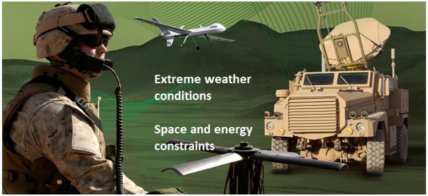
11 March, 2016

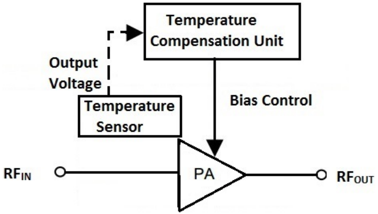
Motivation

- Power amplifiers are the last component in a RF transmitter chain for radar and telecommunication equipments.
- High efficiency and gain are highly commercially important parameters.
- Applications such as wireless communication devices have limited battery. Keeping the efficiency high would provide a better battery life.
- For military application scenarios it is important to maintain the same performance for electrical circuits across wide temperature ranges.



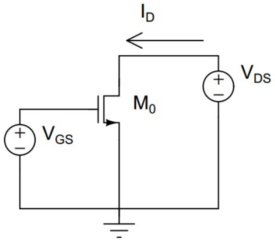
Problem description

- Power Amplifiers (PA) are high power devices which lead to significant rise in temperature due to high power dissipation.
- Temperature rise affects the MOS transistor drain current and transconductance which in turn degrades PA characteristics like gain, linearity and efficiency.



Block diagram of temperature compensation method

- A temperature compensation unit makes the PA characteristics independent of heating.
- Compensation unit can either be feedback based or non-feedback based. A temperature sensor can be used for feedback based control.

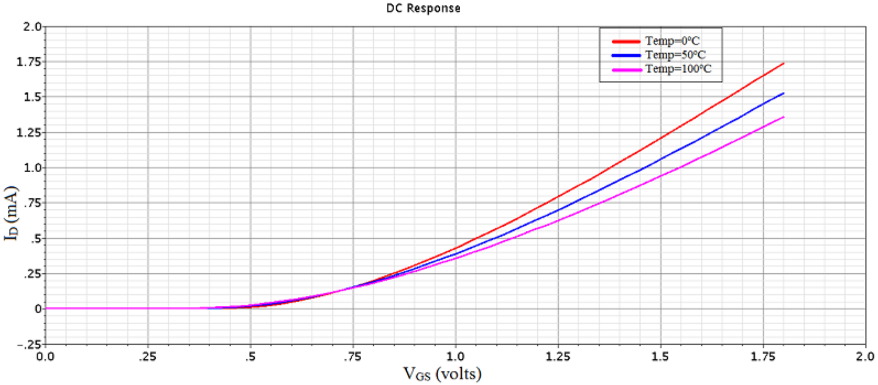


- Drain current in saturation

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2$$

- Mobility dependence on temperature $\mu = \mu_0 (\frac{T}{T_0})^{-m}$ where $m \approx 1.5$.
- Threshold voltage dependence on temperature - $V_{TH} = V_{TH_0} + \chi(T - T_0)$ where $\chi \approx -1 mV/^\circ C$.

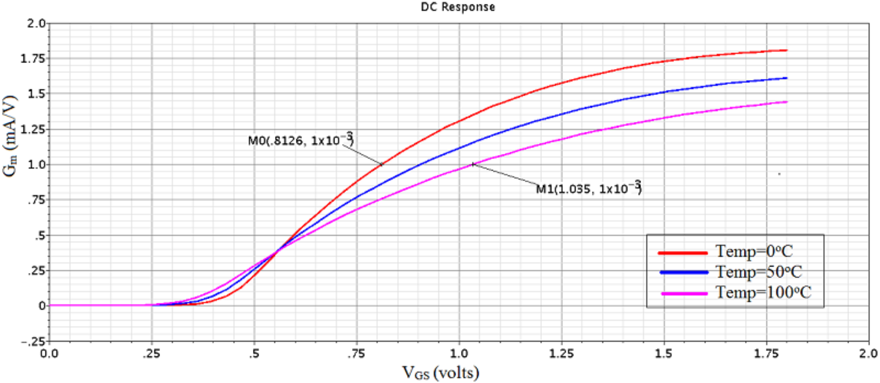
Drain current dependence on temperature



I_D versus V_{GS} with temperature varying from 0 to 100°C

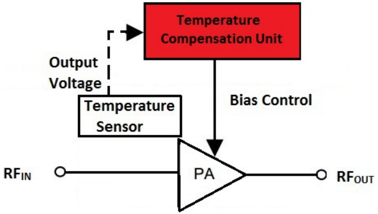
- For very small values of $(V_{GS} - V_{TH})$, I_D increases with increase in temperature and for high values of $(V_{GS} - V_{TH})$, I_D decreases with increase in temperature.
- There exists a point where $\frac{\partial I_D}{\partial T} = 0$(*Drain current is independent of temperature variations*).

$$V_{GS} = V_{TH} - \frac{\chi T}{0.75}$$



G_m versus V_{GS} with temperature varying from 0 to 100°C

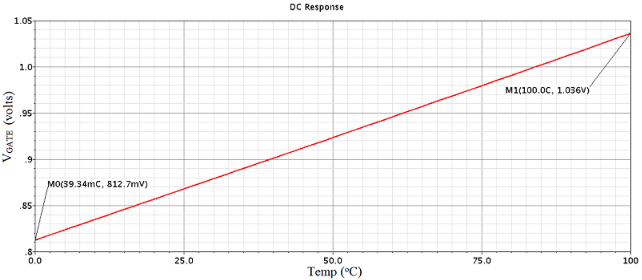
- A similar trend is seen in ac transconductance. For small values of $(V_{GS} - V_{TH})$, G_m increases with increase in temperature and for high values of $(V_{GS} - V_{TH})$, G_m decreases with increase in temperature.
- In order to stabilize PA gain within a temeperature range G_m must be constant.
- Consider a constant G_m of $1mA/V$. V_{GS} must vary from $0.8126V$ at $0^\circ C$ to $1.035V$ at $100^\circ C$.



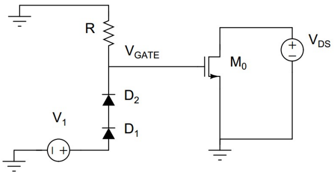
Block diagram of temperature compensation method

- It is now clear that the temperature compensation unit can stabilize the PA gain by changing gate bias voltage from $0.8126V$ at $0^\circ C$ to $1.035V$ at $100^\circ C$.
- So how can one design a circuit that changes its output voltage as a function of temperature?
- **Case 1**:*(No Feedback)* Use some temperature sensitive devices like diodes, BJTs, MOSFETs.
- **Case 2**: *(Feedback from Temperature Sensor)* Temperature sensor output is a voltage/current indicating the temperature. This signal can be used to generate the desired variation in bias voltage either by using an external microcontroller or some on chip circuit.

Method 1: Gate bias control using diodes and resistors

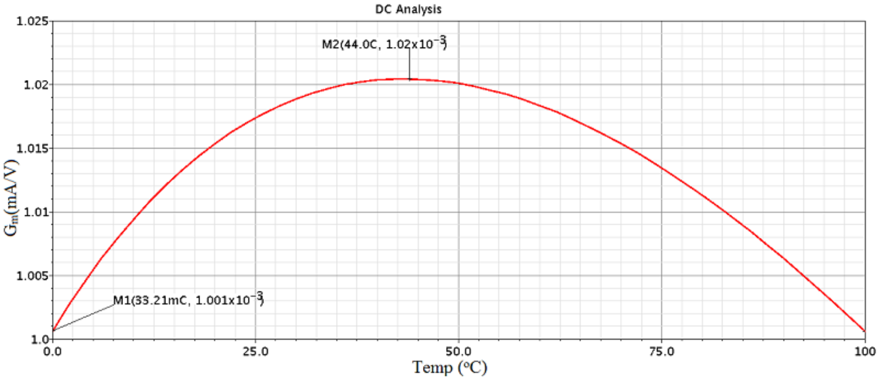


V_{GATE} versus temperature varying from 0 to 100°C



- As the temperature rises, voltage drop across diode reduces and V_{GATE} increases almost linearly with temperature.
- To maintain constant $G_m = 1mA/V$, V_{GATE} varies from $0.8127V$ to $1.036V$.

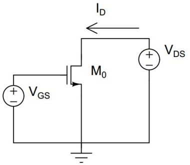
Ref: K. Yamauchi, Y. Iyama, and M. Yamaguchi, "X -Band MMIC power amplifier with an on-chip temperature compensation circuit,*IEEE Tran. Micr. Theory and Techniques*, 2001.

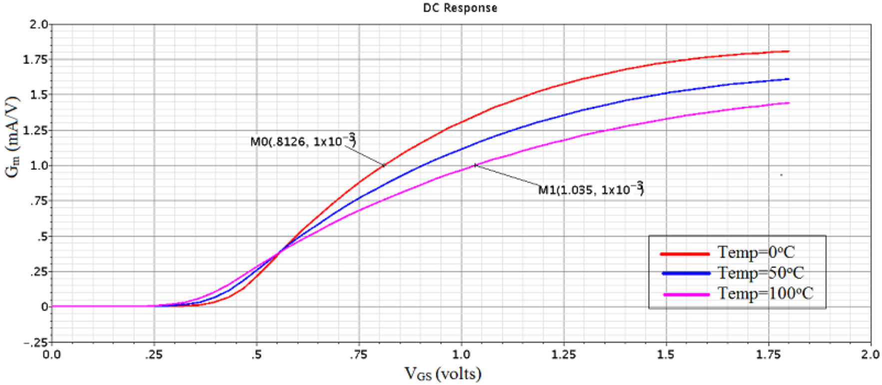


G_m versus temperature varying from 0 to 100°C(with compensation)

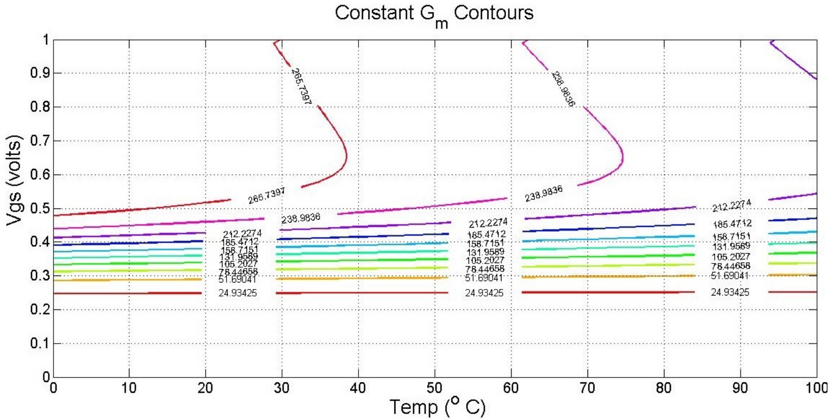
- The variation in G_m is reduced from 27.5% (without compensation) to 1.88% (with compensation) within temperature range 0 to 100°C.

Can we reduce it even further?? (Constant Gm contours)





I_D versus V_{GS} with temperature varying from 0 to 100°C

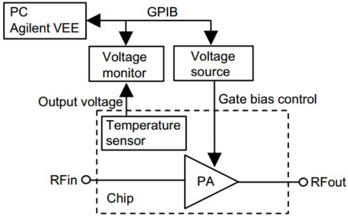


Constant G_m contours on V_{GS} versus temperature plot in 45 nm CMOS Predictive Technology Model

- For very high values of G_m it may not be possible to maintain a constant G_m for any V_{GS} over entire temperature range.
- For $G_m = 185\mu A/V$ the following quadratic equation gives an optimal solution.

$$V_{GS} = 3.45 * 10^{-6} * T^2 + 4.545 * 10^{-4} * T + 0.3927$$

Method 2: Temperature sensor based feedback control of gate bias voltage

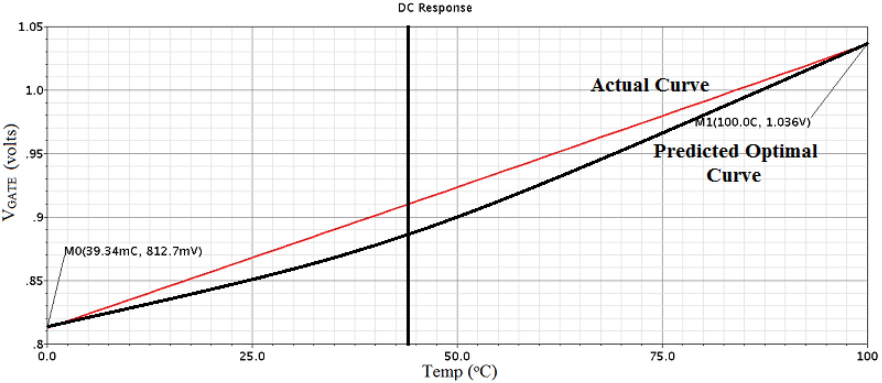


Block diagram of temperature compensation unit

- A temperature sensor senses the on chip temperature in vicinity of PA.
- Microcontroller generates a corresponding bias control voltage depending on output of temperature sensor to stabilize G_m using the optimal quadratic function.
- One drawback is that there is a need for a microcontroller to perform the compensation. Can it been done using some circuit technique??

Ref: T. Yoshida et al., "CMOS power amplifier with temperature compensation for 79 GHz radar system, *Asia-Pacific Microw. Conf. Proceedings*, 2013.

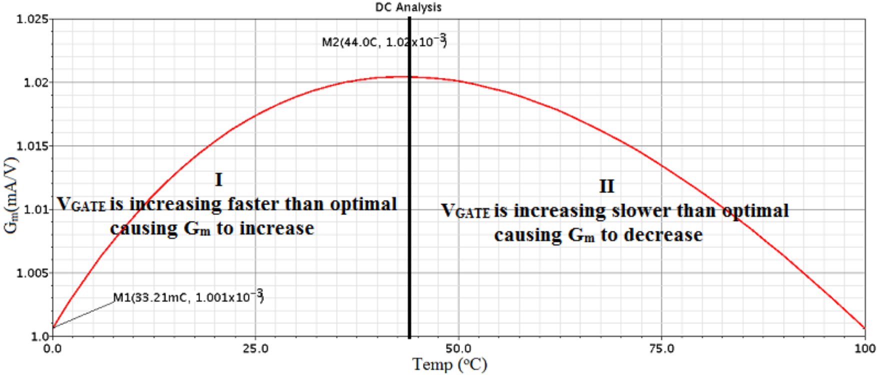
Summary of Methods 1 and 2



V_{GATE1} versus temperature with compensation of Method 1

- Method 1 implements a linear bias control voltage which is not an optimal solution.
- Method 2 implements a quadratic bias voltage control but requires microcontroller for the same.

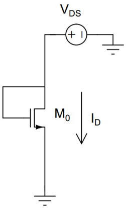
Summary of Methods 1 and 2



G_m versus temperature varying from 0 to 100°C(with compensation of Method 1)

- In method 1 bias voltage varies linearly with temperature.
- V_{GATE1} increases faster than it should from 0 to 44°C causing G_m to increase with temperature.
- V_{GATE1} increases slower for the remaining temperature range causing G_m to decrease with temperature.

Proposed temperature compensation method using MOS diode and resistor



MOS Diode

- In this technique MOS as a diode is used to implement an on chip quadratic bias voltage. Simulations are done in UMC 180nm CMOS technology.
- In saturation MOS current does not show quadratic relation with temperature and can not be used for implementing bias voltage.

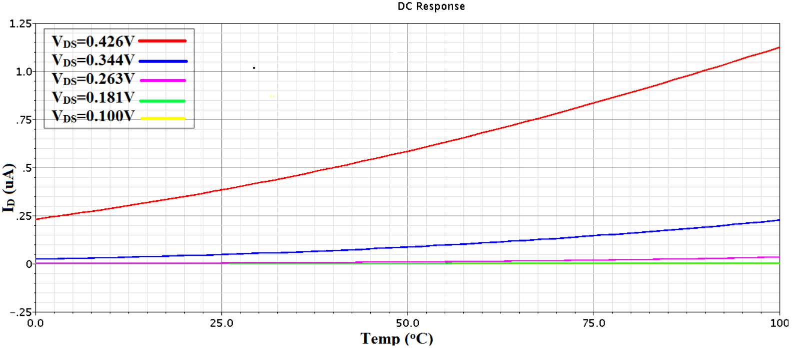
$$\frac{\partial I_D}{\partial T} = -I_D \frac{1.5}{T} - \frac{2 I_D \chi}{V_{GS} - V_{TH}}$$

- Drain current equation in subthreshold is given as

$$I_D = I_0 exp(\frac{V_{GS} - V_{TH}}{nV_T})[1 - exp(\frac{-V_{DS}}{V_T})]$$

where $I_0 \propto T^2$ and $V_T = kT/q$.

Proposed temperature compensation method using MOS diode and resistor



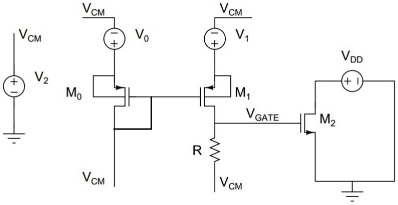
I_D versus temperature in subthreshold region

- V_{DS} is small and the second term is neglected. Using Taylor series expansion for exponential term and neglecting higher order terms,

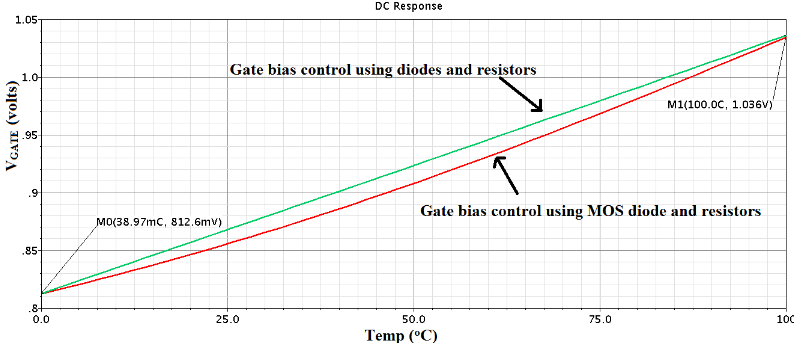
$$I_D = I_0\left(1 + \frac{V_{GS} - V_{TH}}{nV_T} + \frac{1}{2}\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)^2\right)$$

- The first term shows a square law relationship with temperature. So it is possible to get square law relation from MOS diode in subthreshold region.

Proposed temperature compensation method using MOS diode and resistor

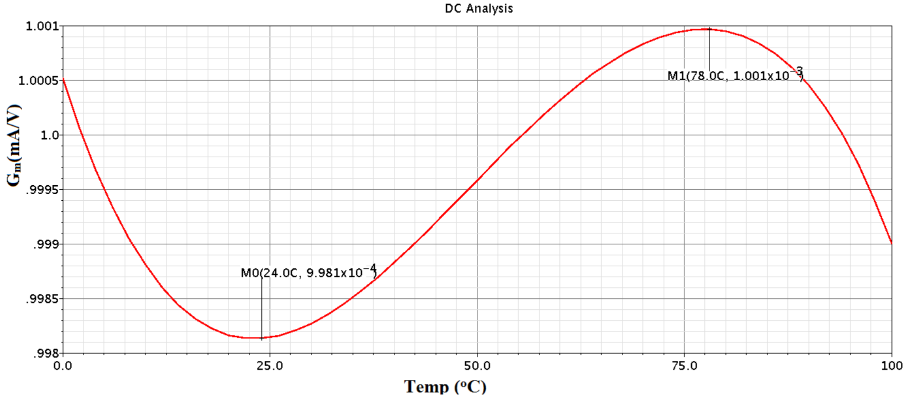


Proposed circuit



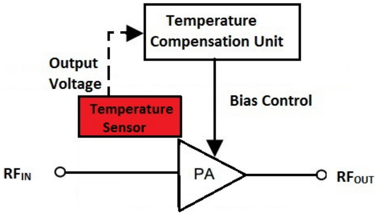
V_{GATE} versus temperature

Proposed temperature compensation method using MOS diode and resistor



G_m versus temperature varying form 0 to 100$^\circ C$.

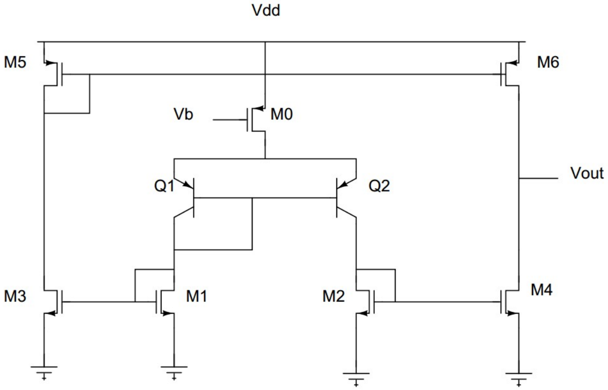
- G_m variation versus temperature is only 0.29% over the entire temperature range.
- As compared to method 1(1.88% variation), variation in G_m has reduced by 6.5 times.
- It shows a promising nearly optimal solution for on chip temperature compensation.



Block diagram of temperature compensation method

- The circuit technique discussed previously is a good biasing circuit but it will be difficult to control the gain after fabrication.
- We wish to explore feedback based approach using the temperature sensor.
- Advantages of using a temperature sensor -
  i. Measures the on chip temperature.
  ii. Estimates the PA power dissipation non invasively.
  iii. May be used to predict characteristics like efficiency and 1-dB compression point.

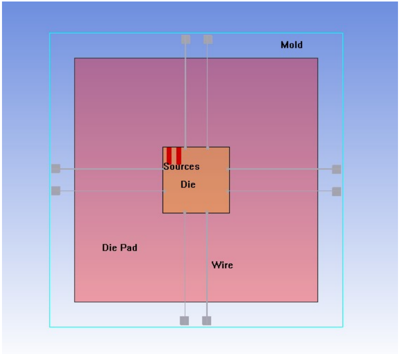
Differential temperature sensor



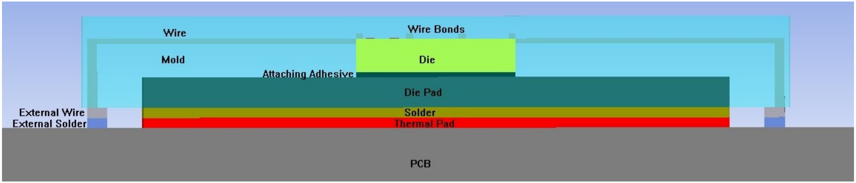
Schematic Diagram

- This sensor has been widely implemented in the past for the purpose of on chip temperature sensing of PAs due to its high sensitivity.
- How do you perform simulations for this circuit ??

Ref: J. L. Gonzlez, B. Martineau, D. Mateo, and J. Altet, "Non-invasive monitoring of CMOS power amplifiers operating at RF and mmW Frequencies using an on-chip thermal sensor, *Dig. Pap. - IEEE Radio Freq. Integr. Circuits Symp.*, 2011.

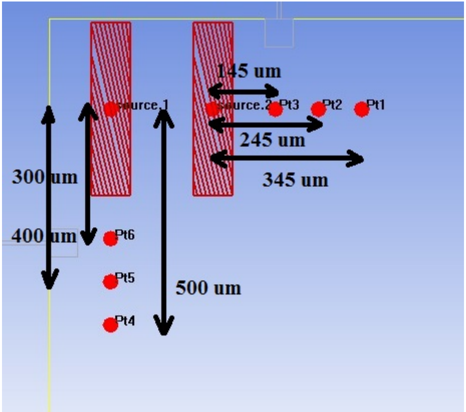


QFN package (top view)



QFN package (side view)

Measuring power dissipation in **ANSYS Icepak**

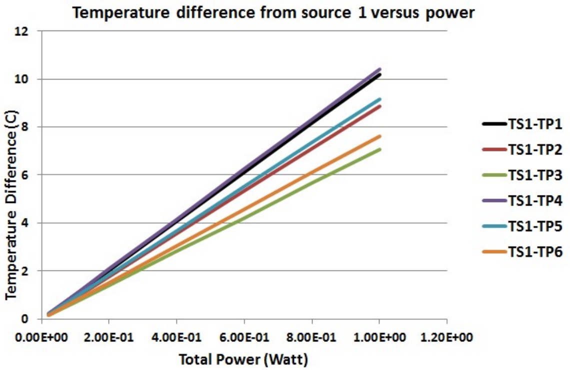


Points where temperature is being monitored

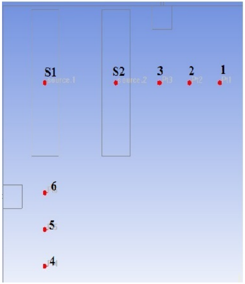
- The two sources represent two separate power amplifiers.
- Separate points to measure temperature are chosen to see the effect of temperature sensitivity versus distance from source.
- The power in each of the sources is changed from 10mW to 0.5W.

Power (Watt)	TS1	TS2	TP1	TP2	TP3	TP4	TP5	TP6
2.00E-02	31.3724	31.3394	31.1687	31.1949	31.2311	31.1642	31.1889	31.22
1.00E-01	48.862	48.6969	47.8434	47.9743	48.1554	47.8212	47.9447	48.1
2.00E-01	70.724	70.3937	68.6868	68.9486	69.3109	68.6424	68.8894	69.1998
4.00E-01	114.448	113.787	110.374	110.897	111.622	110.285	110.779	111.4
6.00E-01	158.172	157.181	152.06	152.843	153.993	151.927	152.668	153.599
8.00E-01	201.896	200.575	193.747	194.794	196.243	193.57	194.55	195.799
1.00E+00	245.62	243.97	235.43	236.74	238.55	235.212	236.447	237.999

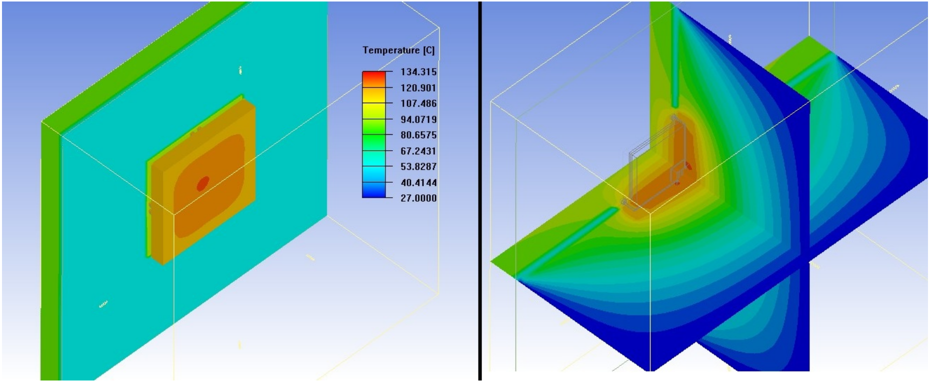
Table: Temperature at monitor points for different source powers



Monitor Point	Sensitivity (C/Watt)
Point 1	10.2
Point 2	8.88
Point 3	7.07
Point 4	10.4
Point 5	9.17
Point 6	7.62



Icepak simulation- temperature profile on chip



- The two figures show temperature contours on the chip and PCB for a specified power.

Thank You

Questions?