A Novel SRAM-Noise-Margin Analysis Technique

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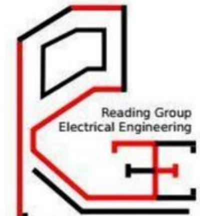

Outline

- Motivation
- SRAM
- Proposed method
- Validation
- Application
- Conclusion

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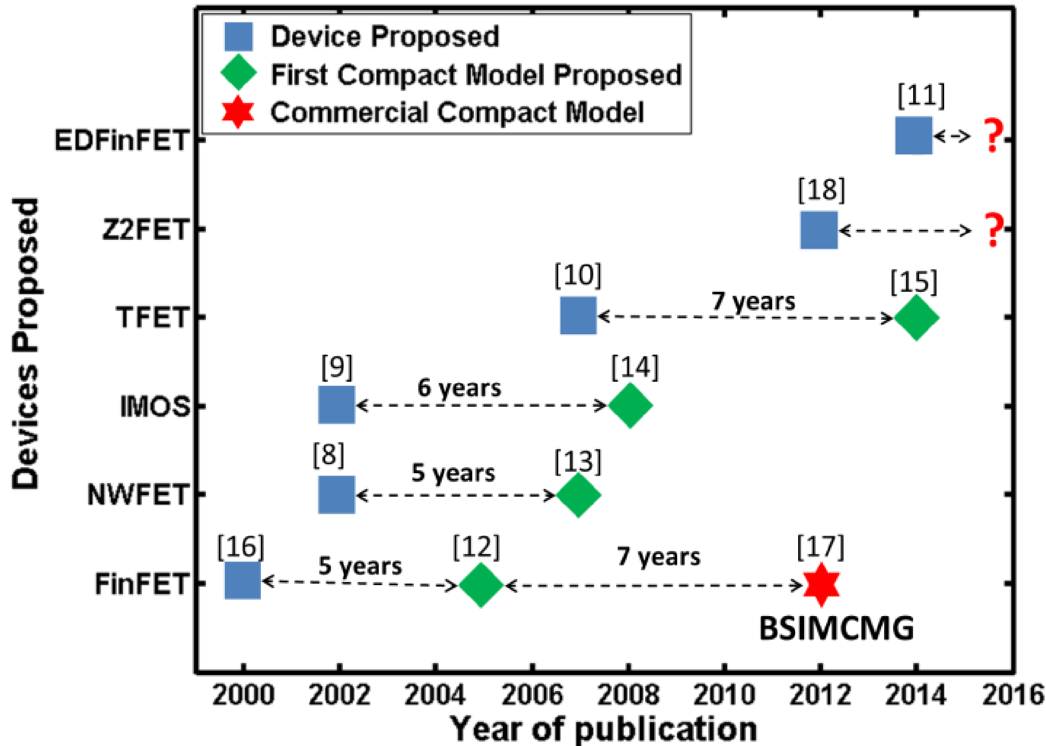
Motivation

- Benchmarking New proposed devices.
  - Device level (σV_T, I_{ON}, SS)
  - Circuit level (SRAM-SNM)
- SPICE simulations with Compact model: [1]
  - Compact model needed.
- Full TCAD mix-mode simulation:[2]
  - Time consuming , Computationally expensive

1. T. Hiramoto, *et. al*. "Direct Measurement of Correlation Between SRAM Noise Margin and Individual Cell Transistor Variability by Using Device Matrix Array," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2249–2256, Aug. 2011
2. V. P.-H. Hu, *et. al*. "FinFET SRAM Cell Optimization Considering Temporal Variability Due to NBTI/PBTI, Surface Orientation and Various Gate Dielectrics," *IEEE Trans. Electron Devices*, vol. 58, no. 3, pp. 805–811, Mar. 2011

Motivation



* References for data points are not shown

- 4+ years needed for compact model after device proposal.
- Further 4+ years needed for commercial models.
- **Need of new method.**

Outline

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- **SRAM**
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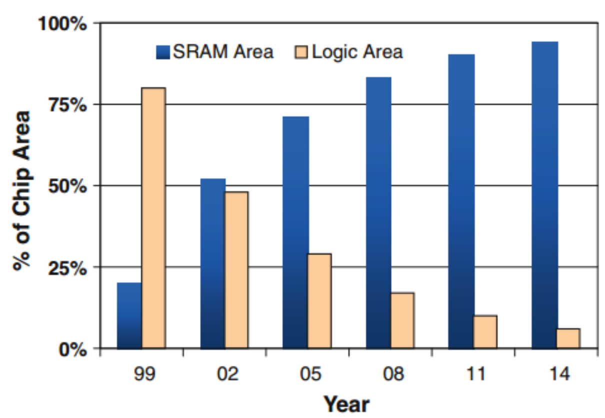
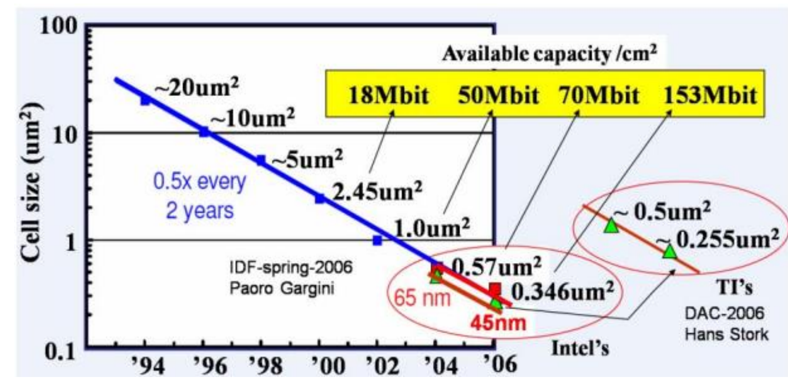
SRAM - Importance

- SRAM consumes 90% area of SoCs and microprocessors. [1]
- To increase memory density, SRAM bitcell area is reduced 50% each technology node. [2]
- Aggressively scaled devices → more variability → less SNM → higher instability

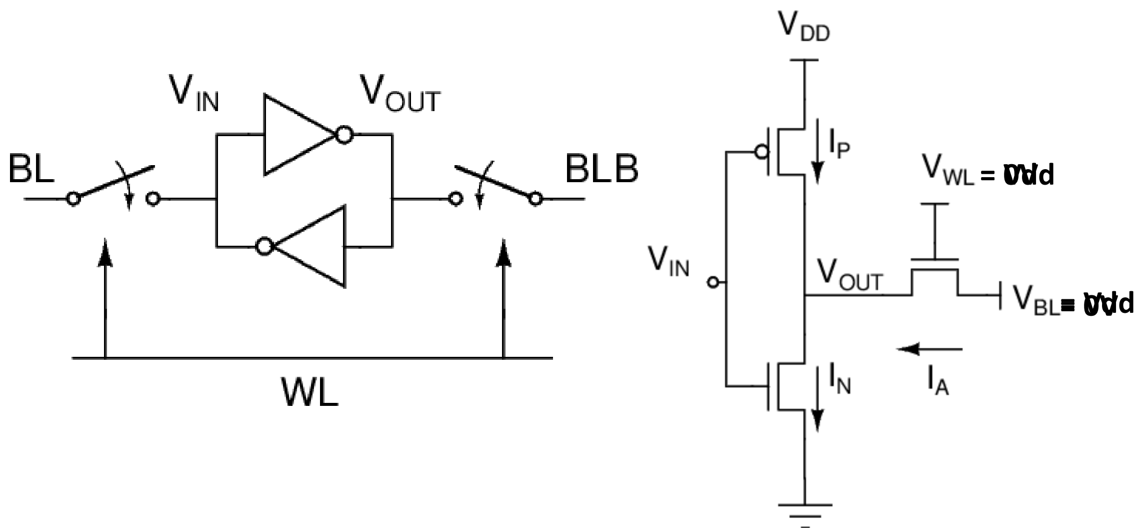


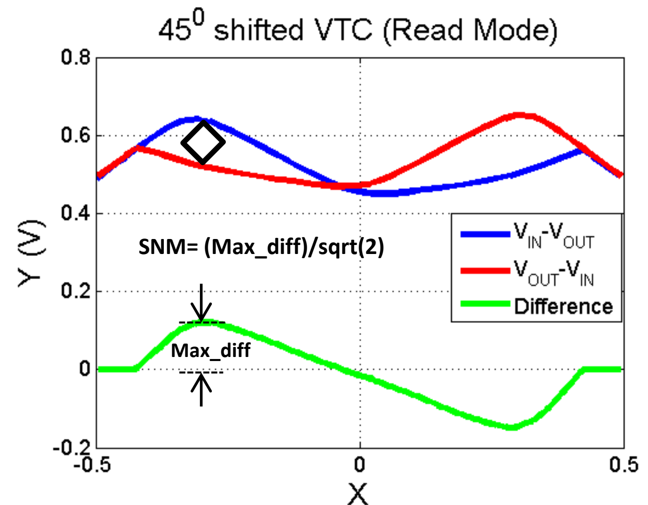


1) A. Allan, D. Edenfeld, W. H. Joyner, A. B. Kahng, M. Rodgers, and Y. Zorian, "2001 technology roadmap for semiconductors," *Computer (Long. Beach. Calif).*, vol. 35, no. 1, pp. 42–53, Jan. 2002
2) Hiroyuki Yamauchi, "Embedded SRAM circuit design technologies for a 45nm and beyond," in *2007 7th International Conference on ASIC*, 2007, pp. 1028–1033.

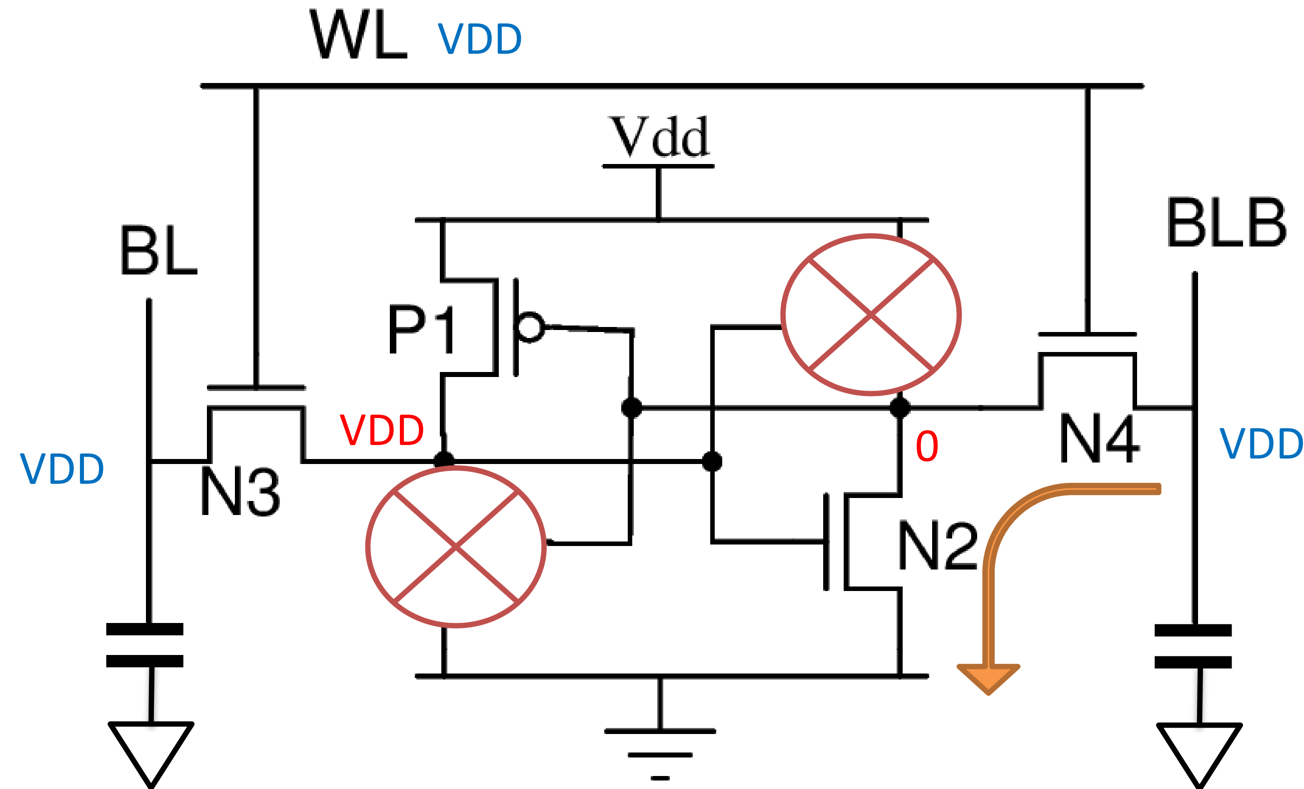
SRAM - Basics

- **SRAM**: Cross coupled CMOS inverters with two access transistor.
- **SNM**: "Minimum noise voltage needed to flip the state."
- **Getting SNM** – Square fit method
- **Modes of operation →**
  - **Hold Mode:** V(BL) = V(BLB) = V(WL) = 0V
  - **Read Mode:** V(BL) = V(BLB) = V(WL) = V_{DD}
  - **Write Mode:** V(WL) = $V_{DD,}$ V(BL) = ~V(BLB)





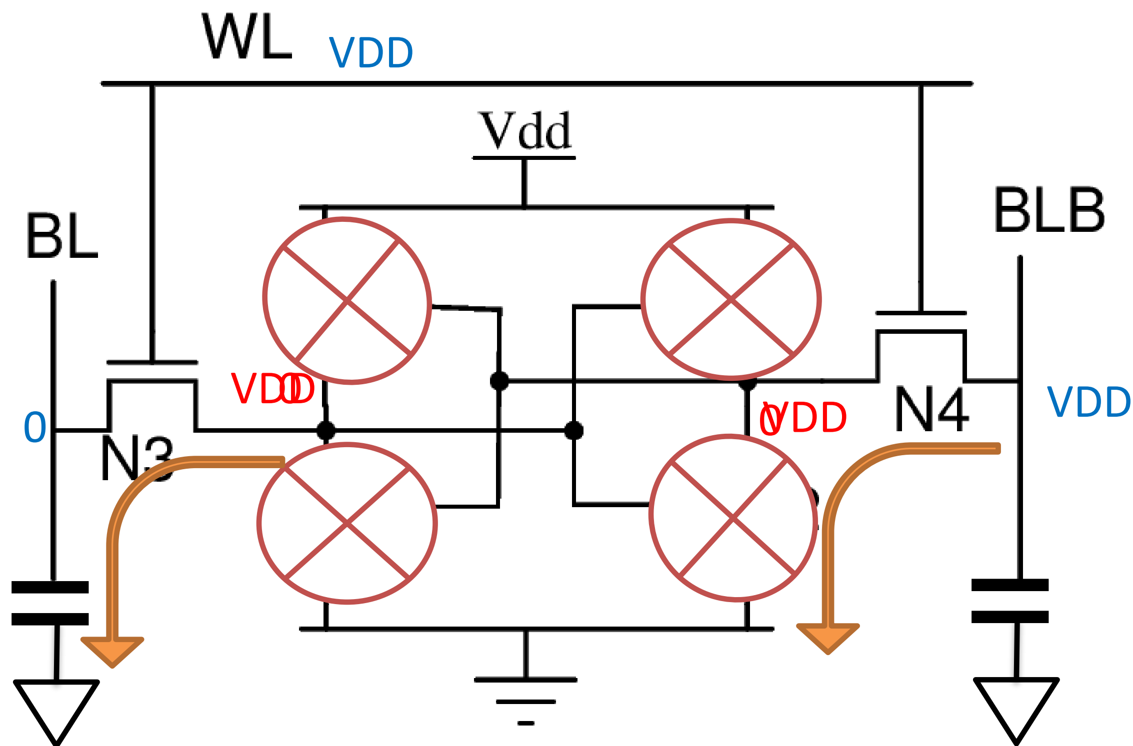
SRAM Basics – Read mode



- P_2,N_1 in Cut off.
- P_1 and N_2 in Linear
- Pre-charge C_{BL}, C_{BLB} to VDD.
- WL = VDD, turns on access transistors.
- $I(N_3) = 0$.
- $V(N_2)$ starts increasing.
- Pull down should be stronger than access transistor.
- Sense amplifier compares values and gives stored value.

→ Non Destructive Read operation: (WL = BL = BLB = VDD)

SRAM Basics – Write mode



- P_2,N_1 in Cut off.
- P_1 and N_2 in Linear.
- Pre-charge C_{BLB} to VDD.
- WL = VDD, turns on access transistors.

- V_{P1} discharges through N3 and turns on P2.
- VN2 increases and turns on N1.
- New values gets stored.

- Access transistor should be stronger than pull up transistor.

→ Error less Write operation: (WL = VDD)

N > NA > P

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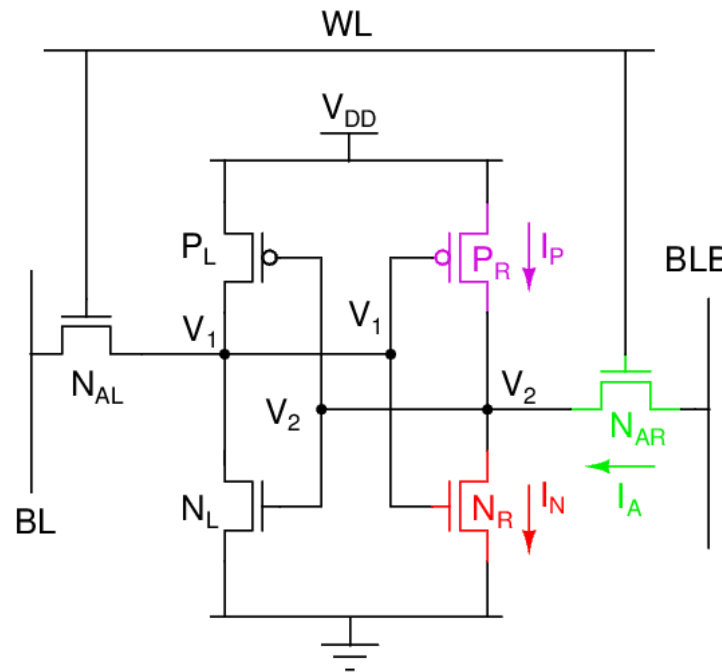
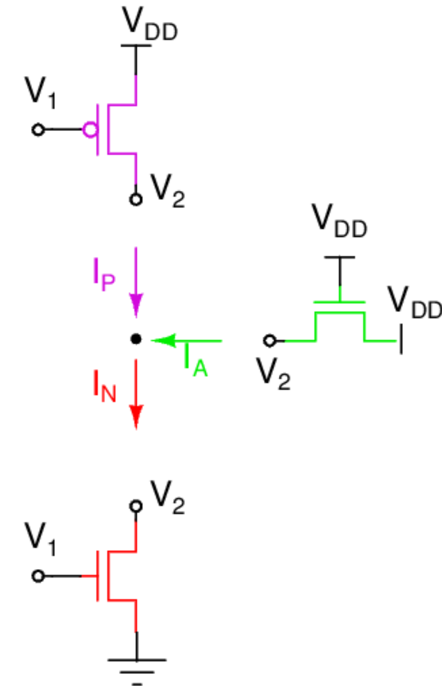
Proposed Method

- For VTC, (V_1, V_2) pairs are needed.
- Two inverters interact in terms of voltages only.
- They can be analyzed separately.
- Kirchhoff's law

  $(I_N = I_P + I_A)$

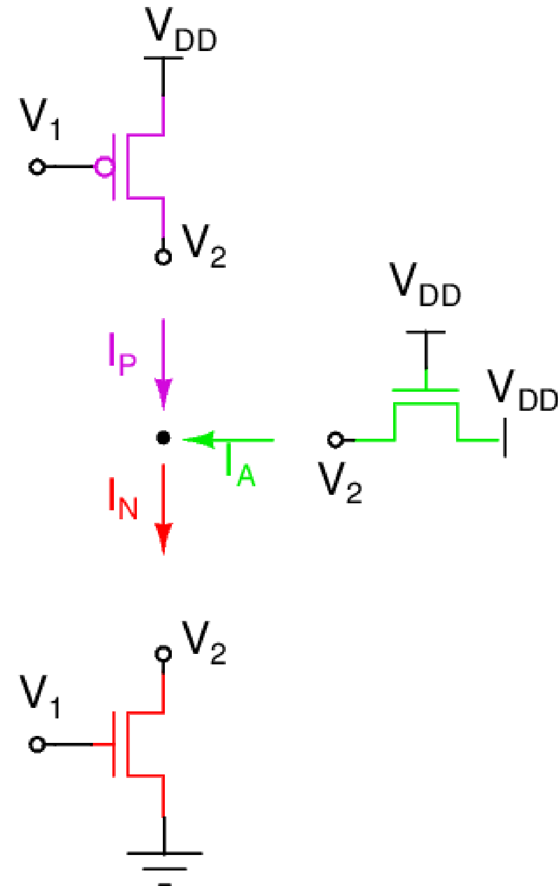




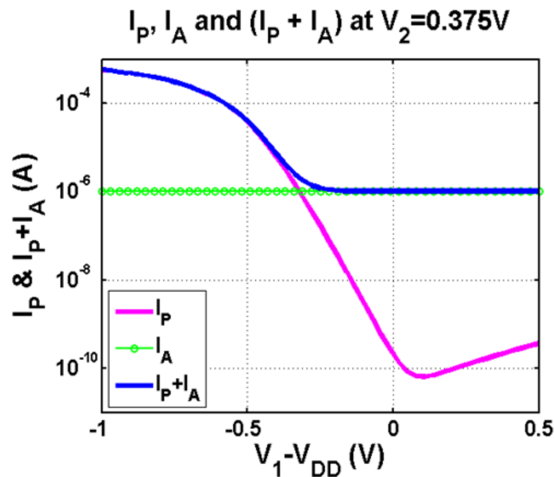
- $I_P = I\ (V_{GS}=V_1\text{-}V_{DD},\ V_{DS}=V_2\text{-}V_{DD})$ → $I_P = f\,(V_1, V_2)$
- $I_N = I\ (V_{GS}=V_1,\ V_{DS}=V_2)$ → $I_N = f\,(V_1, V_2)$
- $I_A = I\ (V_{GS}=V_{DS}=V_{DD}\text{-}V_2)$ → $I_A = f\,(V_2)$

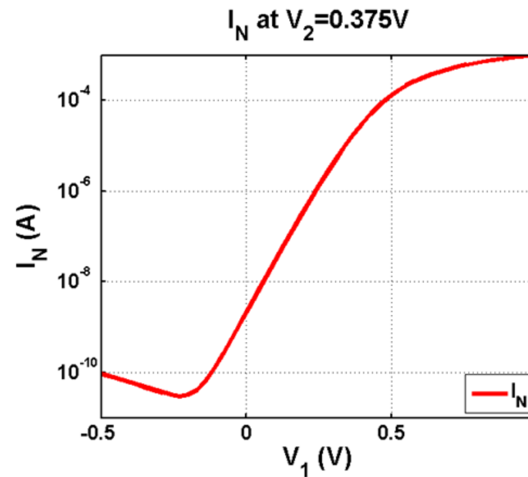
Proposed Method – Getting VTC

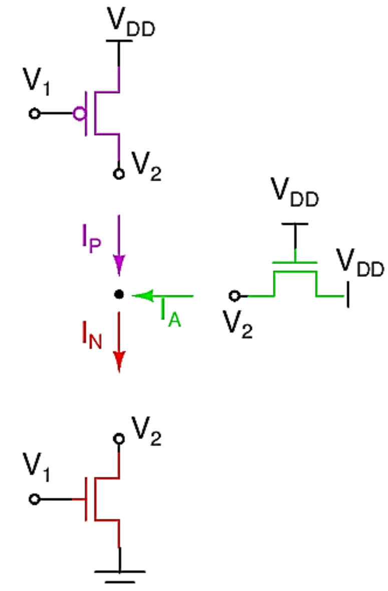
- Fix value of V_2
  - $I_P = f(V_1)$ $I_N = f(V_1)$ and $I_A = const.$
- Plot the functions
  - $[\, I_P(V_1) + I_A \,]$ and $I_N(V_1)$
- Find Value of V_1, such that
  - $[\, I_P(V_1) + I_A \,] = I_N(V_1)$ → intersection point
- Hence we get V_1 for a given V_2.
- Similarly, Get all (V_1, V_2) pairs for complete range.

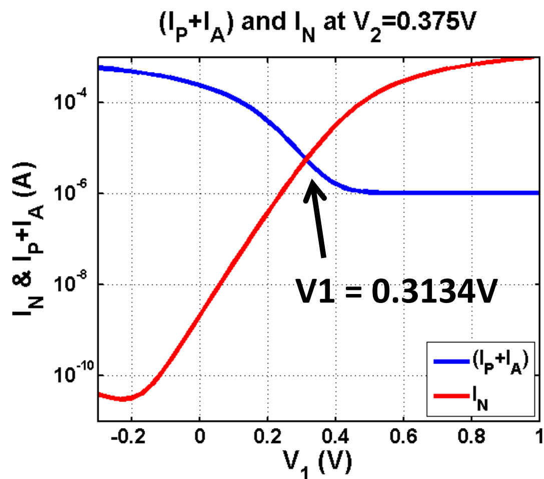


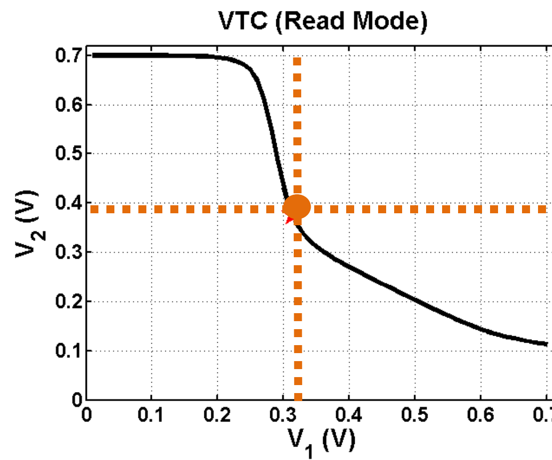
Proposed Method – Getting VTC

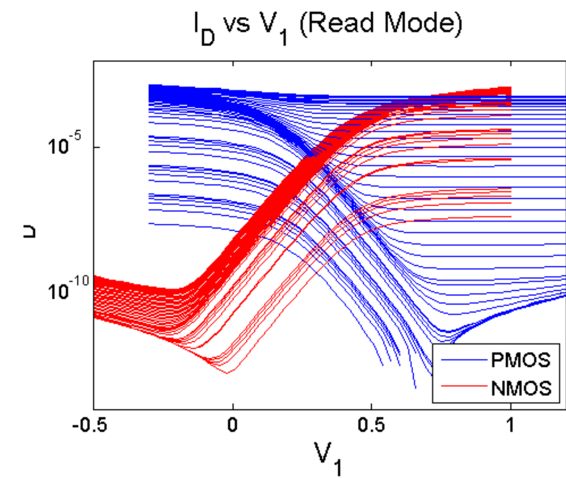






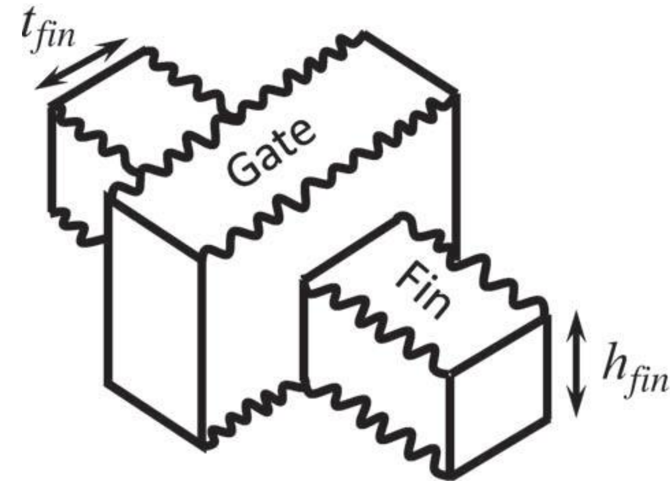






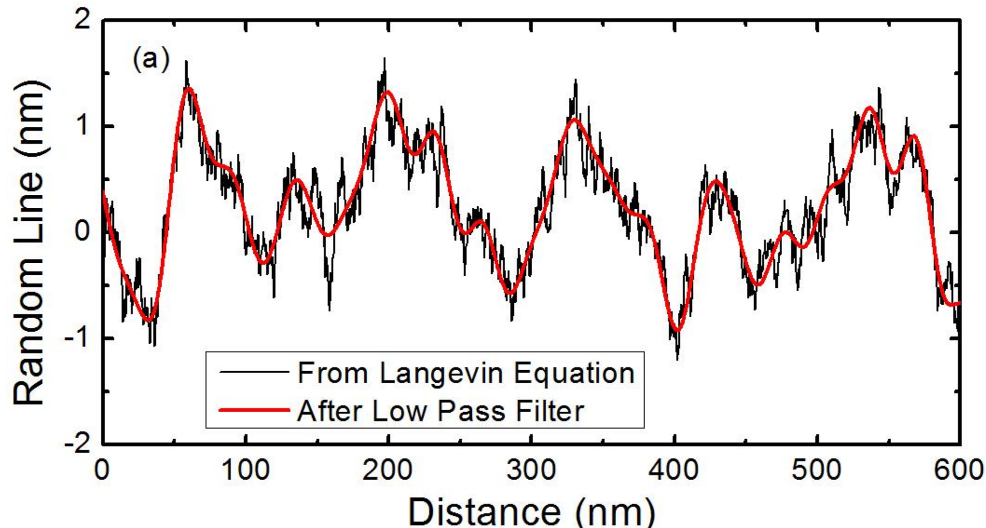
Variability Effect Study

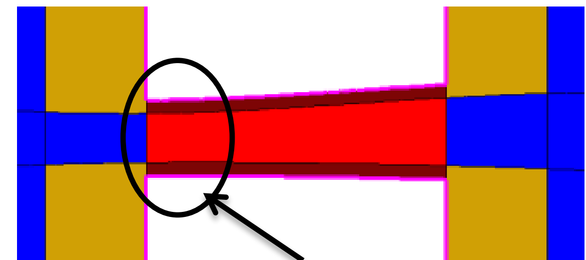
- Process variations
  - → Random Dopant Fluctuations (RDF)
  - → Line Edge Roughness (LER)
  - → Gate Edge Roughness (GER)
  - → Metal gate granularity (MGG)
- Random lines from Langevin Equation.
  - → Λ=30 nm and 3σ =2 nm.



Sketch demonstrating LER & GER in FinFET.

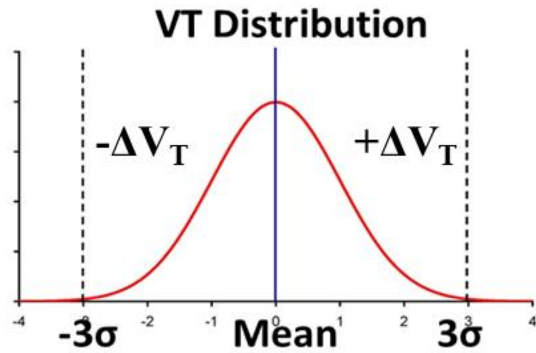
Kedar Patel, et.al. "IEEE TED VOL. 56, NO. 12, DECEMBER 2009"

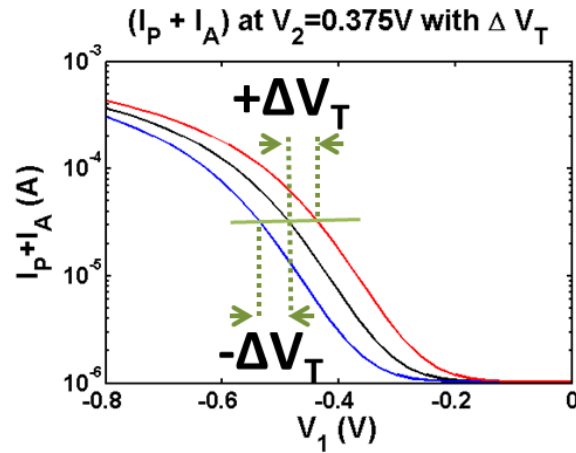


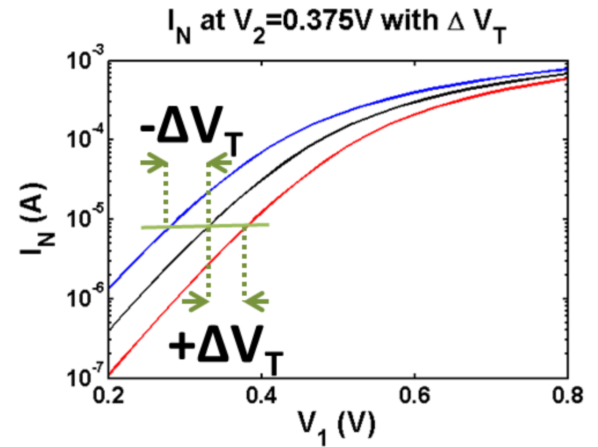


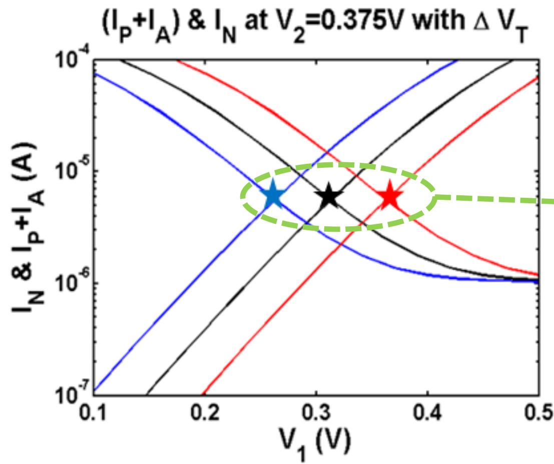
→Change in channel width due to LER.

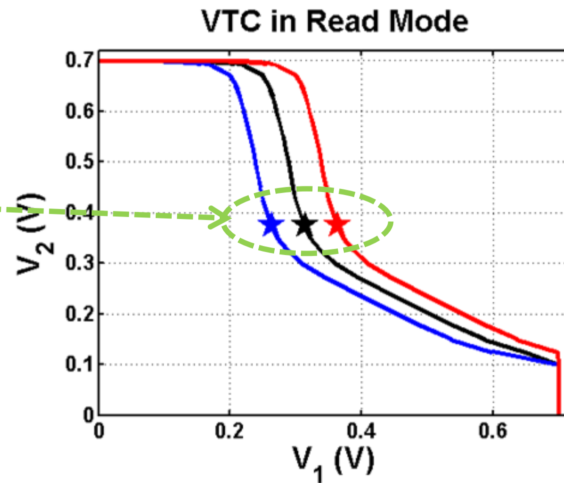
Proposed Method – Adding Variability

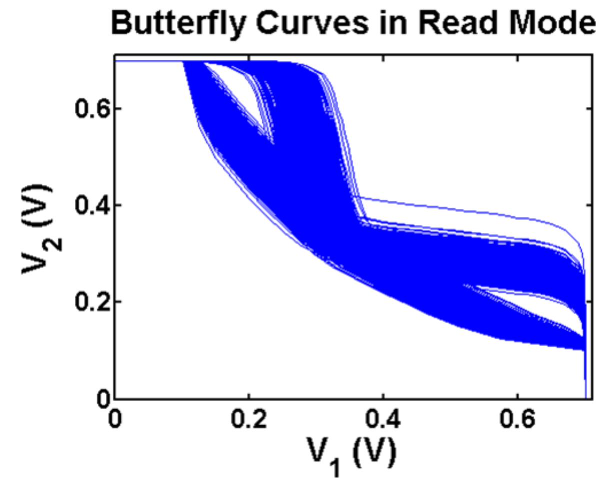




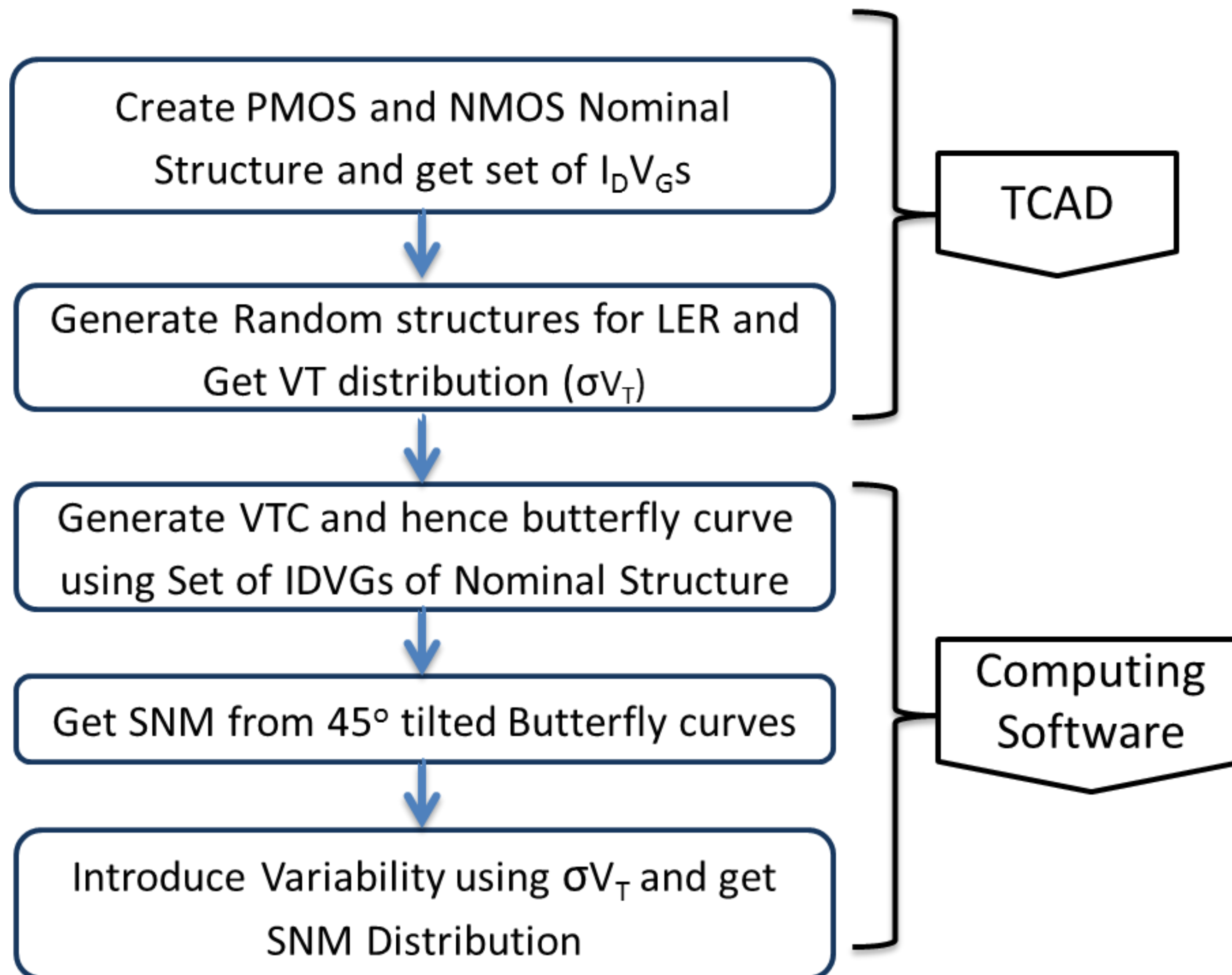








Proposed Method – Process Flow



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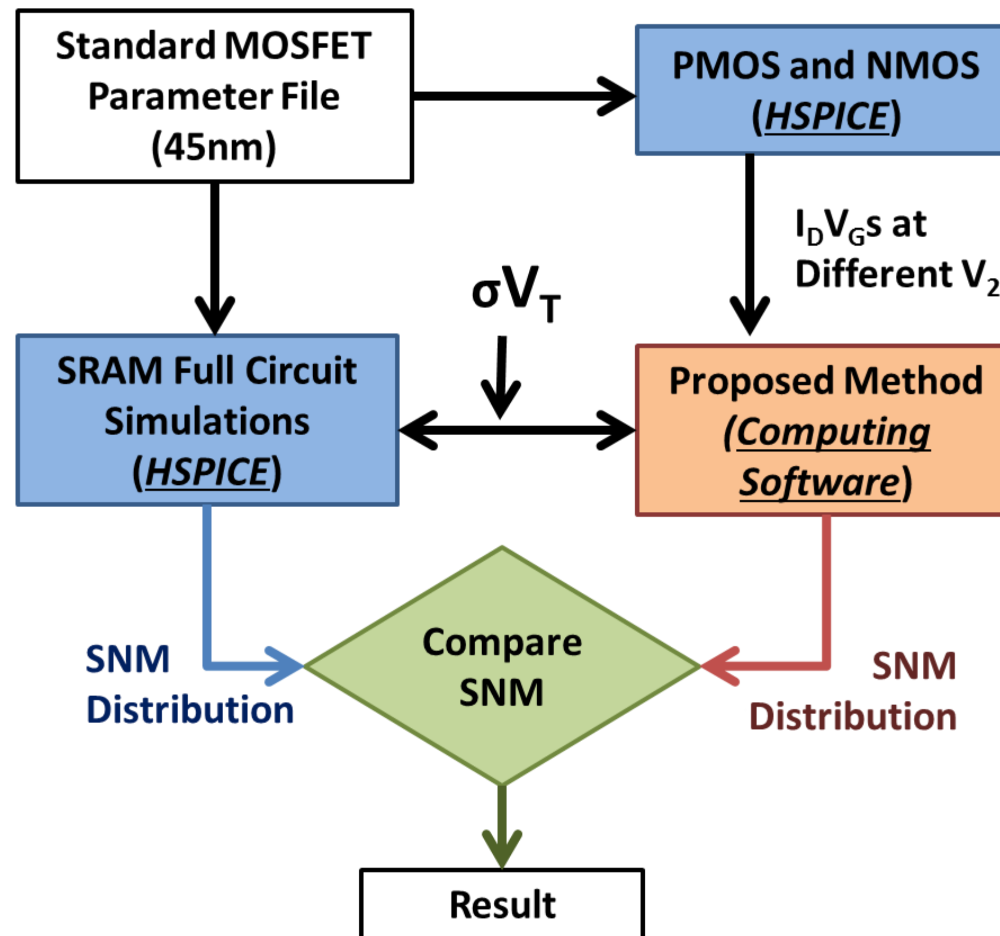
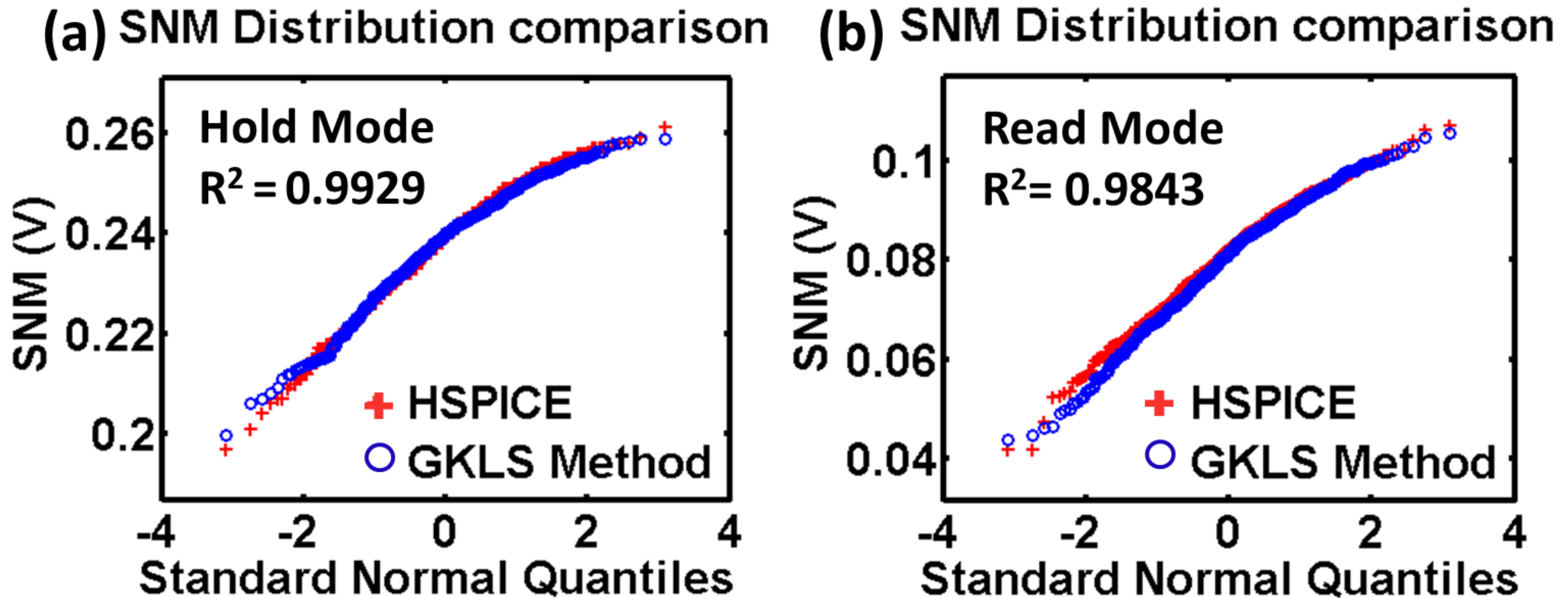
Validation of Method – Process flow



→ **Validating against industry standard HSPICE circuit simulator**

Validation - Results



*GKLS method is proposed method.

→SNM distribution matches with acceptable marginal error.

→ **Method is Validated**

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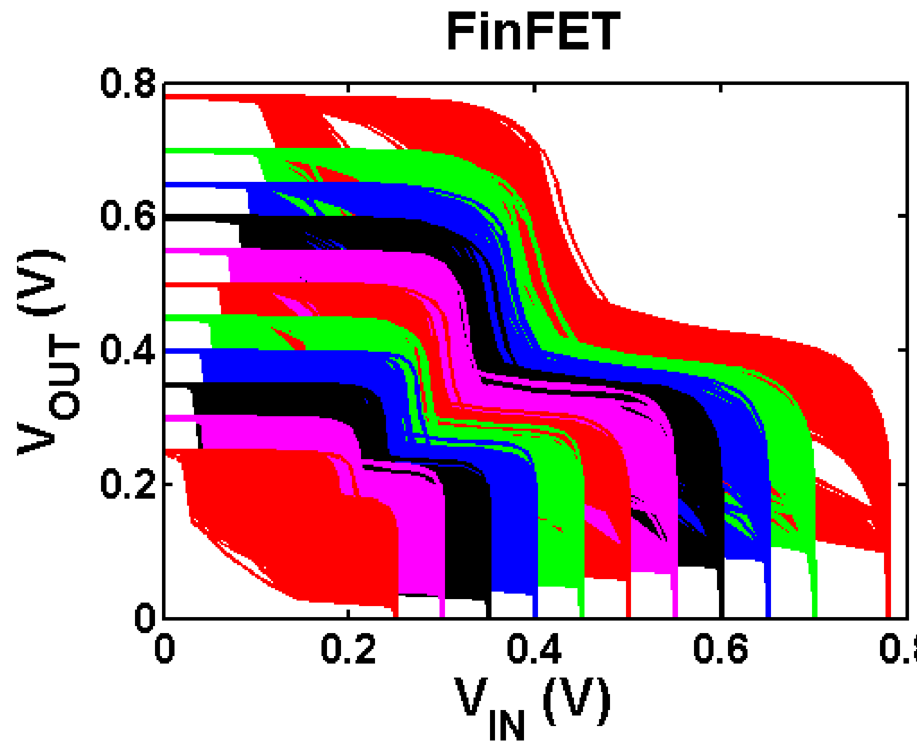
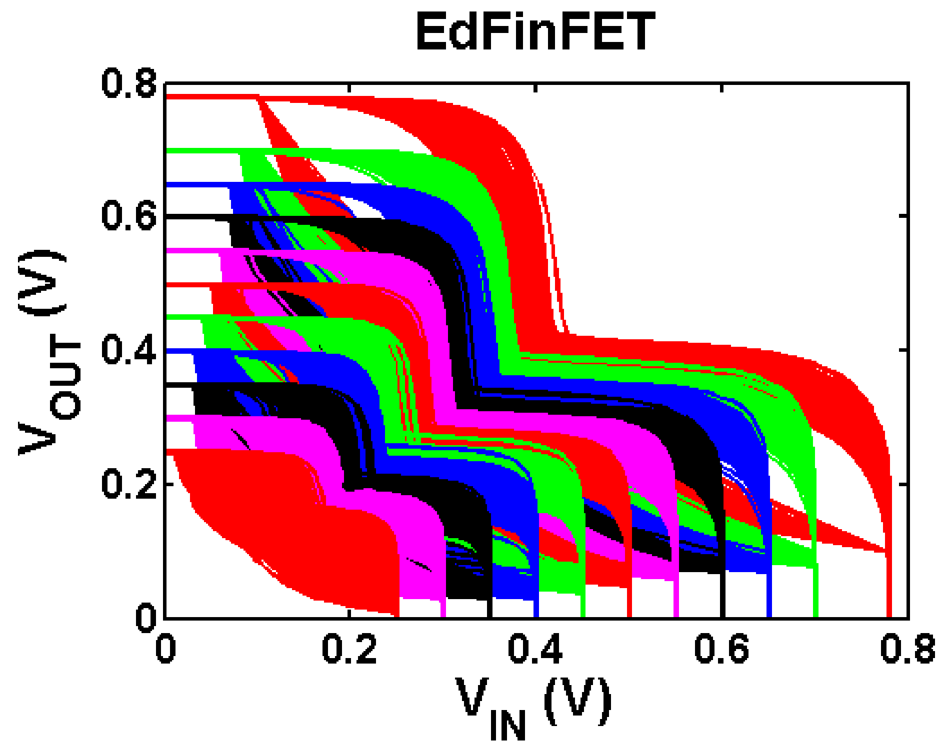
EdFinFET vs FinFET – Butterfly plots vs VDD

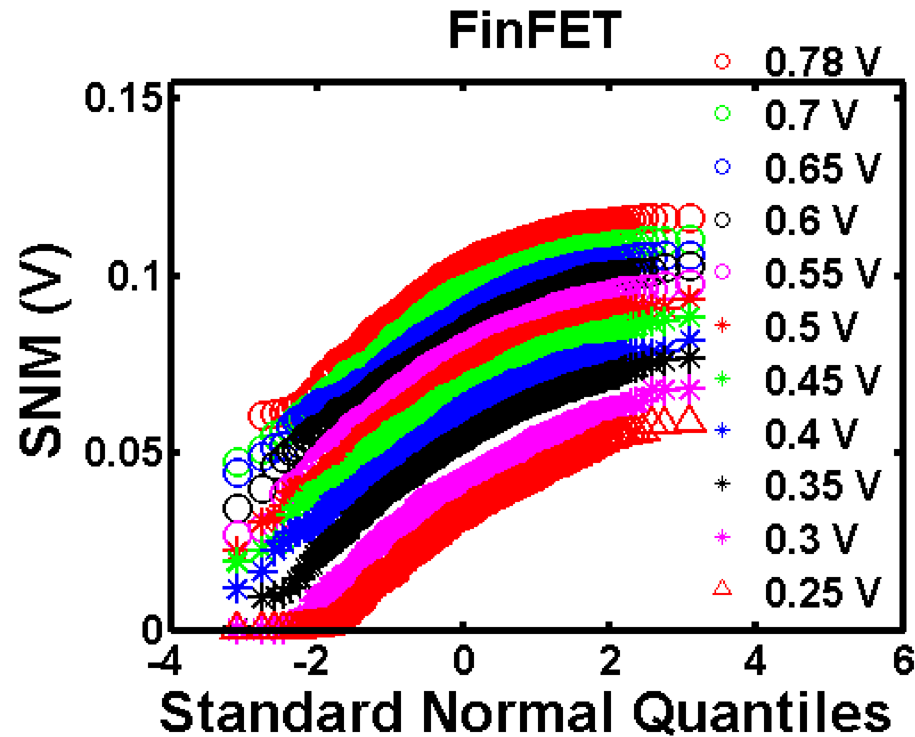


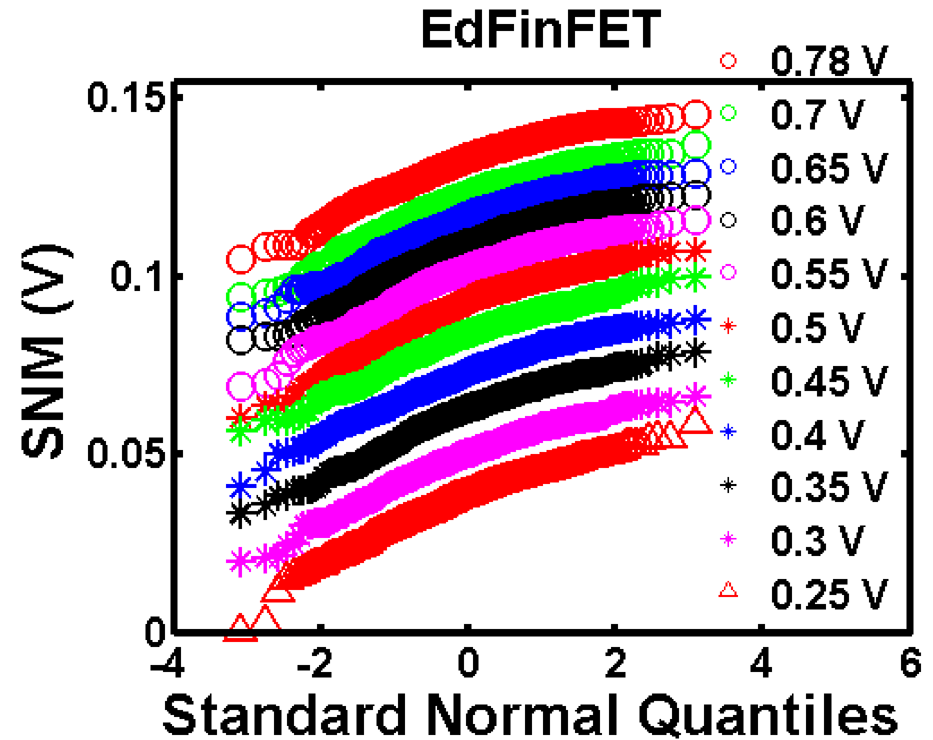


FinFET σVT = 33 mV

EdFinFET σVT = 22 mV

EdFinFET vs FinFET – SNM vs VDD

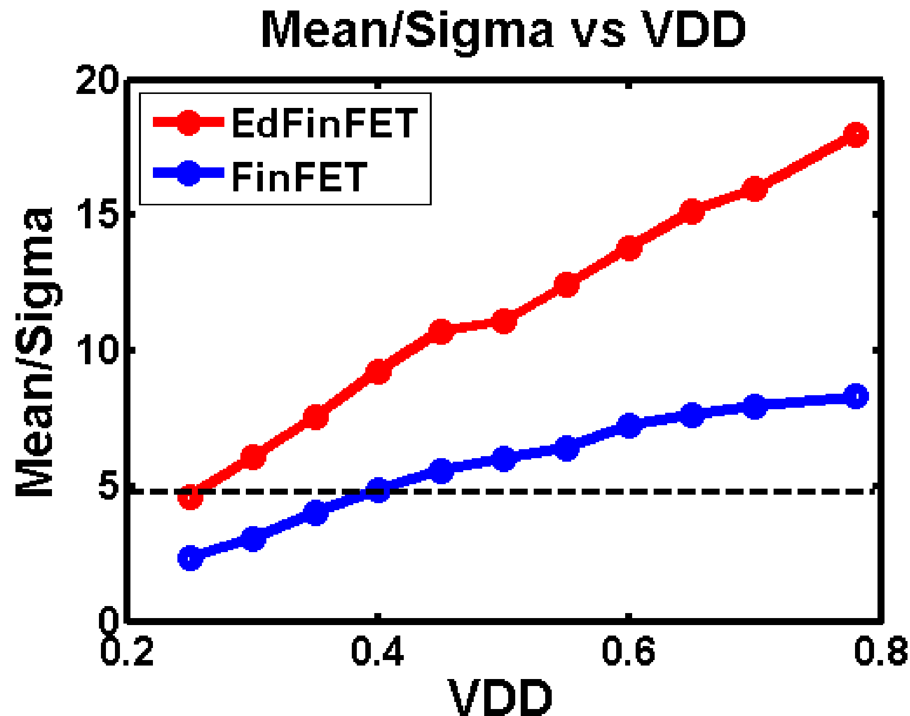




Lower SNM
Higher Variability

Higher SNM
Lower Variability

EdFinFET vs FinFET – Mean/Sigma vs VDD



Minimum allowed VDD →

EdFinFET = 0.3V

FinFET = 0.45V

→ Mean should be 5 times 1σ value for 1Mb SRAM to function [1]

→ 44% power can be saved by EdFinFET.

1) K.Fujita. *et. al.* "Advanced channel engineering achieving aggressive reduction of VT variation for ultra-low-power applications," in *Electron Devices Meeting (IEDM), 2011 IEEE International* , vol., no., pp.32.3.1-32.3.4, 5-7 Dec. 2011

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Conclusion

- Fast and accurate
- No need for compact models
- 1000X reduction in run time compared to TCAD mixed mode simulations
- EdFinFET can be used for low power applications (V_{DD}=0.3V)

THANK YOU