A Novel SRAM-Noise-Margin Analysis Technique

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Outline

- Motivation
- SRAM
- Proposed method
- Validation
- Application
- Conclusion
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Motivation

- Benchmarking New proposed devices.
  - Device level ($\sigma V_T$, $I_{ON}$, SS)
  - Circuit level (SRAM-SNM)

- SPICE simulations with Compact model: [1]
  - Compact model needed.

- Full TCAD mix-mode simulation:[2]
  - Time consuming, Computationally expensive

Motivation

- 4+ years needed for compact model after device proposal.
- Further 4+ years needed for commercial models.
- Need of new method.

* References for data points are not shown
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SRAM - Importance

- SRAM consumes 90% area of SoCs and microprocessors. [1]
- To increase memory density, SRAM bitcell area is reduced 50% each technology node. [2]
- Aggressively scaled devices → more variability → less SNM → higher instability

SRAM Basics

- **SRAM**: Cross coupled CMOS inverters with two access transistor.
- **SNM**: “Minimum noise voltage needed to flip the state.”
- **Getting SNM – Square fit method**
- **Modes of operation**
  - **Hold Mode**: $V(\text{BL}) = V(\text{BLB}) = V(\text{WL}) = 0\text{V}$
  - **Read Mode**: $V(\text{BL}) = V(\text{BLB}) = V(\text{WL}) = V_{\text{DD}}$
  - **Write Mode**: $V(\text{WL}) = V_{\text{DD}}$, $V(\text{BL}) = \sim V(\text{BLB})$

$$\text{SNM} = \frac{\text{Max}_\text{diff}}{\sqrt{2}}$$

![SRAM Diagram](image)
SRAM Basics – Read mode

- $P_2,N_1$ in Cut off.
- $P_1$ and $N_2$ in Linear
- Pre-charge $C_{BL}, C_{BLB}$ to $VDD$.
- $WL = VDD$, turns on access transistors.
- $I(N_3) = 0$.
- $V(N_2)$ starts increasing.
- Pull down should be stronger than access transistor.
- Sense amplifier compares values and gives stored value.

$\Rightarrow$ Non Destructive Read operation: $(WL = BL = BLB = VDD)$
SRAM Basics – Write mode

- $P_2, N_1$ in Cut off.
- $P_1$ and $N_2$ in Linear.
- Pre-charge $C_{\text{BLB}}$ to VDD.
- WL = VDD, turns on access transistors.

- $V_{P_1}$ discharges through N3 and turns on P2.
- $V_{N2}$ increases and turns on N1.
- New values gets stored.

- Access transistor should be stronger than pull up transistor.

$\Rightarrow$ Error less Write operation: (WL = VDD) $N > NA > P$
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Proposed Method

- For VTC, \((V_1, V_2)\) pairs are needed.
- Two inverters interact in terms of voltages only.
- They can be analyzed separately.
- Kirchhoff’s law
  \[
  I_N = I_P + I_A
  \]

- \(I_P = I(V_{GS} = V_1 - V_{DD}, V_{DS} = V_2 - V_{DD}) \rightarrow I_P = f(V_1, V_2)\)
- \(I_N = I(V_{GS} = V_1, V_{DS} = V_2) \rightarrow I_N = f(V_1, V_2)\)
- \(I_A = I(V_{GS} = V_{DS} = V_{DD} - V_2) \rightarrow I_A = f(V_2)\)
Proposed Method – Getting VTC

- Fix value of $V_2$
  - $I_P = f(V_1)$, $I_N = f(V_1)$, and $I_A = \text{const.}$

- Plot the functions
  - $[I_P(V_1) + I_A]$ and $I_N(V_1)$

- Find Value of $V_1$, such that
  - $[I_P(V_1) + I_A] = I_N(V_1)$ → intersection point

- Hence we get $V_1$ for a given $V_2$.

- Similarly, Get all $(V_1, V_2)$ pairs for complete range.
Proposed Method – Getting VTC

\[ V_1 = 0.3134V \]
Variability Effect Study

- Process variations
  - Random Dopant Fluctuations (RDF)
  - Line Edge Roughness (LER)
  - Gate Edge Roughness (GER)
  - Metal gate granularity (MGG)

- Random lines from Langevin Equation.
  - \( \Lambda = 30 \text{ nm} \) and \( 3\sigma = 2 \text{ nm} \).

Sketch demonstrating LER & GER in FinFET.
Kedar Patel, et.al. “IEEE TED VOL. 56, NO. 12, DECEMBER 2009”

\( \Rightarrow \) Change in channel width due to LER.
Proposed Method – Adding Variability

VT Distribution

\[ -\Delta V_T \quad \text{Mean} \quad 3\sigma \]

\[ +\Delta V_T \]

\[ (I_p + I_A) \text{ at } V_2 = 0.375V \text{ with } \Delta V_T \]

\[ I_N \text{ at } V_2 = 0.375V \text{ with } \Delta V_T \]

\[ -\Delta V_T \quad \text{VTC in Read Mode} \]

\[ I_N \quad \text{Butterfly Curves in Read Mode} \]

\[ +\Delta V_T \]

\[ (I_p + I_A) \& I_N \text{ at } V_2 = 0.375V \text{ with } \Delta V_T \]

\[ V_2 \text{ (V)} \]

\[ 0.1 \quad 0.2 \quad 0.3 \quad 0.4 \quad 0.5 \]

\[ V_1 \text{ (V)} \]

\[ 10^{-7} \quad 10^{-5} \quad 10^{-3} \quad 10^{-2} \quad 10^{-1} \]
Proposed Method – Process Flow

1. Create PMOS and NMOS Nominal Structure and get set of $I_D V_{GS}$
2. Generate Random structures for LER and Get VT distribution ($\sigma V_T$)
3. Generate VTC and hence butterfly curve using Set of IDVGs of Nominal Structure
4. Get SNM from 45° tilted Butterfly curves
5. Introduce Variability using $\sigma V_T$ and get SNM Distribution

TCAD

Computing Software
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Validation of Method – Process flow

- Validating against industry standard HSPICE circuit simulator

Flowchart:
- Standard MOSFET Parameter File (45nm) → SRAM Full Circuit Simulations (HSPICE) → PMOS and NMOS (HSPICE) → Proposed Method (Computing Software) → Compare SNM → Result

σVT

I_D V_Gs at Different V_2

SNM Distribution

SNM Distribution
**SNM distribution matches with acceptable marginal error.**

**Method is Validated**
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EdFinFET vs FinFET – Butterfly plots vs VDD

FinFET \( \sigma VT = 33 \text{ mV} \)

EdFinFET \( \sigma VT = 22 \text{ mV} \)
EdFinFET vs FinFET – SNM vs VDD

Lower SNM
Higher Variability

Higher SNM
Lower Variability
EdFinFET vs FinFET – Mean/Sigma vs VDD

Minimum allowed VDD

EdFinFET = 0.3V
FinFET = 0.45V

Mean should be 5 times 1σ value for 1Mb SRAM to function [1]

44% power can be saved by EdFinFET.

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Conclusion

- Fast and accurate
- No need for compact models
- 1000X reduction in run time compared to TCAD mixed mode simulations
- EdFinFET can be used for low power applications ($V_{DD}=0.3V$)
THANK YOU