M.Tech. credit seminar report,
Electronic System Group, EE Department, IIT Bombay,
Submitted November 2003

Time Multiplexed Switched Capacitor Filters

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Abstract

One of the reasons for the attraction towards Switched Capacitor (SC) filters is that the development in the field of MOS integrated circuits have made possible the realisation of *filter on chip* with behaviour similar to active RC or RLC filters. The report discusses in brief, principle involved in operation of SC circuits and properties of various circuit building blocks in MOS technology. The report also covers few important concepts related to stray insensitive design of SC filters. Few topological constraints, which are required to be satisfied to achieve insensitivity against this stray capacitance, are also discussed. Having discussed the basic aspects related to SC filters, focus is made towards time multiplexing of SC filters. General conditions which are necessary for time multiplexing of SC circuits are studied in reference to two different cases. In the first case time multiplexing of an SC subnetwork, which is common in N independent SC circuits, is studied. In the second case, time multiplexing within an SC network is discussed, which covers time multiplexing of SCs and operational amplifiers(OAs). Both the cases are exemplified using stray insensitive SC biquad circuit.

1 Introduction

A filter is a frequency selective circuit designed to pass (or transmit) certain signal frequencies and stop (or reject) other frequencies. They are one of the important building blocks of communication and instrumentation systems. Extensive work has been done in the field of filter design and complete theory exists starting from the specification and ending with a circuit realization.

The oldest technology for realizing filters made use of resistors, capacitors and inductors, which constituted a class of filter circuits commonly known as passive filters. Filters can be realized using only resistors and capacitors (called RC filters) but as such networks can realise only low Q values, which puts limitation on its use. Using an inductor with RC network can help in realizing a network function with high Q, however, such design have their own limitation because of the presence of inductors. Such filters work well at high frequencies, however, in low frequency applications, inductors required are large and physically bulky and above that their characteristics are quite non-ideal. Furthermore, such inductors are impossible to fabricate in monolithic form and are incompatible with any of the modern techniques for assembling electronic systems. Therefore, there has been a considerable interest in inductorless filters. From the various possible types of inductorless filters, the major class is of active RC and SC filters [12].

Active RC filters are realized by using passive RC networks along with active elements like bipolar transistors, operational amplifiers(OAs), current conveyors etc. Such a realization makes it possible to design filter circuits with sharp cutoff and highly selective amplitude and phase response. However, there exists some limitations due to non ideal nature of active

devices, variation in values of resistors and capacitors with temperature, variation in power supply etc. In addition, designers are interested in considering the miniaturization of filters to an extent that they are technologically compatible with other subsystems which uses digital techniques.

Active RC filters can be realized using thin or thick film or silicon bipolar integrated circuit technology. However, such technologies have their own advantages and limitations. The reason for the biggest attraction towards SC filters is that they permit the realization of a *filter on a chip*. The advancement in MOS technology and their distinct advantages, have made possible to achieve alternative configuration for design of filters with a behavior similar to active RC or LC filters merely using switches, capacitors and OAs. This constitutes a class of SC filters.

The SC approach overcomes some of the problems inherent in active RC filters, while adding some interesting capabilities. In SC filters accuracy related to design parameters like cutoff frequency and Q value depends on the ratio of capacitance rather then its absolute values. As this can be obtained and maintained accurately over a wide range of temperature and signal amplitude using MOS fabrication technology, very precise SC filters are possible. In addition to this an SC filter allows tunability of its cutoff frequency simply by varying frequency of clock fed to it, with no change in external circuitry. This, on other hand, is very difficult in conventional active or passive filters.

In SC networks, signals are transmitted from input to output in form of charge packets in sampled data form through SCs. This shows the possibility of time multiplexing, thereby, reducing the resources required in the design. In particular, the concepts can be well appreciated in relation to the design of higher order filters requiring large number of SCs and OAs. Implementing time multiplexing can help to achieve the design occupying smaller silicon area and reduced power requirements.

To the best of author's knowledge, ideas related to the concept of an SC filter trace back to early 1970's, where the concept was presented as an analog sampled data filter [13]. This idea did not grow immediately but much work had been published in late 1970's and early 1980's and the full impact of this new filter technology was appreciated [1]-[6]. The approach of time multiplexing in filter circuits existed, to an extent, even in cascade active RC filters and the same was extended to SC filters. Literatures are available discussing the systematic approach to time multiplexing of stray insensitive SC networks [8], [9]. Much work has also been published on implementation side of SC filters in many signal processing applications [11], [14].

Here, an attempt is made to cover some elementary aspects related to stray insensitive SC networks and as an extension to this, study of time multiplexed SC filters is made. The general conditions for time multiplexing a subnetwork which is common to several independent SC circuits is studied followed by time multiplexing of SCs and OAs within an SC filter. All the time multiplexing schemes discussed are also supported with an example for better insight.

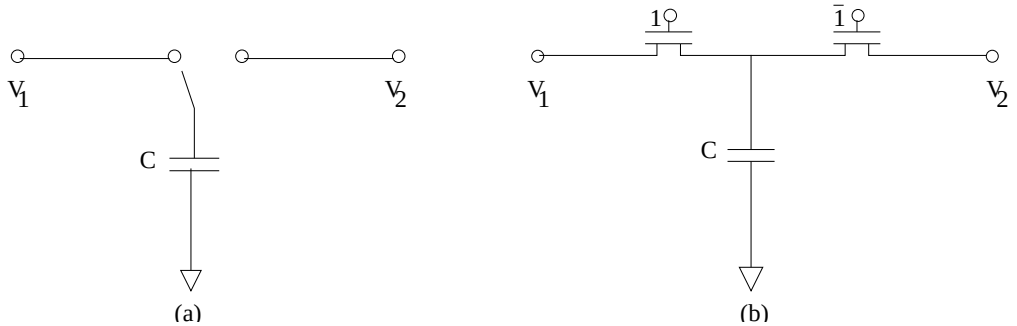

Figure 2.1: (a) A SC which can simulate the function of a resistor; (b) MOS implementation of (a).

2 Principle of Operation of SC Networks

2.1 Resistor Realisation using SC

The main trick in design of an SC filter lies in simulating circuit behaviour of a resistor, utilising capacitor and switches. Consider the simple circuit shown in Figure 2.1(a) explaining the operation of an SC resistor [12].

Consider that the switch is initially in left hand position so that capacitor is charged to voltage V_1. The switch is then thrown to right and the capacitor is discharged to voltage V_2. The amount of charge which flows into (or from) V_2 is thus

$$Q = C(V_2 - V_1). \tag{1}$$

If the switch is thrown back and forth at every T seconds, then average current i from V_1 into V_2 can be given as

$$i = \frac{C(V_2 - V_1)}{T} = \frac{(V_2 - V_1)}{T/C}. \tag{2}$$

The resistor which would give the same average current as this, would be of the value

$$R = \frac{T}{C} = \frac{1}{Cf_c} \tag{3}$$

where f_c is the frequency of clock signal whose time period is T. Figure 2.1(b) shows MOS implementation of the same circuit.

If f_c is much larger than the highest signal frequency of interest, then the time sampling of the signal which occur in this circuit can be ignored and the SC can be considered as direct replacement of conventional resistor. If, however, the switching rate and the signal frequency are comparable, then sampled data techniques are required for analysis. Again here we have considered V_1 and V_2 as voltage source which are not affected by opening and closing of the switch.

The SC resistor requires very little silicon area to implement large resistance values. In fact the silicon area decreases as the required value of resistance increases, which is quite clear form eqns (3). To implement audio frequency filters, a resistance of the order of 10

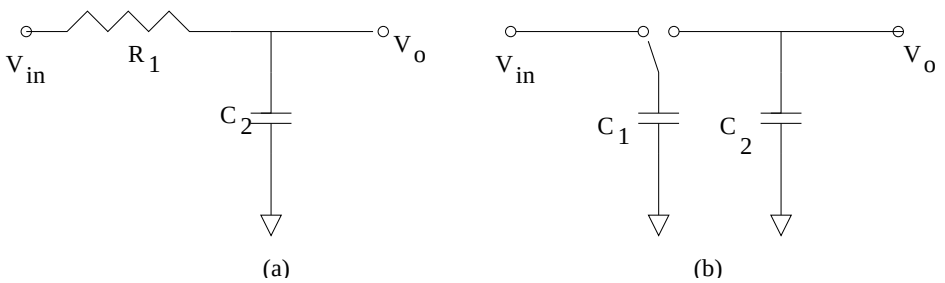

Figure 2.2: (a) Single pole RC lowpass filter; (b) Realisation of (a) using SC resistor.

MΩ is needed, when used with a capacitor of around 10 pF. However, the same value of resistance can be realized by switching a capacitor of around 1 pF at 100 kHz frequency. Doing this would consume 100 times less silicon area in comparison to implementation of 10 MΩ resistance [1].

Consider a conventional single pole RC low pass filter as shown in Figure 2.2(a) with its SC implementation in Figure 2.2(b). The RC time constant of the filter can be given as

$$\tau = R_1 C_2 = \frac{C_1}{C_2}\frac{1}{f_c}. \tag{4}$$

Thus the time constant is determined by the ratio of capacitors. Also the 3 dB cutoff frequency of the conventional filter is

$$\omega_C = \frac{1}{R_1 C_2}. \tag{5}$$

which in case of SC filter will be

$$\omega_C = \frac{C_1}{C_2} f_c. \tag{6}$$

This again shows its dependence on the ratio of capacitance and not the absolute values. In MOS realisation the ratio of capacitance is mainly the function of geometrical shape and hence can be designed accurately with a high degree of stability. In addition, both the time constant and the cutoff frequency are proportional to f_c, i.e., clock frequency used to drive the switches. This allows programmability of circuit by simply varying the clock rate.

2.2 Properties of MOS Capacitors, Switches and OAs

The properties of MOS technology for the elements used in SC filtering are necessary to investigate in detail so as to know the advantages and limitations in the realisation of filter configuration [1], [2].

2.2.1 MOS Capacitors

Within a MOS technology, capacitors are made in several ways. These capacitor structures have some common characteristics of interest which are discussed as under.

Ratio accuracy

The key aspect in performance of any frequency selective filter is the accuracy and reproducibility of the frequency response. In case of SC filters this accuracy, as seen in the previous subsection, depends on the ratio of capacitance. The capacitance of a MOS capacitor can be expressed as

$$C = \frac{\varepsilon_o \varepsilon_r w l}{t} \tag{7}$$

where ε_o = permitivity of free space, ε_r = dielectric constant of silicon dioxide, w = width of the electrode, l = length of the electrode, t = thickness of silicon dioxide dielectric.

Considering variables in eqn (7) statistically independent, standard deviation in the value of C can be given as

$$\sigma = \left[\left(\frac{\Delta \varepsilon_r}{\varepsilon_r} \right)^2 + \left(\frac{\Delta l}{l} \right)^2 + \left(\frac{\Delta w}{w} \right)^2 + \left(\frac{\Delta t}{t} \right)^2 \right] \tag{8}$$

where $\Delta y/y$ is the relative error of respective parameter y. Those error which occur because of variation in dielectric constant and the thickness are termed as Oxide effects, whereas those from other two errors are designated as Edge effects. The former is prominent in large value capacitors whereas later in design of small value capacitors. Thus large value capacitors are realised using small value capacitors, which helps in reducing the dependence of random errors on geometry of the design. Thus these effects are alleviated with careful layout. The achievable ratio accuracies ranges from 1 to 2 percent for small capacitor geometry (around 400 μm^2) to an order of 0.1 percent for economic size (around 4000 μm^2).

Voltage and temperature coefficient

MOS capacitors made with heavily doped silicon plates display voltage coefficients in the range of 10 to 100 ppm/V and the temperature coefficient of 20 to 50 ppm/^oC which are low enough to be insignificant in all applications.

Parasitic capacitance

Parasitic capacitance (stray capacitance) exists between bottom plate of the capacitor and the substrate. Typically this bottom plate parasitic capacitance have a value of one twentieth to one fifth of the MOS capacitor itself. Further, since the top plate is connected to other circuitry on the silicon chip, a small capacitance, in the substrate will exist from the top plate to the substrate due to interconnections. This parasitic capacitance is unavoidable and hence the design of SC filter must be done in such a way that the parasitic capacitance do not degrade the performance of the filter. Fortunately such stray insensitive configurations are available which we would discuss in detail in Section 3.

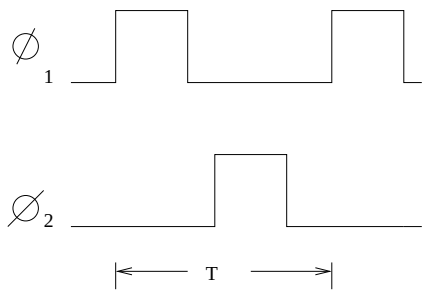

Figure 2.3: Even and odd phase of a two phase clock.

2.2.2 MOS Switches

The second principle component in SC filters is a MOS switch. This device behaves like a resistor in ON state and like an open circuit in OFF state. The important parameters of the switch are ON resistance, OFF leakage current, switching speed and parasitic capacitance. The MOS technology has provided excellent analog switches compared to bipolar switches. Few of the highlighting features are listed below

1. It has low offset voltage in saturation.
2. It offers high input impedance.
3. It is capable of handling input voltages in large range.
4. As the capacitance normally associated with such switches are of smaller value, resulting time constant due to ON resistance would be quite small and hence do not create a problem.

However, there exist following problems.

1. There exists junction leakage current which may result in slow voltage drifts. For example, a leakage current of 10 μA charging a capacitor of 10 pF may cause an offset voltage of 1 mV in 1 msec.
2. Parasitic capacitance exists between gate to source and gate to drain which tend to introduce d.c. offset at signal nodes. These parasitic capacitances are of the order of 0.01 - 0.1 pF.

2.2.3 MOS OA

Realization of OA in MOS technology requires about one third to one fifth of the silicon area compared to bipolar OAs. Typically achieved level of performance are common mode rejection ratio of 60 dB to 80 dB, power supply rejection ratio of 60 dB, unity gain bandwidth of 2 MHz and power dissipation of 5-15 mW.

2.3 Analysis of SC Networks

In case of SC networks containing capacitors and periodically operated switches, the clock frequency used to operate switches have at least two phases as shown in Figure 2.3. The two phases are identified conventionally as ϕ_1 and ϕ_2. In both the phases depending on the manner in which switches and capacitors are connected, topology of the circuit would be different. Phases should be non overlapping. All the SCs close simultaneously on one side at even

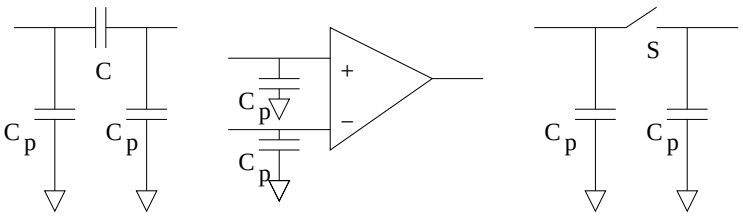

Figure 3.1: Stray capacitance in a capacitor, an OA and a switch

multiple of $T/2$ $(0, T, 2T, ...)$ and on the other side at odd multiple of $T/2$ $(T/2, 3T/2, ...)$. Analysis of the SC network is normally done involving the variables voltage and charge. This is easier as charge remains finite and only entity that can store charge in SC network is a capacitor plate. Hence only the capacitors in the network and not the switches, resistors or voltage sources, are responsible for conservation of charge [3]. However, the relation describing the behaviour of SC network can equally be found out using KVL, $q - v$ relations for capacitor plates etc. Once the set of equations describing an SC network is obtained, we find the overall transfer function which is subsequently used for the analysis. As in nature of operation, the SC networks can be considered as discrete time systems, the tool like z - transform can be quite handy in its analysis.

Another interesting approach in the analysis of SC networks is based on the fact that the structure of the circuit changes in each phase of the clock as switches in the network changes its position. Thus a single SC network can be considered as two subnetworks in each phase of clock (or more than two subnetworks in case of multiphase clock). These are known as equivalent circuits. However this two subnetworks are not independent because of the energy storage property of the capacitor. As a consequence, two circuits corresponding to two phases of clock are *linked* by virtue of *memory* of the capacitor. Much work has been done in this direction and analysis methods based on standard two port and four port equivalent circuits are quite popular [4], [5].

3 Stray Insensitive Design of SC Networks

One of the most important factors that determines the success or failure of an integrated SC filter is the influence of stray capacitance. In realisation of a circuit with nominal capacitances as low as 1 pF, the parasitic capacitances associated with capacitor, OA and switch, as shown in Figure 3.1, can be neither neglected nor considered to be small. Fortunately, there exists few topological constraints which if satisfied guarantees insensitivity to all these stray capacitances [6], [7]. But again, as soon as we abandon hypothesis of an ideal OA, the stray capacitance will influence the transfer function of an SC filter even if the topological constraints are satisfied. However, the corresponding sensitivity is inversely proportional to the amplification factor A_o of the OA at zero frequency. So, as long as A_o is sufficiently large, the influence of stray capacitance can be to an extent acceptable. Therefor, in practice, circuits are designed with A_o greater then 1000.

For the sake of simplicity, we shall limit the discussion to SC filters with two phase switches. As discussed in Section 2.2, SC networks driven by a clock signal with two phases changes its circuit topology on basis of closing and opening of switches in even and odd intervals. Thus we can look upon an SC network as two equivalent networks, one valid for the

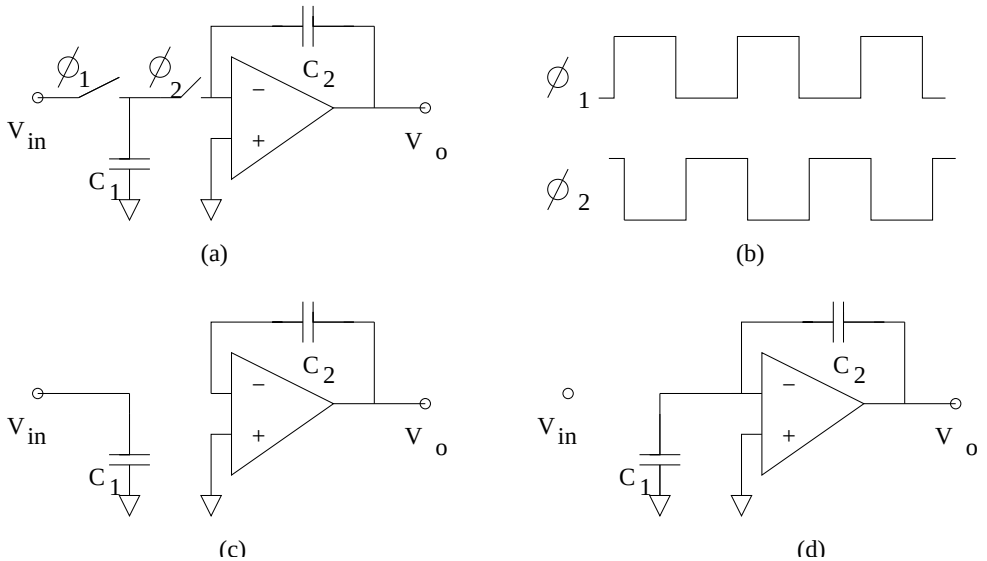

Figure 3.2: (a) SC integrator; (b) Two phase clock with even and odd phase; (c) Equivalent even circuit; (d) Equivalent odd circuit.

even phase and other for the odd phase. We call them as even and odd circuits respectively. The concept can be easily understood from the example of simple SC integrator as shown in Figure 3.2. To analyse the topological constraints let us classify the nodes in the even and odd circuits, in two groups V and I. V is that group of nodes that comprise of OA output node as well as input node, whereas, I group comprises of the virtual ground terminal, i.e., input terminal of an OA whose other input terminal is connected to ground.

It can be analytically shown that if following topological constrains are satisfied by an SC filter, then it attains insensitivity with respect to stray capacitance due to circuit capacitors, OAs and switches [6].

1. Both even and odd circuits do not contain nodes other than V, I and the ground.
2. A terminal of a capacitor is never switched from V node of even circuit to an I node of odd circuit and vice versa.

If we examine the integrator shown in Figure 3.2(a), then the equivalent even and odd circuits satisfy constraint (1) as even and odd circuits have either V node or I node. However, this does not satisfy constraint (2) as the capacitor C_1 has one terminal which is switched from V node to I node. Due to this the parasitic capacitance attached to this terminal simply augment C_1 and there by alters the behaviour of the integrator.

Now consider similar integrator configuration as shown in Figure 3.3, with its equivalent even and odd circuit. The configuration involves use of two more switches compared to the previous case but makes the configuration totally stray insensitive. If we try to see the obeyance of the constraints, then even and odd circuits have no other nodes except V or I node. Hence constraint (1) is satisfied. So far as constraint (2) is concerned, while switching, terminal of the capacitor is connected either from node V to ground or from node I to ground and not for V to I, hence it is also satisfied. Hence, the circuit would not have

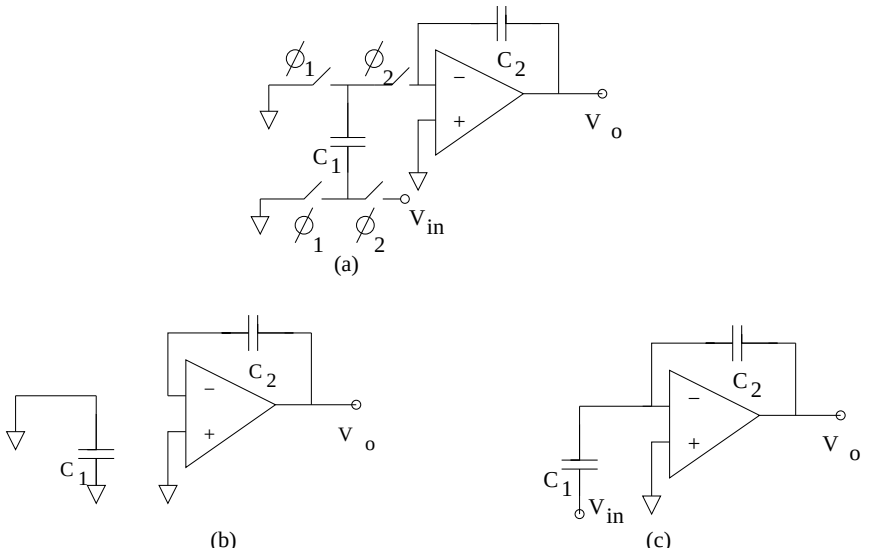

Figure 3.3: (a) Stray insensitive SC integrator; (b) Equivalent even circuit; (c) Equivalent odd circuit.

the effect of parasitic stray capacitance. Insensitivity of the circuit with respect to stray capacitance can more elaborately be explained as follows.

3.1 Insensitivity with respect to Stray Capacitance of the Circuit Capacitors

Stray capacitors associated with the circuit capacitors have their terminals connected either to voltage source, ground or virtual ground terminal. The stray capacitors which are connected directly to voltage source would not effect functioning of the circuit capacitance, because, they would charge independently. Again their discharging is to ground and hence also independent. The stray capacitors which are connected to either ground or virtual ground terminal would never charge as both terminals remains at ground potential [6].

3.2 Insensitivity with respect to Stray Capacitance of the OAs

The parasitic capacitors associated with OAs never charges since the input terminals are either ground or virtual ground and hence they do not contribute in functioning of the circuit.

3.3 Insensitivity with respect to Stray Capacitance of the Switches

The stray insensitive circuit is designed in such a way that there exists no nodes in the circuit other then input/output node and ground/virtual ground node in the equivalent even or odd circuits. Because of this, addition of switches to the OA and capacitor subnetwork does not generate any new node. Thus every switch terminal is connected to either capacitor or OA terminal. Its parasitic capacitance, therefore, combines with the corresponding parasitic capacitance of the capacitor or OA which, as we saw, have no effect on functioning of the network. The other similar configuration is as shown in Figure 3.4. It can be used to realise negative resistance, whereas, that shown in Figure 3.3 in the circuit of integrator realises positive resistance.

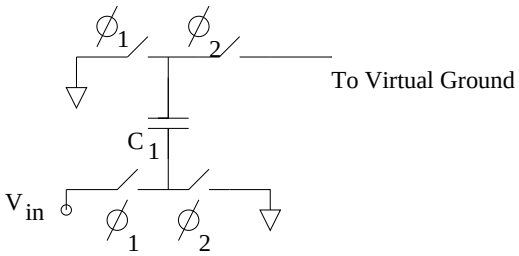

Figure 3.4: Realisation of negative resistance using stray insensitive SC.

4 Time Multiplexing of Stray Insensitive SC Networks

The concept of time multiplexing is known more commonly related to communication, wherein, several signals are transmitted over a single line turn by turn. Thus the concept relates to the usage of same resource in time sharing mode so as to avoid multiplication of the resources. This proves to be economic as well as effective in many applications. In this section we would first review general conditions for time multiplexing a subnetwork which is common in several independent SC circuits. Subsequently, we would discuss time multiplexing within an SC network, which would cover time multiplexing of SCs and time multiplexing of OAs.

4.1 Time Multiplexing of N independent SC Networks

Consider an SC network consisting of N independent units as shown in Figure 4.1. By independent, we mean standalone units where output of a particular unit does not depend on another unit. Each independent unit is divided into two subunits, what we would call subnetworks S_i ($i = 1$ to N) and M. The subnetwork S_i may consist of OAs, switched and unswitched capacitors and M consist of OAs and SCs. Let T_i ($i = 1$ to N) indicates the time slot for working of each individual subnetwork and hence time period of the whole SC network would be NT, considering all time slots of equal value. This is shown in Figure 4.1(b). Each time slot T_i of an individual network may consist of one or more phases of clock.

The general conditions for time multiplexing of M subnetworks are the following [8].

1. All networks should operate independently.
2. The M subnetwork in each independent unit should be identical in terms of both topology and element values.
3. The multiplexing frequency $f_m >> f_h$, the highest signal frequency of interest.
4. At the end of time slot T_i, of each individual subnetwork, no SC in M subnetwork should have memory, i.e., no capacitor should retain charge. For this, if required, an extra phase can be added in T_i to discharge the capacitor.
5. The time slot T_i should be such that each subnetwork M completes integral number of cycles of charge transfer with atleast of one cycle. In other words the operations for all the p phases must be completed at least once.

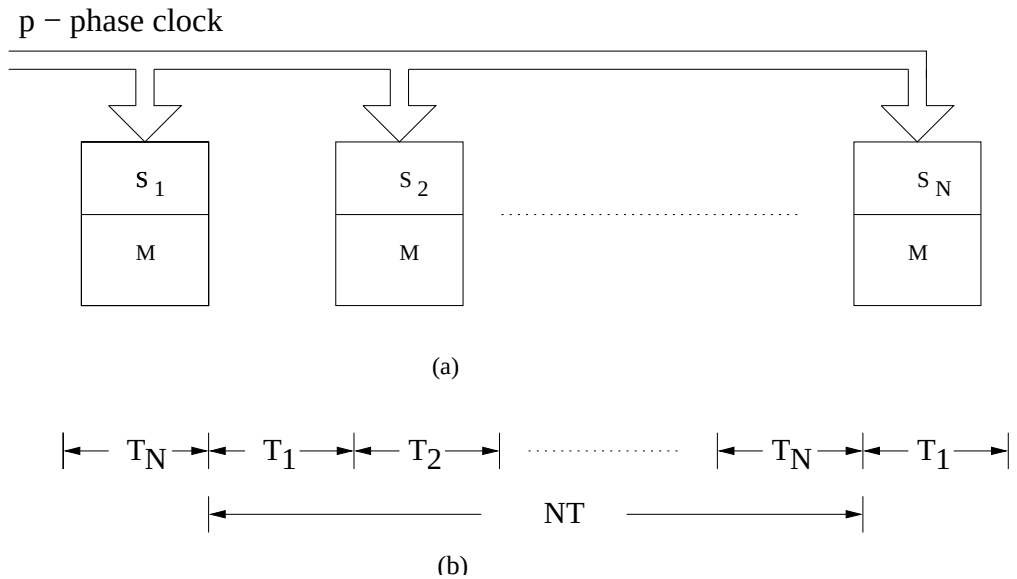

Figure 4.1: (a) N SC networks divided into subnetworks S_i and M; (b) Time slots

Conditions (1) to (4) are self-explanatory and are by and large same as those in the general theory of time multiplexing. However, condition (5) requires some more attention. The condition is necessary, because, in multiplexed mode of operation it is necessary that all the node voltages should be updated for the i^{th} circuit before M is connected to $(i+1)^{th}$ circuit, otherwise as per condition (4), the signal would be lost. To satisfy condition (5), it becomes necessary to have synchronisation between the clock phases and time slot T_i. This is achieved using a master clock. As an illustration, consider the multiplexing of N independent biquads, one of which is shown in Figure 4.2(a). Figure 4.2(b) and (c) shows one possible scheme for time multiplexing and the time slot arrangement. If we analyse operation of SC biquad shown in Figure 4.2, we find that in phase ϕ_1 of the clock all the SCs, i.e., C_5, C_6, C_7 and C_8 get charged and in phase ϕ_2 get discharged. Hence they do not have memory at the end of phase two, so this capacitors can be multiplexed. Thus each unit in the N independent biquad network can be divided in two units. The unit S_i would consist of capacitors C_{i1}, C_{i2}, C_{i3} and C_{i4} whereas the M subnetwork would consist of C_5, C_6, C_7 and C_8, and two OAs. The M subnetwork as multiplexed would remain common to all S_i units. So as shown in Figure 4.2(b) we would have N stack of S network whereas one M network. Figure 4.2(c) indicates the phase and the time slots. Each time slot T_i would consist of two clock phases. One interesting thing to note here is that C_5, C_6, C_7 and C_8, i.e., the multiplexed capacitors, do not retain the charge while switching form phase ϕ_2 to ϕ_1, but have memory or retains charge while switching from ϕ_1 to ϕ_2. Hence time multiplexing is possible only for the time slots and clock phase arrangement shown in Figure 4.2(c). In other words phase ϕ_1 and ϕ_2 cannot be interchanged.

4.2 Time Multiplexing within an SC Network

We shall consider multiplexing of SCs and OAs in a network separately.

4.2.1 Time Multiplexing of SCs

An SC network consisting of more than one SC element if operates on a clock with two phases, then all the SC closes simultaneously on one side in the even phase and change over

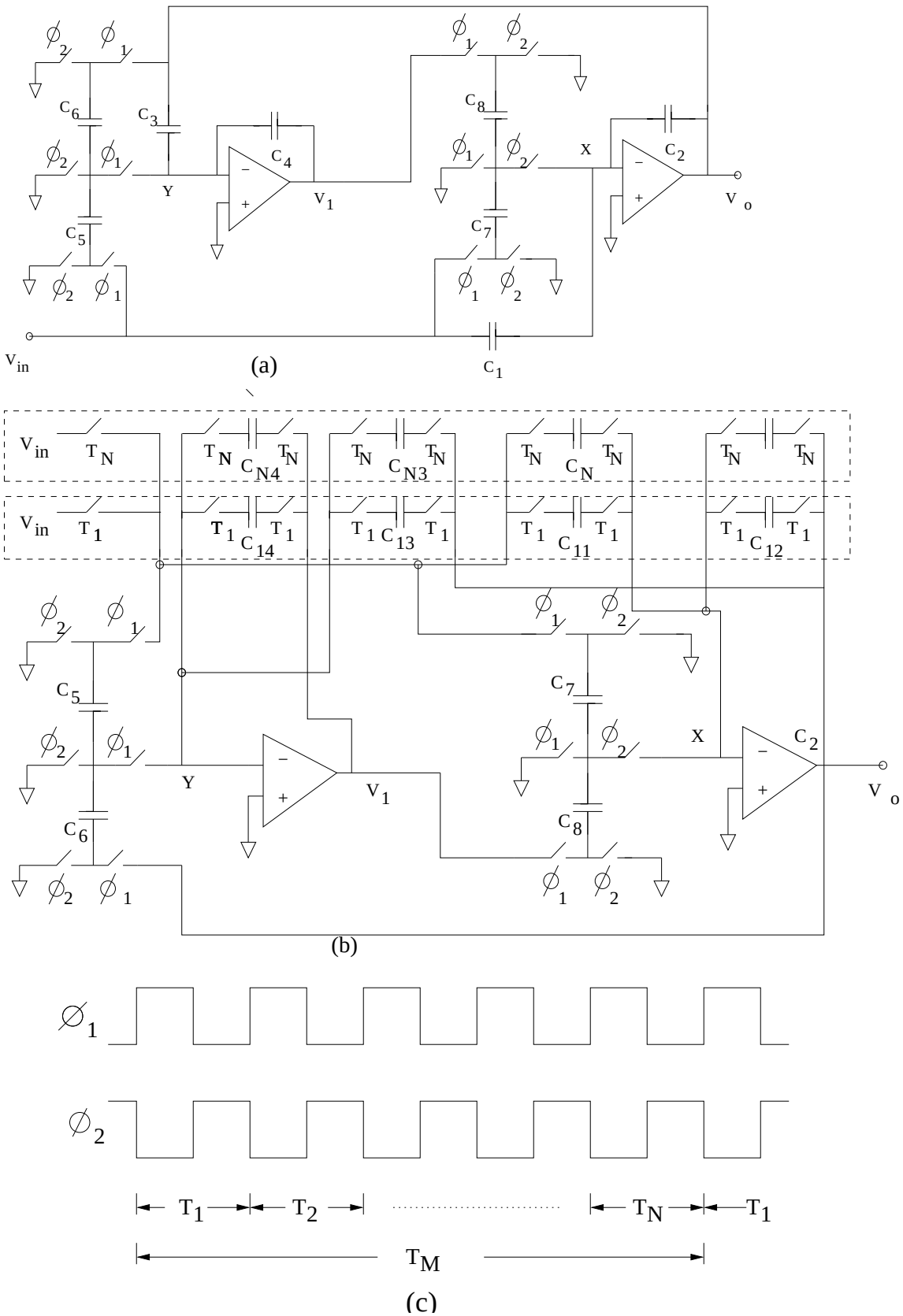

Figure 4.2: (a) Stray insensitive SC biquad; (b) Time multiplexing of N SC biquads; (c) Clock phase and time slots.

simultaneously to other side in the odd phase. If the circuit consists of capacitors of equal value then the work of all these SCs can be realised using a single capacitor in time shared manner, provided they satisfy conditions mentioned in Section 4.1. This multiplexing mode would involve transfer of charge form input to the output in staggered way, i.e., in more than two steps, in contrast to what was achieved exactly in two steps in circuits operating on two phase clock. Thus naturally, a time multiplexed SC network would be operating on the multiphase clock signal. Increase in the number of phases in one clock period would always not lead to increase in the time period and slowing down the speed of operation. This is because, if we consider the input to be constant for one complete clock period T, then in case of two phase clock, the charge transfer takes place only at the edges of clock phase i.e. 0 and $T/2$ and the circuit almost remains standstill at all other time. Now, if this clock period T is split into N different time slots then N charge transfer can be achieved one after the other in staggered manner rather then all simultaneously. However, care is to be taken that each phase should have some minimum time so as to have satisfactory transfer of charge.

As per condition (4) of time multiplexing, capacitors used in time multiplexing should not have memory when it enters form one phase to another within a clock period. This gives the first impression that more number of switching operations would be required in one cycle for discharging the capacitor and hence more number of switches would be needed. However, an SC network designed using a stray insensitive SC unit have only three types of nodes, as discussed in Section 3, which are either input node, output node and ground or virtual ground. This would prevent the large increase in number of switches. As an illustration, consider multiplexing of a stray insensitive SC biquad shown in Figure 4.2(a), which was working as one unit in N independent SC network [9].

The general voltage transfer function of a biquad can be given as

$$T(s) = \frac{N_2 s^2 - N_1 s + N_0}{s^2 + \frac{\omega_p}{Q_p} s + \omega_p^2}. \tag{9}$$

The circuit involves realisation of four resistances in terms of SCs. Out of this four C_7 and C_8 are used to realise negative resistance whereas C_5 and C_6 realises positive resistance. The transfer function of the circuit can be given as

$$T(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{\frac{C_1}{C_2} s^2 - \frac{C_7}{C_2} f_c s + \frac{C_5 C_8}{C_2 C_4} f_c^2}{s^2 + \frac{C_3 C_8}{C_2 C_4} f_c s + \frac{C_6 C_8}{C_2 C_4} f_c^2}. \tag{10}$$

Comparing eqn (10) with eqn (9), we get

$$\omega_p = \sqrt{\frac{C_6 C_8}{C_2 C_4}} f_c, \quad \text{Bandwidth } = \frac{C_3 C_8}{C_2 C_4} \tag{11}$$

and hence

$$Q_p = \frac{1}{C_3} \sqrt{\frac{C_2 C_4 C_6}{C_8}} \tag{12}$$

$$N_0 = \left[\frac{C_5 C_8}{C_2 C_4} {f_c}^2\right], \; N_1 = \frac{C_7}{C_2} f_c \text{ and } N_2 = \frac{C_1}{C_2}. \tag{13}$$

Usually, either Q or bandwidth of the filter is spedified. Thus, we have five design relations (11) - (13), and eight unknown capacitors, and hence the values of three capacitors can be

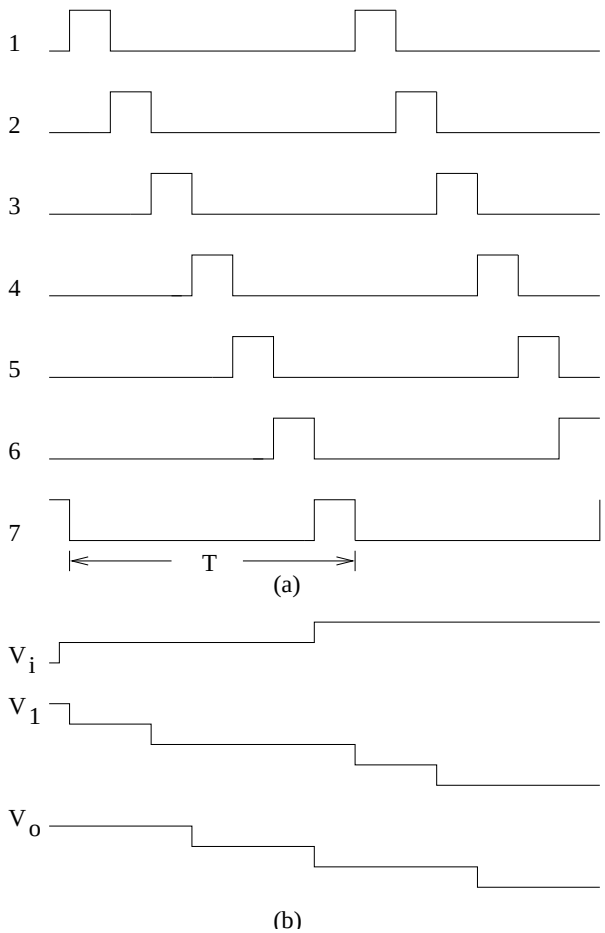

Figure 4.3: (a) Time multiplexed arrangement for the switching capacitors; (b) Waveform of seven phase clock and circuit voltages.

selected arbitrarily. If we make this of same value we can use them in time multiplexing and hence reduce the number of capacitors.

Let $\widetilde{C_5} = \widetilde{C_7} = \widetilde{C_8} = C_w$ be the three equal value capacitors, then values of the other capacitor can be calculated in terms of the design specifications as follows

$$\widetilde{C_2} = \frac{C_w}{N_1} f_c \ , \ \widetilde{C_1} = N_2 \widetilde{C_2} \ , \ \widetilde{C_3} = \frac{1}{Q_p} \sqrt{\frac{\widetilde{C_2}\widetilde{C_4}\widetilde{C_6}}{C_w}} \ , \ \widetilde{C_4} = \frac{C_w^2}{\widetilde{C_2}} f_c^2 \text{ and } \widetilde{C_6} = \frac{\widetilde{C_2}\widetilde{C_4} f_c^2}{C_w w_p^2}.$$

Thus this design allows to vary ω_p and bandwidth independently using C_6 and C_3 respectively and at the same time have three SCs of equal value. The time multiplexing arrangement for the switching capacitors C_5, C_7 and C_8 is shown in the Figure 4.3 (a). The arrangement works on clock signal with seven phases as shown in Figure 4.3 (b) and would require at the most four additional switches. The operation of the circuit is explained below.

Phase 1: Closure of switch 1 would charge $C_w = C_5$, at the same time there would be increment of charge across C_4 making V_1 more negative.

Phase 2: As in phase 1 C_w was charged, before it is used for doing job for other capacitor, it should be discharged. This is achieved by closing switch 2 in this phase.

Phase 3: Closure of switch 3 would charge C_6 and further increment the charge across C_4. C_6 on the other side is connected to ground through switch $\overline{3}$ which would keep it in discharged condition in all other phases except this.

Phase 4: Closure of switch 4 would charge C_w $(= C_7)$ to V_{in} . C_w was already in discharged condition after phase 2.

Phase 5: Closure of switch 5 would discharge C_w $(= C_7)$ at node X. This would increment the charge across C_2 making V_o more negative. C_w is again discharged and hence now can be used for doing job for other capacitor.

Phase 6: Closure of switch 6 would charge C_w $(= C_8)$ by V_1.

Phase 7: Closure of switch 7 would discharge C_w $(= C_8)$ at node X thus incrementing the charge across C_2 and further rising V_o. This discharge of C_w allows its use for the next clock cycle.

The time multiplexed biquad discussed here requires five capacitor instead of eight and requires four additional switches. The silicon area required in fabricating a capacitor in MOS technology is several times larger than that required by an analog switch. Hence, the reduction in the number of capacitors in biquad at the cost of increase in the number of switches is quite agreeable. This is particularly advantageous when higher order filter is realised by cascading more number of such biquads. If there is a coupling through a switched or unswitched capacitor from the output of an operational amplifier OA_1 to virtual ground of another operatonal amplifier OA_2, then at any instant of time if output of OA_1 changes output of OA_2 also changes. Such OAs are called coupled OAs. As far as multiplexing of SCs in such a circuit is concerned, the output voltages of OA_1 and OA_2 are not independent and hence the first condition is not satisfied. However, it is still possible to have switched multiplexing under following constraints.

1. Allow the multiplexing sequence such that all the OAs, associated with the SCs to be time multiplexed, updates their output fully at a stretch in the order the signal flows from the input to the output.

2. Replace each unswitched coupling capacitor between two operational amplifier by an SC, which is connected to the virtual ground in the phase in which the output voltage of OA_1 is completely updated.

4.2.2 Time Multiplexing of OA

If we try to analyse the conditions (1) to (5) for time multiplexing as discussed before to see the possibility of multiplexing of operational amplifiers within a circuit, we can find that except condition (1), rest of all either are obvious or can be satisfied easily. Again the OA does not have property of conserve charge, hence condition (4) and (5) are irrelevant in this regard. However, condition (1) requires a good attention and basically put much constraint on multiplexing of OAs. As per this condition all OA should operate independently, which is not much common. Fortunately, it is possible to time multiplex those OAs in dependent

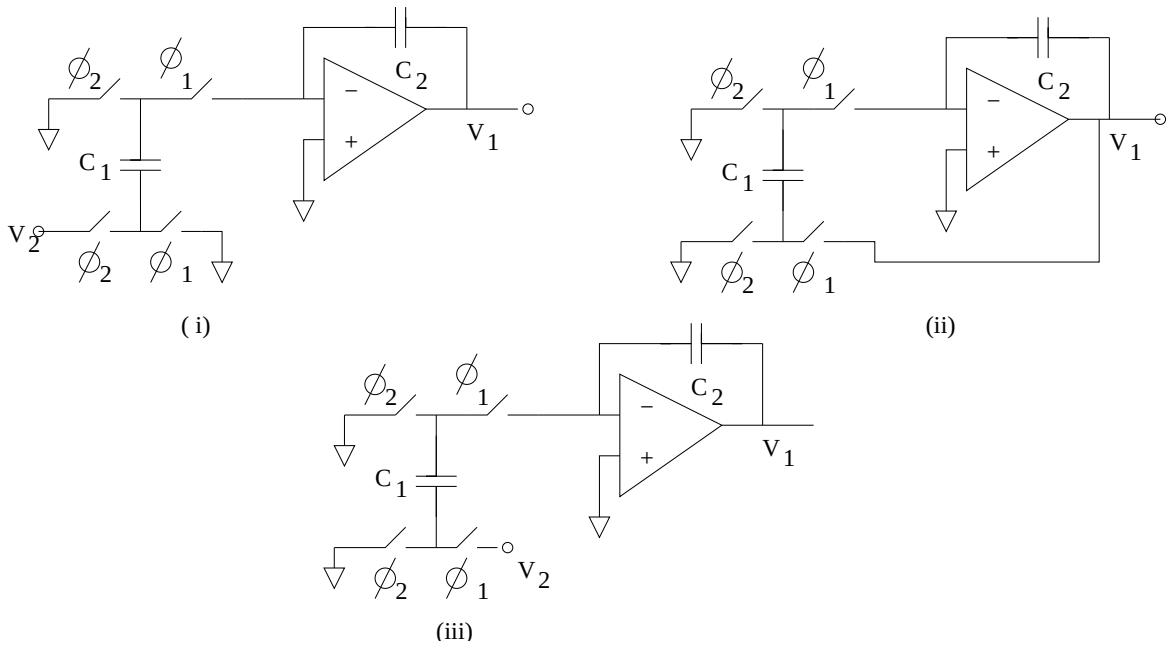

Figure 4.4: Three possible connections for updating the output voltage V_1 of OA_1.

sampled data network, which updates their outputs at different times. As in coupled amplifiers output are updated simultaneously, they cannot be time multiplexed.

For better understanding of the concept, let us discuss the concept with an example of stray insensitive biphase SC circuit consisting of two operational amplifiers OA_1 and OA_2. The respective outputs V_1 and V_2 of these OAs updates their output during phase ϕ_1 and ϕ_2 respectively. In such circuits, the outputs of OA will be updated by SC connected in any one of the three possible connections as shown in Figure 4.4. The connections are shown only for one of the amplifiers, updating the voltage V_1, similar will be the connections for other OA for updating the voltage V_2.

In connection (i), capacitor samples voltage V_2 in phase ϕ_1 and delivers the charge updating the output voltage in phase ϕ_2. The OA_2 is required in phase ϕ_1 whereas OA_1 in phase ϕ_2. In connection (ii), capacitor samples and updates the output only in phase ϕ_2 and hence OA_1 is required in phase ϕ_2 only. Hence connections (i) and (ii) are such that both the operational amplifiers updates their output in different time slots, so it is possible to time multiplex them. In connection (iii) V_2, i.e., output of OA_2, is required in phase ϕ_1, which would charge C_1 and in phase ϕ_2, V_2 would update itself for which again OA_2 would be required. Thus OA_2 is required during both the phases. So unless OA_2 is made free during phase ϕ_1, time multiplexing can not be done. This is however, possible to achieve by altering the circuit configuration [8]. One of such alternative is as shown in Figure 4.5. Here capacitor C_b charges to $0.5V_2$ during phase 2 and delivers the charge in phase 1. Thus, a pair of any two OAs, in a conventional stray insensitive biphase SC circuit can be multiplexed, if they are not coupled.

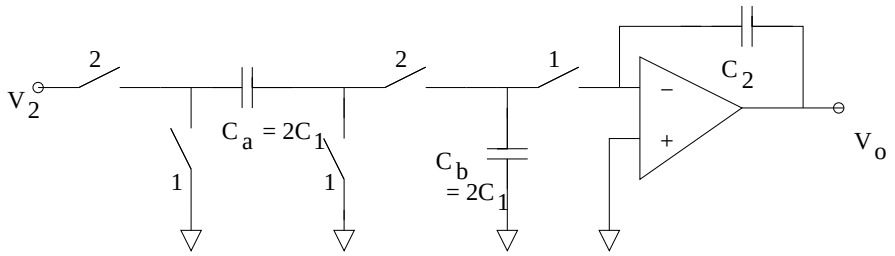

Figure 4.5: Alternative stray insensitive circuit for Figure 4.4(iii).

5 Conclusion

The basic requirement in an SC network is that the clock frequency must be sufficiently large compared to the highest signal frequency. In case of SC networks, which operates on time multiplexing, for proper operation $f_c >> f_m >> f_h$ where f_c, f_m and f_h are clock frequency, multiplexing frequency and highest signal frequency respectively. In addition, there should be a synchronism between the clock phase and the time slots. The maximum clock frequency at which we can use the SC network is restricted by the following factors [8].

1. Highest speed at which analog switches can operate.
2. Value of ON resistance of the switch, as minimum time of $5R_{on}C_s$, should be allowed for an SC C_s to charge fully to its steady value.
3. Highest speed at which OA can operate depends on many factors like its slew rate, settling time, offset voltage etc.

Again the number of clock phases roughly doubles with the number SC multiplexed and equals the number of OAs multiplexed (assuming a single OA multiplexed circuit). Thus, a large number of phases would be required when a large number of SCs or OAs are time multiplexed. Therefore, one has to trade off between the saving of die area due to the reduction in number of OAs and SCs and the increased complexity in generating and laying out the large number of clock phases.

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