M-Tech credit seminar report

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"Sinewave histogram testing of ADC"

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Abstract

The report discusses the use of sine wave histogram testing method of analog to digital converter (ADC). The method helps reducing the time required for ADC testing for a given accuracy and confidence level. Mathematical relationships are produced to determine *differential nonlinearity* (DNL), *integral nonlinearity* (INL), *amount of overdrive required*, *effective number of bits* and *number of samples required* as a function of desired accuracy using histogram method. The report covers uniform sampling method in detail while, a brief about random and Quasi-coherent sampling.

Comparison of the method and the classical approach is given shortly while discussing advantages of the present method over classical methods using some examples. The *Histogram Testing method* using *uniform sampling* can prove to be useful in mass production testing of ADCs where time required for such tests are directly related to economical aspects.

1 Introduction

The assurance and improvement of quality levels characterizing the performance of analog to digital converter (ADC) require a careful selection of device testing methods. Due to economical reasons, the tests need to be quick, effective, easily reproducible, and simple. Many different testing approaches have been suggested in the *IEEE standards for ADC testing* and *IEEE standard for testing of waveform digitising recorders.* Also, number of ADC testing methods have been presented in literature published in past few decades. Among all the testing methods, histogram testing, FFT analysis and sinewave curve fitting are most commonly used by ADC manufacturing industries and by the major users of the ADCs.

Generally, both the static and the dynamic characteristics are required to study the behaviour of the ADC. It is observed that, among all the parameters, the ADC Integral (INL) and Differential (DNL) nonlinearities represent the quantities of more importance for the description of the tested device quality under both static and dynamic conditions

[6]. These two characteristics gain more significance in the higher-resolution applications. We will deal with the sinewave histogram testing method here.

The method of histogram testing has been discussed in [1] and [2] in detail. We will reproduce it here in brief for the purpose of understanding. The technique is based on the use of a signal source exciting the ADC under test and on the evaluation of the histogram of the device output codes. A known periodic input is converted by an ADC under test at some sampling rate F_s. The relative number of occurences of the distinct digital output codes is termed the code density [1]. These data are viewed in the form of a Normalized Histogram showing the frequency of occurences of each code from zero to full scale. The code density data are used to compute all bit transition levels. Linearity, Gain and Offset errors are readily calculated from a knowledge of the transition levels. This provides a complete characterization of the ADC in the amplitude domain. The precision of this measurement may be extended without limit by taking additional data [1].

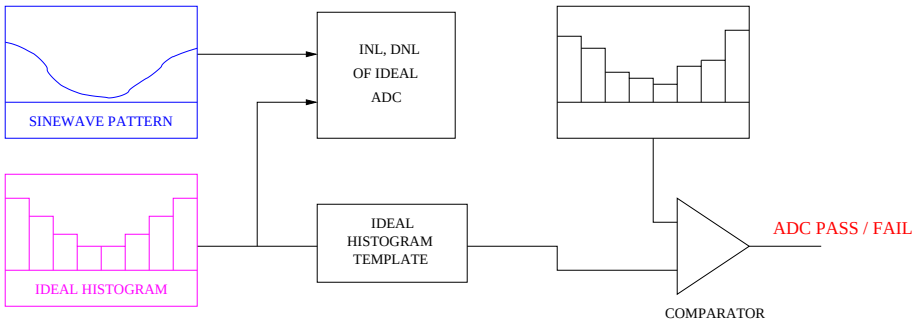

Figure 1: Setup for ADC Histogram Testing.

Figure 1 shows the schematic of the test setup used in industries where only critical parameters have to be tested. In the test procedure, the histogram obtained after the measurement is compared with the ideal histogram to identify the behaviour of ADC. The characteristic parameters such as Transfer curve, INL, DNL are also calculated. If all the parameters are within acceptable limits then the ADC is qualified otherwise discarded.

For an ideal ADC, the code density is independent of conversion rate and input frequency [2]. The characteristics of practical ADCs can be studied by varying both the sampling frequency and input frequency. Overall frequency response can be evaluated using the code density test for various frequencies.

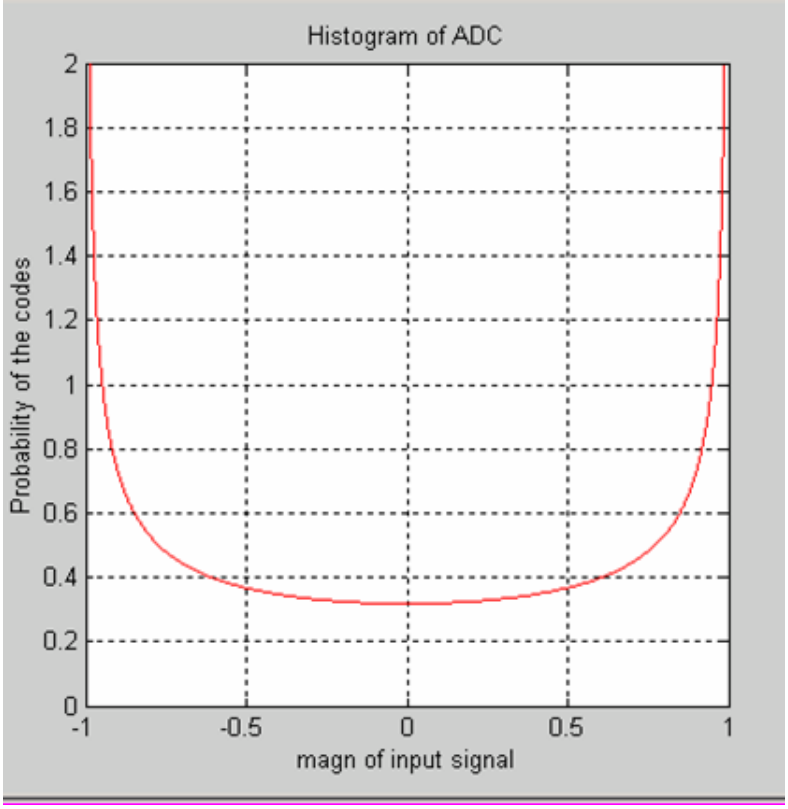

Figure 2: Typical Histogram of ADC.

1.1 Selection of Test Waveform

The first choice for input waveform would be a ramp or triangular wave since it would give the same code bin count for each code. But, the basic disadvantage of using ramp or triangular wave is distortion or nonlinearity in it. For a differential nonlinearity test, a 1 percent change in the slope of the ramp would change the expected number of codes by 1 percent. But these errors would quickly accumulate to make the integral nonlinearity test unfeasible [2]. However, some of the ADC parameters such as noise characteristics, word error rate etc. can be calculated by using triangular wave histogram method. In these measurements the nonlinearity in the triangular wave does not affect the accuracy of the measurements. One of the advantage of using the triangular wave is that, additive noise has no effect on the results [1].

The input source must be known with better precision than the converter being tested. A sine wave would be better choice because, it is precisely known mathematically and commercial oscillators and waveform synthesizers having very low total harmonic distortion are available. This can be confirmed by spectral analysis of the test waveform.

It is much harder to measure the linearity of a ramp to a comparable level of accuracy [2].

When sine wave is used, an error is produced which becomes larger near peaks. This error can be made small and as desired by sufficiently overdriving the ADC. The required amount of overdrive can be calculated as a function of given accuracy. The amount of overdrive also affects the errors in DNL due to harmonic distortion of the signal source.

In this report we will study uniform sampling in detail while random and Quasi-coherent sampling are introduced in brief, in succeeding section. In uniform sampling, sample points are taken from records with a fixed sampling frequency, where this frequency is chosen to minimize the errors. The selection of the sampling frequency is such that an integer number of waveform cycles of a input signal fall in a particular data record. It is shown that the number of samples required with this approach is smaller than the number required with the random sampling.

2 Random and Quasi-coherent sampling

In random sampling, the foundation of test is sinewave sampled randomly [2]. Sampling at random by its strict definition would be impossible; what must be done is to assure that, the sine wave input is not sampled repeatitively at the same level. By choosing the sample frequency to be non-harmonically related to the sine wave frequency, we are assured of this. Any jitter in the sample timing or drift in the oscillator frequency will just tend to randomize the sampling. The detail procedure of sinewave histogram testing by using random sampling is discussed in [2]

In coherent or uniform sampling, the ratio of signal frequency F and sampling rate F_s are selected such that coherence condition is met. This requirement is satisfied when $F/F_s = D/M$ where D and M are mutually prime integer numbers. Coherent sampling can be used to reduce the required number of samples for the given estimated accuracy. The samples required are less than that of the random sampling. Thus coherent sampling is useful to improve efficiency of sinewave histogram testing of ADC by saving the time required for testing.

However, such condition can never be perfectly met because of phase noise and because of the finite frequency resolution of the synthesizers [3]. The solution on this is to use Quasi-coherent sampling. In this, the ratio of signal and sampling frequencies is modeled as

$$\frac{F}{F_s} = \frac{D}{M} + \Delta\rho$$

where, $\Delta\rho$ is the fractional frequency deviation. The ADC sinewave histogram testing with Quasi-coherent sampling technique is discussed in [3]

3 Measurement Procedure

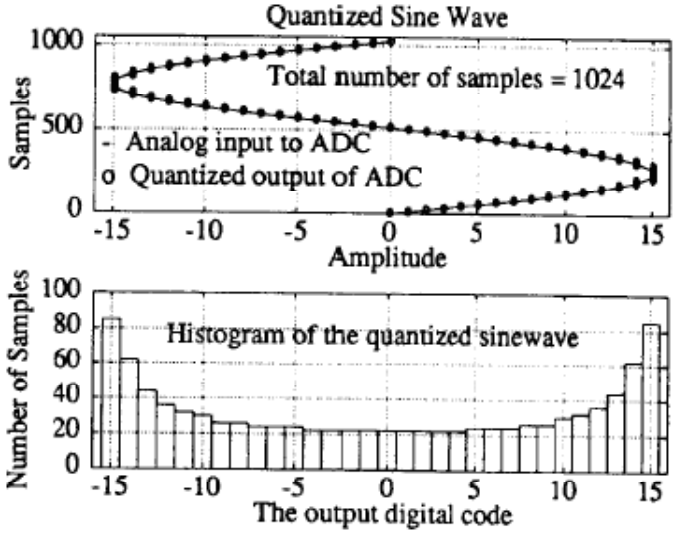

Figure 3: The Histogram of a Sampled Sinewave. Adapted from [7]

A sine wave that slightly overdrives the ADC is sampled many times. The data is collected as a series of R records each of which contains M samples. Thus, a suitable model of the record input data can be represented as [6]

$$x[n] = d - A\cos\left(2\pi\frac{D}{M}n + \phi\right), \qquad n = 0, 1, 2 \ldots, M-1$$

with A, ϕ, and d as the sinewave amplitude, initial record phase and offset, respectively, while D/M represents the ratio between sinewave frequency and converter sampling rate. Each record is taken with same constant sampling rate [1]. The record length and the ratio of the sampling rate to the signal frequency are chosen so that the phases of the samples are uniformly distributed between 0 and 2π. Since the phase difference between sinewave and ADC sampling sequence is not controlled and varies at random between separate data records, the phase ϕ of the first sample point of each record is assumed

to be randomly and uniformly distributed between 0 and 2π with the phases of different records being independent.

If the range of the ADC is not symmetrical about 0 volt, a constant, approximately equal to the mid-scale voltage of the ADC, must be added to the sine wave.

Following are some of the general notations and definitions used in this report.

$N =$ number of bits of the ADC. The output codes of the ADC are integers between 0 and $2^N - 1$.

$T[k] = k^{th}$ transition level. The voltage level at which the ADC will produce an output code of k-1 or less, 50 percent of the time and an output of k or more, 50 percent of the time.

$W[k] = T[k+1] - T[k] =$ the k^{th} code bin width.

$V = T[2^N - 1] - T[1] =$ the reduced full scale voltage of the ADC.

$Q = V/(2^N - 2) =$ the average code bin width.

The reduced full scale voltage, V, is the difference between the last and first transition levels. It is one code bin width smaller than the full scale voltage of ADC.

Additional parameters relating to the ADC depend on the *Gain* and *Offset*. The gain and offset are parameters of a straight line fit to $T[k]$ versus k (transfer characteristics of ADC), and will have different values depending on how the fit is done [1]. The relation to define gain and offset is

$$G \cdot T[k] + V_{os} + \epsilon[k] = (k-1) \cdot Q + T[1]$$

where

$G =$ the gain, nominally 1.

$V_{os} =$ the offset voltage, nominally 0.

$\epsilon[k] =$ the residual error.

The fit might be done to minimize the sums of the squares of the residuals, to minimize the maximum residual, to make the residual zero at the end points, or by some other method. Different methods yield slightly different values for the gain, the offset, and the residuals.

Let,

$h[i]$ = the total number of samples received in code bin i
and let,

$$ch[k] = \sum_{i=0}^{k} h[i] \tag{1}$$

and

$$S = M \cdot R = \text{the total number of samples.}$$

The applied signal is of the form

$$v[t] = A \sin [\omega t + \phi] + d$$

Here, the values of A and d are assumed to be known but it is not necessary. Errors in the values for A and d will affect the values calculated for the gain and the offset of the ADC but will not affect values for DNL or INL. The transition levels are calculated from the data, by

$$T[k] = d - A \cos \left[\frac{\pi ch[k-1]}{S} \right] \tag{2}$$

The code bin widths are given by

$$W[k] = T[K+1] - T[k] \tag{3}$$

If the values of A and d are not known, approximate values can be obtained from (2) [1] and approximate values for the first and last transition levels. Values for gain and offset may then be determined by any desired method, and INL and DNL can be determined by formulae given in subsequent sections.

3.1 Tolerance and Confidence Level

The Histogram approach is based on the assumption that the relative number of counts occuring in that code bin is equal to the probability of a measurement occuring in that code bin [1]. This is true only if the number of samples are infinite. For any finite number of samples there is a statistical error, and the number of samples must be chosen large enough to make this error sufficiently small.

Two quantities are used to describe the errors – the tolerance and the confidence level. Here tolerances are expressed in terms of *Code bin Width*. Suppose a code bin

width, W, is measured with tolerance, B, and confidence $1-u$ if the probabilty is equal to or greater than $1-u$ that

$$W_T/(1+B) \leq W_M \leq W_T(1+B) \tag{4}$$

where W_M is the measured value and W_T is the true value.

The tolerance and confidence level can also be expressed in terms of *Transition levels*. Suppose a transition level, T, is measured with tolerance, B, and confidence $1-u$ if the probability is equal to or greater than $1-u$ that

$$T_T - BQ \leq T_M \leq T_T + BQ \tag{5}$$

Where T_T and T_M are the true and measured values, and Q is the average code bin width.

Generally, the amount of required tolerance for code bin width and Transition level is different [1]. e.g. The required DNL may be upto ± 5 percent (B=0.05), but INL may only be needed to ± 1 percent. After deciding the required amount of tolerance, amount of overdrive required can be determined. The amount of overdrive required depends on the combined noise level of the signal source and the ADC [1]. The upper limit on the RMS noise level, is the sufficient information for this. The amount of overdrive required is same in both random as well as uniform sampling discussed here [1].

After determining the overdrive required, one can go for minimum number of samples required. This depends on the tolerance, the confidence level, and on the overdrive. For given values of these parameters, the number of samples required depends whether one is specifying the tolerance for an individual measurement or for the worst case. The total number of samples required also depends on record length chosen. The longer the record, the fewer are the samples required. However, the accuracy required of the input signal frequency increases with increasing record length.

3.2 Overdrive and Noise Level

The positive overdrive voltage is the difference between the maximum voltage of the applied signal and the largest transition level of the ADC. The negative overdrive voltage is the difference between the smallest transition level of the ADC and the minimum of the applied signal. The overdrive voltage, V_{OD}, is the smallest of the positive and negative overdrives [1].

If the required tolerance in code bin width is B, then the overdrive voltage is selected to satisfy the following condition.

$$V_{OD} \geq \sigma \cdot max\left(3, \sqrt{\frac{3}{2B}}\right) \tag{6}$$

where σ is the combined rms noise level (in Volts) of the signal source and the ADC.

If the required tolerance in transition level is B, then the overdrive voltage is selected to satisfy the following condition.

$$V_{OD} \geq \sigma \cdot max\left(2, \frac{\sigma 2^N}{VB}\right) \tag{7}$$

The effect of noise on the results is not random, but systematic. The error is largest near the peaks of the sine wave; the overdrive keeps the measurements far enough from the peaks to make the error as small as desired. The amount of overdrive in (6) and (7) is sufficient to keep the errors due to noise to $\leq B/3$ code bin widths so that these errors are neglible when added to the statistical errors due to taking finite number of samples.

3.3 Selection of Signal Frequency

To obtain meaningful measurements of transition levels and of integral and differential nonlinearity, it is important to choose the signal frequency low enough so that dynamic errors are negligible. The frequency should be selected such that, there must be an exact integer number of cycles in a record, and the number of cycles in a record must be relatively prime to the number of samples in the record. This guarantees that the samples in each record are uniformly distributed in phase from 0 to 2π. The selection procedure for the frequency to meet above requirements is given next [1].

> Choose the number of cycles per record, D, and a record length, M, such that $M + 1$ is an integer multiple of D. Choose the ratio of the signal frequency to the sampling frequency by the following formula,

$$\frac{F}{F_s} = \frac{D}{M} \tag{8}$$

where,

F = the signal frequency, and
F_s = the sampling frequency.

It can be shown that the larger values of M or D require more accurate frequencies. Also, fewer total number of samples are required with larger values of M, so the best approach is to choose the largest value of M compatible with the frequency accuracy obtainable.

3.4 Required Number of Samples

The relation giving the number of records required for a given tolerance and confidence level contain a constant that depends on whether the confidence level is for individual values or for worst case values. For worst case values the constant depends on the number of bits, N, of the ADC. In both the cases, the values from table (1) are used. The values Z_α and $Z_{N,\alpha}$ in the table are defined as follows [1].

> If x is a random variable with a Guassian distribution with a mean of zero and a standard deviation of one, then the probability that $|x| \geq Z_\alpha$ is 2α. If x is the maximum of the absolute values of 2^N independent random variables with mean zero and standard deviation one, then the probability that $|x| \geq Z_{N,\alpha}$ is 2α. The values of $Z_{N,u/2}$ are calculated by the formula,

$$Z_{N,u/2} = \sqrt{2} \cdot erfc^{-1}[1 - (1-u)^{2^{-N}}]$$

where, $erfc$ is the complementary error function.

Table 1: Table for selecting constant [1]

u	$Z_{u/2}$	$Z_{4,u/2}$	$Z_{8,u/2}$	$Z_{12,u/2}$	$Z_{16,u/2}$	$Z_{20,u/2}$
0.2	1.28	2.46	3.33	4.04	4.64	5.19
0.1	1.64	2.72	3.53	4.21	4.80	5.33
0.05	1.96	2.95	3.72	4.37	4.94	5.46
0.02	2.33	3.22	3.95	4.57	5.12	5.62
0.01	2.58	3.42	4.11	4.71	5.25	5.74
0.005	2.81	3.60	4.27	4.85	5.38	5.85
0.002	3.09	3.84	4.47	5.03	5.54	6.01
0.001	3.29	4.00	4.62	5.16	5.66	6.12

Values of $Z_{u/2}$ are calculated by same formula using $N = 0$. The number of records required also depends on whether the tolerances are specified for transition levels (INL) or for code bin widths (DNL). After choosing the record length, M, the number of records required to obtain a tolerance of B and confidence of $1 - u$ is given by [1],

$$R = C\left[\frac{2^{N-1}K_u}{B}\right]^2\left[\alpha\frac{\pi}{M}\right]\left[1.13\left(\frac{\sigma^*}{V}\right) + 0.2\left(\alpha\frac{\pi}{M}\right)\right] \tag{9}$$

4 Applications

The applications of the Histogram Testing covers calculation of most important parameters of the ADC viz. differential nonlinearity, integral nonlinearity, offset error, gain error etc. Apart from these, effective number of bits of ADC can be determined by this technique. The *Integral Nonlinearity* and *Differential Nonlinearity* are discussed here and determining *ADC Effective number of Bits* is introduced briefly in the following paragraphs.

4.1 Integral Nonlinearity

Integral nonlinearity is the deviation of the transfer curve from ideality [2]. Mathematically, Integral nonlinearity is defined in terms of code bin widths. For given values of gain and offset, Integral nonlinearity is defined as follows:

$$\begin{aligned} INL[k] &= \frac{\epsilon[k]}{Q} \\ INL &= max|INL[k]| \end{aligned} \tag{10}$$

4.2 Differential Nonlinearity

Differential nonlinearity is the deviation from the least significant bit (LSB) of the range of input voltages that give the same output code. The number of counts in the i^{th} bin divided by the total number of samples N, is the width of the bin as a fraction of full scale [2]. The ratio of bin width to the ideal bin width is the differential linearity and should be unity. Subtracting one LSB gives the differential nonlinearity. Mathematically, differential nonlinearity is defined in terms of code bin widths. For given values of gain and offset, differential nonlinearity is defined as follows [1]:

$$\begin{aligned} DNL[k] &= \frac{G \cdot W[k] - Q}{Q} \\ DNL &= max|DNL[k]| \end{aligned} \tag{11}$$

4.3 ADC Effective Number of Bits

One of the application of sinewave histogram testing of ADC is to determine the effective number of bits (ENOB). The effective number of bits of an ADC is figure of indication of how close the ADC can work to the ideal performance. The figure can be fraction as well,

varying from 0 to actual number of bits of ADC. The detailed method for estimation of ENOB using sinewave histogram testing approach is given in [4]

Here, we consider the ADC under test is bipolar one, with n bits. The threshold (bit transition) voltage for level k is given by [4]:

$$V_k = -A\cos\left[\frac{\pi \cdot ch(k)}{N}\right], \quad k = 1, 2, \ldots, 2^n \tag{12}$$

where, N be the total number of samples taken. and $ch(k)$ is as defined in (1) known as *Cumulative Histogram.*

Denoting the quantization step size by Δ, and assuming no missing codes for simplicity, the ADC transfer characteristic is given by:

$$V_o = -\Delta \cdot 2^{n-1} + \Delta \sum_{i=1}^{2^n-1} u[V_{in} - V_i] \tag{13}$$

where, V_{in} and V_o are the ADC input and output voltages, respectively, and $u[\cdot]$ is the step function. When missing codes exist, this equation has to be modified accordingly. The ADC quantization error function is taken as

$$e(V_{in}) = V_o - V_{in}$$

For an ideal ADC, e is a sawtooth waveform with zero mean and uniform distribution between $\pm\Delta/2$, but for non-ideal ADC, e is different. It can be shown that the quantization power associated with level k is given by

$$P_k = ({a_k}^2 + a_k b_k + {b_k}^2)/3 \tag{14}$$

where the term $a_k b_k$ is either positive or negative. It is obvious that,

$$a_k = (-2^{n-1} + k)\Delta - V_k$$

$$b_k = (-2^{n-1} + k)\Delta - V_{k+1}$$

$$I_k = V_{k+1} - V_k \tag{15}$$

where k lies in the range $1 \leq k \leq 2^n$. Now the average quantization power, ${\sigma_q}^2$, of an n-bit ADC is a weighted average of all the individual noise powers P_k throughout the entire voltage range given by

$$\sum_{k=1}^{2^n} l_k = 2^n \cdot \Delta. \tag{16}$$

Thus

$$\sigma_q{}^2 = \frac{1}{2^n \Delta} \sum_{k=1}^{2^n} l_k P_k \tag{17}$$

From (14) and (17) it follows that,

$$\sigma_q{}^2 = \frac{1}{3(2^n \Delta)} \sum_{k=1}^{2^n} l_k (a_k{}^2 + a_k b_k + b_k{}^2) \tag{18}$$

which is directly computed from the actual ADC transfer charactristics.

Denoting the ADC reference voltage by V_{ref}, the effective number of bits, n_1, is determined from:

$$\frac{\sigma_q{}^2(actual)}{\sigma_q{}^2(ideal)} = \frac{\left(\frac{V_{ref}}{2^{n_1}}\right)/12}{\left(\frac{V_{ref}}{2^n}\right)^2/12} \tag{19}$$

therefore,

$$n_1 = n - \log_2 \left[\frac{\sigma_q(actual)}{\sigma_q(ideal)}\right] \tag{20}$$

For arbitrary input signals, which are equi-probable throughuot the ADC voltage range, it is known that,

$$\sigma_q{}^2(ideal) = \frac{\Delta^2}{12} \tag{21}$$

Thus (20) and (21) lead to

$$n_1 = n - \log_2 \left[\frac{\sqrt{12}\sigma_q(actual)}{\Delta}\right] \tag{22}$$

5 Comparison with Classical Methods

A classical ADC testing method is shown schematically in fig.(4)(Adapted from [2]). The integrator is driven to each transition and held at that voltage while a computer controlled DVM measures the transition point. This is an extremely slow process, since the integrator loop must settle and then the DVM takes a reading.

The first drawback to this test is that the accuracy of the test depend upon the DVM. Also this technique is static testing of ADC because in this method ADC is measuring a dc voltage, not a high frequency input. Hence there is no measurement of dynamic

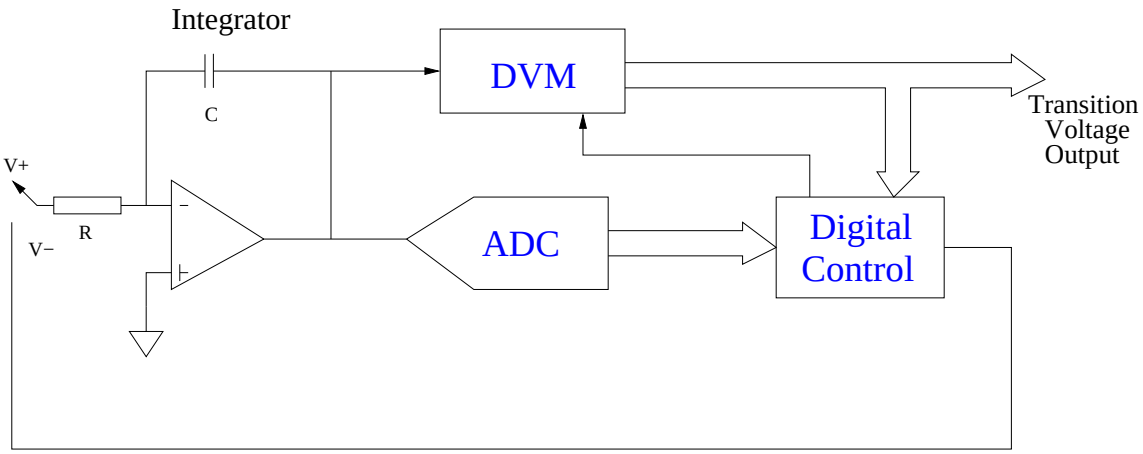

Figure 4: Classical Method of ADC Testing.

errors. With the histogram, the input can be a high frequency signal as desired to the test, for measurement of frequency dependent errors.

Testing a high precision converter by the classical method can be in error due to noise at the ADC input. But the histogram test being statistical and sampling each bin many times rather than once will average out any random noise.

The precision of the classical test is limited by the DVM. But in the histogram test, taking more samples increases the precision. With a histogram test, the input source must be known to more precision than the ADC and can be easily verified with a spectrum analyser.

The integrator loop takes approximately 5 Sec to measure each transition or $5\frac{2}{3}$ Hrs to completely test a 12 bit ADC [2]. If the precision DAC is used instead of an integrator, the speed should increase by a factor of 10 to about 30 min, which is still very slow. With Histogram test method, the time of testing reduces considerably. In case of mass production testing, this is directly related to economical savings.

6 Conclusion

In the report, the Sinewave Histogram Testing of ADC by using uniform sampling has been discussed in detail while the Random sampling and Quasi-coherent sampling has been introduced in brief. The selection of test waveform and detailed measurement procedure has been presented. The formulas for required amount of overdrive for reducing the errors have been given as a function of noise level. It has been shown that if the ratio of sampling frequency to signal frequency is chosen appropriately, the number of records

required to obtain any desired tolerance and confidence level is smaller than that required with Random sampling. Application of Histogram Testing for determining the INL, DNL and effective number of bits have been discussed.

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