Capacitance Effects ON D/A Converters

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Abstract **: This paper discusses the effects of parasitic capacitances on various architectures of Digital to Analog Converters. These parasitic elements govern the performance of data converters as they contribute to various error parameters. To select a suitable architecture for a particular application, one has to consider the effect of parasitic elements, also for high speed operation, the parasitic capacitance is a major issue. Here, we treat various architectures of DAC for capacitance effects from the point of view of high speed operation and look for ways to keep their effects to the minimum.**

Index terms **: Spurious free dynamic range (SFDR), Integral non linearity (INL), Differential non linearity (DNL), Current steering.**

I. INTRODUCTION

There is a continuous pressure on designers to improve the speed performance of data converters as well as to have a high resolution. Applications like HDTV demand D/A Converters with operating speed of ten's of MHz and resolution of 10 bits or better. Some audio and instrumentation applications demand resolutions better than 16 bits. Moreover, cost aspects, integration with memories and digital processing IC's mandate the CMOS implementation. There are various architectures which support high resolution and are monotonous but exhibit high parasitic capacitance, limiting the speed of operation.

The resistor string architecture supports high resolution but puts large input capacitance on buffer, that limits its speed. Popular CMOS current steering versions are low cost, low power, but their maximum speed is limited by capacitances in basic current cell. Such effects are studied and alternative schemes are considered so as to deal with the effects of the parasitic capacitances. First we discuss some DAC parameters to which parasitics contribute and then treat the architectures.

II. DAC PARAMETERS

Monotonicity

For a monotonic function, the derivative of the function with respect to independent variable never becomes negative. That means its slope never changes its sign. A digital-to-analog converter is said to be monotonic if, as the DAC code is incremented, the analog output never decreases. Even if the rise in the value is not equal to the theoretically determined step size, as long as its rise for incremented code, we have a monotonous DAC. In other words we say that if the converter steps deviate at the maximum by ±1/2LSB from the correct step size, our digital-to-analog converter is monotonic. Same is true for DAC specified with DNL (explained below) of < ½ LSB[6].

Gain Error

There is a difference between ideal (say theoretically specified) transfer function and actual one. The slope of the function theoretically specified or given by data sheet differs from actually observed one. This is known as gain error. A gain error poses problems only if it drifts

significantly. The causes for the gain error are temperature and time dependence of gain and also the stability of reference source used.

Zero Error

This is the deviation of output from true zero when the input code corresponds to appropriate code for zero output. Zero error can be particularly troublesome if it drifts and is more likely to be a problem than gain error. Sometimes it is termed as "Offset error"[6][9].

Settling Time

This parameter is specified for a Full-scale change. It can be defined as the time taken from the change in the input code for the converter to produce output within some specified error band.

Glitch

Glitch is unintended excursion in the output of DAC. A switching transient can appear on the output during a code transition. Data skews put us in such situation. Glitch characteristics depend nonlinearly on codes, hence they result in spurious tones in output frequency spectrum. Thus degrade the SFDR (explained below) [6].

Data skew occurs when all the digital inputs do not change at exactly the same time. It can be defined as the difference between Tplh and Tphl. Tplh is the positive going propagation delay while Tphl is its negative counterpart. Lets consider an example of this phenomenon, for a 12-bit DAC. For a 1LSB change around the MSB, the code would change from 0111 1111 1111 to 1000 0000 0000 under ideal conditions. With the presence of data skew, all bits might not change at the same time and we may have some intermediate code existing. To think of worst, consider that the MSB changed more rapidly compared to the rest of the bits, so that the code transition pattern would be: 0111 1111 1111 to 1111 1111 1111 to 1000 0000 0000, as shown in fig. 1.

Here, we see that, for a period of time, the DAC output would start to head in the direction of an output that corresponds to unintended intermediate code. Our expected change from the previous code here is 1LSB change, but DAC output is reaching to a very large value in between. This large transient-like waveform that is created at DAC output, is often referred to as a "glitch."

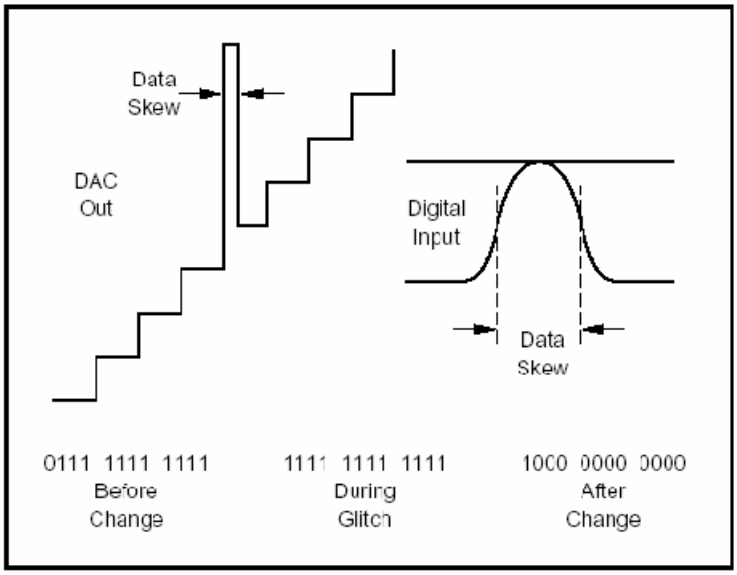

Fig. 1. Glitch in DAC as a result of data skew [3].

Power Supply Sensitivity

It is nothing but the change in output of the DAC due to a change in the power supply voltage(s). We usually express this as %full scale / % supply change.

Compliance and Output Resistance

DAC's with current as well as voltage outputs are available. Compliance and Output Resistance are specified for current and voltage DACs respectively. These parameters relate how close the outputs are from ideal sources under different load conditions. For a fixed load condition, these parameters will appear as a simple gain error. Hence, we prefer to have a fixed load on DAC output.

Accuracy

It is a measure of, how closely the output of actual DAC follows the expected output of ideal DAC, having the same input code, but an ideal reference voltage. However, we note here that even if the full-scale output is accurate, the accuracy of intermediate values will depend upon the Integral Non-Linearity of the converter (explained below).

Resolution

The Resolution of a DAC is the smallest change in the output. It depends on Integral Non-Linearity and Differential Non-Linearity (explained below).

Non-Linearity

It is the deviation from ideal straight line transfer function. Two types of non-linearity in the mapping of input code to output are, INL and DNL.

Integral Non-Linearity

INL [6] is the degree to which the line deviates from the ideal straight line through all the states (or more usefully the line joining the zero and full- scale points). Good INL means that the converter has good accuracy and a low distortion of a digital waveform being converted, i.e. if asked to convert a sine wave, a converter with good INL will produce less harmonic content than one with a poor INL.

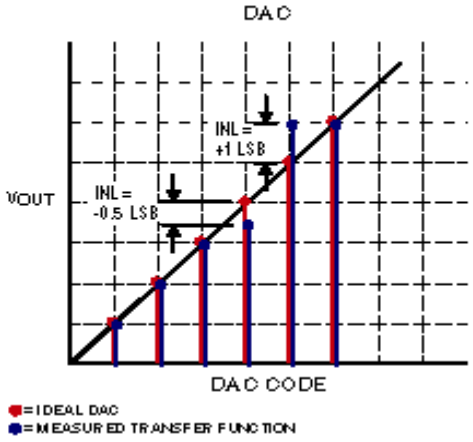

Fig. 2. INL in DAC [6].

Differential Non-Linearity

DNL [6] is the degree to which the steps between the codes are uniform. Good DNL implies good resolution, because all the steps are almost exactly the same size, and a good noise performance . Notice that, good DNL does not mean good INL as there could be a systematic variation in the steps which produces a curve. Even though the deviation for each step is small, the effect is cumulative. However, good INL tends to imply good, but not necessarily excellent, DNL. Crudely speaking INL controls the "straightness" of the transfer characteristic whereas DNL controls the "smoothness". INL and DNL are becoming more important as converters

become more sophisticated. However, at the time of writing, not all manufacturers are good about distinguishing between them and providing the necessary data to assist you in your choices.

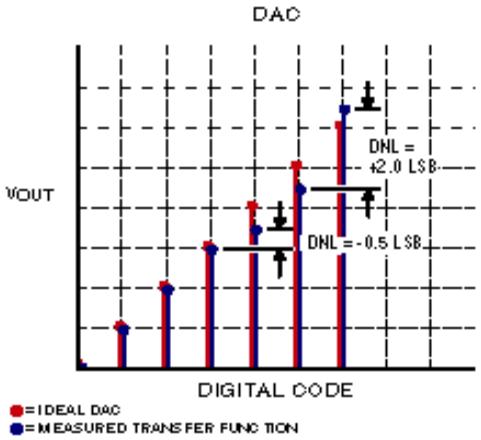

Fig. 3. INL in DAC [6].

Spurious Free Dynamic Range

SFDR [7] is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of the difference in amplitude between the fundamental and the largest harmonically or non-harmonically related spur from DC to the full Nyquist bandwidth (half the DAC sampling rate, or fS/2). A spur is any frequency bin on a spectrum analyzer, or from a Fourier transform, of the analog output of DAC. Fig. 4 shows how SFDR is measured correctly (SFDR is usually specified in dBc).

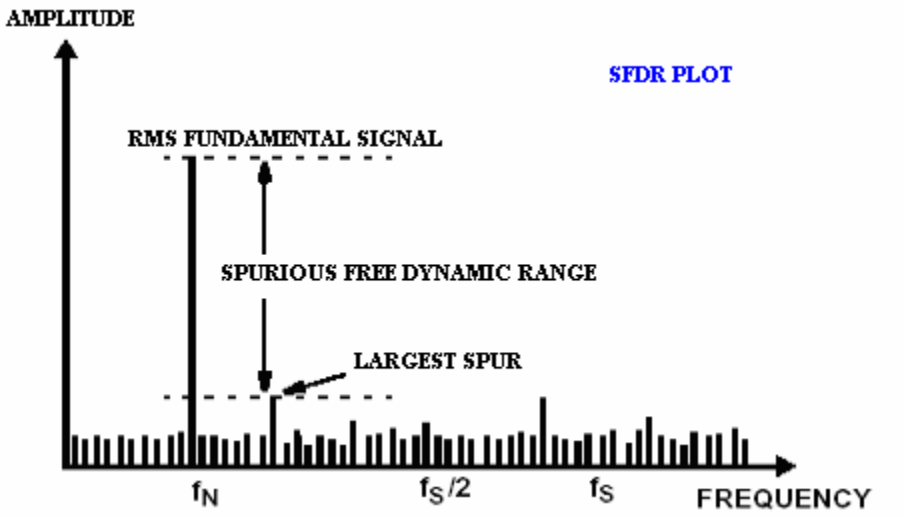

Fig. 4. Measure of spurious free dynamic range [7].

Signal-to-noise and distortion ratio

SNDR is the ratio of RMS value of the sine wave f(IN) (input sine wave for an ADC, reconstructed output sine wave for a DAC) to the RMS value of the noise of the converter extending from DC to the Nyquist frequency, including harmonic content. It is typically expressed in decibels.

$$SNDR = 20Log_{(10)} \frac{Input(volts, RMS)}{Noise + Harmonics}$$

III. DAC ARCHITECTURES AND CAPACITANCE EFFECTS

1. D/A Resistor-String – Binary Switch Architecture.

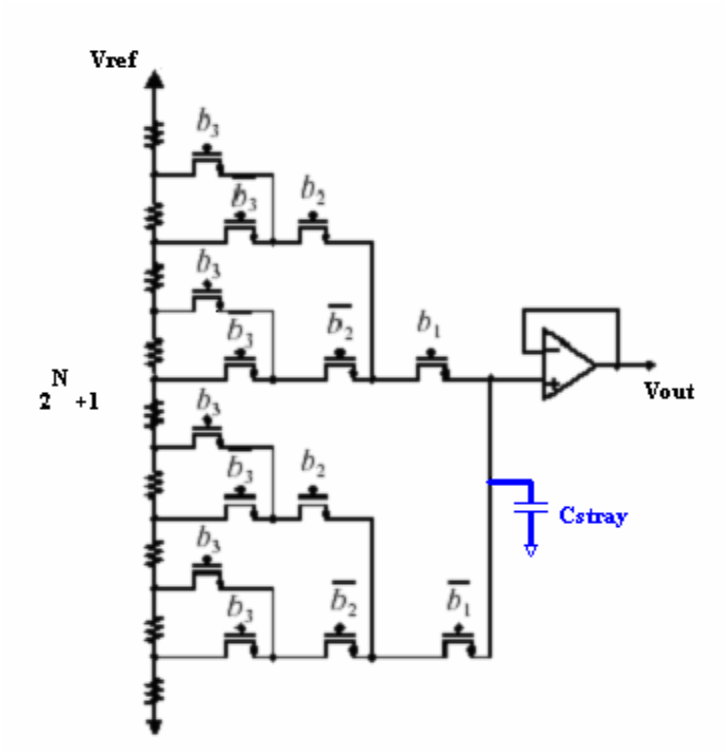

Fig. 5. Resistor-String– Binary Switch D/A Architecture [8].

This architecture uses (2^N+1) resistors. Thus the string divides reference voltage in 2^N parts at respective nodes. Each voltage corresponding to every input code is fed to output buffer through proper selection of switches. LSB is connected to switches towards resister string and MSB towards buffer. This architecture is guaranteed to be monotonic. Being a string based architecture, it is a high resolution structure and can support 16 bit DAC with good accuracy.

This scheme, as we can see, poses *less capacitive* load on input of buffer. But delay through the switch network limits the speed of operation.

2. D/A Resistor-String — Digital Decoding

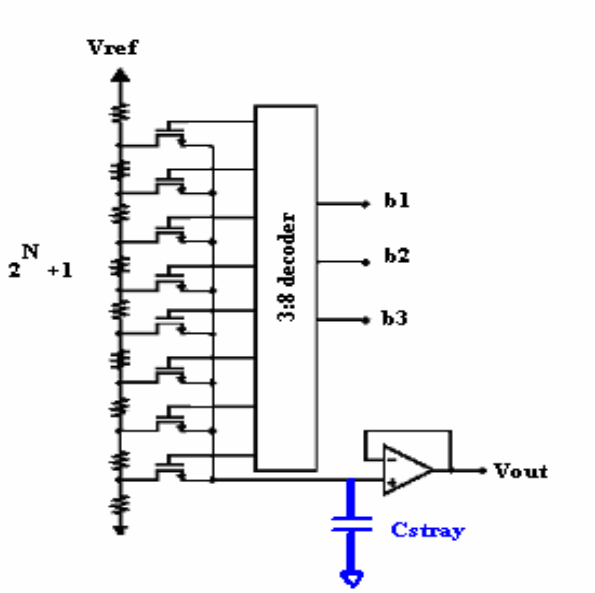

Fig. 6. Resistor-String– Digital Decoding D/A Architecture [8].

This architecture also, uses (2^N+1) resistors. and the string divides reference voltage in 2^N parts. But, an internal N : 2^N digital decoder is used to select one of 2^N switches. When any one of 2^N analog switches, corresponding to input code, turns on, it transfers the voltage at that node to input of buffer.

So, as scheme shows, delay through the switches is less, but there is a *large capacitive load* at the input of the buffer, as all the switches are connected to the same line. It shares the other features of the resistor string based architecture.

3. Binary-Weighted Resistor D/A's.

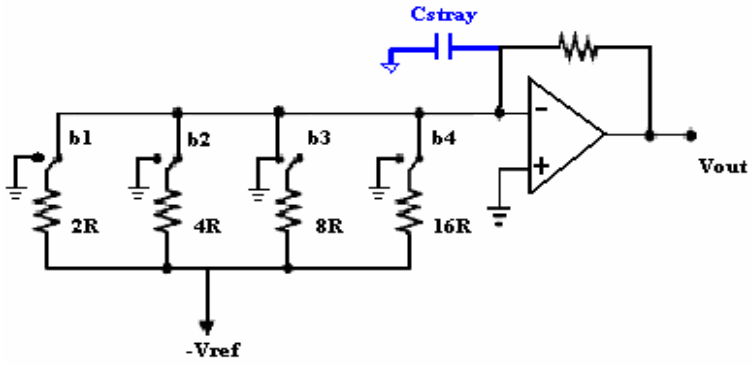

Fig. 7. Binary-Weighted Resistor D/A Architecture [1].

This architecture can be called as current mode, as currents are switched to generate the output. It uses only N binary weighted resistors, as shown in fig. 7. So, important aspect to note is that the resistor and the current ratios are of the order 2^N. High accuracy can not be achieved using this method as it is difficult to accurately match the separate resistors and switches over

such a wide range of currents. If the current at full scale output of the 12-bit DAC is 10mA, then at the output corresponding to one LSB, current would be 4.9 μamp. The good feature of this binary weighted type DAC is that there would be no wasted current and the net power dissipation for this type of digital to analog converter would be the least as compared to other design approaches. Also, there is no guarantee of the DAC being monotonic and it is prone to glitches.

Here, from the scheme, note that, the switch *capacitances do not experience any voltage change*, as the voltage at node is constant (ground). Thus, it is a high speed implementation.

4. R-2R Based Resistor Ladders with current sources

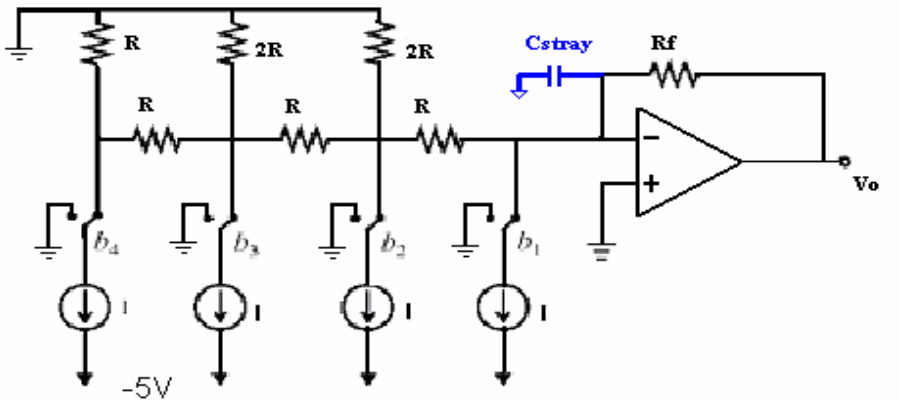

Fig. 8. R-2R Based Resistor Ladder D/A, current source Architecture [1].

This architecture uses *equal* valued current sources and *resistors ratios are of the order* 2. Better matching is possible compared to binary weighted architecture where ratios are large. So, there is no need to scale size of the switches. Thus this architecture provides better monotonicity and accuracy and, it is less prone to glitches.

Here, the scheme shows that, switch *capacitances experience voltage change* as voltage at nodes changes as per switch positions. Thus there is a speed limitation for this implementation.

5. R-2R Based Resistor Ladder switch voltage source

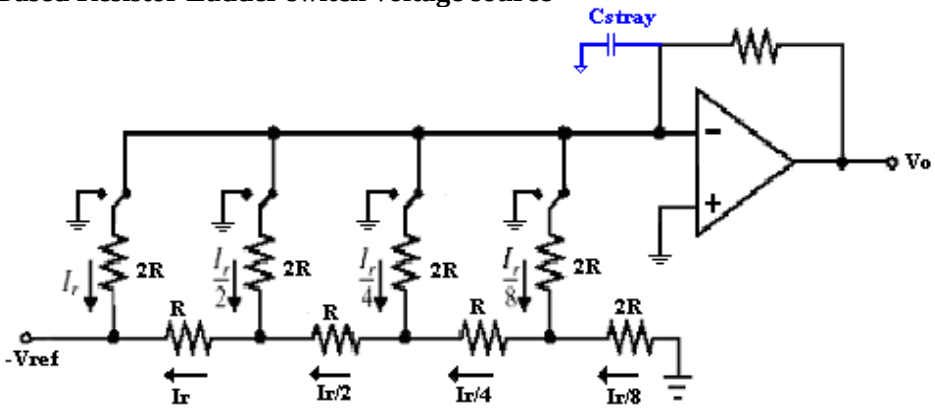

Fig. 9. R-2R Based Resistor Ladder D/A, Vref Architecture [1].

This is again R-2R based DAC architecture, where resistance ratios are of the order 2, but here, the *currents* which are switched are *having ratios of the order* 2^N, means they are scaled. Thus, for good accuracy we should scale size of the switchs. Also, the monotonicity is poor compared to above R-2R DAC with equal current sources.

In this architecture scheme, we note that, switch *capacitances do not experience any voltage change* as voltage at the node is at ground. Thus, this is a fast architecture.

6. Current-Steered D/A

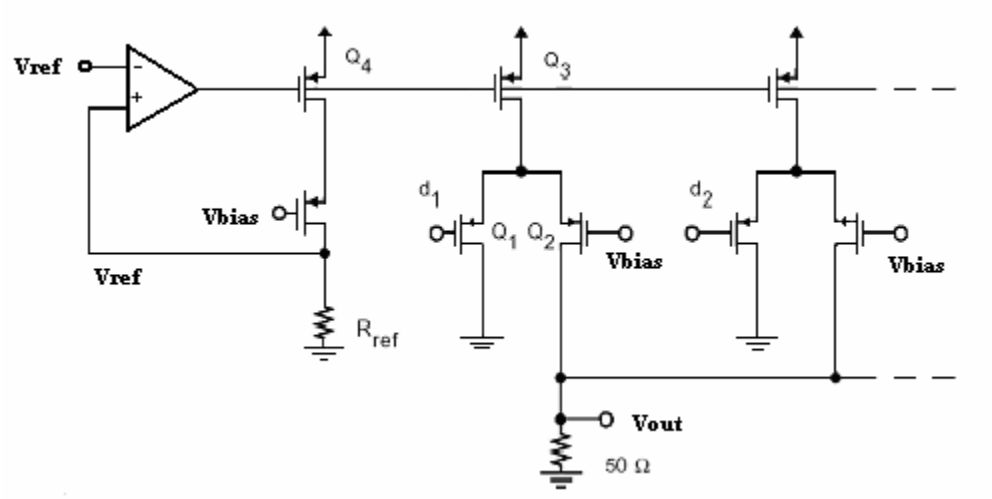

Fig. 10. Current steering D/A Architecture [8]

This is a very popular architecture [8], suitable for high speed implementation, but at the cost of some static dissipation. It operates as cascode current sources with differential switches which steer the current to and from the output. At the output, we need a current to voltage converter. A bipolar transistor equivalent of this circuit uses switches that are driven in a non-saturating manner. In order to steer the current as fast as possible through the output switch, it is very important to avoid saturation; once a transistor saturates, the recovery time can easily increase by a factor of twenty or more [3].

In the above architecture shown, basic current cell has some parasitics which degrade its performance. Parasitic *Tail Capacitance* appearing at the current source transistor, *reduces current source impedance* at higher frequencies.

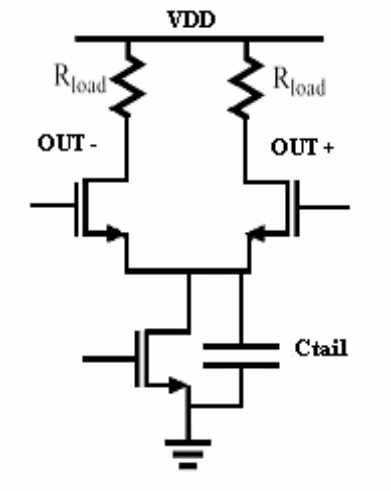

Fig. 11-1. Basic current source cell [1].

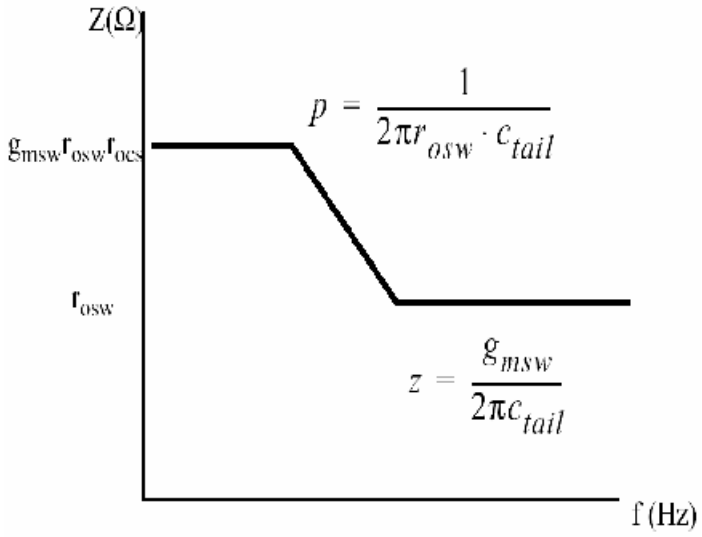

Fig.11-2. Output impedance as function of frequency [1].

It is important to note here that, output impedance of the current source should be high, otherwise the SFDR parameter of DAC degrades. This architecture has a code dependent output resistance. If the ratio of current source output resistance to load resistance is *Low* then INL, SFDR degrades. Thus, it becomes more critical for higher resolution. So, the *Tail Node capacitance must be minimized*.

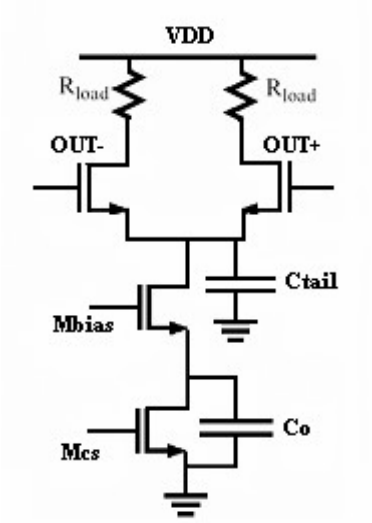

Fig. 12-1. Basic current source cell in cascode configuration [1].

Cascoding, as shown in Fig. 12-1, can be employed at the tail node. It will extend the frequency range with acceptable current source output impedance, as shown in Fig. 12-2.

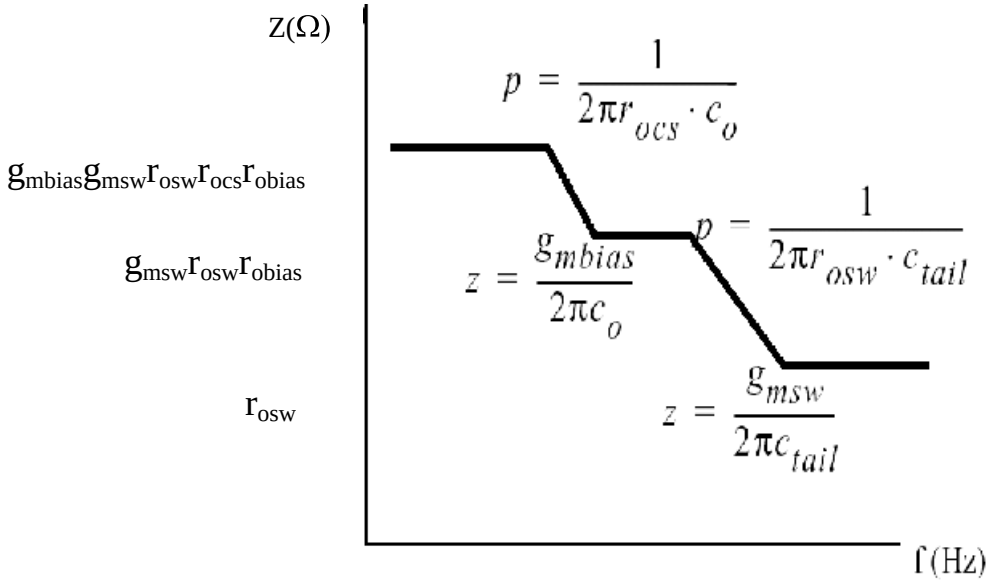

Fig. 12-2. Output impedance as function of frequency for cascode configuration [1].

Tail capacitance is a major contributor in current source switching non idealities, shown in Fig. 13. Charging and discharging of Ctail will limits the speed of the converter. Hence, Switch drivers must be designed to prevent charging/discharging of Ctail.

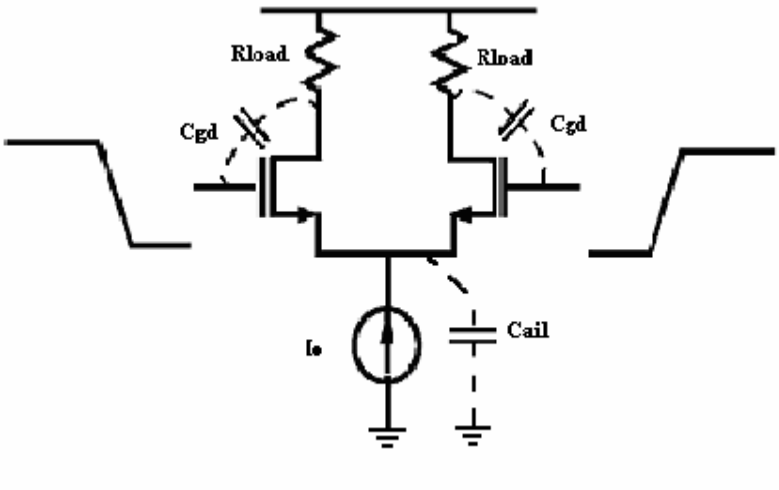

Fig. 13. Switching non idealities [2].

The voltage variation in the common source node of the differential pair causes the stray capacitance to be charged and discharged which in turn slows down the settling of the output We should use high Crossing point signals, which guarantees that both switch transistors do not turn off at the same time, and parasitic Ctail does not discharge current. The voltage variation is minimized by overlapping the control signals in such a way that their cross point lies slightly below the maximum voltage level.

Also, *Low swing* signals minimize capacitively coupled switching noise to the output nodes. So, switch drivers must be designed to minimize coupling through parasitic Cgd to the output nodes.

High Crossing point and *Low swing* signals can be generated as shown in the Fig. 14. It uses a differential buffer with a cross coupled PMOS load [10]. Proper threshold voltage of n channel ensures high crossing and the swing is limited by limiting the amplitudes of the control signals just high enough for switching.

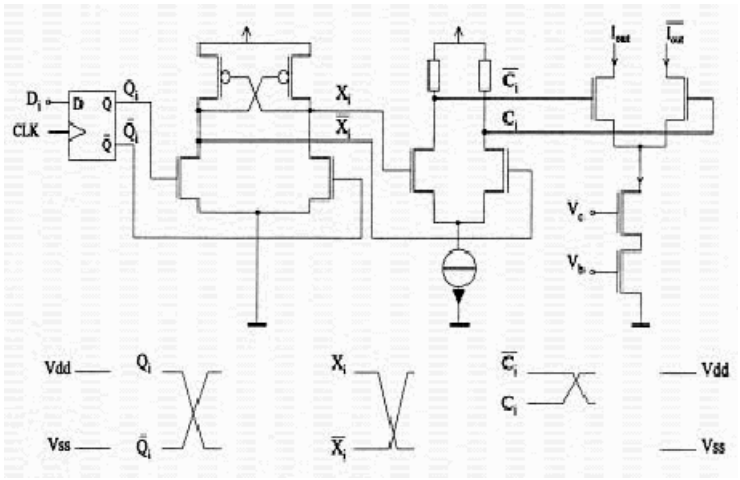

Fig. 14. Generating high crossing point and low swing signals [10].

Switched current source cell matrix based Digital to Analog converters are very popular. They provide fast settling and can operate at high speed. But, as we go for higher resolution 10 bits or more, we start facing the problems of matching. Mutual matching between the parameters of current sources and switches contribute to error, which is comparable to quantization error or *even more* for higher resolution. So, current source cell matrix based architectures become unsuitable when high resolution DACs are designed.

Earlier, in this report we have discussed Resistor string architectures. Resistors on chip can have high mutual agreement amongst each other if they hold same resistance. Thus a Digital to Analog converters based on this architecture are inherently of high resolution type. The circuit in Fig. 15 shows such architecture, though requiring 2^N resistors but a modified version, and a technique is used for operating speed to improve upon.

Folded-resistor-string D/A

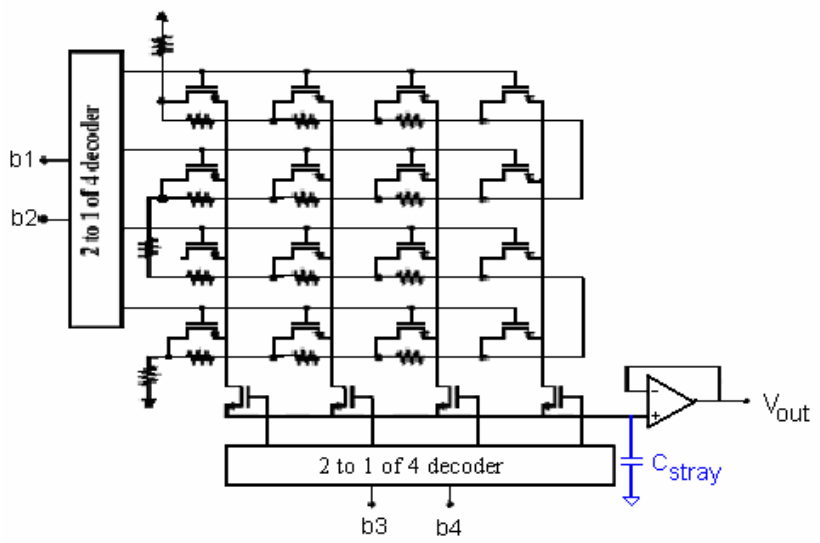

Fig. 15. Folded Resistor-String D/A Architecture [5].

The Input code selects the output analog voltage by activating two series analog switches. One switch is activated by MSB's decoder (with inputs b1, b2) and other switch is activated by LSB's decoder(with inputs b3, b4). This architecture will allow us to design converter with high Integral and Differential linearity and it is also intrinsically monotonic.

Although folded sting architecture poses less capacitance load over the single bus (not folded) approach, which explained earlier as resistor string converter, but there are considerable number of analog switches and it causes large capacitive load on buffer input. Thus, operating speed is limited.

Before going for the proposed solution we take a look into the obvious question, why not to have a switch with low capacitance? Going for the low switch capacitance, we need to decrease the channel width. But this creates a problem, switch ON resistance also increases with decrease in width which in turn reduces the settling time. So, we need the width for faster settling. Thus, we have to reach a trade-off and accept some amount of capacitance.

Effect of this parasitic capacitance can be reduced by providing *Active Compensation*.

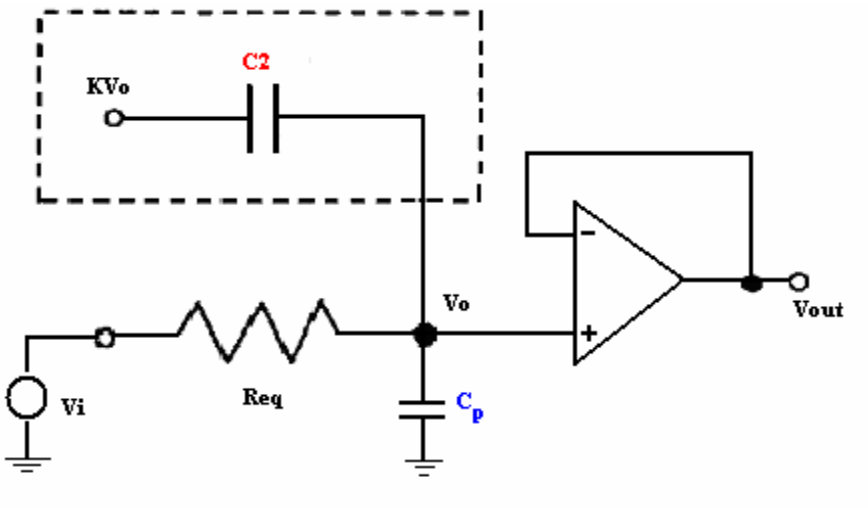

Fig. 16. Basic idea of active compensation [5].

The circuit in Fig. 16 shows the output section of the converter [5]. Vi is the converted voltage delivered by resistive matrix. The resistance R_{eq} is the equivalent resistance of switch on-resistance and the equivalent resistance of resistance matrix. The capacitor Cp is given by:

$$C_p \cong C_{in,b} + 2C_{sw,on} + (2^{\frac{N}{2}} - 1)C_{sw,off}. \tag{1}$$

where $C_{in,b}$ is the input capacitance of the output buffer. $C_{sw,on}$ and $C_{sw,off}$ are paracitic capacitances of a closed and open switch, respectively, and N is the resolution of the converter.

Here we note that, the *time constant* of the effective resistance and capacitance appearing at the input of buffer, causes the speed limitation. Dynamic performance can be improved by active compensation for Cp. This can be done as shown in the above diagram. An additional capacitance Cp is connected to the input of the buffer, and is driven by the voltage *kVo* which is obtained by suitable amplification of Vo. The voltage Vo can be calculated as follows:

$$V_o s(k-1)C_2 + \frac{V_i}{R_{eq}} = V_o \frac{(1 + sC_p R_{eq})}{R_{eq}} \tag{2}$$

Hence,

$$\frac{V_o}{V_i} = \frac{1}{1 + sR_{eq}(C_p - (k-1)C_2)}. \tag{3}$$

The transfer function in equation (3), if we compared with standard RC low pass transfer function, which is similar to the uncompensated model of DAC circuit at input of buffer, the equivalent capacitance has reduced :

$$C_{eq} = C_p - (k-1)C_2. \tag{4}$$

The new value of the time constant, R_{eq} C_{eq} depends on gain k and injection capacitance C_2. Dependence is such that it reduces the effect of C_{eq}. For the compensation loop to be stable, k must be smaller than $1 + Cp / C_2$. Bandwidth of the amplifier used for gain k must be high.

IV. CONCLUSION

Current steering architectures are capable of providing high operating speeds, if the basic current source cell is properly designed. Effects of parasitic tail capacitance can be minimized using cascode configuration and designing switch drivers so that they have high crossing to avoid charge and discharge of Ctail, as well as extended driving transitions can be used to minimize coupling at output through parasitic capacitances. For high resolution application where accuracy is important and monotonous DAC is required, resistor string architecture can be used with active compensation for high buffer input capacitance so as to have high speed operation.

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