Rating Issues and DC Bus Capacitor Selection for Design of a Three-Phase Four-Wire Active Filters

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Abstract- This paper presents the required harmonic power and rating issues of the active filter and power components. A design procedure is presented to select the dc bus capacitor that covers all modes of operation. The effect of the dc bus ripple on the compensation capacity is analyzed. A typical problem is included to illustrate the design approach followed by a simulation results showing the static performance of the active filter.

I. INTRODUCTION

A design procedure to select the capacitor value in such a way as to ensure the proper operation of the harmonic compensator for various load environments. The impact of the ripple voltage on the active filter compensation capability is also investigated. Rating issues of the active filter and the power components are also considered as a function of various system parameters. A problem is considered to illustrate the complete design process for the power circuit. Finally, simulation results are presented to show the static performance of the active filter and to confirm theoretical calculations.

II. DESIGN OF THE CAPACITORS

Under steady state operating conditions the dc voltage control loop keeps the dc voltage constant. However, transient changes in the instantaneous power absorbed by the load generate voltage fluctuations across the dc capacitor. The amplitude of these voltage fluctuations can be controlled effectively with an appropriate dc capacitor value [1]:

When designing the capacitor the following assumptions are made:

i) In steady state, the fluctuating voltage of the capacitor is very small compared to the average voltage.

ii) The converter is lossless.

The voltage fluctuation in the dc capacitor under steady state is due to the variation of the harmonic power flow [1],[2] and the energy stored in the inductor. The current in the inductor has two components, the distorted current and the ripple current superimposed on the reference due to the switching action of the converter. The first current is periodic ac waveform, hence energy variation is null. The second part consist of the energy that the inductor discharges in the capacitor within one switching period. During the on state, energy is accumulated across the inductor and this energy is absorbed by the capacitor during the off state. Because the switching frequency is high, the effect of this energy variation on the dc bus is neglected.

![Fig.1 Four wire half-bridge active filter](image)

For the single phase case, by equalizing the instantaneous input power to the instantaneous output power we obtain.

![Fig.2 Half-bridge active filter](image)
Fig. 3 Active filter control block diagram

\[ v_s \cdot i_{af} = i_{dc1} \cdot v_{dc1} + i_{dc2} \cdot v_{dc2} \]  
(1)

\[ v_{dc1} = V_{dc1} + \tilde{V}_{dc1} \quad \text{and} \quad v_{dc2} = V_{dc2} + \tilde{V}_{dc2} \]  
(2)

\[ i_{af} = 2C \cdot \frac{dV_{dc1}}{dt} \quad \text{and} \quad i_{af} = 2C \cdot \frac{dV_{dc2}}{dt} \]  
(3)

Using the fact that the average dc voltage of each capacitor are approximately equal, (1) could be written as:

\[ v_s \cdot i_{af} = CV_{dc} \cdot \frac{dV_{dc}}{dt} \]  
(4)

\[ \dot{V}_s = \sqrt{2} \cdot \sin \omega t \]  
(5)

\[ i_{af} = \sum_{h=3,5}^{\infty} I_{afh} \cdot \sqrt{2} \cdot \sin(h \cdot \omega t - \phi_h) \]  
(6)

The voltage fluctuation, \( \Delta V_{dc} \), across the capacitor is:

\[ \Delta V_{dc} = (V)_{\max} - (V)_{\min} \]  
(7)

The energy variation, \( \Delta E \), across the capacitor is:

\[ \Delta E = E_{\max} - E_{\min} \]  
where

\[ E = \int_0^t v_s \cdot i_{af} \cdot dt \]  
(9)

\[ \Delta V_{dc} = \frac{\Delta E}{C \cdot V_{dc}} \]  
(10)

It can be shown that using reasonably high switching frequency the instantaneous energy can be written as:

\[ E = \int_0^t v_s \cdot i_{load,h} \cdot dt \]  
(11)

Equation (10) shows that the voltage fluctuation across the capacitor is a function of the converter instantaneous energy fluctuation, the dc bus voltage and the size of the capacitor.

The dc voltage regulation ratio is defined as:

\[ r_v = \frac{\Delta V_{dc}}{V_{dc}} \]  
(12)

Finally, the minimum capacitor value to meet the required voltage regulation is given by:

\[ C_{\min} = \frac{1}{V_{dc}^2 \cdot r_v} \Delta E \]  
(13)

For three phase case equation (13) is replaced by:

\[ E = \int_0^t \left( \sum_{j=a,b,c} v_{s,j} \cdot i_{j,h} \right) \cdot dt \]  
(14)

The capacitors are designed to limit the dc voltage to a specified value, typically 1 to 2 %. In this case the capacitor should designed for the worst case. Since the active filter will operate in several modes (single phase or unbalanced load). It follows that the capacitor value is load dependent and simulation is one way of evaluating the worst possible case. The worst case occurs when the active filter is compensating a single phase load. The harmonic frequencies of the dc bus voltage in the case of a single phase load, can be found by expanding (13),

\[ E = \int_0^t \sum_{h=2,4} (V_s \cdot \sqrt{2} \cdot I_{h} \cdot \sqrt{2} \cdot \sin(\omega t) \cdot \sin(h \cdot \omega t - \phi_h)) \cdot dt \]  
(15)

Transforming the product into summation yields:

\[ E = \int_0^t \left\{ \sum_{h=2,4} \left[ 2V_s \cdot I_h \cdot (\cos[(h-1)\omega t - \phi_h] - \cos(h+1)\omega t - \phi_h] \right) \right\} \cdot dt \]  
(16)

Integrating above equation we obtain:

\[ E = \sum_{h=2,4} \left[ V_s \cdot I_h \cdot \frac{1}{(h-1)\omega} \sin[(h-1)\omega t - \phi_h] - \frac{1}{(h+1)\omega} \sin[(h+1)\omega t - \phi_h] \right] + cte \]  
(17)

Where cte is a constant of integration. The above expression shows that the dc bus voltage has harmonic components at twice the mains frequency, resulting from the third harmonic of the load, harmonic component at four times the mains frequency, which is the contribution of the third and fifth harmonic of the load, hence all the even harmonics are present in the spectrum of the dc bus voltage. A similar reasoning shows that, under balanced load condition, the spectrum of the dc bus has similar harmonic distribution. However, under balanced load condition, the dc bus ripple components are located at multiples of six times the mains
III. DC CAPACITOR VOLTAGE FOR STEP CHANGING LOAD

In some cases, a load has a sudden change, such as disconnection from the ac line or sudden connection to the ac line. When the load current is dropped, the active filter current has not yet changed until the next cycle. Hence this extra current, \( \Delta I_{af} \), will change the capacitor [2],[3]. Where \( \Delta I_{af} \) is the step drop of the peak value of the active filter accompanied with the drop of the fundamental load current. From (1) we have:

\[
C \cdot \frac{(dv_{dc}^2)}{2} = V_s \cdot i_{af}
\]  

(18)

Let \( V_{dc}(\infty) = V_{dc} + \Delta V_{dc} \), then (18) becomes:

\[
\Delta V_{dc}^2 + 2V_{dc} \cdot \Delta V_{dc} - \frac{4V_s \cdot \sqrt{2} \Delta I_{af}}{C \cdot \omega} = 0
\]  

(19)

The previous equation shows that the voltage rises when the load steps down. For the calculated value \( C \), the voltage rise is obtained by solving the second order equation. If the voltage rise is not permissible, then the new value of the capacitor is obtained by imposing a permissible voltage range. It is found that the new value of the capacitor is greater than the first value obtained before.

Similarly, when the load current has a step increase, the energy stored in the capacitor must be released immediately to support the step increase of the power consumed by the load. In this case the \( \Delta I_{af} \) is replaced by \( -\Delta I_{af} \) and the voltage drop \( \Delta V_{dc} \) is replaced by \( \Delta V_{dc} \) in (19), hence obtaining the voltage drop.

IV. ACTIVE FILTER CURRENT COMPENSATION CAPACITY

The maximum current that the active filter can compensate is calculated in function of the frequency of the current to track. The information is obtained using the maximum rate of rise of the current to compensate as equal to the maximum rate of rise generated by the load.

The current to compensate is given by:

\[
i_n = I_s \cdot \sin(\omega t - \varphi_n)
\]  

(20)

Since the \( di/dt \) capability of the active filter is dictated by

\[
\frac{di_{af}}{dt} = \frac{0.5V_{dc} - V_s \cdot \sqrt{2}}{L_{af}}
\]  

(21)

The compensation capability is calculated by combining (20) and (21):

\[
\hat{I} = \frac{0.5V_{dc} - V_s \cdot \sqrt{2}}{2\pi f_s L_{af}}
\]  

(22)

Fig.5 below shows that the compensation capability of the active filter increases if the dc bus voltage is increased.

V. EFFECT OF THE DC BUS RIPPLE ON THE COMPENSATION CAPABILITY

The effect of the capacitor, a ripple component at twice the mains frequency is considered in the dc bus voltage. The instantaneous dc bus voltage is expressed as:

\[
v_{dc} = V_{dc} + A_r \cdot \sin(2\omega t - \varphi_r)
\]  

(23)

where \( A_r \) is the amplitude of the ripple component. Relating the amplitude of the ripple to the voltage regulation ratio one obtains:

\[
v_{dc} = V_{dc} + \frac{V_{dc}}{2} \cdot r_r \cdot \sin(\omega t - \varphi_r)
\]  

(24)

The compensation capability of the active filter is given by:

\[
\left(\frac{di}{dt}\right)_{af} = \frac{0.5V_{dc} - V_s}{L_{af}}
\]  

(25)

Within a switching period of the converter, the worst case occurs when the ripple component is at its minimum value, thus reducing the driving voltage necessary to generate the \( di/dt \):

\[
\left(\frac{di}{dt}\right)_{af} = \frac{0.5V_{dc} - r_r V_{dc} / 4 - V_s \cdot \sqrt{2}}{L_{af}}
\]  

(26)

Let \( d \) represents the ratio of the \( di/dt \) of the active filter with ripple over the \( di/dt \) of the active filter without ripple. Moreover, this ratio represents also the ratio by which the peak current is reduced in the presence of ripple in the dc bus voltage.

\[
d = \frac{(di/dt)_{with\;ripple}}{(di/dt)_{without\;ripple}}
\]  

(27)

\[
d = \frac{1 - 0.5r_r - m_0}{1 - m_0}
\]  

(28)

The ripple in the dc bus introduces a voltage drop at the output of the active filter, thus reducing the driving voltage across the inductor. The effect of the ripple is presented in fig. 6. The curves show that the compensation capability of the active filter decreases when the ripple in the dc bus voltage increases. A smaller capacitor value is allowed, provide that the \( di/dt \) of active filter remains higher than the \( di/dt \) of the distorting current.
VI. REQUIRED HARMONIC POWER BY THE ACTIVE FILTER

To obtain sinusoidal current at the mains, harmonic power is injected into the system, thus canceling the distorting power of the load. In general case, if reactive power and harmonic power is injected, then

\[ H + Q = \sqrt{\left(\sin \phi\right)^2 + \text{THD}_i^2} \]

From simulation fig. 7 gives the required reactive and harmonic power from the active filter relative to the rating of the load converter, as a function of total harmonic distortion of load current, \( \text{THD}_i \), for several displacement power factors. The curves shows that if reactive power is combined with harmonic compensation, the required rating is substantially increased. Also, the curve shown in simulation shows that the required rating increases with a faster rate as the load \( \text{THD}_i \) increases. For harmonic compensation, the expressions given below are used:

\[ H = V_s I_1 \cdot \text{THD}_i \]

\[ \frac{H}{S_{\text{conv}}} = \frac{\text{THD}_i}{\sqrt{1 + \text{THD}_i^2}} \]

The main difference between combined harmonic and reactive compensation, \( H + Q \), and harmonic injection, \( H \), is power factor correction. In the first case the current in the mains has a unity power factor and sinusoidal power factor and a sinusoidal waveform, in the latter case, the supply is harmonic free, however the supply voltage and current are not in phase.

VII. RATING OF SYNCHRONOUS LINK REACTOR

The rating of the synchronous link reactor is specified in terms of an inductor equivalent rating at 60 Hz, giving an indication of inductor cost/size.

\[ S_{Laf} = \omega L_{af} \left( i_{af} \right)_{\text{rms}}^2 \]

The dominant components in the expression of the active filter current are the low frequency harmonics, therefore we obtain:

\[ \frac{S_{Laf}}{S_{\text{load}}} = \frac{L_{af} \omega I_1}{V_s} \cdot \text{THD}_i \]

VIII. CAPACITOR AND INVERTER RATING

The total VA rating of the dc side capacitors is the product of the rms current and rms voltage:

\[ S_{\text{cap}} = V_{dc1,\text{rms}} I_{dc1,\text{rms}} + V_{dc2,\text{rms}} I_{dc2,\text{rms}} \]

\[ S_{af} = V_{af,\text{rms}} I_{af,\text{rms}} \]

The rating of the inverter is different from the injected harmonic power, since the voltage at the point of common coupling is similar than the terminal voltage of the inverter due to the voltage drop across inductor.

\[ \frac{S_{af}}{S_{\text{load}}} = \frac{S_{\text{cap}}}{S_{\text{load}}} = \text{THD}_i \sqrt{1 + \left( \frac{\nu_{af}}{\nu_s} \right)^2 \sum_{h=2}^{\infty} \left( \frac{I_h}{I_1} \right)^2} \]

IX. SYSTEM UNDER STUDY

Apparent power of the load and supply voltage are selected as base values

\[ S_{\text{base}} = S_{\text{load}} = 3V_s I_1 \]

\[ V_{\text{base}} = V_s \text{ and } I_{\text{base}} = \frac{S_{\text{base}}}{V_{\text{base}}} \]

Fig.4 Per phase equivalent circuit of the system

1. Load specification

In this problem the mains supplying three unbalanced single phase loads, connected between the lines and neutral. Each load consists of a diode rectifier with a capacitive output in parallel with the load resistor. The data for the single phase load is:
\[ V_s = 60V, I_1 = 7.8A \]

\[ I_{h,peak} = 11A, THD_t = 70\% , \]

\[ (di/dt)_{max} @ positive slope = 11KA/s. \]

2. **Active Filter**

The switching frequency is chosen equal to 10.3 kHz. The modulation index must be close as possible to 1.0, so that inverter output exhibits low harmonic content. In this case, modulation index is chosen equal to 0.9. The dc bus voltage value \( V_{dc} \) and the reactor value \( L_{af} \), are extracted by iteration. Choosing \( V_{dc}=265V, (m_0=0.65) \), the minimum required inductance becomes 2.2 mH. Fig. 8 shows that the maximum positive slope of the distorting current represents the worst condition. In order to meet the modulation index requirement, the inductor is chosen equal to 3 mH.

For single phase operation, the capacitor value is selected according to equation (15). Simulation results show that the voltage fluctuation is \( \Delta V_{dc} = \frac{1.17}{C.V_{dc}} \), for balanced three phase operation \( \Delta V_{dc} = \frac{0.32}{C.V_{dc}} \), and for unbalanced three phase operation \( \Delta V_{dc} = \frac{0.776}{C.V_{dc}} \). Choosing a voltage regulation ratio \( r_v < 2\% (\Delta V_{dc} < 5V) \), for single phase operation the minimum required capacitor is 800 \( \mu F \), for the same percentage of ripple, calculations show that for a typical unbalanced load case \( C_{min} = 500 \mu F \) and for the balanced three single phase loads case \( C_{min} = 200 \mu F \). It is obvious that the single phase operation represents the worst case, thus the capacitor will be designed for this mode of operation. In this case a capacitor of 900 \( \mu F \) is chosen. Table I summarizes the design data of the active filter valid for balanced, unbalanced and single phase load operation. The designed system is simulated and results are presented. Simulation results show that after compensation, the supply current is perfectly sinusoidal and the distorted current is eliminated. The spectrum of the supply current shows that the remaining dominant low harmonic current is at the fundamental frequency.

<table>
<thead>
<tr>
<th>( S_{base} = S_{load} )</th>
<th>1.4kVA = 1pu</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{base} )</td>
<td>60V = 1pu</td>
</tr>
<tr>
<td>( I_{base} )</td>
<td>7.8A = 1pu</td>
</tr>
<tr>
<td>( f_{sw}/f )</td>
<td>170 pu</td>
</tr>
<tr>
<td>( x_{af} )</td>
<td>0.146 pu</td>
</tr>
<tr>
<td>( x_c )</td>
<td>0.38 pu</td>
</tr>
<tr>
<td>( S_{Laf} )</td>
<td>0.11 pu</td>
</tr>
<tr>
<td>( S_{cap} = S_{af} )</td>
<td>0.75 pu</td>
</tr>
<tr>
<td>( V_{af.pk} )</td>
<td>1.65 pu</td>
</tr>
</tbody>
</table>
that after compensation, supply current in Fig. 9 (c) is perfectly sinusoidal and the distorted current is eliminated. The spectrum of the supply current in Fig. 10(b), show that the remaining dominant low harmonic current is at the fundamental frequency.

![Fig.8](image)

Fig. 8 shows that the maximum positive slope of the distorting current represents the worst condition. In order to meet the modulation index requirement, the inductor is chosen equal to $3mH$.

The designed system is simulated and result are presented in Fig. 8 & 9 respectively. Simulated results show

Fig. 7 Required harmonic and reactive power from the active filter in function of load THDi for different values of fundamental power factors

![Fig.7](image)

Fig.9 (a) load current (b) injected current (c) supply current after compensation

![Fig.10](image)

Fig.10 (a) Load and (b) supply currents spectrum

X. CONCLUSIONS

This paper, presented a detailed analysis to design the dc capacitors of voltage source inverter based active filter. The effect of the ripple in the dc bus on the compensation capacity of the active filter was also studied. It was shown that the ripple reduces the rate of rise of current, and the compensation capability of the active filter. Moreover, it was shown that the worst possible case for the four wire active filter occurs when it is compensating a single phase load. On the other hand, rating issues such as rating of reactor, rating of the capacitors and rating of the active filter were evaluated in function of the parameters, thus giving an insight to size and cost of the converter. A complete design of the power circuit which is valid for balanced, unbalanced and single phase load conditions. Finally theoretically results and design values have been validated by simulation.

REFERENCES