RASDAT 2017

8th IEEE International Workshop on Reliability Aware System Design and Test 2017

Technical Program

January 9, 2015 – Wednesday

10:45 am - 10:50 am	Opening Ceremony
10:50 am - 11:15 am	Keynote Talk - I Speaker: Prof. Siddhartha Duttagupta, IIT Bombay Topic: Reliability Issues in MEMS
11:15 am - 11:40 am	Keynote Talk – II
11:40 am - 12:35 pm	Technical Session -1 (S1) Circuit Level Reliability S1.1: On Leveraging formal methods to enhance trace mechanisms for efficient post-silicon debug Binod Kumar and Brajesh Pandey S1.2 Design for testability technique of reversible logic circuit based on exclusive testing Joyati Mondal and Debesh Das S1.3 Multiple fault testability of BDD based circuit synthesis Toral Shah
12:45 pm - 1:30 pm	LUNCH
1:30 pm - 3:10 pm	Session A6 on Test, Reliability and Fault Tolerance (with VLSI Design Conference)
3:10 pm - 3:30 pm	COFFEE BREAK
3:30 pm - 3:50 pm	Invited Talk – I Speaker: Prof. Debesh Das, Jadavpur University Topic: Testability of Reversible Circuits
3:50 pm - 4:10 pm	Invited Talk – II Speaker: Prof. Susanta Chakrabarti, IIEST, Kolkata
4:10 pm - 5:15 pm	Technical Session –II (S2) System Level Reliability S2.1 An Integrated solution for manufacturing testing and post-silicon validation Binod Kumar, Ankit Jindal, Jaynarayan Tudu, and Brajesh Pandey S2.2 On securing scan chain from side channel attack Satyadev Ahlawat and Darshit Vaghani S2.3 On improving fault tolerance through hardware software techniques Shoba Gopalkrishnan S2.4 J-Scan: An efficient scan technique for test, diagnosis and post silicon debug, Jaynarayan Tudu