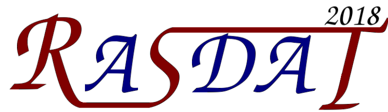

8th IEEE International Workshop on Reliability Aware System Design and Test 2017

Technical Program

January 11, 2018 – Thursday

10:00 am - 10:05am	Opening Ceremony
10:05am - 10:50am	Keynote Talk - I Speaker: Prof. Masahiro Fujita, The University of Tokyo Topic: Template based CPS Design methodology
10:50 am - 11:30 am	Keynote Talk – II Prof. Debesh Das, Jadavpur University
11:30 am – 11:45 am	Coffee Break
11:45 am – 01:00 pm	Technical Session -1 (S1) S1.1: Optimization of Test Wrapper Length for TSV based 3D SoCs using Heuristic Approach Tanusree Kaibartta and Debesh Das S1.2 An Efficient Test and Fault Tolerant Technique for Paper-based Digital Microfluidic Biochips Chandan Das, Sarit Chakraborty, and Susanta Chakraborty S1.3 Debugging Consistency Bugs in Modern Processors Binod Kumar
1:00 pm - 2:00 pm	LUNCH
2:00 pm - 2:45 pm	Invited Talk – I Speaker: Prof. Jaideep Vaidya, Rutgers University
2:45 pm - 3:30 pm	Invited Talk – II Speaker: Prof. Susanta Chakraborty, IIEST, Kolkata Topic: Gene Regulatory network for detection of cancer using Boolean network
3:30 pm – 3:45 pm	Coffee Break
3:45 pm - 4:45 pm	Technical Session –II (S2) S2.1 An Efficient Secure Scan Technique from Scan based Side Channel Attack Satyadev Ahlawat and Darshit Vaghani S2.2 Completely Multiple Fault Testable Design Toral Shah