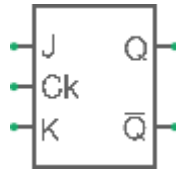


jkff\_1\_pos.dce



### Attributes

```
mainnodes: clk j k q qbar
outvar: st0=dstate_of_ff0
rparms: dlyhl=5n dlylh=5n
stparms: state_sv=0 q_sv=0
```

### Description

jkff\_1\_pos.dce is a positive edge-triggered JK flip-flop. `clk`, `j`, `k`, `q`, `qbar` are the Clock,  $J$ ,  $K$ ,  $Q$ , and  $\overline{Q}$  nodes of the flip-flop, respectively. The real parameters, `dlyhl` and `dlylh`, are the delays associated with high-to-low and low-to-high transitions at the output, respectively.

The start-up parameter `q_sv` decides the state of the flip-flop in start-up simulation.