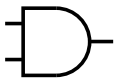
and_2.dce



Attributes

```
mainnodes: a1 a2 b
rparms: dlyhl=5n dlylh=5n
stparms: state_sv=0
```

Description

`and_2.dce` is a 2-input AND gate, with inputs `a1` and `a2`, and output `b`. The real parameters, `dlyhl` and `dlylh`, are the delays associated with high-to-low and low-to-high transitions at the output, respectively.

The start-up parameter `state_sv` decides the output value in start-up simulation.