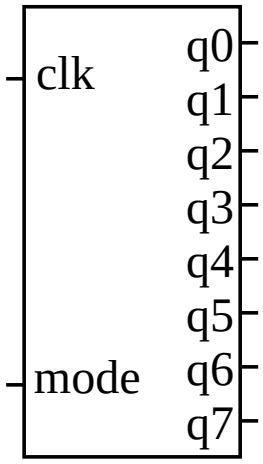
counter_8_gnrl.dce



Attributes

```
  mainnodes: clk mode q0 q1 q2 q3 q4 q5 q6 q7
  iparms:
+   state_begin=0
+   state_end=255
  rparms: dly=5n
  stparms: q_sv=0
```

Description

`counter_8_gnrl.dce` is an 8-bit counter, with `clk` as the clock (negative edge being the active edge), `q7`, `q6`, `q5`, `q4`, `q3`, `q2`, `q1`, `q0` as outputs. If `mode` is `1`, the counter counts up; else, it counts down. The real parameter `dly` denotes the delay between the active clock edge and an output transition.

The parameters `state_begin` and `state_end` are used to specify the beginning and ending states of the counter (and therefore its modulo number).

The start-up parameter `q_sv` is used to specify the initial state of the counter in start-up or transient simulation.