`ee101_shift_reg_1.sqproj`
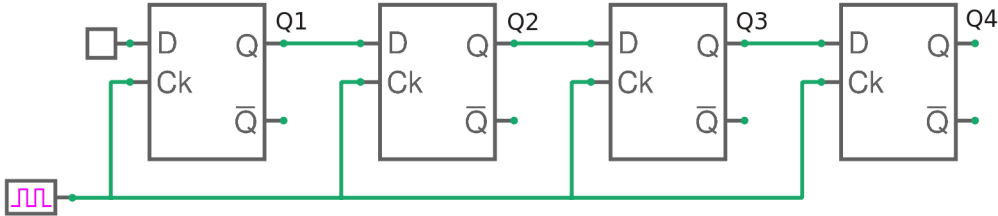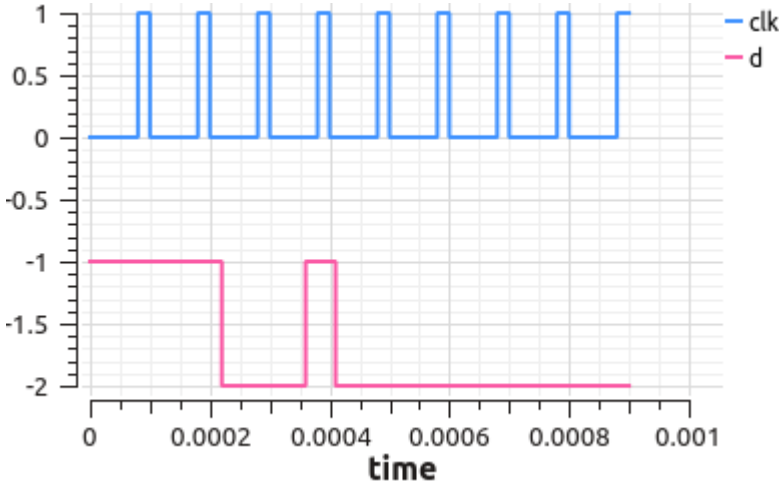

Note: flip-flops are negative edge-triggered.

Shown in the figure is a shift register with some given clock and input waveforms.

(Note that the y-axis values vary between 0 and 1 in reality; for convenience, an offset has been used for the waveforms in the above plot.)

Exercise Set

1. Plot Q_1, Q_2, Q_3, Q_4 versus time.

2. Compare your plot with simulation results.