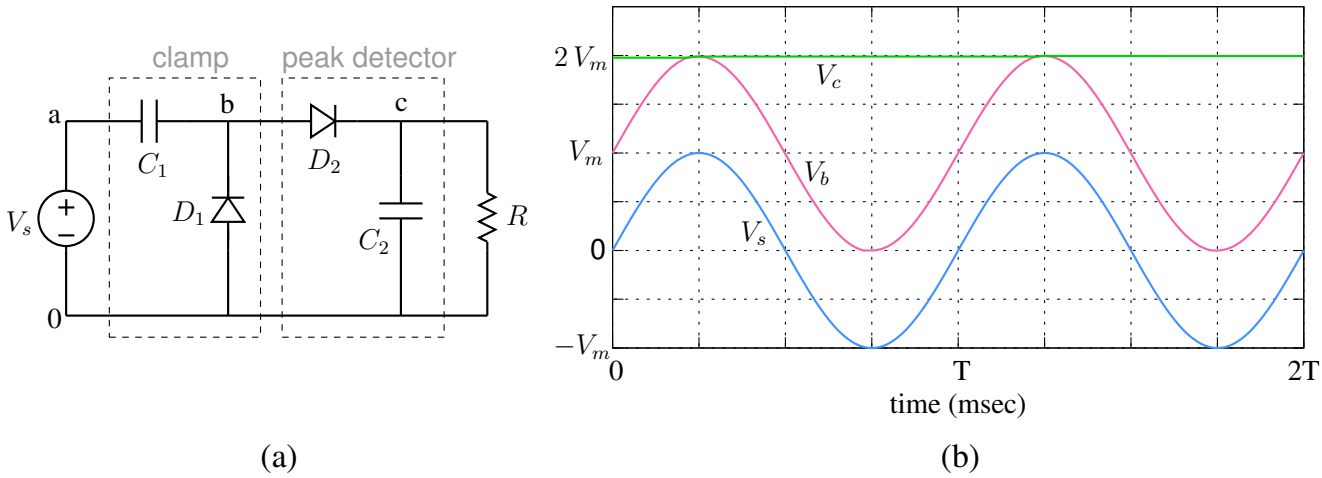
`ee101_voltage_doubler.sqproj`



(a) (b)

Figure 1: (a) Voltage doubler circuit, (b) Ideal waveforms with $V_{\text{on}} = 0\,V$ for the diodes, and $R \to \infty$.

Shown in Fig. 1 (a) is a voltage doubler circuit which produces a DC output voltage $V_o = 2\,V_m$ where V_m is the amplitude of the AC input voltage, $V_i(t) = V_m \sin \omega t$. The circuit operation is easier to understand if we make some simplifying assumptions: (a) V_{on} for the diodes is 0 V, (b) The load resistance is large, i.e., $R \to \infty$. With these assumptions, the waveforms shown in Fig. 1 (b) are obtained. The first part of the circuit serves to clamp $V_b(t)$ at 0 V (as the lower limit). The second part detects the peak of this clamped voltage and holds it constant. If the resistance R is finite, it draws some current, causing a voltage drop (ripple) in V_c.

Exercise Set

1. Let $C_1 = C_2 = 1\,\mu$F, and for the voltage source, $V_m = 10$ V and $f = 1$ kHz. Simulate the circuit with $V_{\text{on}} = 0$ V for the diodes and with a large value of R (say, 10 MΩ), and verify that you get the theoretically expected waveforms shown in Fig. 1 (b).

   Note that the simulation plot will include the initial transient leading to the steady state. Our main interest is in the steady-state behaviour; however, it is instructive to look at how the capacitor charging takes place in the beginning as described by the initial transient.

2. What will happen to $V_c(t)$ if $V_{\text{on}} = 0.7$ V for the diodes? Verify with simulation.

3. Simulate the circuit with (a) $R = 100\,\text{k}\Omega$ and (b) $R = 10\,\text{k}\Omega$. Comment on your observations.

4. For $R = 10\,\text{k}\Omega$, what will you do to reduce the ripple voltage at the output? Verify with simulation.

5. Compare the $V_o(t)$ waveforms for two values of C_2: $1\,\mu\text{F}$ and $10\,\mu\text{F}$, with $C_1 = 1\,\mu\text{F}$. Explain your observations.

   (Hint: See `ee101_rc8.sqproj`.)