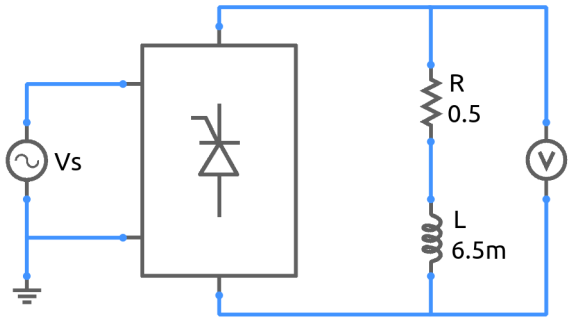
controlled_rectifier_3a.sqproj



Note: clock signals are generated within the bridge element.