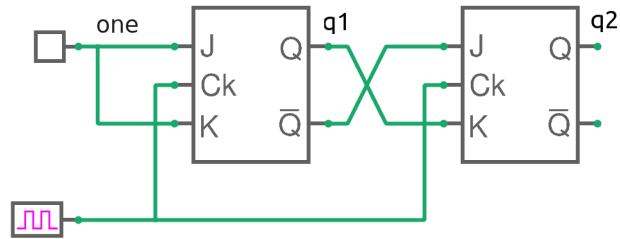# ee101_jk_3.sqproj

Note: positive edge-triggered flip-flops

The flip-flops in the above circuit start initially with $Q_2 Q_1 = 00$. We are interested in their behaviour for the next few (say, four) clock cycles. Toward this goal, we can prepare a table in the following format:

clock	Q_1	Q_2	J_1	K_1	J_2	K_2	Q_1^{next}	Q_2^{next}
1								
2								
3								
4								

Note that Q_1^{next}, Q_2^{next} of the first row will be Q_1, Q_2, respectively, of the second row, and so on.

Exercise Set

1. Work out the counter sequence.

2. Verify your sequence with simulation.

3. Is this circuit doing anything useful?

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