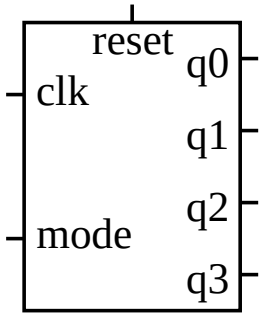
counter_4.dce



Attributes

```
mainnodes: clk mode reset q0 q1 q2 q3
rparms: dly=5n
stparms: q_sv=0
```

Description

`counter_4.dce` is a 4-bit counter, with `clk` as the clock (negative edge being the active edge), `q3`, `q2`, `q1`, `q0` as outputs. The counter can be reset to 0000 with the asynchronous input `reset`. If `mode` is 1, the counter counts up; else, it counts down. The real parameter `dly` denotes the delay between the active clock edge and an output transition.

The start-up parameter `q_sv` is used to specify the initial state of the counter in start-up or transient simulation.