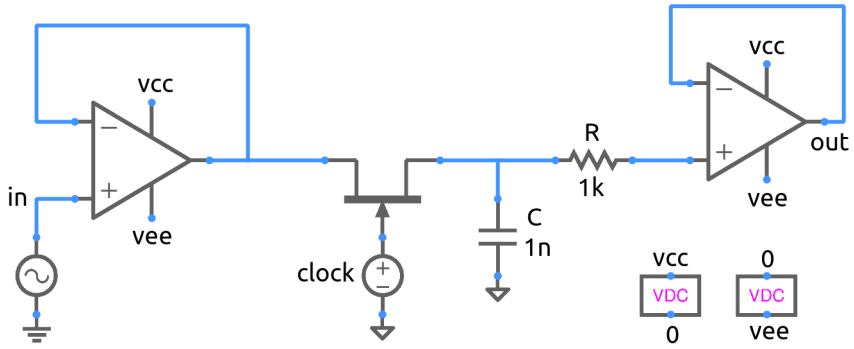
sample_hold.sqproj



Shown in the figure is a sample-and-hold circuit. The sampling function is performed by the JFET switch, and the capacitor is used to hold the sampled voltage for one clock period. The buffers at either end are used to minimise loading effects. A sinusoidal voltage is used as input.

Exercise Set

1. Run the simulation. Plot the input and output voltages versus time, and verify the sample-and-hold functionality.

2. Plot the switch current versus time, and explain its variation with time.

References

1. H. Taub and D. Schilling, *Digital Integrated Electronics*, McGraw-Hill, 1977.

2. J. Millman and A. Grabel, *Microelectronics,* McGraw-Hill, 1988.