ee101_counter_4.sqproj

one

J Q Q0
Ck
K Q̄

J Q Q1
Ck
K Q̄

J Q Q2
Ck
K Q̄

clock

(Flip-flops are negative-edge triggered)
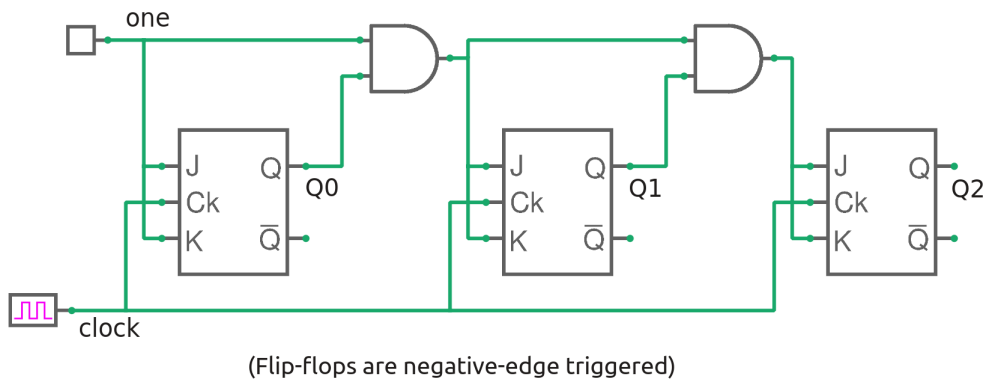
This example illustrates the working of a counter made up of JK flip-flops.

Exercise Set

1. Assuming that all flip-flops are originally reset, sketch the outputs Q_0, Q_1, Q_2 as a function of time. Verify with simulation.

2. What is the advantage of this configuration as compared to the binary ripple counter?