SC_SOURCE_3.ece

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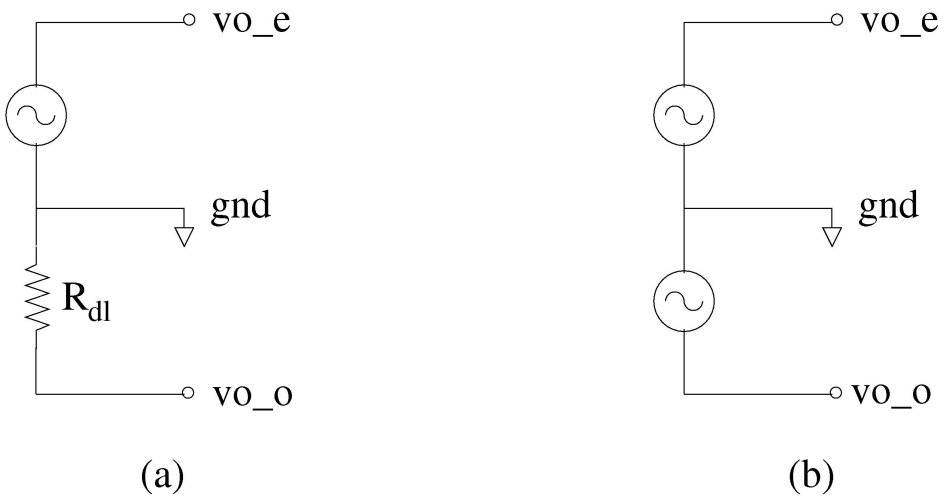

Sampled Source (Time and Frequency Domain)

Attributes:

```
mainnodes: vo_e vo_o gnd
digital_nodes:
stparms:
rparms: tc=0.11 t0=0 v_previous=0 dt=5u s_2=0.11 tau_1=0.11
tau_2=0.11
```

Description:

SC_SOURCE_3.ece is a voltage source element, commonly used in the switched capacitor (SC) circuits. The time-domain description of this element is shown in Fig. a., it is a single-port output block (ignore R_{dl} connected between `vo_o`). The small-signal equivalent is shown in Fig. b, which is a two-port output element.

This element provides sampled signal in time-domain as well as in frequency domain. It means the frequency domain is the equivalent of sampled time-domain signal.

As the same file contains time-domain and frequency-domain descriptions, the number of ports in both is made equal. It is the reason that the source element is realized as a two-port element in time-domain, and unused port/node is connected with low-value resistance (R_{dl}).

`vo_e` and `vo_o` are output nodes. `tc` should be assigned **half the period of clock signal**. `t0` is starting sampling time. `v_previous` is previous sampling voltage. `dt` is separation between two samples. `s_2`, `tau_1`, and `tau_2` should be assigned half the clock period. R_{dl} is internally set to 1 Ω.