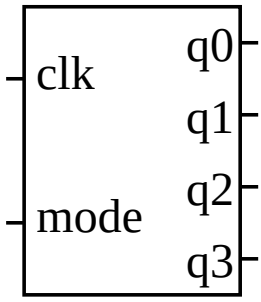
counter_4_gnrl.dce



Attributes

```
  mainnodes: clk mode q0 q1 q2 q3
  iparms:
+   state_begin=0
+   state_end=15
  rparms: dly=5n
  stparms: q_sv=0
```

Description

`counter_4_gnrl.dce` is a 4-bit counter, with `clk` as the clock (negative edge being the active edge), `q3`, `q2`, `q1`, `q0` as outputs. If `mode` is `1`, the counter counts up; else, it counts down. The real parameter `dly` denotes the delay between the active clock edge and an output transition.

The parameters `state_begin` and `state_end` are used to specify the beginning and ending states of the counter (and therefore its modulo number). For example, `state_begin` = 5 and `state_end` = 12 will make the counter count from $Q_3Q_2Q_1Q_0 =$ `0101` to $Q_3Q_2Q_1Q_0 =$ `1100` if `mode` is `1` and from $Q_3Q_2Q_1Q_0 =$ `1100` to $Q_3Q_2Q_1Q_0 =$ `0101` if `mode` is `0`.

The start-up parameter `q_sv` is used to specify the initial state of the counter in start-up or transient simulation.