ee101_counter_9.sqproj

(Flip-flops are positive-edge triggered)
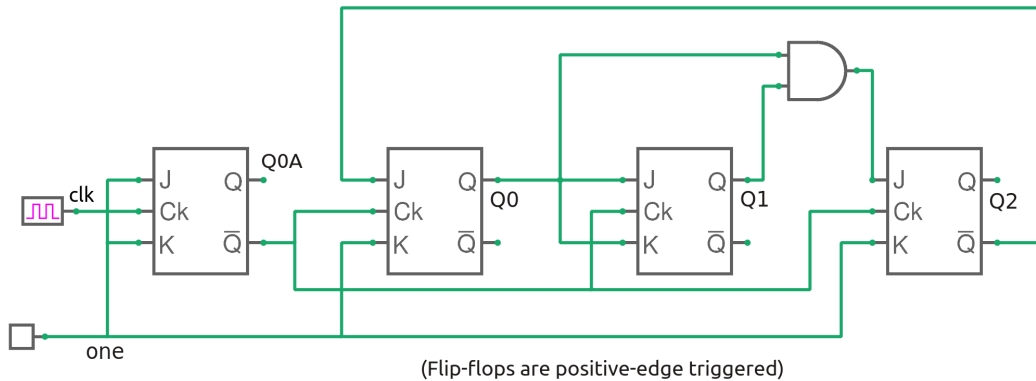
We are interested in the sequence produced by the synchronous counter shown in the figure, starting with the initial state $Q_2Q_1Q_0Q_{0A} = 0000$.

Exercise Set

1. Sketch the waveforms for Q_{0A}, Q_0, Q_1, Q_2. Use the fact that the counter is in fact a combination of two counters: (a) a divide-by-2 counter (with output Q_{0A}) and (b) a three-bit counter $(Q_2Q_1Q_0)$ for which the counting sequence has already been worked out in ee101_counter_6.sqproj.

   The output $(\overline{Q_{0A}})$ of the divide-by-2 counter serves as the clock for the three-bit counter. Note that the counter in this example is different than that of ee101_counter_7.sqproj where the output (Q_{0A}) of the divide-by-2 counter was used as the clock of the three-bit counter.

2. Verify your results with simulation.