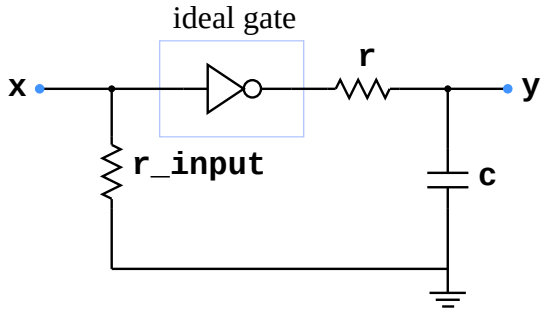
not_dly.ece



Attributes

```
  mainnodes: x y
  rparms:
+    v_high=5.0
+    r_input=100M
+    r=1k
+    c=10p
```

Description

`not_dly.ece` is a NOT gate implemented as an electrical element at the behavioral level (see figure). Voltages 0 V and `v_high` (w.r.t. the reference node, i.e., ground of the circuit) are considered to be low and high logic levels, respectively.

`r_input` is the input resistance seen at the input node `x`. The gate has an *RC* type delay, which is specified by the real parameters `r` and `c`.

AC behaviour is not implemented.