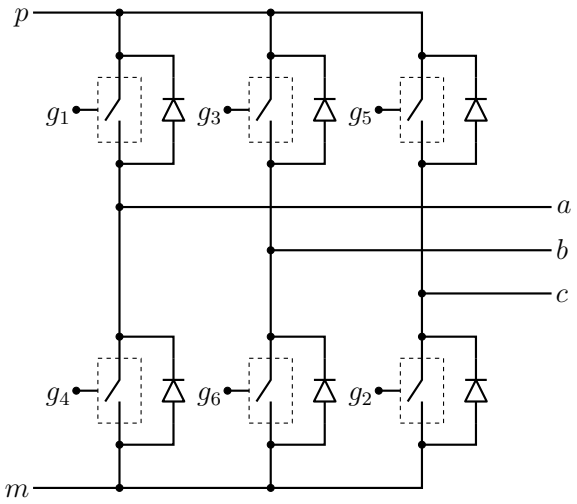
vsi3_3.gme



Attributes

```
mainnodes_anlg: a b c p m
main_var: g1
aux_var: g2 g3 g4 g5 g6
iparms:
+  flag_frequency=1
+  flag_period=0
rparms:
+  r_on=1m
+  r_off=100k
+  g_high=1.0
+  t_period=20m
+  frequency=50
+  r_snubber=0.01
+  c_snubber=10p
outvar_anlg:
+  g1=var_of_g1
+  g2=var_of_g2
+  g3=var_of_g3
+  g4=var_of_g4
+  g5=var_of_g5
+  g6=var_of_g6
+  is1=is_of_s1
+  id1=id_of_s1
+  is2=is_of_s2
+  id2=id_of_s2
+  is3=is_of_s3
+  id3=id_of_s3
```

```
+  is4=is_of_s4
+  id4=id_of_s4
+  is5=is_of_s5
+  id5=id_of_s5
+  is6=is_of_s6
+  id6=id_of_s6
```

Description

`vsi3_3.gme` is a voltage source inverter as shown in the figure. $R_{\text{on}}/R_{\text{off}}$-type switches are used in the model. The gate signal `g1` is externally supplied, and the other gate signals (`g2` to `g6`) are internally generated. The switch resistance is `r_on` if the corresponding gate input is greater than `g_high`/2; else, it is `r_off`.
The other parameters have the following meaning:

`flag_frequency`: If this parameter is set to `1`, the period of the gate signals is computed using the real parameter `frequency`.

`flag_period`: If this parameter is set to `1`, the period of the gate signals is given by the real parameter `t_period`.

A series RC snubber (with component values `r_snubber` and `c_snubber`) is connected in parallel with each switch (not shown in the figure).
AC behaviour is not implemented.