jkffcntr.sqproj

Description

Fig. 1 shows an asynchronous counter made up of T flip-flops (i.e., J-K flip-flops, with $J = k = 1$). When the count become decimal 10 (i.e., binary 1010), the direct reset input becomes active, and the counter gets reset to the condition 0000. The waveforms obtained are shown in Fig. 2. Note, in particular, the short spike in Q_0 which arises because the flip-flop gets reset as its output goes high.

Assignments

1. Design a modulo-12 asynchronous counter with the sequence given below.

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
0	0	0	0

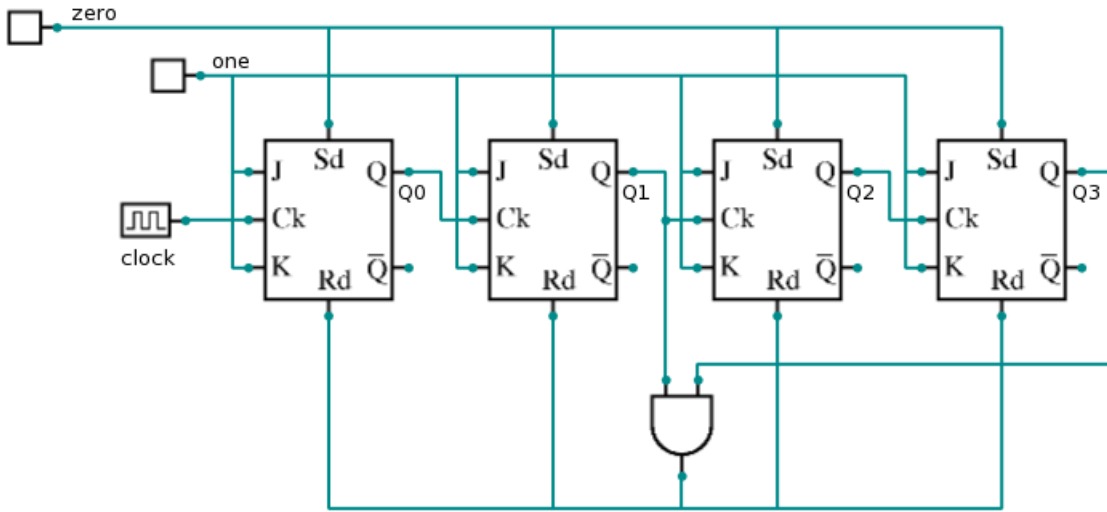2. Simulate the counter designed in (a), and verify its operation.
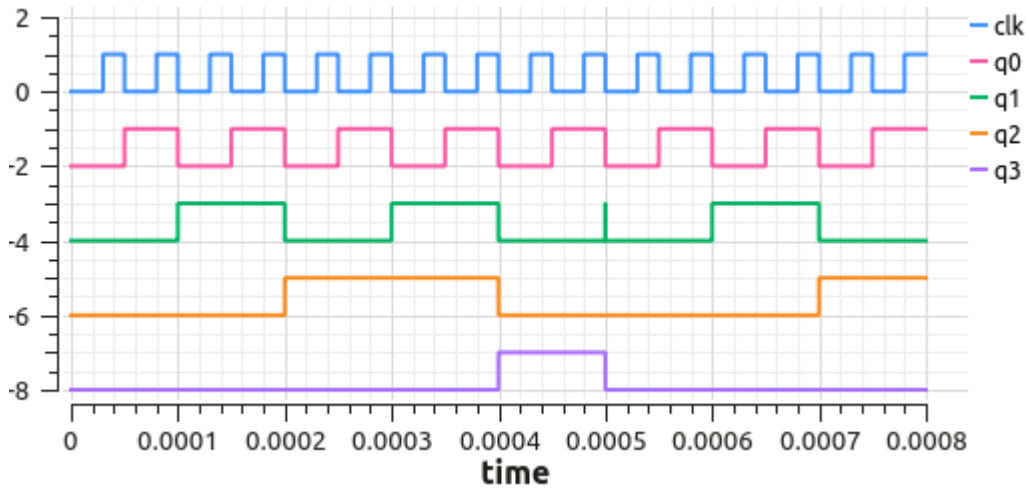
Figure 1: Circuit schematic for asynchronous decade counter.

Figure 2: Output of the counter shown in Fig. 1.

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