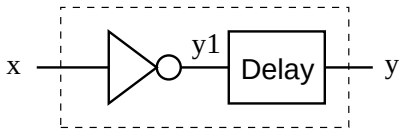
not_dly.gce



Attributes

```
mainvars: x y
auxvars: y1
rparms: g_high=1 dly=10n
```

Description

`not_dly.gce` is a NOT gate implemented with general variables. The parameter `g_high` specifies the high logic level, the low logic level being zero. The output `y` of `not_dly` is a delayed version of the gate output (`y1` in the figure), and is given by,

$$\frac{dy}{dt} = \frac{1}{T_r}\left(-y + y_1\right),$$

where T_r is the same as the real parameter `dly`.

AC behaviour is not implemented.