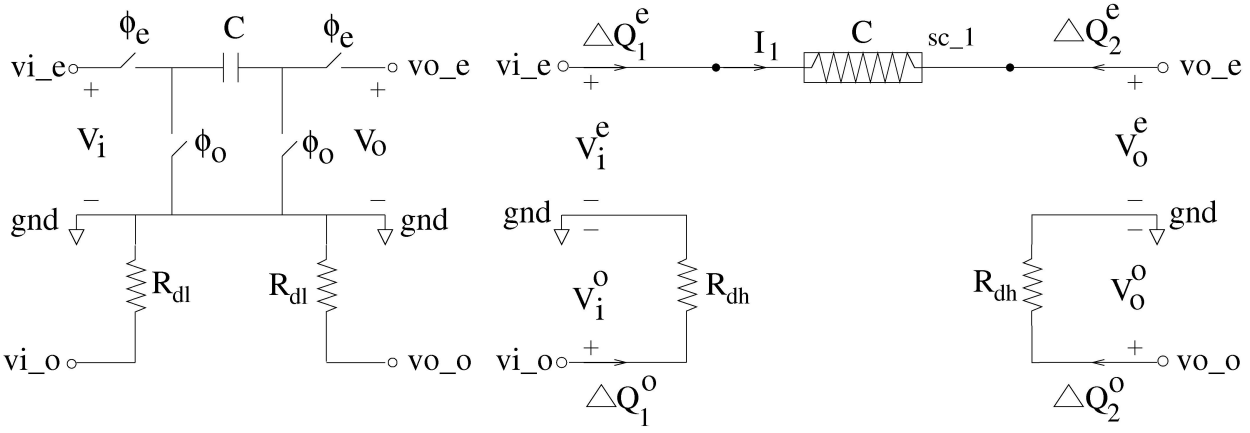
SC_RES_1.ece

(Prepared by: Rajesh A. Thakker, Govt. Engg. College, Chandkheda, Gandhinagar, Email id: rathakker2008@gmail.com)



Resistor

Attributes:

```
mainnodes: vi_e vi_o vo_e vo_o g
digital_nodes: phi_e phi_o
rparms: ron=1e-3 roff=100M c=10p tc=10n rd=1e18
```

Description:

SC_RES_1.ece is a commonly used block in the bi-phase switched capacitor (SC) circuits, which provides a behavior of resistor. The circuit diagram of this element is shown in Fig. a. It consists of four switches and one capacitor (ignore R_{dl} connected between `vi_o` and `vo_o`), and it is a two-port element. The z-domain (small-signal) equivalent circuit is shown in Fig. b, which is a four-port.

As the same file contains time-domain and frequency-domain descriptions, the number of ports in both is made equal. It is the reason that this element is realized as four-port element in time-domain and unused ports/nodes are connected with low-value resistance (R_{dl}). In z-domain unused ports are connected to high-value resistance (R_{dh}).

`vi_e` and `vi_o` are input nodes. `vo_e` and `vo_o` are output nodes. ϕ_e (`phi_e`) and ϕ_o (`phi_o`) are digital nodes, and it should be connected to clock signal. `ron` is switch on resistance and `roff` is switch off resistance. `tc` is clock period. `c` is capacitance value and `rd` is high value resistance (R_{dh}). R_{dl} is internally set to 1 Ω.