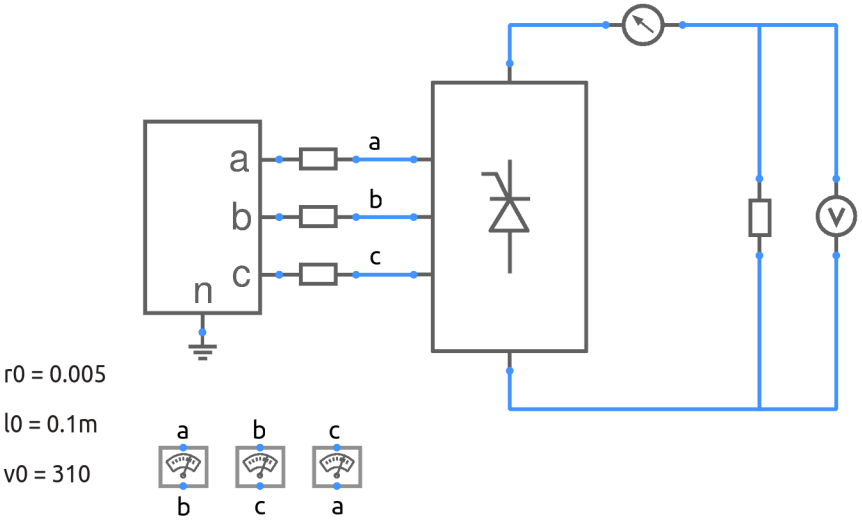
bridge_thyristor_3p_1.sqproj



Note: clock signals are generated within the bridge element.