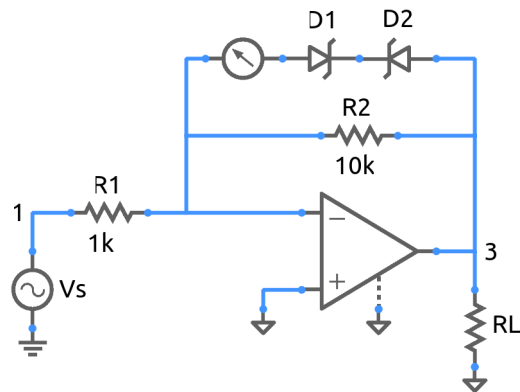# opamp_limiter_1.sqproj

Shown in the figure is an Op Amp amplifier with the feature of limiting the output voltage to $\pm(V_Z + V_D)$, where V_Z is the Zener voltage and V_D is the forward turn-on voltage of the Zener diodes.

Exercise Set

1. Run the simulation with the amplitude of V_s equal to $0.1\,\text{V}$ and $1\,\text{V}$. Plot V_s and V_o versus time in each case. Comment on your observations.

2. When the amplitude of V_s is equal to $1\,\text{V}$, plot (on paper) the current through the ammeter versus time. Verify with simulation.

References

1. J. M. Fiore, *Op Amps and Linear Integrated Circuits,* Delmar, 2001.