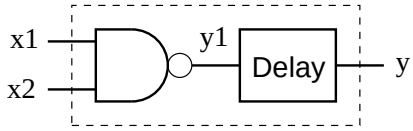
nand_2_dly.gce



Attributes

```
mainvars: x1 x2 y
auxvars: y1
rparms: g_high=1 dly=10n
```

Description

`nand_2_dly.gce` is a NAND gate implemented with general variables. The output `y` of `nand_2_dly` is a delayed version of The parameter `g_high` specifies the high logic level, the low logic level being zero. The high level of `y1` (see figure) is given by the real parameter `g_high`; the low level is assumed to be zero. the gate output (`y1` in the figure), and is given by,

$$\frac{dy}{dt} = \frac{1}{T_r}\left(-y + y_1\right),$$

where T_r is the same as the real parameter `dly`.

AC behaviour is not implemented.