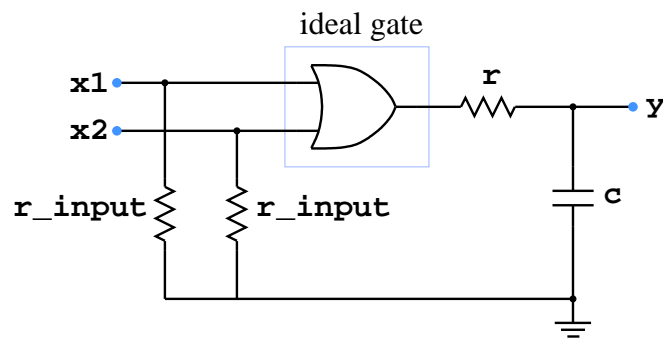


or_2_dly.ece



Attributes

```
mainnodes: x1 x2 y
rparms:
+   v_high=5.0
+   r_input=100M
+   r=1k
+   c=10p
```

Description

or_2_dly.ece is an OR gate implemented as an electrical element at the behavioral level (see figure). Voltages 0 V and **v_high** (w.r.t. the reference node, i.e., ground of the circuit) are considered to be low and high logic levels, respectively.

r_input is the input resistance seen at the input nodes **x1** and **x2**. The gate has an RC type delay, which is specified by the real parameters **r** and **c**.

AC behaviour is not implemented.