A Field-Effect Transistor (FET) has a gate (G) terminal which controls the current flow between the other two terminals, viz., source (S) and drain (D).

In simple terms, a FET can be thought of as a resistance connected between S and D, which is a function of the gate voltage $V_G$.

The mechanism of gate control varies in different types of FETs, e.g., JFET, MESFET, MOSFET, HEMT.

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JFET with $V_S = V_D = 0 \, V$

- Neutral depletion
- Depleted region

$V_G = 0 \, V$

- $V_G = -1 \, V$
- $V_G = -2 \, V$

The bias across the $p-n$ junction is $(V_G - V_S)$, i.e., $V_G$, since $V_S = V_D = 0 \, V$.

As the reverse bias across the junction is increased (by making $V_G$ more negative), the depletion region widens, and the resistance offered by the $n$-region increases.

When the reverse bias becomes large enough, the depletion region consumes the entire $n$-region. The corresponding $V_G$ is called the "pinch-off" voltage.
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JFET: pinch-off voltage

For a p+−n junction, 

\[ W = s^2 \varepsilon (V_{bi} - V) \]

\[ q N_d \]

For pinch-off, 

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For a $p^+ - n$ junction, $W = s_2 \varepsilon (V_{bi} - V) q N_d$, where $V_{bi}$ is the built-in potential of the junction.

For pinch-off, $W = a = s_2 \varepsilon (V_{bi} - V) q N_d \Rightarrow V_P = V_{bi} - q N_d a^2 s_2 \varepsilon$.

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\[ \Rightarrow V_P = V_{bi} - \frac{q N_d a^2}{2 \epsilon} . \]
For pinch-off, \( W = a = \frac{s}{2} \epsilon (V_{bi} - V) \).

\[ W = 0.8 - (1.6 \times 10^{-19} \text{Coul})(2 \times 10^{15} \text{cm}^{-3})((1.5 \times 10^{-4})^2 \text{cm}) = 0.8 - 3.48 \approx -2.7 \text{V}. \]

⇒ If a gate voltage \( V_G = -2.7 \text{V} \) is applied, the n-channel gets pinched off, and the device resistance becomes very large.
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Example: $N_d = 2 \times 10^{15} \text{ cm}^{-3}$, $a = 1.5 \mu\text{m}$, $V_{bi} = 0.8 \text{ V}$. 
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\( \Rightarrow \) If a gate voltage \( V_G = -2.7 \text{ V} \) is applied, the \( n \)-channel gets pinched off, and the device resistance becomes very large.
Consider an n-JFET with $V_G$ constant (and not in pinch-off mode). If a positive $V_D$ is applied, the potential $V(x)$ inside the channel from S to D (along the dashed line) increases from 0 V to $V_D$. Note that $W$ and $h$ are now functions of $x$ such that, $W(x) + h(x) = a$.

Since the p-n junction bias at a given $x$ is $(V_G - V(x))$, the drain end of the channel has a larger reverse bias than the source end. ⇒ the depletion region is wider at the drain.

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**JFET with** $V_G = \text{constant}$, $V_D \neq 0 \text{ V}$

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Consider a slice of the device. The current density at any point in the neutral region is assumed to be in the $x$ direction, and given by,

$$J_n = q \mu_n n E + q D n \frac{dn}{dx} \approx q \mu_n n E = q \mu_n N d \frac{dV}{dx},$$

where we have neglected the diffusion current, since $n \approx N_d \Rightarrow \frac{dn}{dx} = 0$.

Note that only the neutral part of the $n$-Si conducts since there are no carriers in the depletion regions.

At a given $x$, the current $I_D$ is obtained by integrating $J_n$ over the area of the neutral channel region (see figure on the right). Since $J_n$ is constant over this area,

$$I_D(x) = \int_{-h}^{h} J_n dx \approx \int_{-h}^{h} q \mu_n N d \frac{dV}{dx} \approx qZ \mu_n N d a \frac{dV}{dx},$$

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JFET: derivation of $I_D$ equation

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Since $I_D(x)$ is constant from $x = 0$ to $x = L$, we get,

\[ \int_0^L I_D dx = I_D L = 2qZ\mu_n N_d a \int_0^{V_D} \left(1 - \sqrt{\frac{2\epsilon}{qN_d a^2}} \sqrt{V_{bi} - (V_G - V)}\right) dV, \]

where we have used, for the depletion width $W$,

\[ W(x) = \sqrt{\frac{2\epsilon}{qN_d}} \left[V_{bi} - (V_G - V]\right]. \]
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Evaluating the integral and using $V_{bi} - V_P = \frac{qN_d a^2}{2\epsilon}$, we get (do this!)

$$I_D = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[ \left( \frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left( \frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\},$$

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where $G_0 = 2qZ \mu_n N_d a / L$.

Note that $G_0$ is the channel conductance if there was no depletion, i.e., if $h(x) = a$ throughout the channel.
Special case: \( V_D \approx 0 \, V \)

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Since \( W = 2 \epsilon q N d \left( V_{bi} - V_G \right)^{1/2} \), and \( a = 2 \epsilon q N d \left( V_{bi} - V_P \right)^{1/2} \), we get

\( I_D = G_0 V_D \left( 1 - \frac{W}{a} \right) \).

This simply shows that the channel conductance reduces linearly with \( W \) (as seen before the \( V_S = V_S = 0 \, V \) condition), and for \( V_G = V_P \) (i.e., \( W = a \)), the conductance becomes zero.
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JFET: pinch-off near drain

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For a given \( V_G \), \( I_D \) reaches a maximum at \( V_D = V_G - V_P \) (show this by differentiating the above equation).
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At this value of \( V_D \), the bias across the \( p-n \) junction at the drain end is \( V_G - V_D = V_P \).
\[ I_D = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[ \left( \frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left( \frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\} \]

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JFET: pinch-off near drain

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What happens if \( V_D \) is increased further?
Consider a fixed $V_G$ with $V_D$ varying from $\sim 0$ V to a value beyond condition C.
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In this situation, i.e., $V_D > V_{D}^{\text{sat}}$, a short high-field region develops near the drain end, and the “excess” voltage, $V_D - V_{D}^{\text{sat}}$ drops across this region.
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Consider a fixed $V_G$ with $V_D$ varying from $\sim 0 \, \text{V}$ to a value beyond condition C.

In this situation, i.e., $V_D > V_D^{\text{sat}}$, a *short* high-field region develops near the drain end, and the “excess” voltage, $V_D - V_D^{\text{sat}}$, drops across this region.

Because the high-filed region is confined to a very small distance, the conditions in the device are almost identical in C and D.

$\Rightarrow$ The current in case D is almost the same as that for case C.

The region $V_D > V_D^{\text{sat}}$ is therefore called the “saturation region.”
An $n$-channel silicon JFET has the following parameters (at $T = 300 \, K$): $a = 1.5 \, \mu m$, $L = 5 \, \mu m$, $Z = 50 \, \mu m$, $N_d = 2 \times 10^{15} \, cm^{-3}$, $V_{bi} = 0.8 \, V$, $\mu_n = 300 \, cm^2/V$-sec.

(a) What is the pinch-off voltage?

(b) Write a program to generate $I_D-V_D$ characteristics for $V_G = 0 \, V$, $-0.5 \, V$, $-1 \, V$, $-1.5 \, V$, $-2 \, V$.

(c) For each of the above $V_G$ values, compute $V_{Dsat}$, and show it on the $I_D-V_D$ plot. The part of an $I_D-V_D$ corresponding to $V_D < V_{Dsat}$ is called the “linear” region, and that corresponding to $V_D > V_{Dsat}$ is called the “saturation” region.
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Answer:

(a) $V_P = -2.68 \, V$.

(b)
\[ I_D = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[ \left( \frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left( \frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\}. \]
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At saturation, \( V_D^{sat} = V_G - V_P \), giving

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The following approximate model is found to be adequate in circuit design:
\[ I_D^{\text{sat}}(V_G) = I_{DSS} \left( 1 - \frac{V_G}{V_P} \right)^2, \] where \( I_{DSS} = I_D^{\text{sat}}(V_G = 0 \, V) \).
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In amplifier design, we are interested in \( g_m = \frac{\partial I_D}{\partial V_G} \bigg|_{V_D=\text{constant}}, \) which is obtained as:
\[ I_D = G_0 \left\{ V_D - \frac{2}{3} (V_{bi} - V_P) \left[ \left( \frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left( \frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\}. \]

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In real JFETs, there is a separation between the source/drain contacts and the active channel. The $n$-type semiconductor regions between the active channel and the source/drain contacts can be modelled by resistances $R_S$ and $R_D$.

Cross-sectional view

(Not drawn to scale. Typically, $L \gg 2a$.)
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$g_m$ and $g_d$ can be obtained by differentiating $I_D(V_G, V_D)$. Note that, in our simple model, short-channel effects have not been included; we would therefore obtain $g_d = 0$ $\Omega$ in saturation. However, a real device would show a small increase in $I_D$ with an increase in $V_D$ in saturation, giving rise to a non-zero $g_d$.

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