Chapter 3

Diode Circuits

3.1 Background

Diodes are non-linear elements described by the Shockley equation,

$$I = I_S \left[\exp\left(\frac{V}{\eta V_T} \right) - 1 \right], \tag{3.1}$$

where I_S is the reverse saturation current (of the order of pA for typical low-power diodes), $V_T = k_B T/q$ is the thermal voltage (about 26 mV at room temperature, $T = 300\,K$), and η is the ideality factor ($1 < \eta < 2$). A plot of Eq. 3.1 is shown in Fig. 3.1. Note that, as V is made

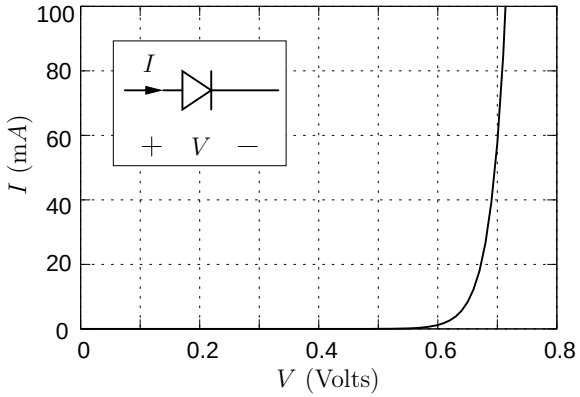

Figure 3.1: Diode $I-V$ curve with forward bias. The parameters, $I_S = 1 \times 10^{-13}\,A$, $V_T = 25\,\mathrm{m}V$, $\eta = 1$, were used for the Shockley model.

negative and more than a few V_T, the exponential term in Eq. 3.1 becomes zero, and $I \approx -I_S$, a negligibly small current. However, a real diode cannot withstand an arbitrarily large reverse voltage and breaks down at some point, the breakdown voltage V_{BR} ranging from a few Volts to a thousand Volts, depending on the diode material, device structure, doping densities, etc. A diode $I-V$ curve with reverse breakdown is shown in Fig. 3.2.
The non-linear model of Eq. 3.1 is too complex for circuit analysis. A much simpler model – which is excellent for a large variety of applications – is derived by noting that the diode current in the forward direction becomes significant (a few mA) at about $0.7\,V$ (defined as V_{on}) for a typical low-power silicon diode and thereafter shoots up rapidly (see Fig. 3.1). In the

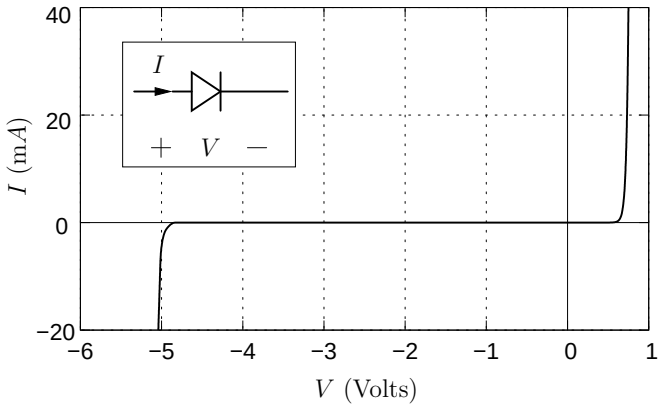

Figure 3.2: Diode $I - V$ curve showing forward and reverse bias.

simplified model, the diode voltage drop is therefore assumed to be constant (equal to V_{on}) for any current in the forward direction, and the diode current is assumed to be zero for any voltage $V < V_{\text{on}}$, as shown in Fig. 3.3 (a). The equivalent circuit of the diode is then simply a

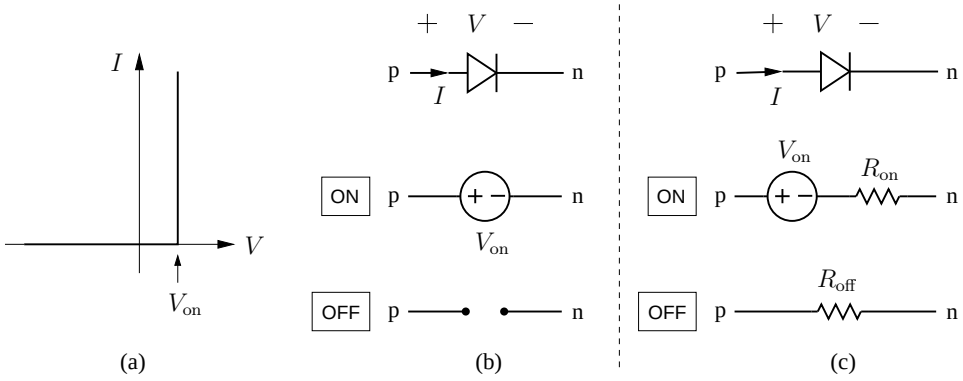

Figure 3.3: (a) Idealized diode $I - V$ plot, (b) diode model with $R_{\text{on}} = 0\,\Omega$, $R_{\text{off}} = \infty\,\Omega$, (c) diode model with finite R_{on} and R_{off}.

voltage source of magnitude V_{on} when it conducts, and an open circuit (assuming no breakdown) when $V < V_{\text{on}}$ (see Fig. 3.3 (b)).

A better approximation of the diode behaviour is obtained by including an on-resistance R_{on} and an off-resistance R_{off} (see Fig. 3.3 (c)). For our purpose, the model in Fig. 3.3 (b) would be generally adequate.

Most of the diode circuits are designed such that the maximum reverse voltage expected to appear across any diode in the circuit is less than its breakdown voltage, and each diode can be simply replaced by an open circuit (Fig. 3.3 (b)) or a large off-resistance R_{off} (Fig. 3.3 (c)). On the other hand, in circuits using Zener diodes, the diode(s) often operates in its breakdown region, with a voltage drop of V_Z Volts. In these circuits, we will idealize the diode $I - V$ characteristic as shown in Fig. 3.4, i.e., the diode has a constant voltage drop V_{on} when conducting in the forward direction, a constant voltage drop of $-V_Z$ when conducting in the reverse direction, and it does not allow any current for $-V_Z < V < V_{\text{on}}$.

In many of the diode circuits, the above simple models help us to gain an excellent idea of the circuit behaviour. The key decision to be made in this simple analysis is whether a given diode, at a given time, is conducting or not. If the diode is conducting, we replace it with a constant

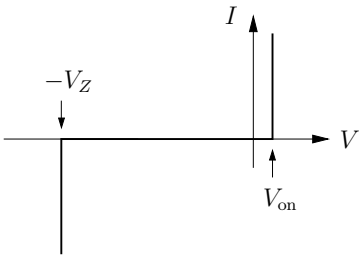

Figure 3.4: Idealized $I-V$ plot for a Zener diode

voltage source ($0.7\,V$ for a silicon diode); if it is not, we replace it with an open circuit. For a Zener diode, we also need to check if the diode could be conducting in the reverse direction. Finally, a note on power consumption of a diode: If a diode in not conducting, it carries a negligible current and therefore does not dissipate any significant power. If it is conducting, its power dissipation is V_{on} multiplied by the forward current. Note that the voltage source (V_{on}) in Fig. 3.3 (b) can only absorb power (see the signs of V and I), and in that sense, it is very different from a battery which can deliver power to an external circuit. The same comment holds for a Zener diode conducting in the reverse direction as well.
In passing, we note that solar cells are also diodes, but they are capable of delivering power to an external circuit. The equivalent circuit of a solar cell is different than those we have discussed; it includes a current source which represents generation of electron-hole pairs due to the solar radiation falling on the $p-n$ junction.

3.2 Examples

1. For the circuit shown in Fig. 3.5 (a), find the current i. For this example and for those to follow, assume the diode to have $V_{\text{on}} = 0.7\,V$, $R_{\text{on}} = 0\,\Omega$, and $R_{\text{off}} = \infty\,\Omega$ (unless specified otherwise).

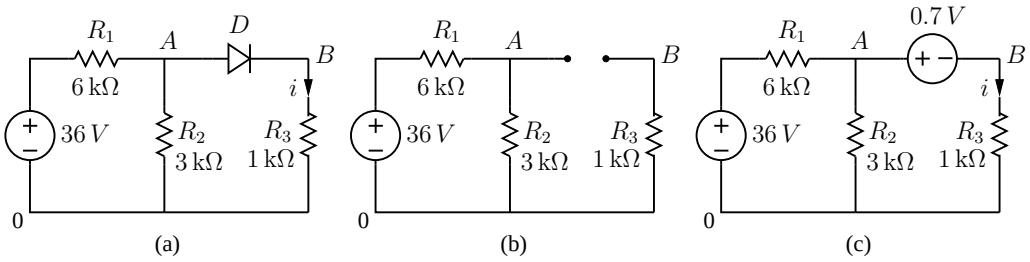

Figure 3.5: (a) Circuit for Example 1, (b) Circuit with diode not conducting, (c) Circuit with diode conducting.

We first need to determine if the diode is conducting or not. Consider the case that it is not conducting, i.e., the diode is replaced with an open circuit (Fig. 3.5 (b)). In this case, $A_{AB} = V_A - V_B = \dfrac{R_2}{R_1+R_2} \times 36\,V = 12\,V$. This is obviously inconsistent with our assumption that the diode is not conducting, and this case is therefore ruled out.

Fig. 3.5 (c) shows the other case in which D is conducting and is replaced with a voltage source of $0.7\,V$. Writing KCL at node A, we get

$$\frac{V_A - 36}{R_1} + \frac{V_A}{R_2} + \frac{V_A - 0.7}{R_3} = 0\,, \tag{3.2}$$

yielding $V_A = 4.47\,V$ and $i = \dfrac{V_A - 0.7}{R_3} = 3.77\,\mathrm{m}A$. Since the direction of the current is from A to B (i.e., from p to n for the diode), our assumption that the diode is conducting in the forward direction is validated.

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2. For the circuit shown in Fig. 3.6,

   (a) Plot V_o versus V_i.

   (b) Plot $V_o(t)$ for a triangular input: $-5\,V$ to $5\,V$, 500 Hz.

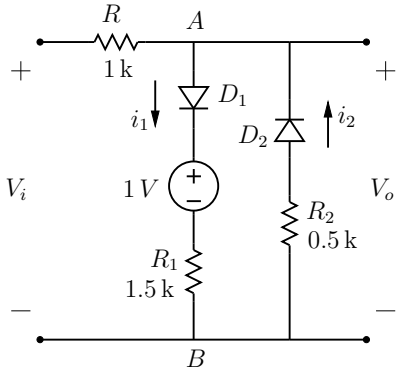

Figure 3.6: Circuit for Example 2.

To start with, we note that D_1 allows a current (marked i_1 in Fig. 3.6) only from node A to node B. Similarly, D_2 allows a current (marked i_2 in Fig. 3.6) only from node B to node A. When D_1 conducts, $V_{AB} = V_A - V_B = (0.7 + 1)\,V + i_1 R_1$ can only be greater than $1.7\,V$. When D_2 conducts, $V_{BA} = V_B - V_A = 0.7\,V + i_2 R_2$ can only be greater than $0.7\,V$, i.e., V_{AB} can only be smaller than $-0.7\,V$. Clearly, the two requirements, $V_{AB} > 1.7\,V$ for D_1 to conduct and $V_{AB} < -0.7\,V$ for D_2 to conduct, are in conflict. As a result, we conclude that, for a given value of V_i, either D_1 can conduct or D_2 can conduct, but not both.

Next, we establish a range of V_i for D_1 to conduct. In this case, we have

$$\begin{aligned} V_i &= i_1 R + 0.7\,V + 1\,V + i_1 R_1\,, \\ &= 1.7\,V + i_1(R + R_1)\,. \end{aligned} \tag{3.3}$$

The boundary between D_1 conducting and D_1 not conducting is given by the condition, $i_1 = 0\,A$, i.e., $V_i = 1.7\,V$. For $V_i > 1.7\,V$, D_1 conducts, and we get

$$\begin{aligned} V_o &= 1.7\,V + i_1 R_1\,, \\ &= 1.7\,V + (V_i - 1.7\,V)\,\frac{R_1}{R + R_1}\,, \end{aligned} \tag{3.4}$$

where we have substituted for i_1 using Eq. 3.3.

The slope of the line described by Eq. 3.4 is $\dfrac{R_1}{R + R_1} = 0.6$.

When D_2 conducts, we have

$$-V_i = 0.7\,V + i_2(R + R_2)\,. \tag{3.5}$$

The condition $i_2 = 0\,A$ gives the boundary between D_2 conducting and D_2 not conducting: $V_i = -0.7\,V$. For $V_i < -0.7\,V$, D_2 conducts, and we get

$$\begin{aligned} V_o &= -(0.7\,V + i_2 R_2)\,, \\ &= -0.7\,V + (V_i + 0.7\,V)\,\frac{R_2}{R + R_2}\,, \end{aligned} \tag{3.6}$$

a straight line with a slope of $\dfrac{R_2}{R + R_2} = 0.33$.

For $-0.7\,V < V_i < 0.7\,V$, neither D_1 nor D_2 conducts, there is no voltage drop across R, and we get $V_o = V_i$, a straight line passing through the origin, with a slope of 1.

Putting the three cases together, we get the V_o versus V_i plot shown in Fig. 3.7. Using

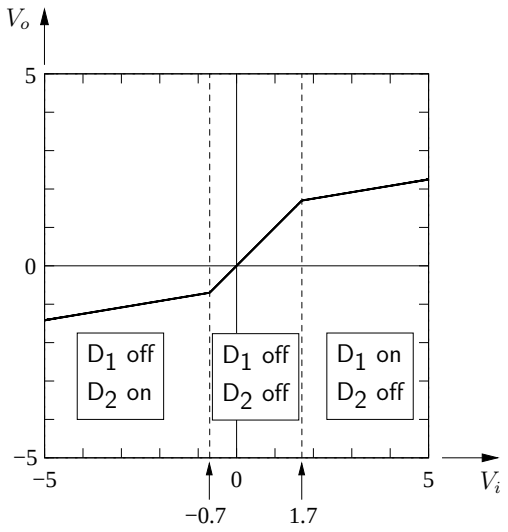

Figure 3.7: V_o (Volts) versus V_i (Volts) for Example 2.

this plot, $V_o(t)$ can be constructed for a given $V_i(t)$. For a triangular $V_i(t)$, the output voltage is shown in Fig. 3.8. The reader is encouraged to compute $V_o^{\min}$, $V_o^{\max}$ from $V_i^{\min}$, $V_i^{\max}$, and check the results against this plot.

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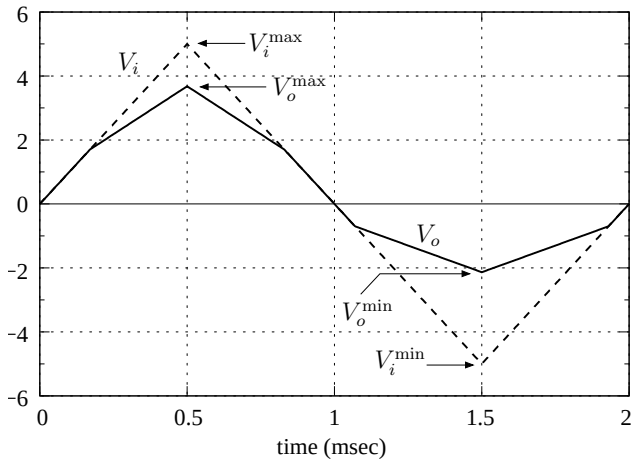

Figure 3.8: $V_o(t)$ (Volts) for a triangular $V_i(t)$ for Example 2.

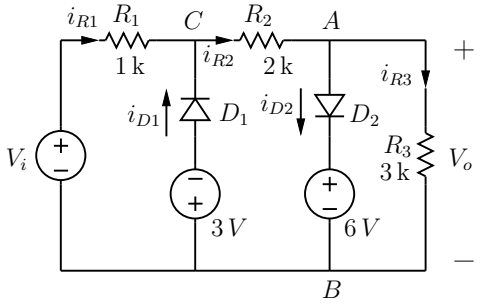

Figure 3.9: Circuit for Example 3.

3. For the circuit shown in Fig. 3.9, plot V_o versus V_i for $-20\,V < V_i < 20\,V$.

   Let us first establish the range of V_i for which D_1/D_2 is on/off. If D_2 is on, we have $i_{D2} > 0\,A$, $V_A - V_B = 6.7\,V$. With this condition, let us see if D_1 can also conduct. Since $V_{AB} = 6.7\,V$, we have $i_{R3} > 0\,A$, leading to $i_{R2} = i_{R3} + i_{D2} > 0\,A$, i.e., $V_{CA} > 0\,V$. The voltage drop $V_{CB} = V_{CA} + V_{AB}$ is therefore positive. For D_1 to conduct, we need $V_B - V_C = 3.7\,V$, or $V_{CB} = -3.7\,V$. Clearly, D_1 and D_2 cannot conduct simultaneously, and the problem is now simplified to the following three cases:

   (a) D_2 on, D_1 off: For this condition, we have $V_o = V_{AB} = 6.7\,V$. The value of V_i for which D_2 *just* starts conducting can be found by using $i_{D2} = 0\,A$, $V_{AB} = 6.7\,V$, i.e., $i_{R1} = i_{R2} = i_{R3} = 6.7\,V/R_3 = 2.23\,\mathrm{m}A$, giving $V_i = V_{AB} + i_{R1}(R_1 + R_2) = 13.4\,V$.

   (b) D_1 on, D_2 off: For this condition, we have $V_{CB} = -3.7\,V$, and $V_o = \dfrac{R_3}{R_2 + R_3}\,V_{CB} = -2.22\,V$. The value of V_i for which D_1 *just* starts conducting can be found by using $i_{D1} = 0\,A$, i.e., $i_{R1} = i_{R2} = i_{R3} = -3.7\,V/(R_2 + R_3)$, and $V_i = -3.7\,V + i_{R1}\,R_1 = -4.44\,V$.

   (c) D_1 off, D_2 off: This condition occurs when (a) and (b) do not occur, i.e., for $-4.44\,V < V_i < 13.4\,V$. In this case, V_o is given by voltage division, viz., $V_o = \dfrac{R_3}{R_1 + R_2 + R_3}\,V_i = 0.5\,V_i\,.$

Fig. 3.10 shows V_o versus V_i for $-20\,V < V_i < 20\,V$.

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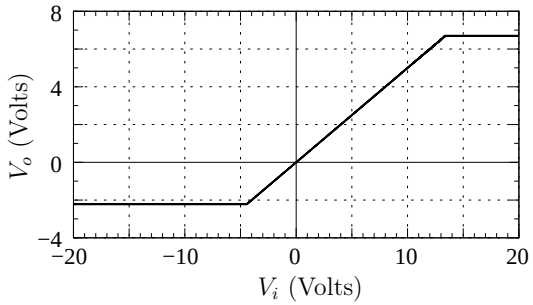

Figure 3.10: V_o versus V_i for the circuit of Example 3.

4. For the circuit shown in Fig. 3.11, $R_4 = 10\,\text{k}$, $R_{1A} = R_{1B} = 5\,\text{k}$, $R_{2A} = R_{2B} = 1.25\,\text{k}$, $R_{3A} = R_{3B} = 1.25\,\text{k}$, $R_{5A} = R_{5B} = 10\,\text{k}$. Sketch V_o versus V_i for $-10\,V < V_i < 10\,V$.

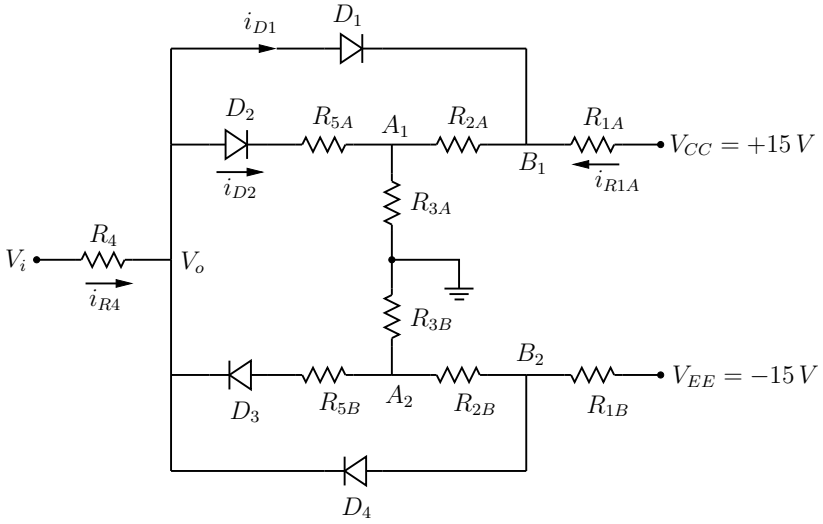

Figure 3.11: Circuit for Example 4.

Let us first take up the condition that all diodes are off. In this case, $i_{R1A} = \dfrac{15\,V}{R_{1A} + R_{2A} + R_{3A}} = 2\,\text{m}A$, giving $V_{A1} = 2.5\,,V$ and $V_{B1} = 5\,,V$. Similarly, $V_{A2} = -2.5\,,V$ and $V_{B2} = -5\,,V$. Since there is no current through R_4, we have $V_o = V_i$.

Consider $V_o = V_i = 0\,V$ which is consistent with the condition that all diodes are off (show this). As V_i is increased from $0\,V$, $V_o = V_i$ increases. For D_1 to conduct, we need $V_i = V_{B1} + 0.7\,V = 5.7\,V$, and for D_2 to conduct, we need $V_i = V_{A1} + 0.7\,V = 3.2\,V$. Clearly, as V_i is increased, D_2 will start conducting first. Note also that a positive V_i is not favourable for D_3 or D_4 to conduct. We therefore have a range of V_i beginning at $V_i = 3.2\,V$, for which only D_2 is on (see Fig. 3.12 (a)).

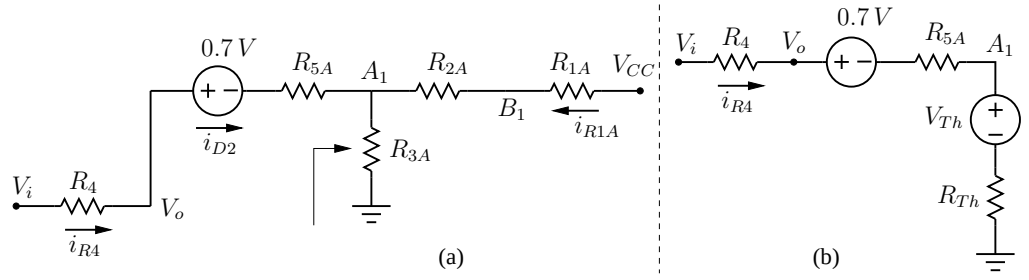

Figure 3.12: (a) Circuit of Fig. 3.11 with only D_2 conducting, (b) simplified circuit.

Using Thevenin's theorem, the circuit can be simplified (see Fig. 3.12 (b)), with $V_{Th} = 2.5\,V$, $R_{Th} = 1.04\,\mathrm{k}\Omega$ (show this), giving

$$V_o = V_i - R_4\, i_{R4} = 0.523\, V_i - 1.524\,, \tag{3.7}$$

$$V_{A1} = V_i - 0.7 - (R_4 + R_{5A})\, i_{R4} = 0.0476\, V_i + 2.35\,, \tag{3.8}$$

$$V_{B1} = V_{A1}\, \frac{R_{1A}}{R_{1A} + R_{2A}} + V_{CC}\, \frac{R_{2A}}{R_{1A} + R_{2A}} = 0.038\, V_i + 4.88\,. \tag{3.9}$$

As V_i is increased, $V_{D1} = V_o - V_{B1}$ increases (see Eqs. 3.7 and 3.9). When V_{D1} becomes equal to $0.7\,V$, D_1 begins to conduct. The corresponding value of V_i is obtained by using the condition, $V_o - V_{B1} = 0.7\,V$, and solving for V_i using Eqs. 3.7 and 3.9. This gives $V_i \approx 8.4\,V$.

When D_1 starts conducting (in addition to D_2), the slope of the V_o versus V_i plot changes. To find this slope, we redraw the circuit (see Fig. 3.13 (a)) and find R_{Th}, the Thevenin resistance as seen from PQ. For this purpose, we deactivate the voltage

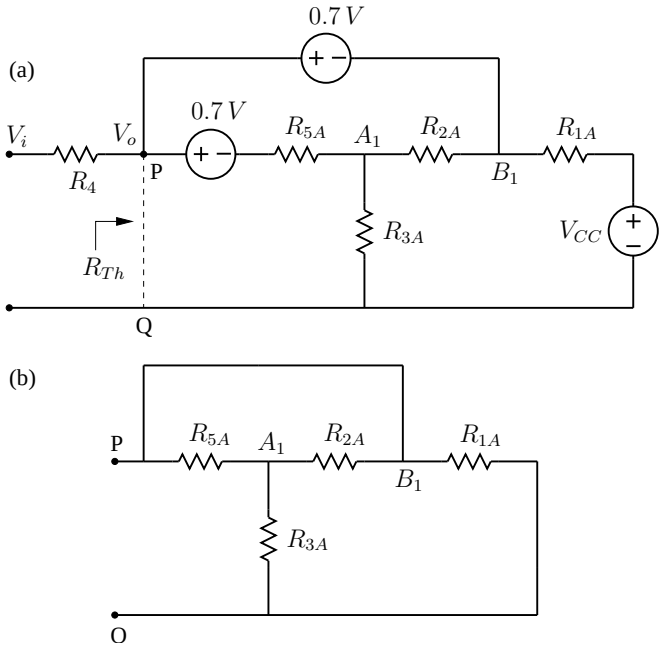

Figure 3.13: (a) Circuit of Fig. 3.11 with D_1 and D_2 conducting, (b) Computation of R_{Th}.

sources (see Fig. 3.13 (b)) and get $R_{Th} = [(R_{5A} \parallel R_{2A}) + R_{3A}] \parallel R_{1A} = 1.6\,\mathrm{k}$. The slope

$\dfrac{dV_o}{dV_i}$ is then given by,

$$\frac{dV_o}{dV_i} = \frac{R_{Th}}{R_{Th} + R_4} = 0.138 \text{ (Show this.)} \tag{3.10}$$

Combining the above three cases, viz., (a) all diodes off, (b) only D_2 on, (c) D_1 and D_2 on, and using symmetry between the upper and lower parts of the circuit (see Fig. 3.11), we get the V_o versus V_i curve shown in Fig. 3.14 (a). If a triangular input $V_i(t)$ is applied, the output $V_o(t)$ is almost sinusoidal (see Fig. 3.14 (b)). For this reason, this circuit is called triangle-to-sine converter.

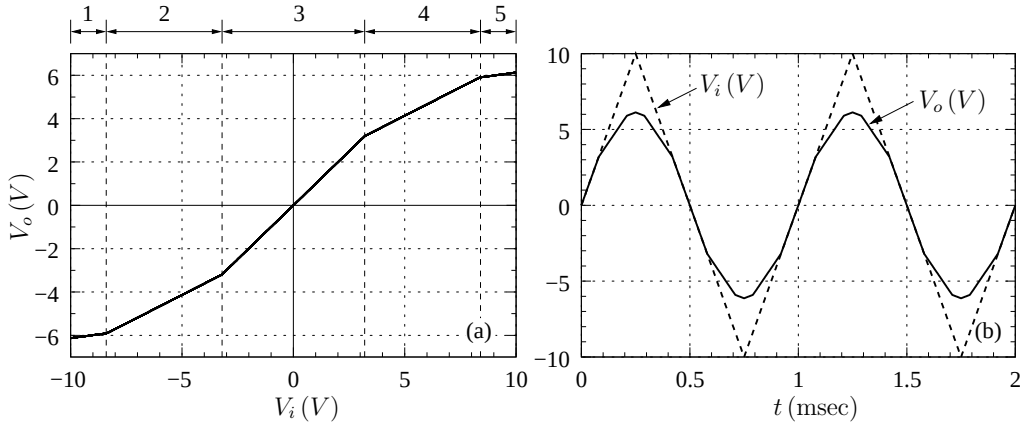

Figure 3.14: (a) V_o versus V_i for the circuit of Fig. 3.11. Region 1: D_3 and D_4 on, Region 2: D_3 on, Region 3: all diodes off, Region 4: D_2 on, Region 5: D_1 and D_2 on, (b) $V_o(t)$ for a triangular input $V_i(t)$.

The reader is encouraged to simulate the circuit and plot versus V_i the diode currents, i_{D1}, i_{D2}, i_{D3}, i_{D4}, and the node voltages, V_{A1}, V_{B1}, and verify that they conform with the above analysis.

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5. For the half-wave rectifier circuit shown in Fig. 3.15 (a), $C = 1\,\text{m}F$, $= 200\,\Omega$, $V_m = 10\,V$. Estimate the peak diode current.

   Let us consider the diode to be ideal, with $V_{\text{on}} = 0\,V$, which results in the output waveform shown in Fig. 3.15 (b). In the discharging phase (Fig. 3.16 (b)), the diode is off, and the capacitor discharges through R. In the charging phase (Fig. 3.16 (a)), the capacitor charges with a time constant $\tau = C\,(R \parallel R_{\text{on}})$, which is very small since the on resistance of a diode (R_{on}) is small. The charging process therefore takes place "instantaneously," and V_o and V_i coincide with each other, as seen in Fig. 3.15 (b).

   In a well-designed rectifier circuit, the charging phase is much shorter than the discharging phase so that the ripple voltage is minimized. This observation has an important implication for the diode current, as we explain in the following.

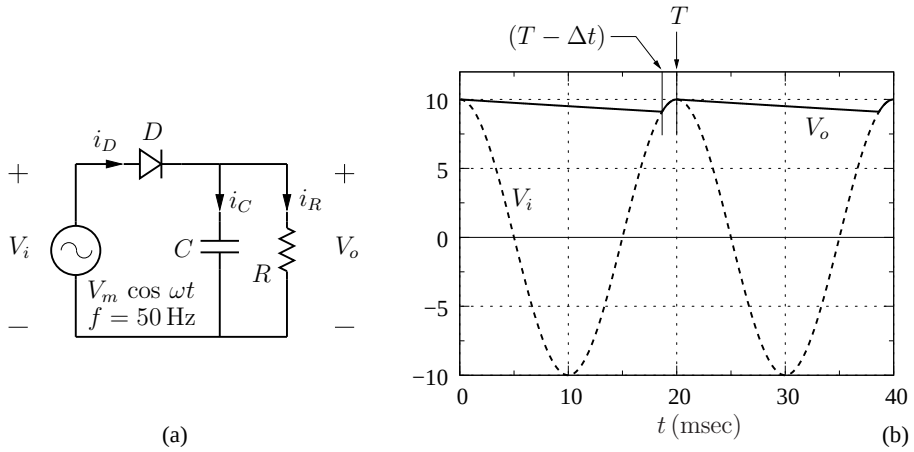

Figure 3.15: (a) Circuit for Example 5, (b) V_i and V_o versus time, with $V_{\rm on} = 0\,V$.

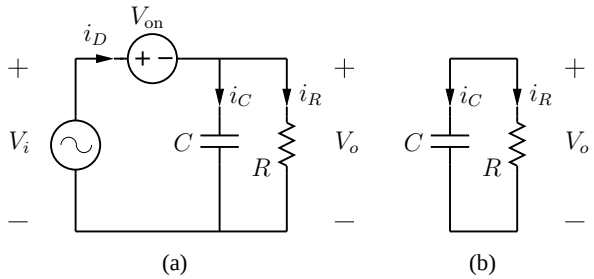

Figure 3.16: (a) Charging phase, (b) discharging phase for the Circuit of Fig. 3.15 (a).

In steady state, the charge gained by the capacitor in the charging phase is equal to the charge lost in the discharging phase. Refering to Fig. 3.15 (b),

$$\int_{T-\Delta t}^{T} (i_D - i_R)\, dt = \int_0^{T-\Delta t} i_R\, dt \qquad \text{i.e,} \quad \frac{1}{T}\int_0^T i_D\, dt = \frac{1}{T}\int_0^T i_R\, dt\,. \tag{3.11}$$

In other words, the average values of the diode current and the load (resistor) current must be exactly equal. Since the diode current flows for a small interval ($(T - \Delta t)$ to T), it is clear that the peak value of i_D would be much larger than i_R if their average values are to be the same. Let us now estimate $i_D(t)$.

Consider the charging phase shown in Fig. 3.16 (a). Since the diode drop is assumed to be $0\,V$,

$$i_C(t) = C\,\frac{dV_o}{dt} = C\,\frac{dV_i}{dt} = -\omega C V_m\, \sin\omega t\,, \tag{3.12}$$

$$i_D(t) = i_C(t) + i_R(t) \approx -\omega C V_m\, \sin\omega t + \frac{V_m}{R}\,, \tag{3.13}$$

since $V_o \approx V_m$. To estimate the peak diode current, we need to find Δt in Fig. 3.15 (b). As an approximation, we first compute the ripple voltage from

$$i_R = \frac{V_m}{R} \approx C\,\frac{V_R}{T} \rightarrow V_R = V_m\,\frac{T}{RC} = 1\,V\,. \tag{3.14}$$

The charging interval Δt can now be obtained by using (see Fig. 3.15 (b)),

$$V_o(T-\Delta t) = V_o(-\Delta t) = V_m - V_R\,, \quad \text{or} \tag{3.15}$$

$$V_m\,\cos\omega(-\Delta t) = V_m - V_R\,, \tag{3.16}$$

giving $\omega\Delta t = 25.8°$. The peak diode current occurs at $t = T - \Delta t$ (which is the same as $t = -\Delta t$ because the waveform is periodic) since, at that time in the charging phase, $i_C = \dfrac{dV_o}{dt}$ is maximum; therefore we have,

$$i_D^{\max} = \omega C V_m\,\cos(\omega\Delta t) + \frac{V_m}{R} = 1.3\,A\,, \tag{3.17}$$

which agrees well with the simulation result shown in Fig. 3.17 (a).

The diode current plot we have obtained gives a reasonable estimate of $i_D^{\max}$; however, the exact shape of $i_D(t)$ would depend on the on resistance of the diode and also on which diode model is used. For example, with $R_{\text{on}} = 0.5\,\Omega$, the peak diode current reduces, as shown in Fig. 3.17 (b).

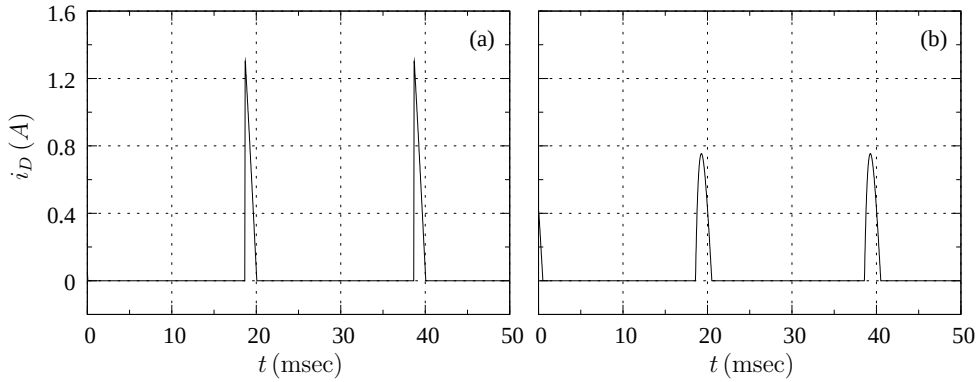

Figure 3.17: Diode current $i_D(t)$ for the half-wave rectifier of Fig. 3.11: (a) $R_{\text{on}} = 1\,\text{m}\Omega$, (b) $R_{\text{on}} = 0.5\,\Omega$.

On the other hand, the ripple voltage would be relatively insensitive to the diode on resistance since its computation depends on the capacitor discharge through the load resistor only. The reader is encouraged to simulate the circuit with the Shockley model as well and see how it affects the ripple voltage and diode current.

This is a good example to demonstrate that a good knowledge of the circuit behaviour is indispensable in making a judicious choice of device models in circuit simulation. Depending on what information we are looking for, we could choose different models. Simple models (such as the $R_{\text{on}}/R_{\text{off}}$ model) are attractive from the computation point of view, but complex models (such as the Shockley model which involves e^{V/V_T}) may be necessary for higher accuracy in certain cases.

SEQUEL file: `ee101_half_rectifier.sqproj`

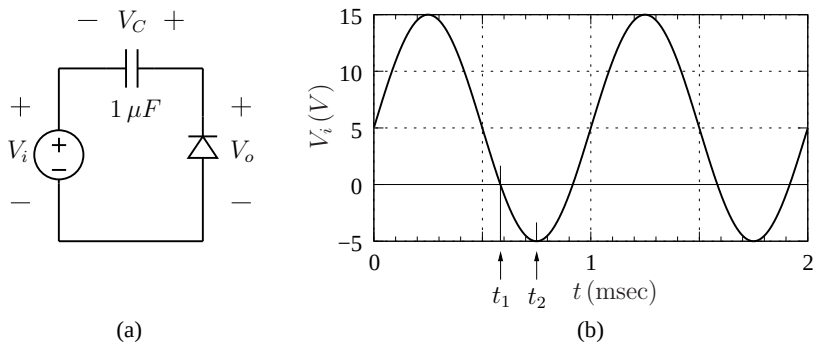

Figure 3.18: (a) Circuit for Example 6, (b) Input voltage V_i versus time.

6. For the circuit shown in Fig. 3.18 (a), assume that the diode has $V_{\text{on}} = 0\,V$. The capacitor is initially uncharged. Plot V_o versus time.

   This circuit is easy to understand when we recognise the following features:

   (a) The capacitor can only charge (with the polarity shown in the figure) since the diode allows current only in one direction.

   (b) Once the capacitor is charged to a maximum value, it holds the charge for ever since there is no discharge path.

   (c) Since the diode has a small on resistance, the charging process is instantaneous.

   It is instructive to view the circuit as an RC circuit (see Fig. 3.19 (a)) with C initially uncharged and the diode replaced by a resistance R_D which is small if $V_D > 0\,V$ and large if $V_D < 0\,V$. Up to time t_1, $V_i > 0\,V$, and a current would flow from A to B. However, since R_D is very large in this direction, the current is almost zero, and the capacitor voltage does not change up to $t = t_1$.

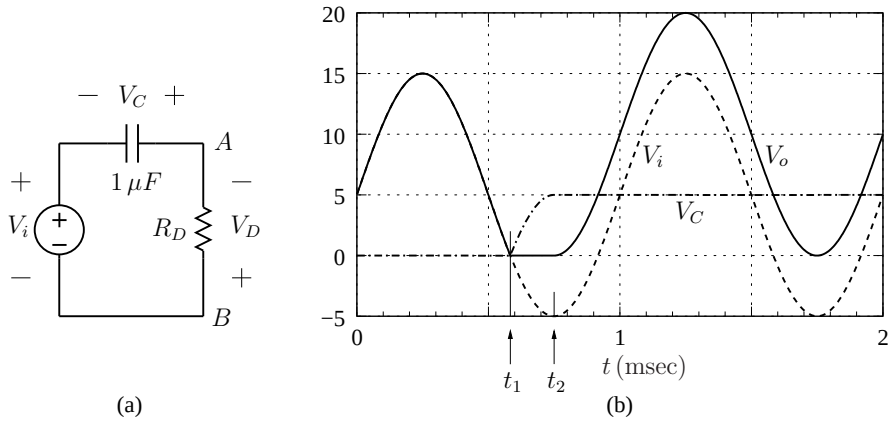

Figure 3.19: (a) Equivalent circuit for Example 6, (b) V_i, V_C, and V_o $(= -V_D)$ versus time.

After t_1, V_i becomes negative, the current direction is from B to A, and because of a small R_D in this current direction, the capacitor charges instantaneously. In other words, since the diode is replaced by $R_D \approx 0\,\Omega$, we have $V_C(t) = -V_i(t)$.

At $t = t_2$, $V_C(t) = -(-5\,V) = +5\,V$. This is the maximum possible value for V_C (since $-5\,V$ is the maximum negative value of V_i). For $t > t_2$, V_C can only decrease, but that would require a reverse current flow in the diode, which is ruled out. Therefore, $V_C(t)$ remains constant after t_2 at $V_C = 5\,V$ (Fig. 3.19 (b)).

Since $V_o(t) = V_i(t) + V_C(t)$ (see Fig. 3.18 (a)), the net effect is that, for $t > t_2$, V_o is simply a shifted version of $V_i(t)$. The output voltage is thus *clamped* at the lower end at $0\,V$.

SEQUEL file: `ee101_diode_circuit_6.sqproj`

3.3 Exercise Set:

1. For the circuit shown in Fig. 3.20, find i_{R1}, i_{R2}, i_{R3}, assuming $V_{\text{on}} = 0.7\,V$ for the diode. (Hint: First, find i_{R3} by replacing the combination of R_1, R_2, V_{CC} with a Thevenin equivalent circuit.)

   SEQUEL file: `ee101_diode_circuit_9.sqproj`

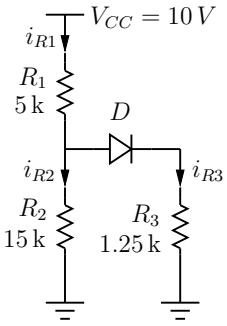

Figure 3.20: Circuit for Exercise 1.

2. For the circuits shown in Figs. 3.21 (a) and (b), assume $V_{\text{on}} = 0.7\,V$ for all diodes.

   (a) Plot V_o versus i for the circuit in Fig. 3.21 (a).

   (b) Repeat for the circuit in Fig. 3.21 (b).

   (c) By simulation, obtain plots of the diode currents (i_{D1A}, i_{D2A}, i_{D1B}, i_{D2B}) versus i, and validate your approach in (b).

   SEQUEL file: `ee101_diode_circuit_10.sqproj`

3. In the full-wave rectifier circuit shown in Fig. 3.22, $R = 1\,\text{k}$, $C = 200\,\mu F$, $V_m = 20\,V$ (peak source voltage), $f = 50\,\text{Hz}$. Assume $V_{\text{on}} = 0\,V$ for the diodes.

   (a) Estimate the ripple voltage.

   (b) Estimate the peak diode current.

   (c) Find the maximum reverse voltage seen by each diode.

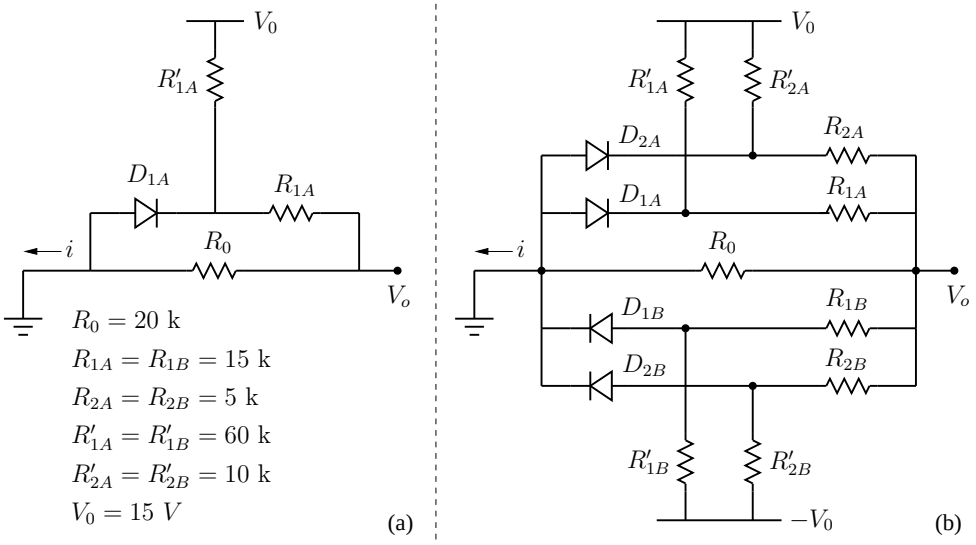

Figure 3.21: Circuits for Exercise 2.

(d) Verify your results with simulation.

(e) Repeat with $V_{\text{on}} = 0.7\,V$ for the diodes.

SEQUEL file: `diode_rectifier_4.sqproj`

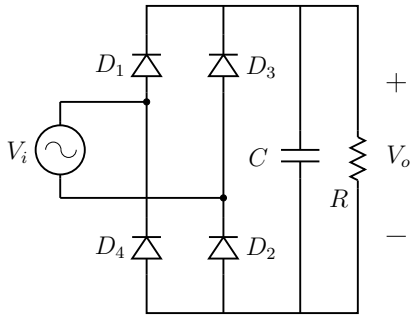

Figure 3.22: Circuit for Exercise 3.

4. In the clamped capacitor circuit of Fig. 3.18,

   (a) How will the output voltage change if $V_{\text{on}} = 0.7\,V$ for the diode (instead of $0\,V$)?

   (b) If a load resistance, $R = 5\,\text{k}$, is connected across the diode, how will V_o change?

   (c) Verify your results with simulation.

   SEQUEL file: `ee101_diode_circuit_6.sqproj`

5. In the circuit shown in Fig. 3.23, $V_i(t) = V_m \sin \omega t$, with $V_m = 10\,V$ and $f = 1\,\text{kHz}$. D_1 is a diode with $V_{\text{on}} = 0.7\,V$ and no reverse breakdown. D_2 is a Zener diode with $V_{\text{on}} = 0.7\,V$ and $V_Z = 4.3\,V$.

   (a) Starting from $V_C = 0\,V$ at $t = 0\,\text{s}$, sketch $V_o(t)$ for the first two cycles.

(b) What will happen if $R_L = 10\,\text{k}$ is connected as shown?

(c) Verify your results with simulation.

SEQUEL file: `ee101_diode_circuit_11.sqproj`

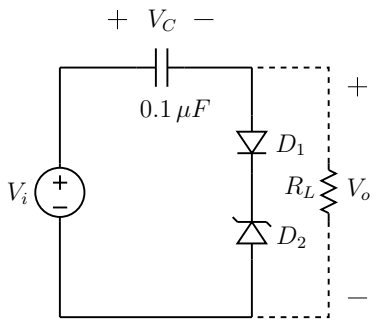

Figure 3.23: Circuit for Exercise 5.