Semiconductor Devices

Junction Field-Effect Transistors: Part 1

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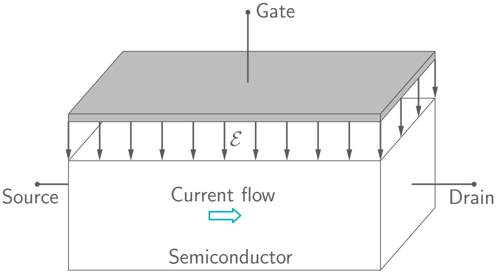
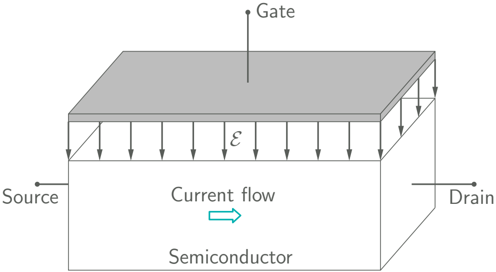
Junction field-effect transistors





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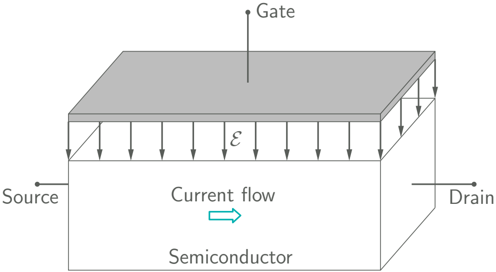

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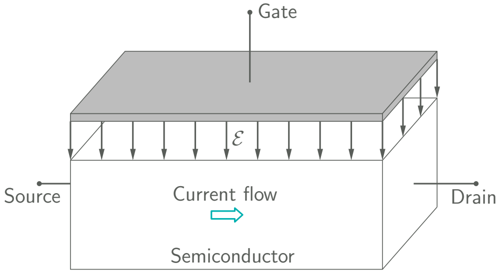
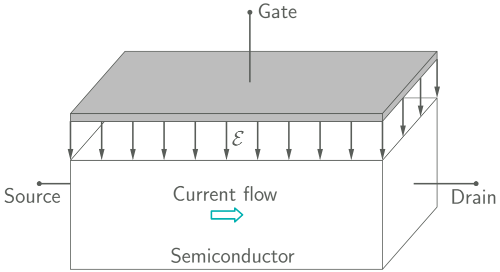
* The change in field is brought about by a voltage applied to the "gate" terminal.


Gate
$\mathcal{E}$
Source
Current flow
Drain
Semiconductor



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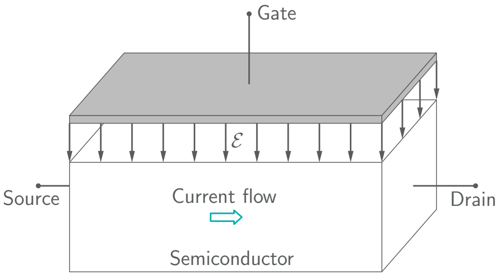

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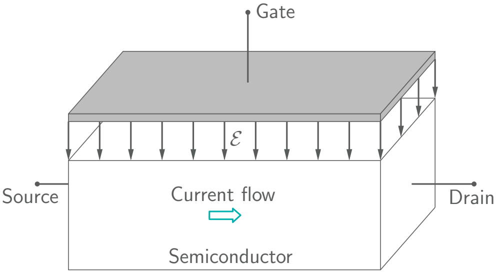

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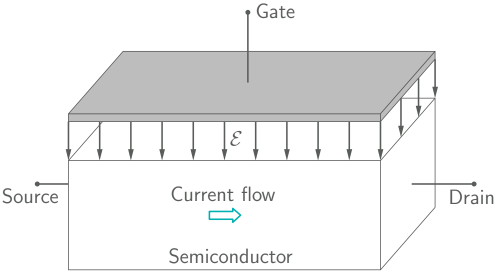

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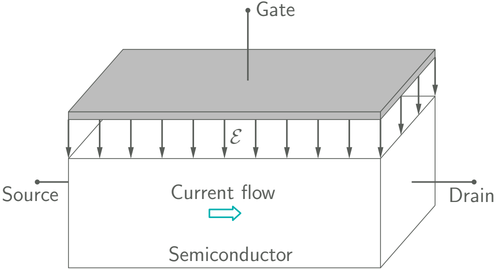

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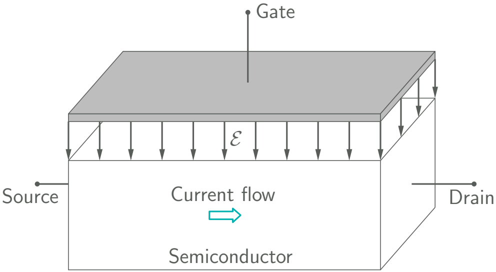

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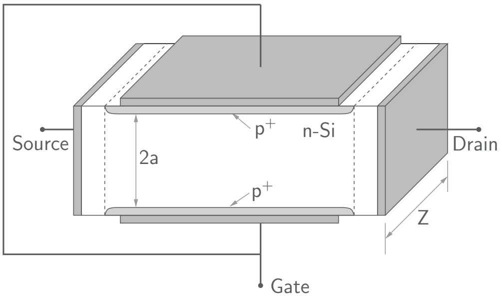
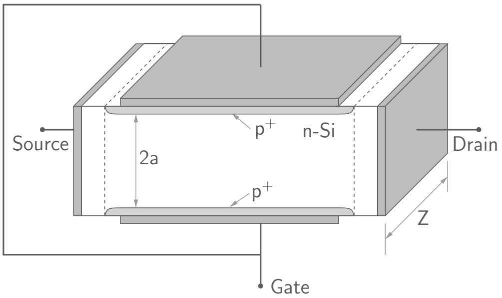
    In a FET, V_{GS} controls the drain current by modulating the resistance between the source and the drain.


Source
p+
n-Si
2a
p+
Drain
Z
Gate



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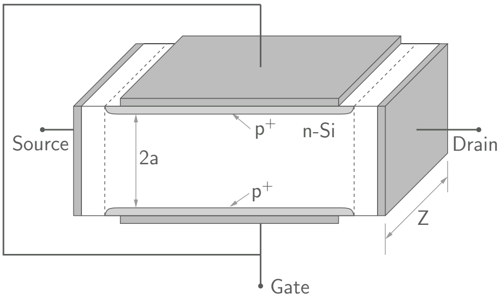
Junction field-effect transistors



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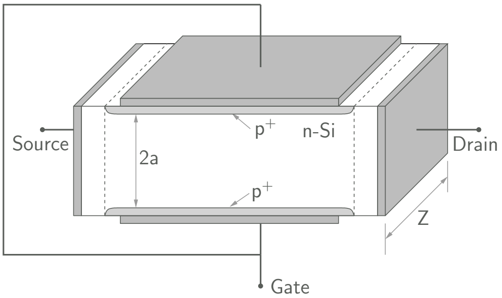

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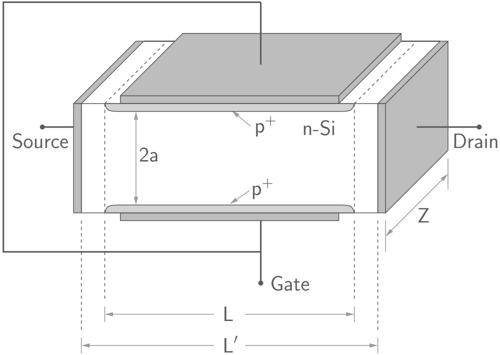
* The top and bottom regions of the semiconductor are doped p^+ and are connected together as the gate terminal.

Junction field-effect transistors



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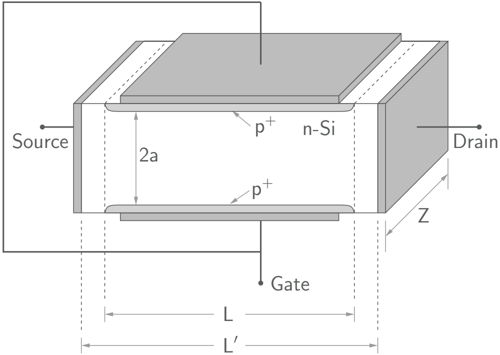
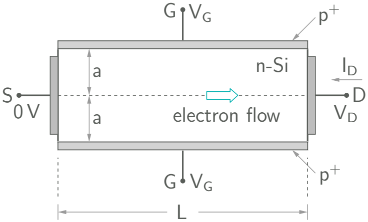
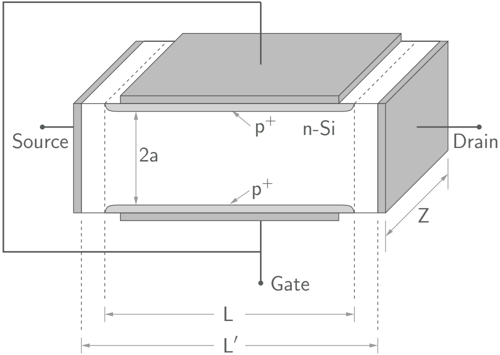
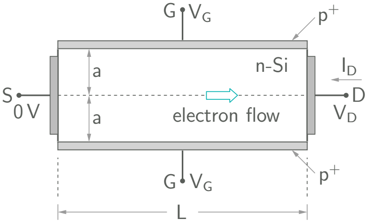




Simplified structure

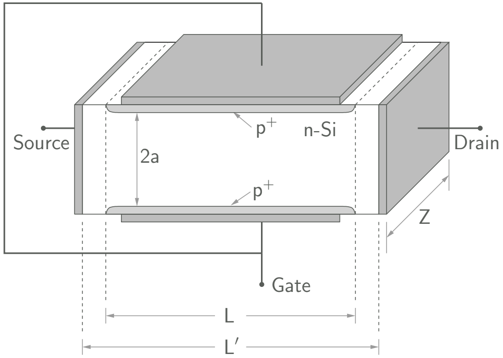


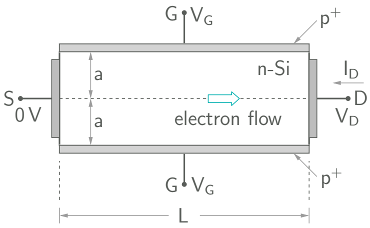


Simplified structure

* A positive drain voltage V_D causes an electron flow from source to drain (i.e., a current I_D in the opposite direction).

Junction field-effect transistors





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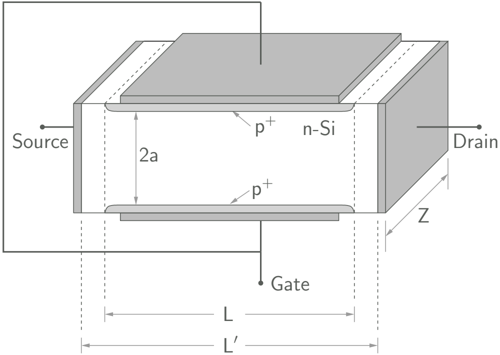
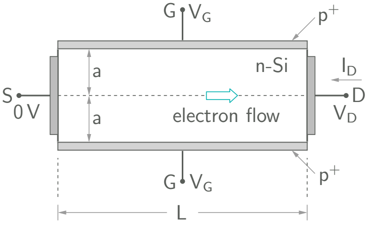
* A negative gate voltage V_G causes the p^+n junctions to be reverse biased, and through this "field effect," the conductance of the channel is modulated.

Junction field-effect transistors





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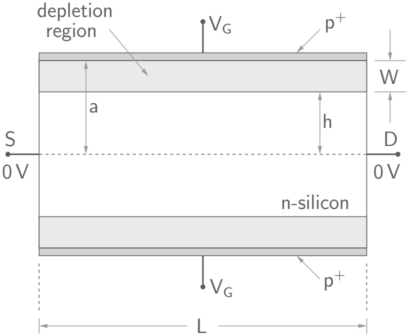
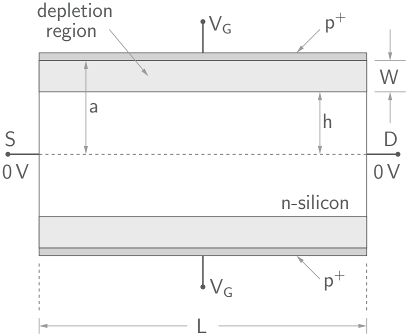
* A negative gate voltage V_G causes the p^+n junctions to be reverse biased, and through this "field effect," the conductance of the channel is modulated.
* This mechanism leads to a change ΔI_D in the drain current when a change ΔV_G is applied in the gate voltage.



(a) $V_G = 0\,\mathrm{V}$

Consider $V_D = V_S = 0\,\mathrm{V}$, and $V_G < 0\,\mathrm{V}$ (reverse bias).

Junction field-effect transistors



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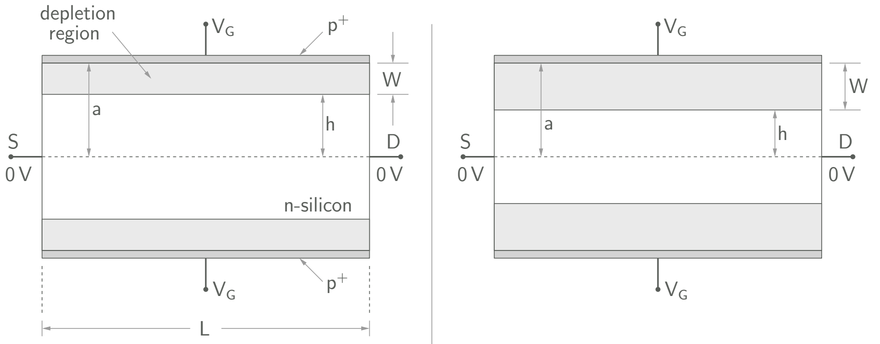
* Since the doping density in the p^+ region is much larger than that in the n region, the depletion region extends mostly on the n-side.



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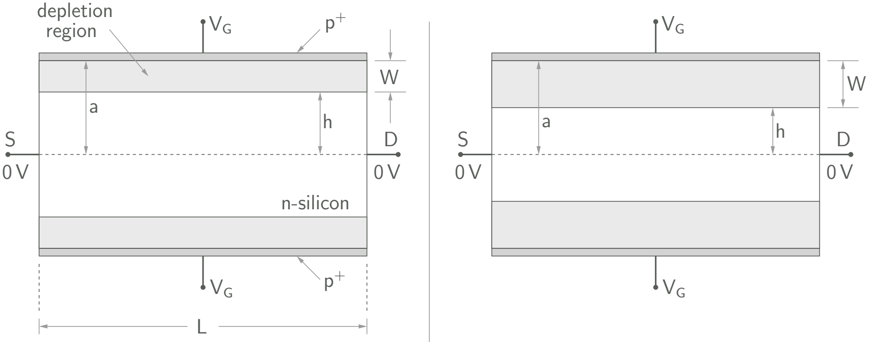

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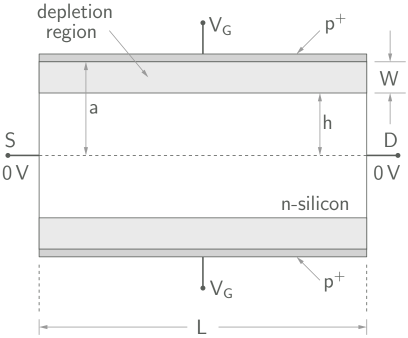
* Since the doping density in the p^+ region is much larger than that in the n region, the depletion region extends mostly on the n-side.
* As the gate reverse bias is increased, the depletion width (W) increases, and the width of the neutral region ($2h$) decreases, since $h = a - W$.



depletion region
V_G
p^+
W
a
h
S
D
0 V
0 V
n-silicon
V_G
p^+
L

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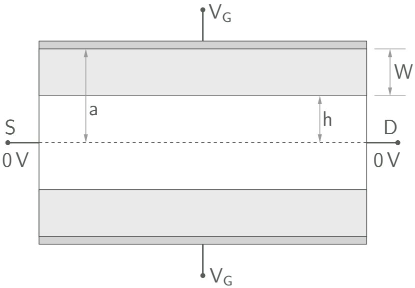
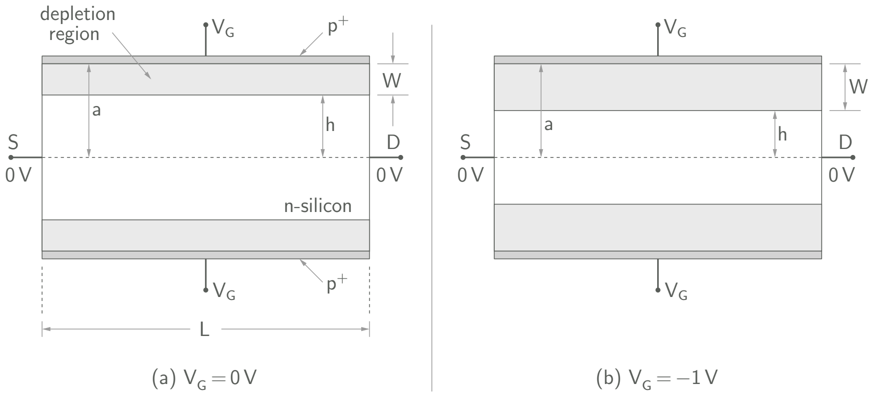
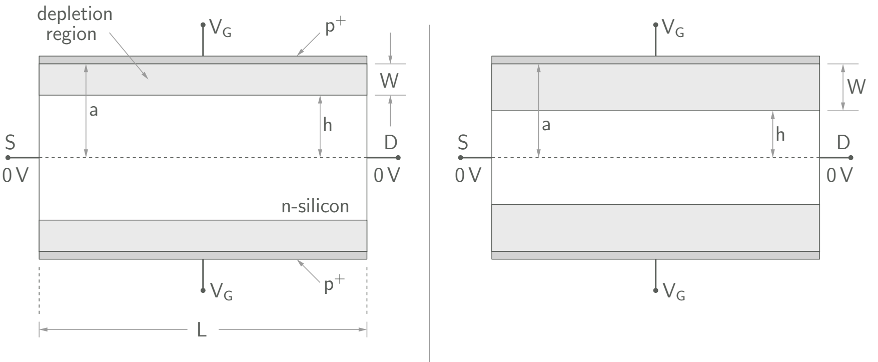


V_G
W
a
h
S
D
0 V
0 V
V_G

(b) $V_G = -1\,V$



* The resistance offered by the *n* region (the "channel") is $R_{\text{ch}} = \dfrac{1}{\sigma}\,\dfrac{L}{\text{Area}} = \dfrac{L}{qN_d\mu_n(2hZ)}$.



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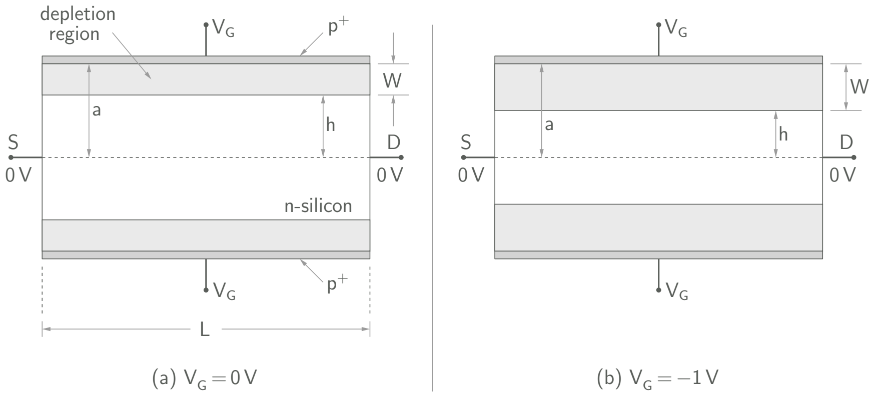

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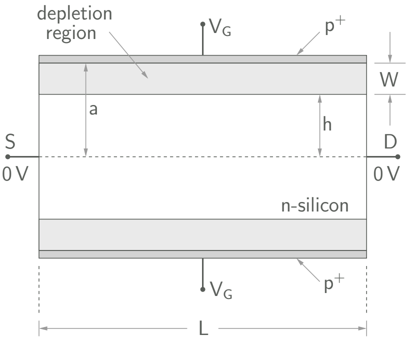
* $R_{ch} \propto \dfrac{1}{h} \rightarrow R_{ch} \uparrow$ as $h \downarrow$, i.e., as V_G is made more negative.
* When $W = a$ (i.e., $h = 0$), $R_{ch} \rightarrow \infty$, and the channel is said to be "pinched off."
  The corresponding gate voltage V_G is known as the "pinch-off" voltage V_P.

Example



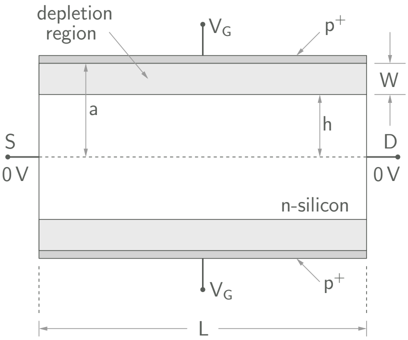
Consider an n-channel Si JFET with $N_d = 2 \times 10^{15}\,\text{cm}^{-3}$, $\mu_n = 1000\,\text{cm}^2/\text{V-s}$, $a = 1.5\,\mu\text{m}$, $L = 10\,\mu\text{m}$, $Z = 50\,\mu\text{m}$. Let the built-in voltage for the p^+n (gate-to-channel) junction be 0.8 V.

(a) Find the pinch-off voltage V_P.

(b) Compute the device resistance for $V_G = 0\,\text{V}, -1\,\text{V}, -2\,\text{V}$.

(c) Plot the I_D–V_D characteristics for $V_G = 0\,\text{V}, -1\,\text{V}, -2\,\text{V}$, for $0 < V_D < 50\,\text{mV}$.

Example

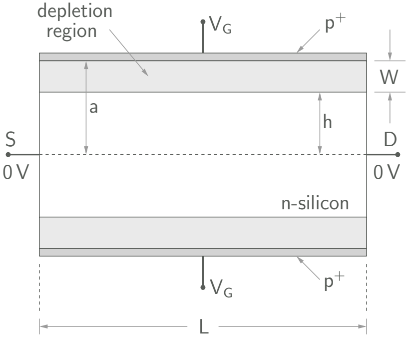


(a) For a p^+n junction, $W = \sqrt{\dfrac{2\epsilon}{qN_d}(V_{bi} - V)}$ where $V = V_G - 0 = V_G$, since $V_S = V_D = 0\,\text{V}$.

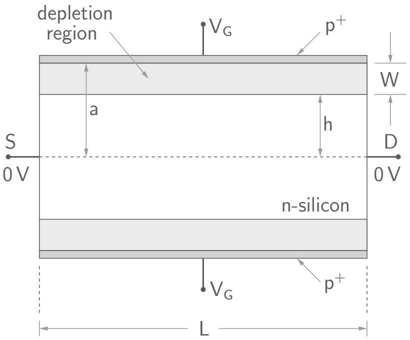
At pinch-off, $V_G = V_P$, and $W = a \;\rightarrow\; a = \sqrt{\dfrac{2\epsilon}{qN_d}(V_{bi} - V_P)} \rightarrow V_P = V_{bi} - \dfrac{qN_d}{2\epsilon}\,a^2$.

$\rightarrow V_P = 0.8 - \dfrac{1.6 \times 10^{-19} \times 2 \times 10^{15}}{2 \times 11.7 \times 8.85 \times 10^{-14}}\,(1.5 \times 10^{-4})^2 = 0.8 - 3.48 \approx -2.7\,\text{V}.$

Example

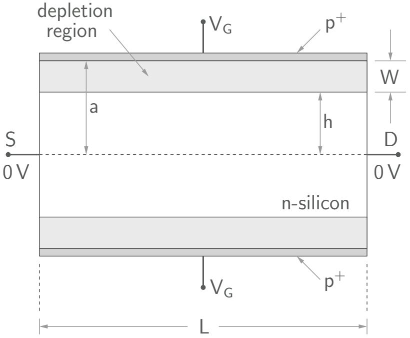


Example



(b) The channel resistance is $R_{\rm ch} = \dfrac{1}{\sigma}\dfrac{L}{\rm Area} = \dfrac{1}{qN_d\mu_n}\dfrac{L}{2hZ}$, $\quad h = a - W = a - \sqrt{\dfrac{2\epsilon}{qN_d}(V_{\rm bi} - V_G)}$.

Example



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V_G	R_{ch}
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−1 V	7.4 kΩ
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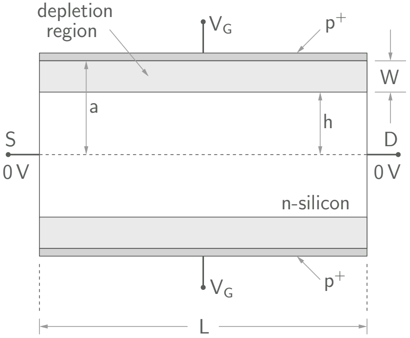
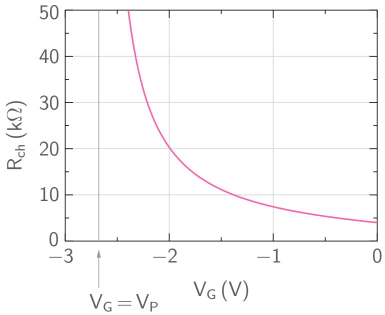
Example





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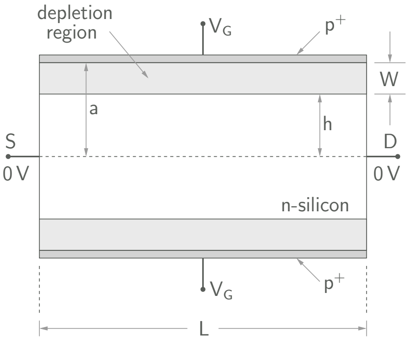

(c) Since V_D is small ($< 50\,\text{mV}$), h can be assumed to be constant from the source end to the drain end.

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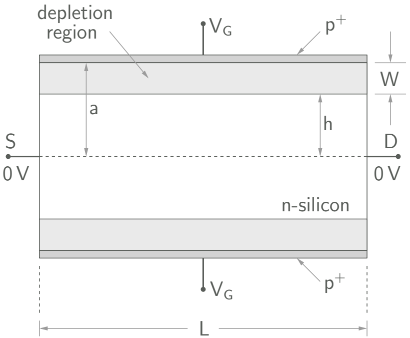

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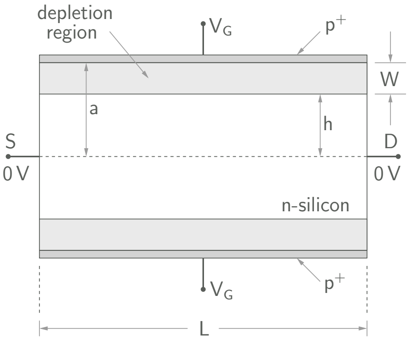
$$R_{\text{ch}} = \frac{1}{qN_d\mu_n}\frac{L}{2hZ} = \frac{1}{qN_d\mu_n}\frac{L}{2Z}\frac{1}{a - \sqrt{\dfrac{2\epsilon}{qN_d}(V_{\text{bi}} - V_G)}}$$

Example



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$$\rightarrow I_D = \frac{V_D}{R_{\text{ch}}(V_G)}.$$

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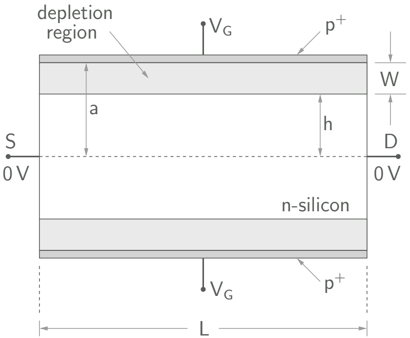

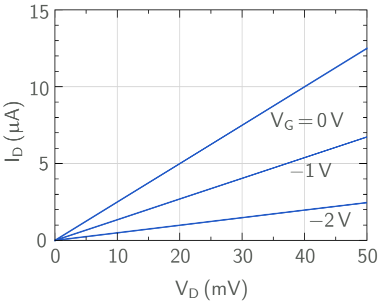

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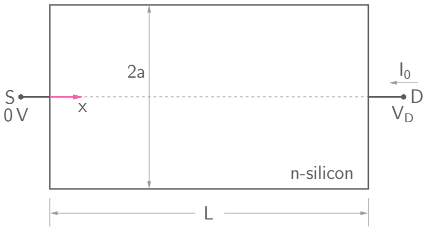
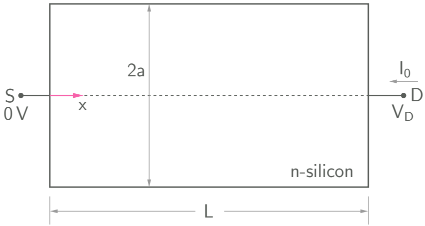
Consider a rectangular bar of *n*-type silicon with a uniform doping density N_d.



JFET I-V relationship

Consider a rectangular bar of n-type silicon with a uniform doping density N_d.

* $I_D = \text{Area} \times |J|$



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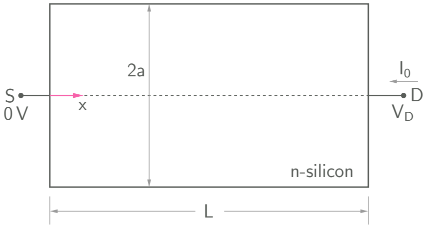

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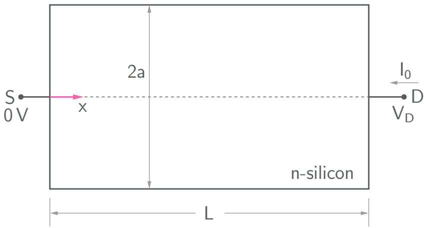

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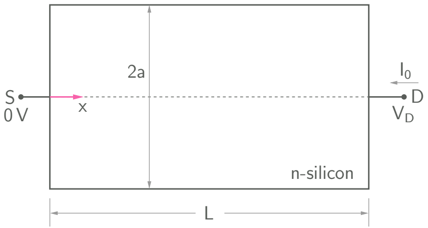

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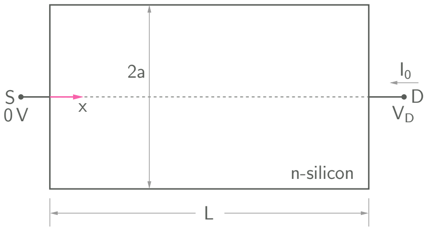

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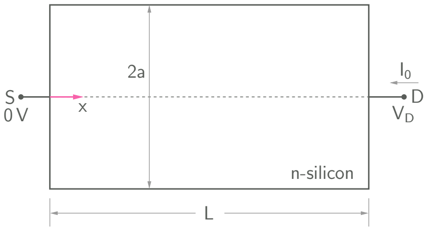
  $\rightarrow V(L) - V(0) = -\mathcal{E}_0 L \rightarrow \mathcal{E}_0 = -\dfrac{V_D}{L}.$



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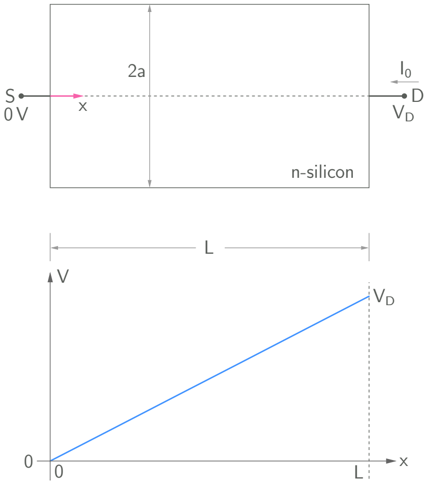

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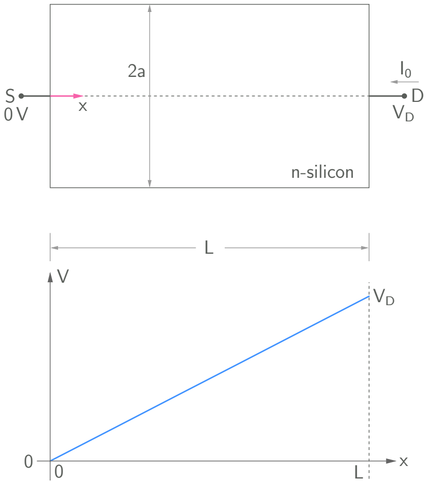

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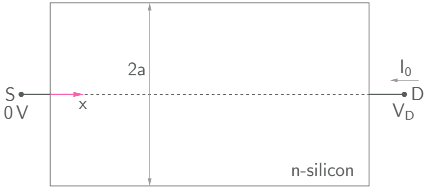

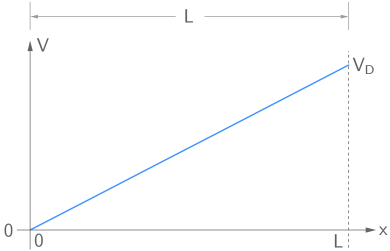

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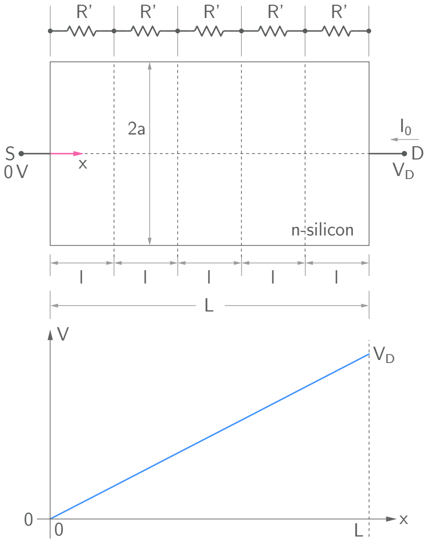

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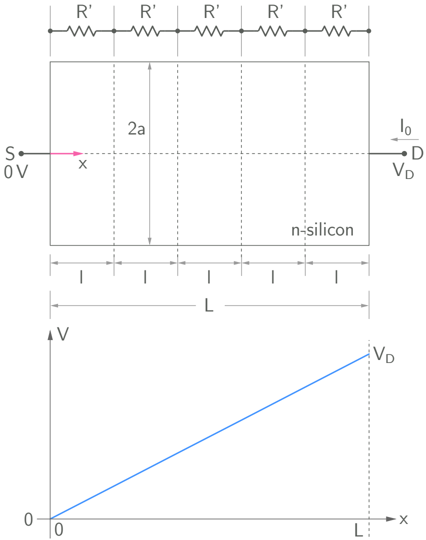

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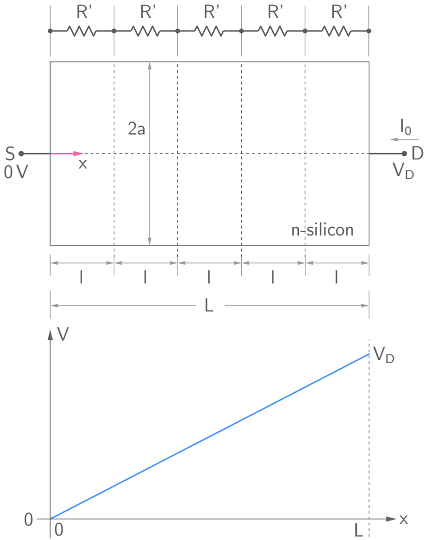

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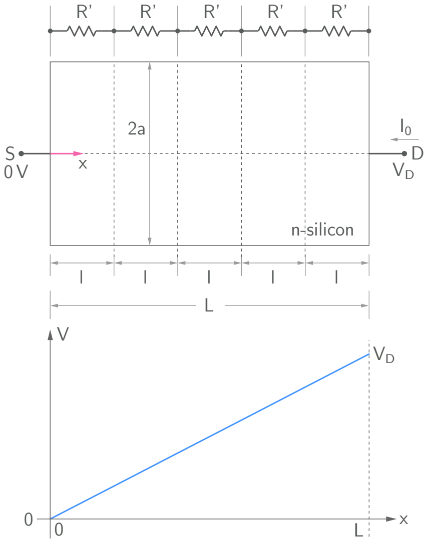
We will find this picture useful in understanding the functioning of the JFET.



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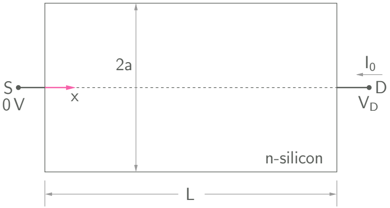

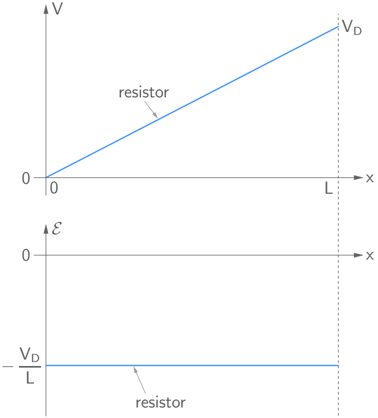

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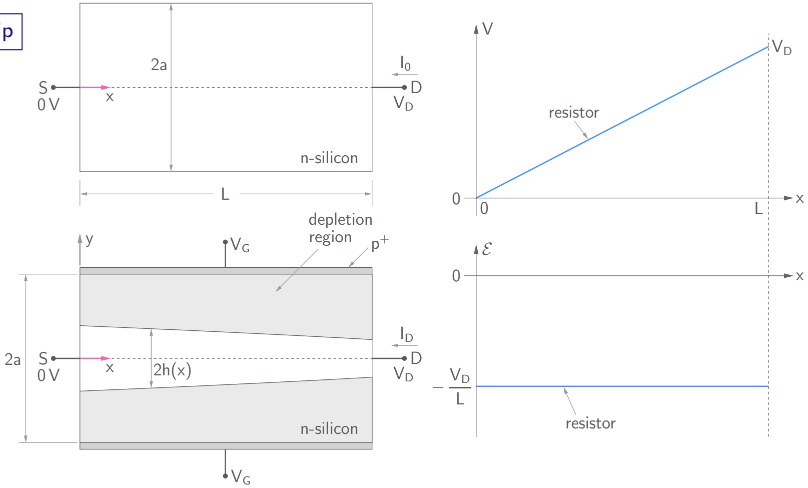

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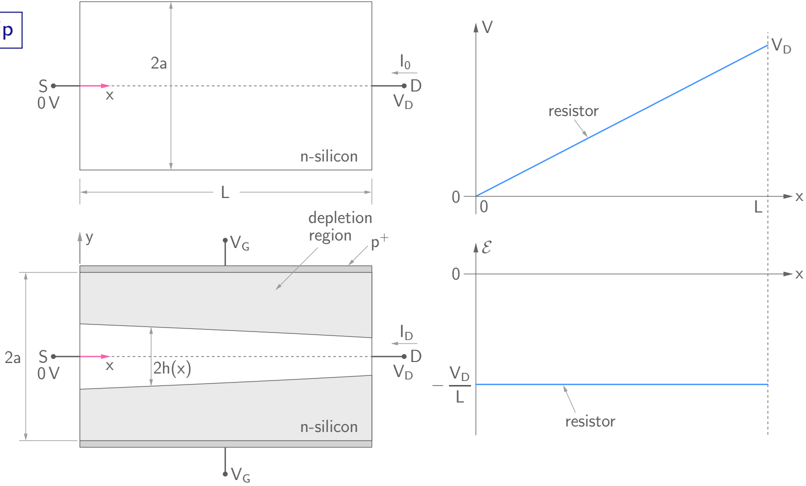
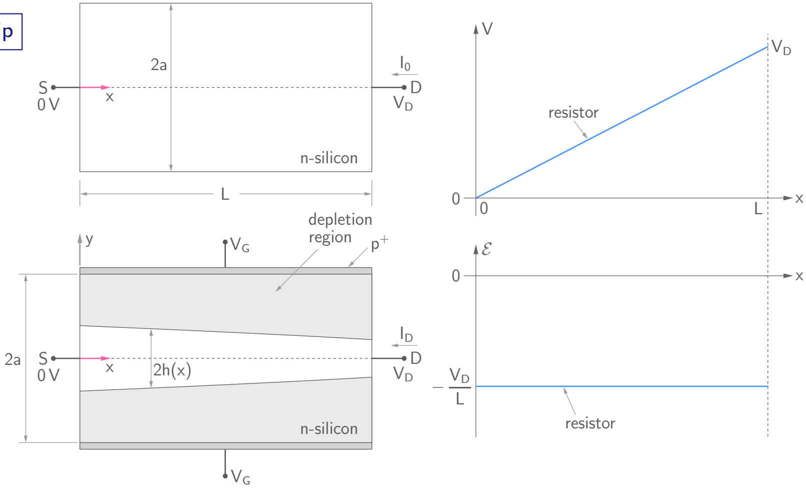


Consider an n-channel JFET with a drain voltage V_D.

JFET I-V relationship



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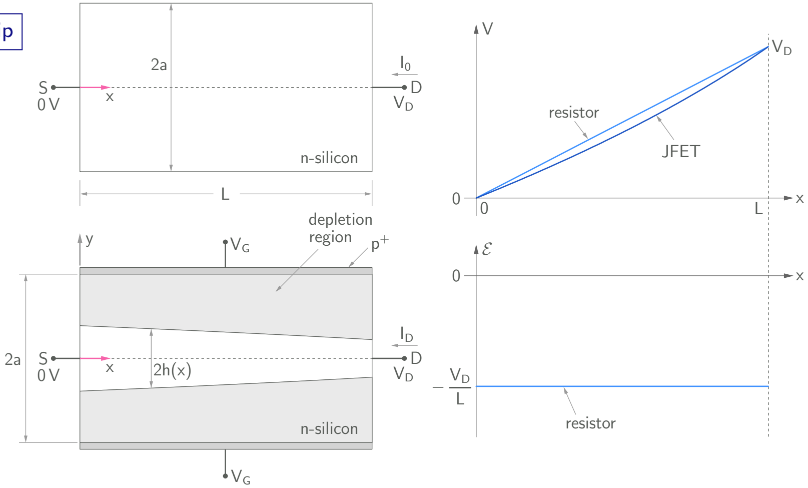
- We expect the potential to rise from 0 V at the source end to V_D at the drain end.

JFET I-V relationship



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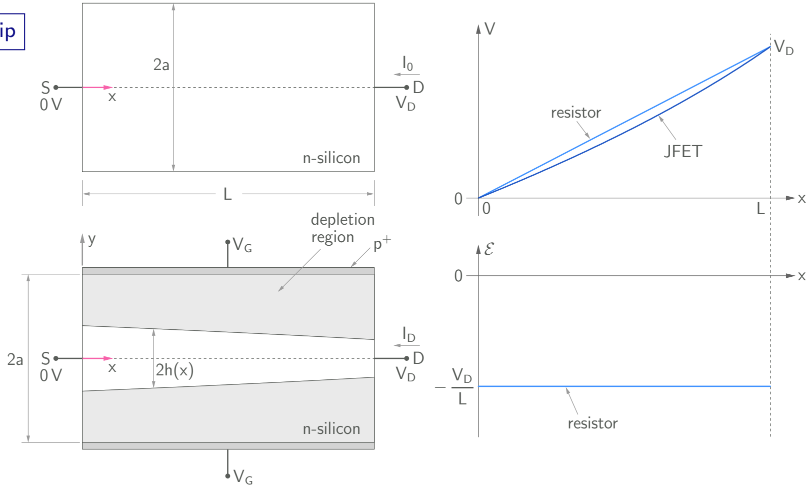

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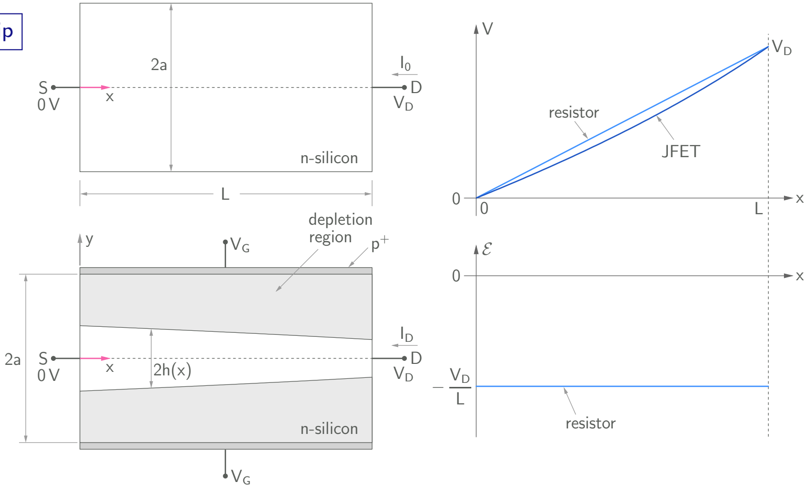

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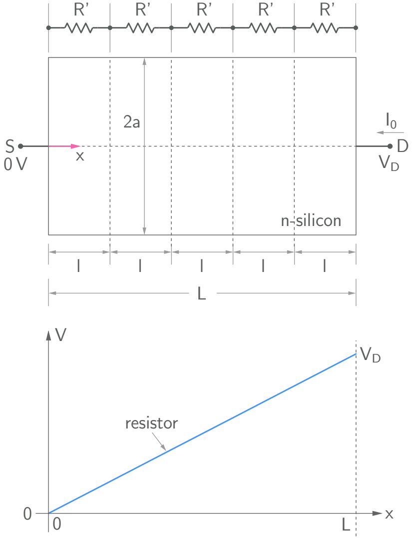
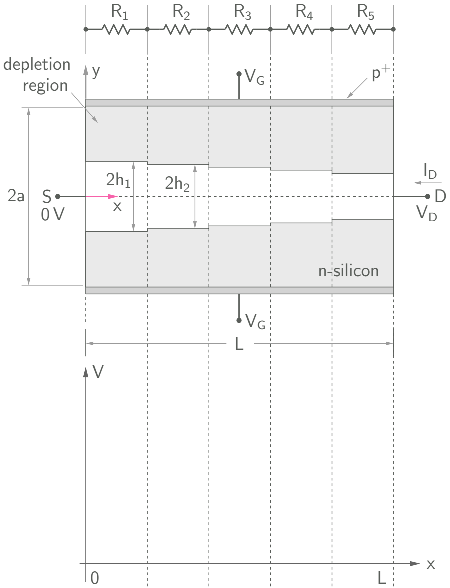
* V_R increases with x $\rightarrow$ $W\,(\propto \sqrt{V_{bi} + V_R})\uparrow$ $\rightarrow$ $h\downarrow$

JFET: a discretised view





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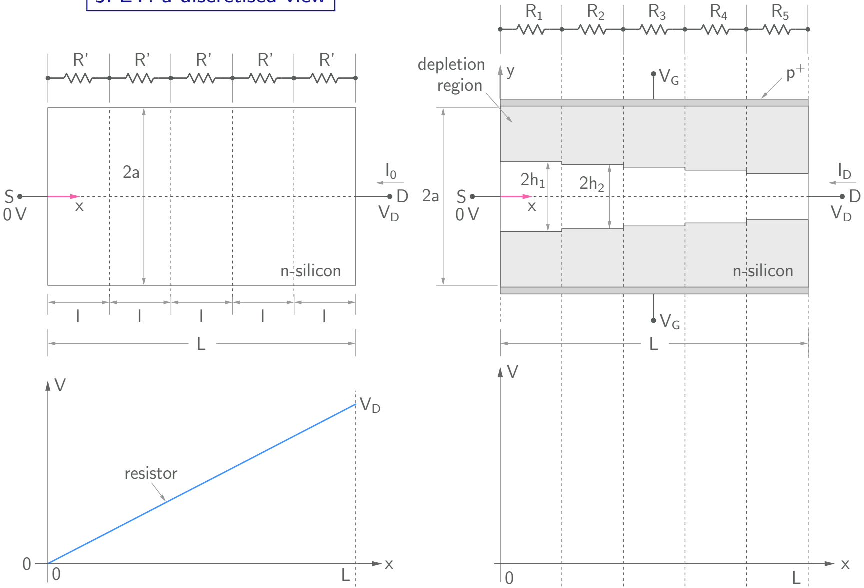

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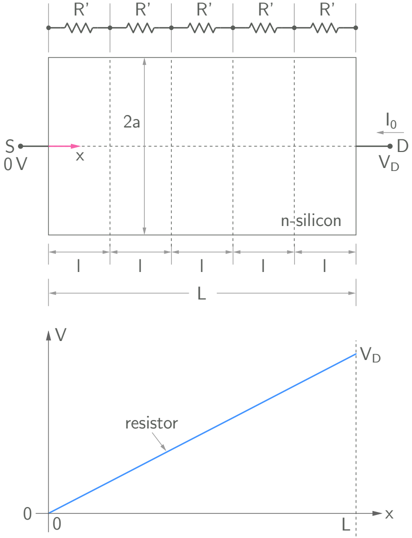

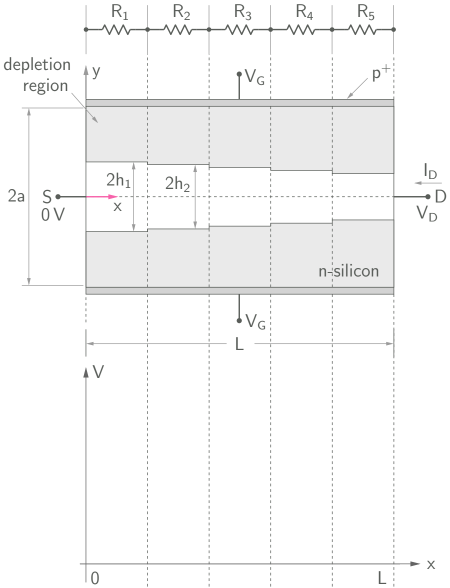

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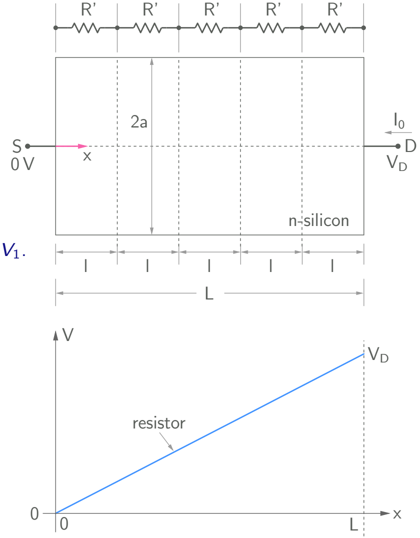

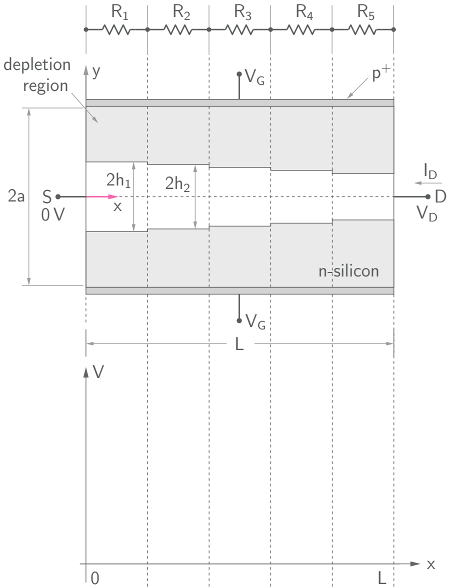

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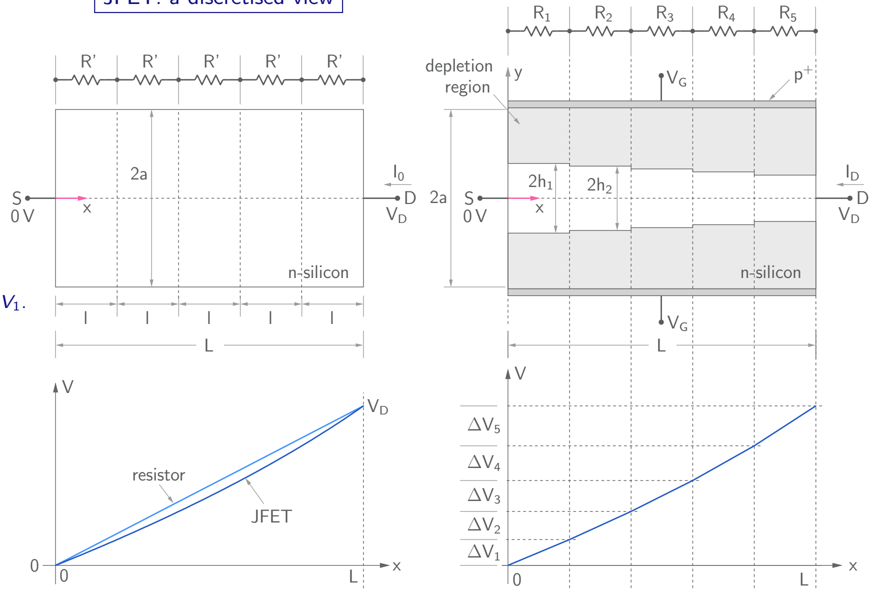

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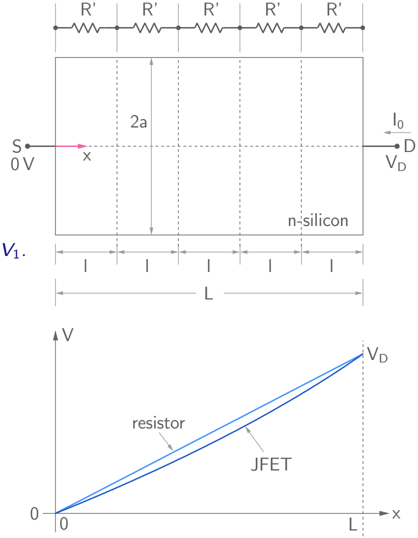

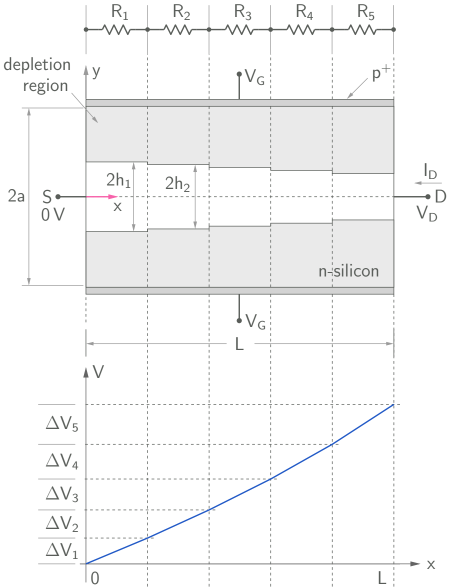

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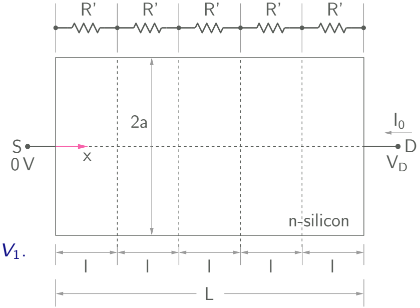

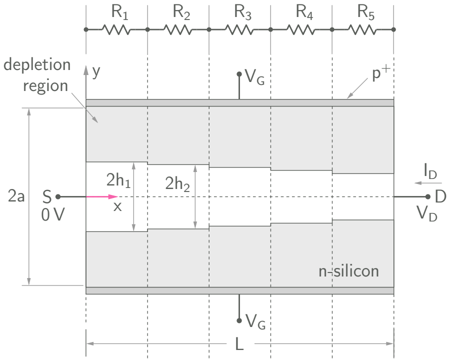

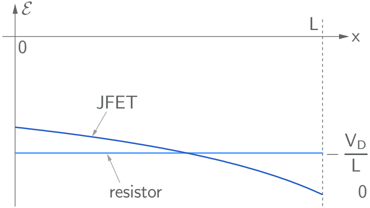

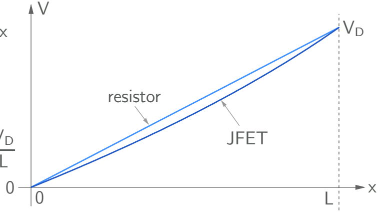

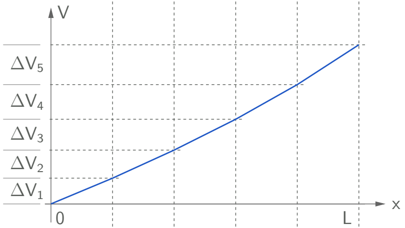

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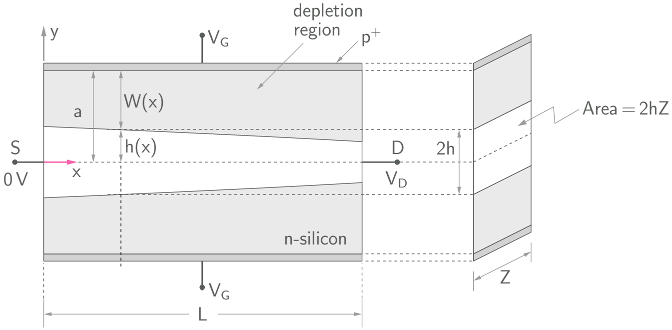
JFET I-V relationship



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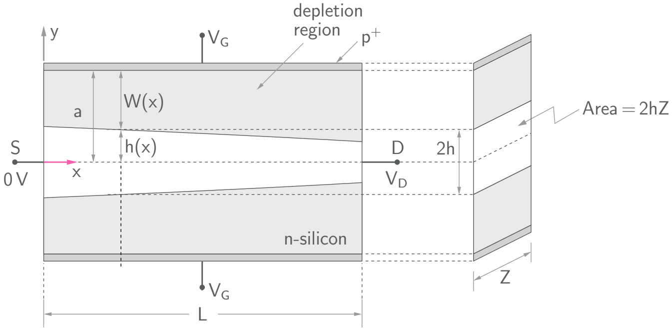
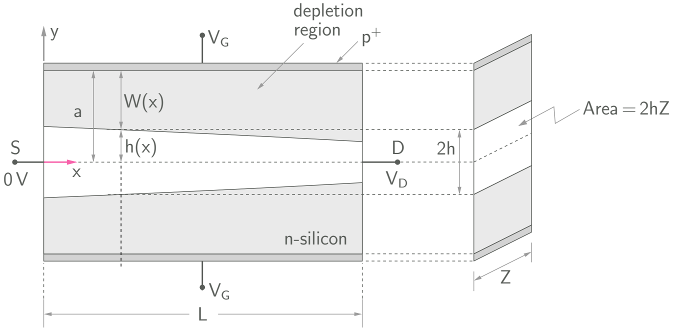


* Gradual channel approximation:

JFET I-V relationship



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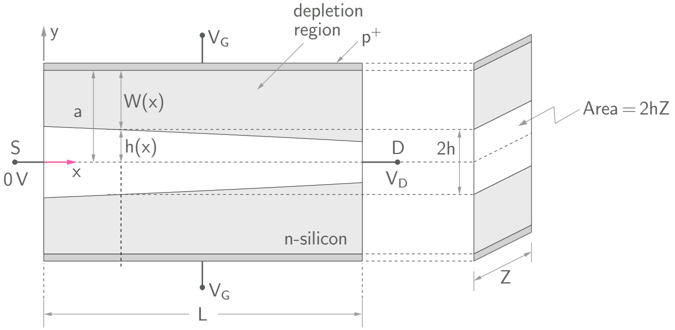

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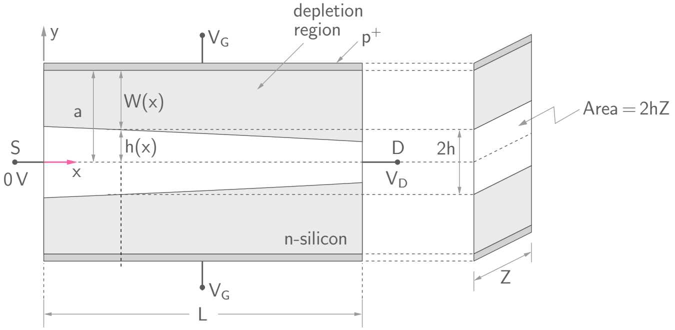

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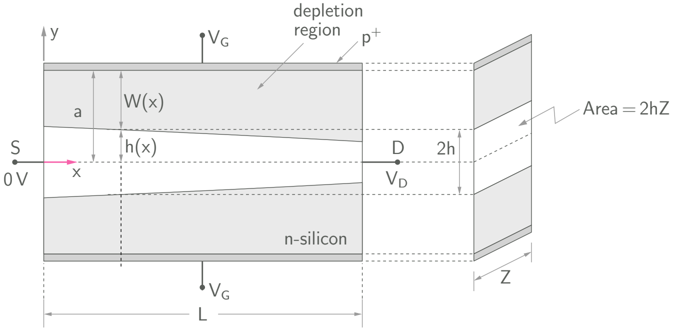
JFET I-V relationship



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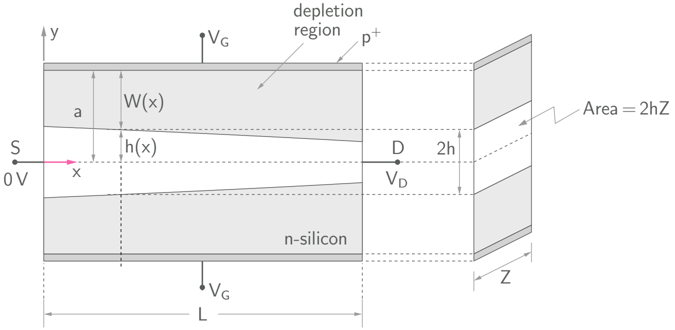
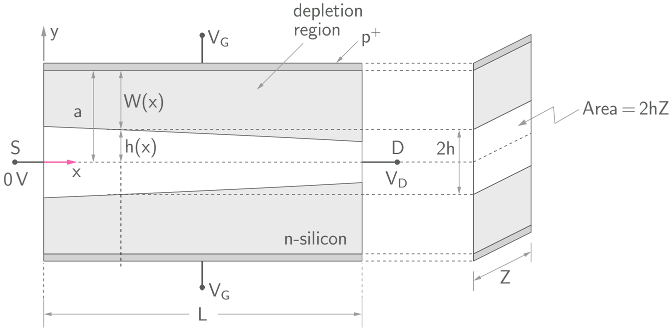
  $\rightarrow W(x) = \sqrt{\frac{2\epsilon}{qN_d}(V_{bi} - V(x))}$, as in a 1D *pn* junction.

JFET I-V relationship



In the neutral channel region, $V(x,y) \approx V(x) \rightarrow \mathbf{J}_n^{\text{drift}}$ has only x-component.

JFET I-V relationship

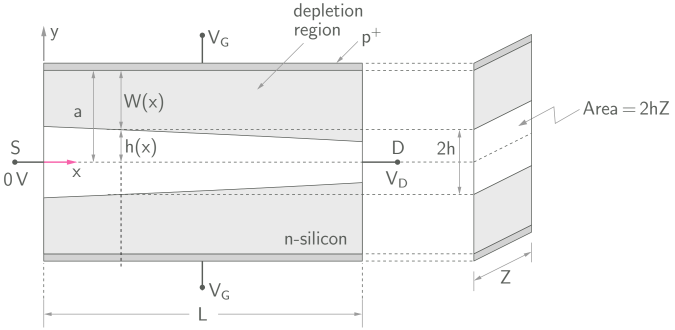


In the neutral channel region, $V(x,y) \approx V(x) \rightarrow \mathbf{J}_n^{\text{drift}}$ has only x-component.

$\rightarrow J_n(x,y) = -q\mu_n N_d \dfrac{dV}{dx}$,

where we have neglected J_n^{diff}, a second-order effect.

JFET I-V relationship



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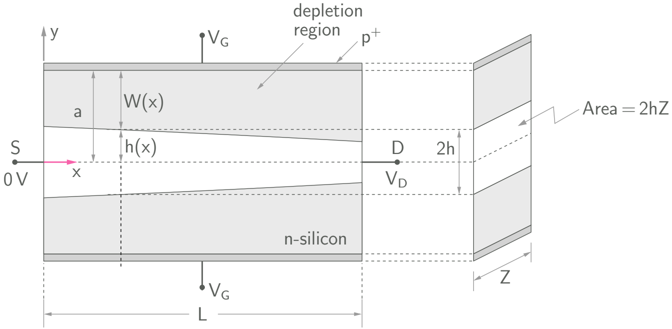
where we have neglected J_n^{diff}, a second-order effect.

Since the same current flows throughout the device,

$$I_D = \iint J_n(x,y)\, dy\, dz = -q\mu_n N_d \iint \frac{dV}{dx}\, dy\, dz.$$

JFET I-V relationship



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Since the same current flows throughout the device,

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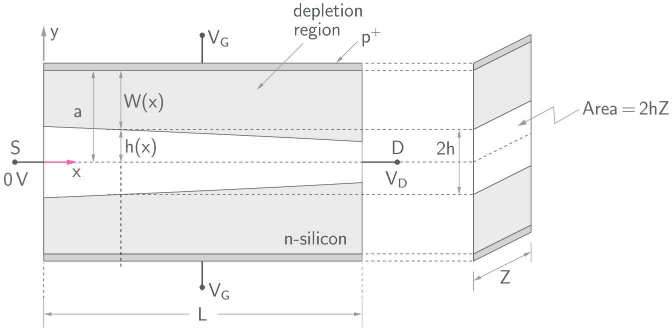
With $L \gg a$, we can say that $\dfrac{dV}{dx}$ depends only on x.

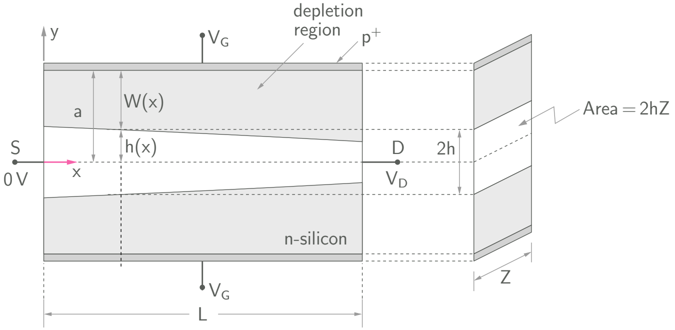
$\rightarrow I_D = -q\mu_n N_d\,(2hZ)\dfrac{dV}{dx}$.

JFET I-V relationship



$$I_D = -q\mu_n N_d\,(2hZ)\,\frac{dV}{dx}\,.$$

JFET I-V relationship

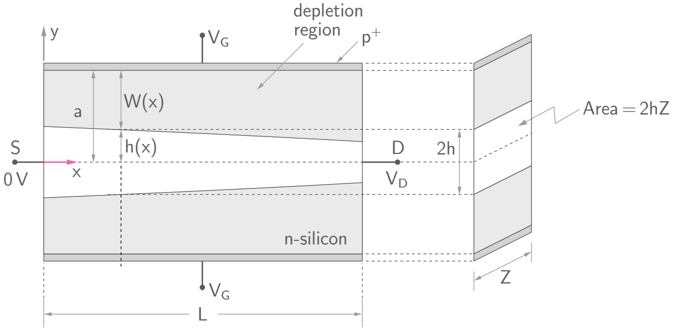


$$I_D = -q\mu_n N_d\,(2hZ)\,\frac{dV}{dx}.$$

Integrating from $x=0$ to $x=L$,

$$\int_0^L I_D\,dx = -q\mu_n N_d\,(2Z)\int_0^{V_D} h\,dV \rightarrow I_D L = -q\mu_n N_d\,(2Z)a\int_0^{V_D}\left(1-\frac{W}{a}\right)dV \;\because\; h = a - W = a\left(1-\frac{W}{a}\right).$$

JFET I-V relationship



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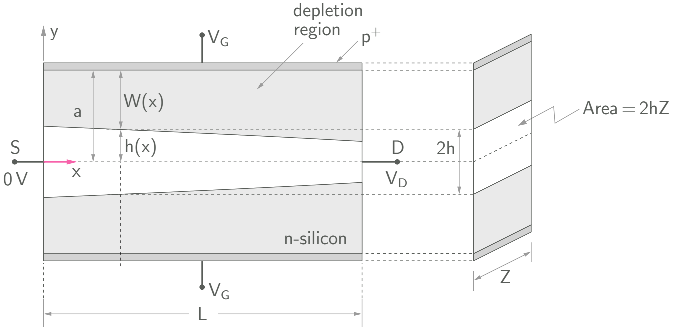
The depletion width W is $W(V) = \sqrt{\dfrac{2\epsilon}{qN_d}\,[V_{\rm bi} - (V_G - V)]}$.

JFET I-V relationship



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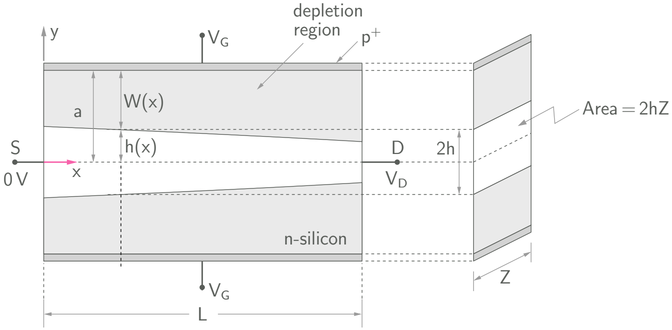
$$\rightarrow I_D = G_0\left\{V_D - \frac{2}{3}\,(V_{\text{bi}} - V_P)\left[\left(\frac{V_D + V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P}\right)^{3/2} - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P}\right)^{3/2}\right]\right\},$$

JFET I-V relationship



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$$\rightarrow I_D = G_0\left\{V_D - \frac{2}{3}\,(V_{\rm bi}-V_P)\left[\left(\frac{V_D+V_{\rm bi}-V_G}{V_{\rm bi}-V_P}\right)^{3/2} - \left(\frac{V_{\rm bi}-V_G}{V_{\rm bi}-V_P}\right)^{3/2}\right]\right\},$$

where $G_0 = \dfrac{(2aZ)}{L} \times (q\mu_n N_d)$ is the conductance of the channel if there was no depletion, i.e., $h = a$ throughout.

JFET *I*-*V* relationship

$V_G = -0.5\,V$

$a = 1.5\,\mu m$

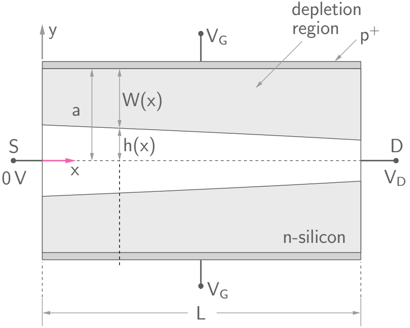
$L = 10\,\mu m$

$Z = 50\,\mu m$

$V_{bi} = 0.8\,V$

$N_d = 2 \times 10^{15}\,cm^{-3}$

$\mu_n = 1000\,cm^2/V\text{-}s$



JFET I-V relationship

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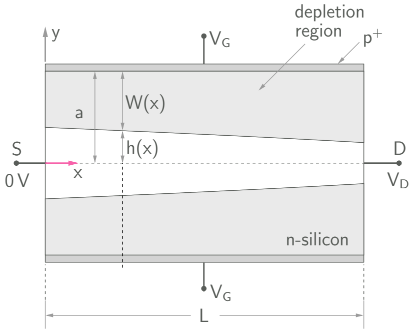

$$I_D = G_0 \left\{ V_D - \frac{2}{3}(V_{bi} - V_P)\left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P}\right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P}\right)^{3/2}\right]\right\}, \quad G_0 = \frac{(2aZ)}{L} \times (q\mu_n N_d).$$

JFET I-V relationship

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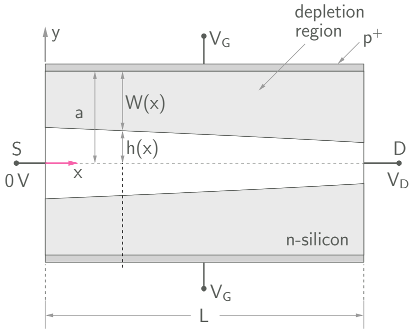

$$I_D = G_0 \left\{ V_D - \frac{2}{3}(V_{\text{bi}} - V_P) \left[\left(\frac{V_D + V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P} \right)^{3/2} - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P} \right)^{3/2} \right] \right\}, \quad G_0 = \frac{(2aZ)}{L} \times (q\mu_n N_d).$$

* The first term $G_0 V_D$ represents the maximum current that we can get from the JFET structure without any channel depletion.

JFET I-V relationship

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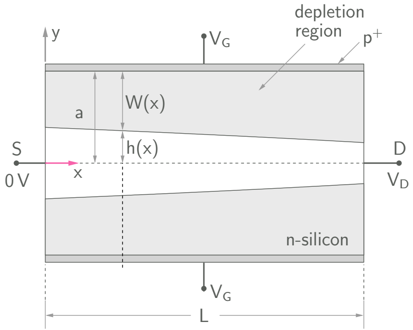

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* The second term represents reduction of the current due to channel depletion.

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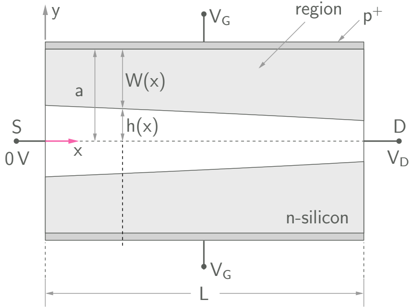

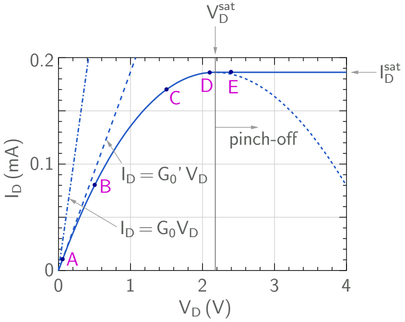

$$I_D = G_0 \left\{ V_D - \frac{2}{3}\,(V_{\text{bi}} - V_P) \left[\left(\frac{V_D + V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P} \right)^{3/2} - \left(\frac{V_{\text{bi}} - V_G}{V_{\text{bi}} - V_P} \right)^{3/2} \right] \right\}, \quad G_0 = \frac{(2aZ)}{L} \times (q\mu_n N_d).$$

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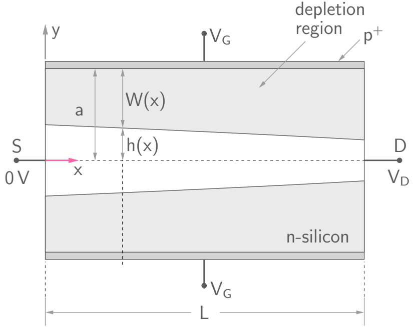

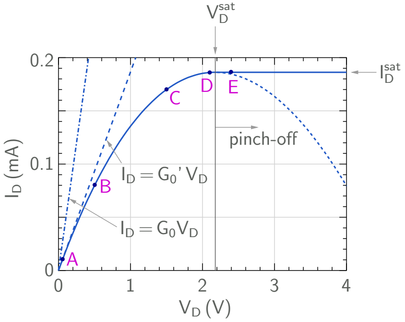

$$I_D = G_0\left\{V_D - \frac{2}{3}\left(V_{bi} - V_P\right)\left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P}\right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P}\right)^{3/2}\right]\right\},\quad G_0 = \frac{(2aZ)}{L}\times(q\mu_n N_d).$$

* The first term $G_0 V_D$ represents the maximum current that we can get from the JFET structure without any channel depletion.
* The second term represents reduction of the current due to channel depletion.
* Consider low values of V_D ($V_D \approx 0\,\text{V}$).
  - $\left.\dfrac{dI_D}{dV_D}\right|_{V_D\to 0} = G_0' = \dfrac{(2h_0 Z)}{L}\times(q\mu_n N_d)$, with $h_0 = a - \sqrt{\dfrac{2\epsilon}{qN_d}\left(V_{bi} - V_G\right)}$.

JFET I-V relationship

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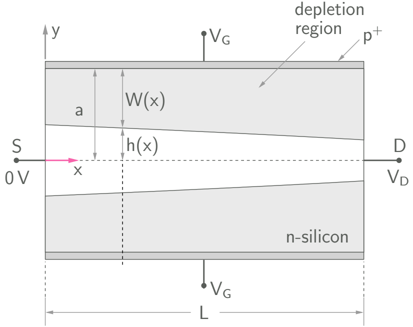

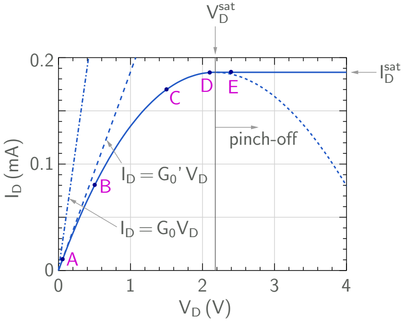

$$I_D = G_0 \left\{ V_D - \frac{2}{3}(V_{bi} - V_P) \left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\}, \quad G_0 = \frac{(2aZ)}{L} \times (q\mu_n N_d).$$

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* The second term represents reduction of the current due to channel depletion.
* Consider low values of V_D ($V_D \approx 0\,\text{V}$).
  - $\left.\dfrac{dI_D}{dV_D}\right|_{V_D \to 0} = G_0' = \dfrac{(2h_0 Z)}{L} \times (q\mu_n N_d)$, with $h_0 = a - \sqrt{\dfrac{2\epsilon}{qN_d}(V_{bi} - V_G)}$.
  - Note that G_0' is smaller than G_0, the channel conductance with *no* depletion.

M. B. Patil, IIT Bombay

JFET I-V relationship

$$I_D = -q\mu_n N_d\,(2hZ)\,\frac{dV}{dx}.$$

$V_G = -0.5\,\mathrm{V}$
$a = 1.5\,\mu\mathrm{m}$
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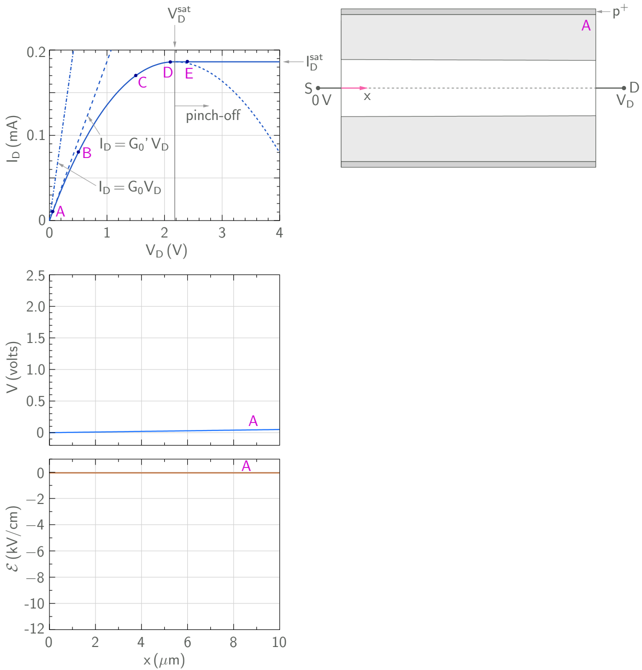

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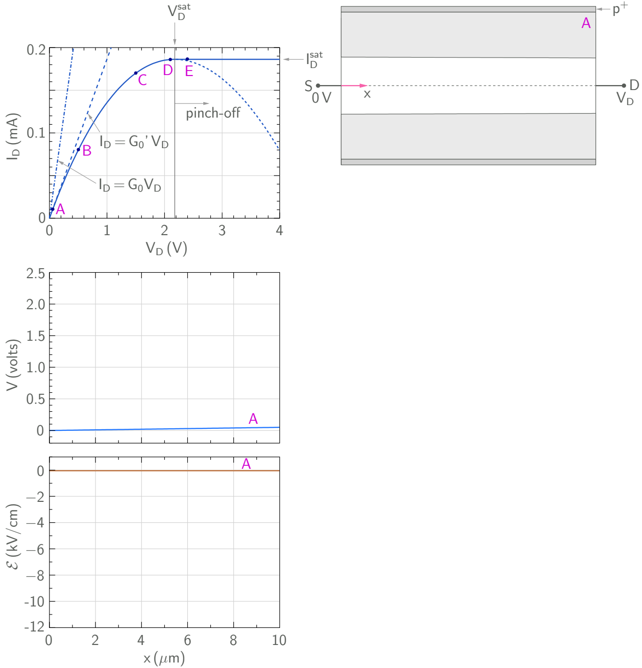
$$I_D = -q\mu_n N_d\,(2hZ)\,\frac{dV}{dx}.$$

* When V_D is increased, the reverse bias at the drain end increases, and the depletion width becomes larger at the drain end, causing the conduction channel to shrink.



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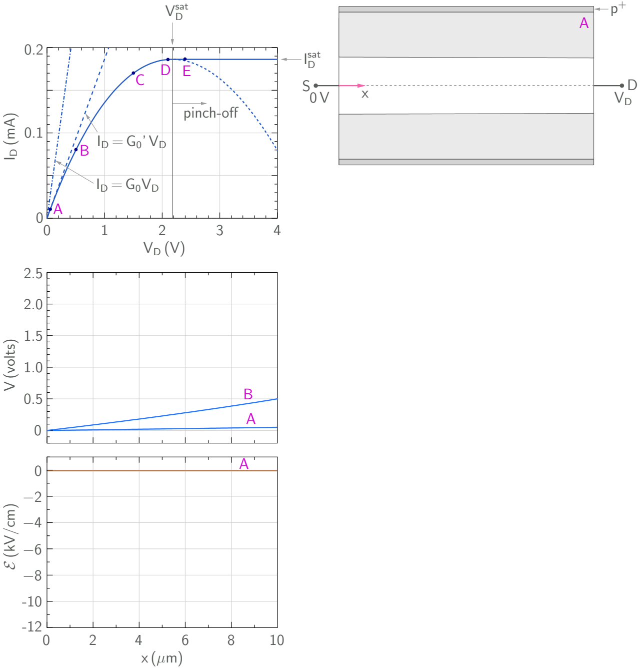

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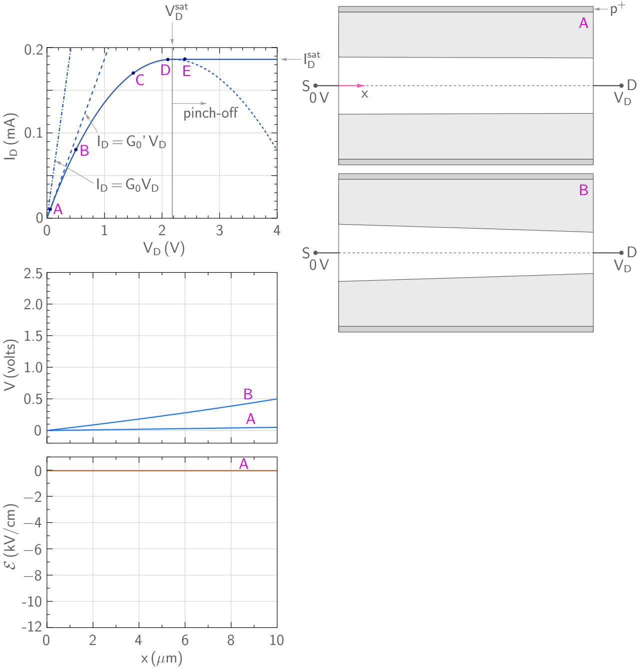

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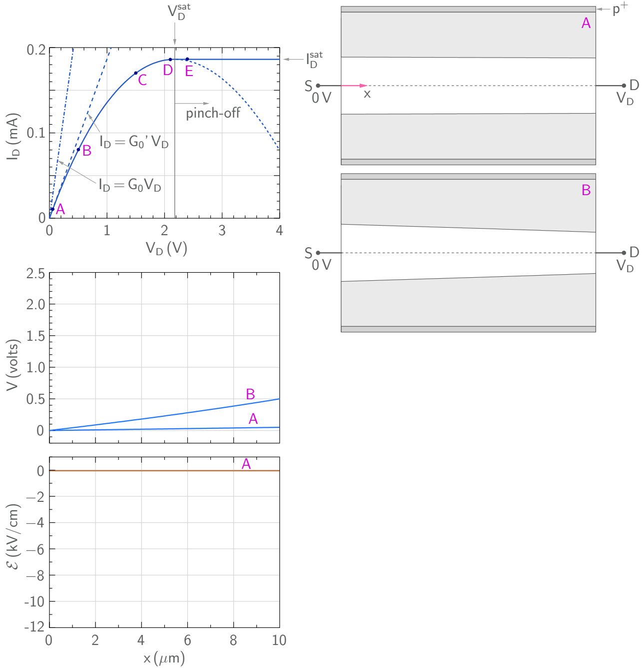
* When V_D is increased, the reverse bias at the drain end increases, and the depletion width becomes larger at the drain end, causing the conduction channel to shrink.
* Since the current, which is proportional to $h\,\dfrac{dV}{dx}$, is independent of x, a narrower channel at the drain end is accompanied by a larger electric field.



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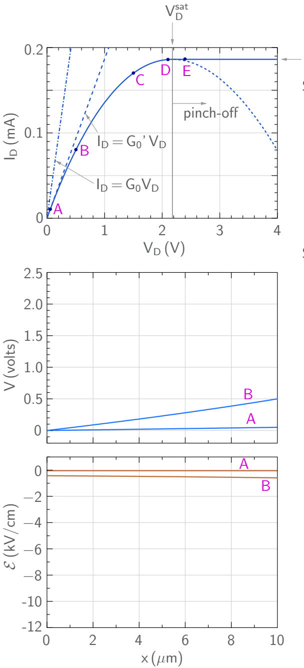

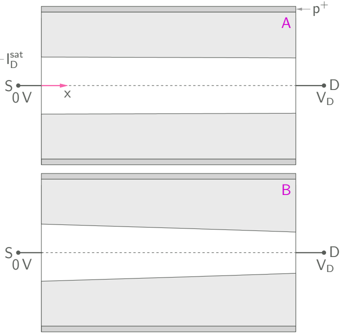

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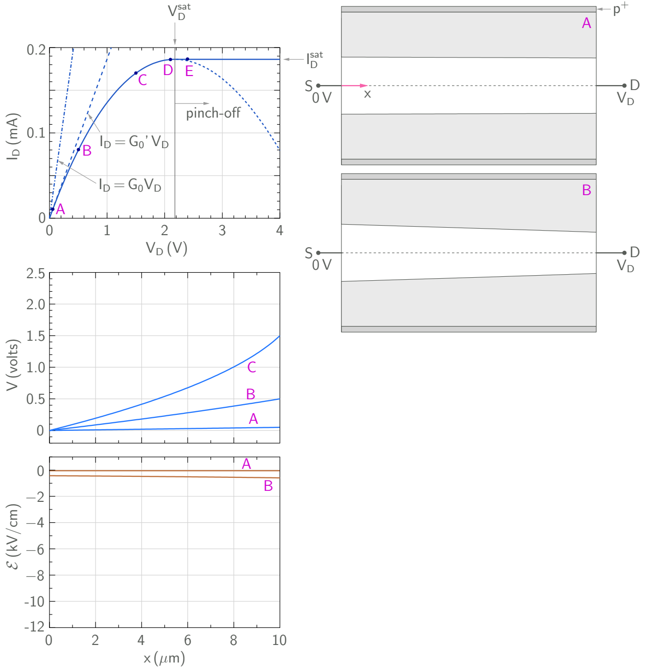

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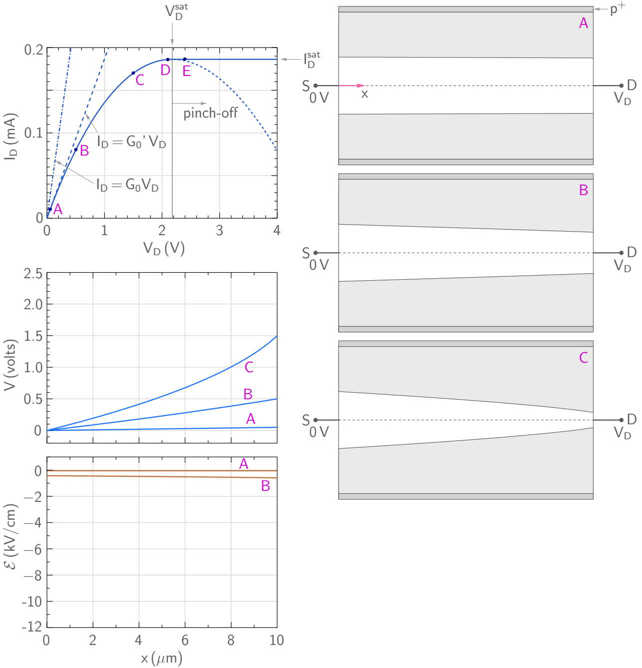
* Since the current, which is proportional to $h\,\dfrac{dV}{dx}$, is independent of x, a narrower channel at the drain end is accompanied by a larger electric field.



JFET I-V relationship

$V_G = -0.5\,\mathrm{V}$
$a = 1.5\,\mu\mathrm{m}$
$L = 10\,\mu\mathrm{m}$
$Z = 50\,\mu\mathrm{m}$
$V_{bi} = 0.8\,\mathrm{V}$
$N_d = 2 \times 10^{15}\,\mathrm{cm}^{-3}$
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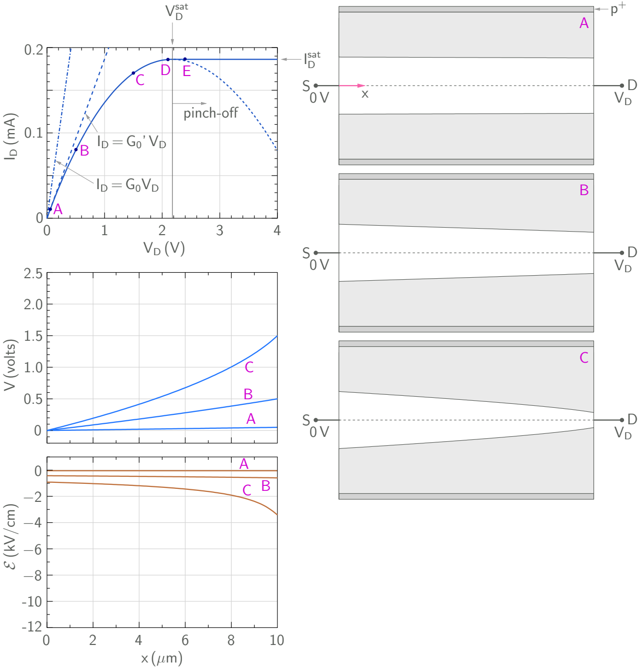

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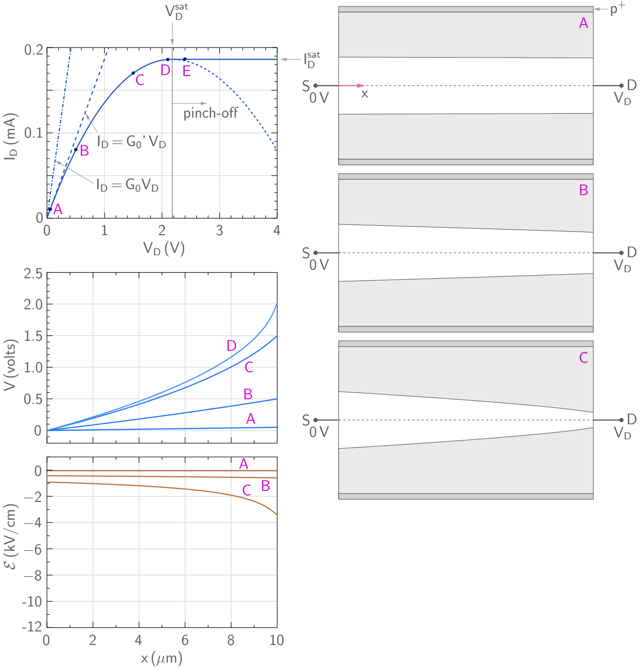

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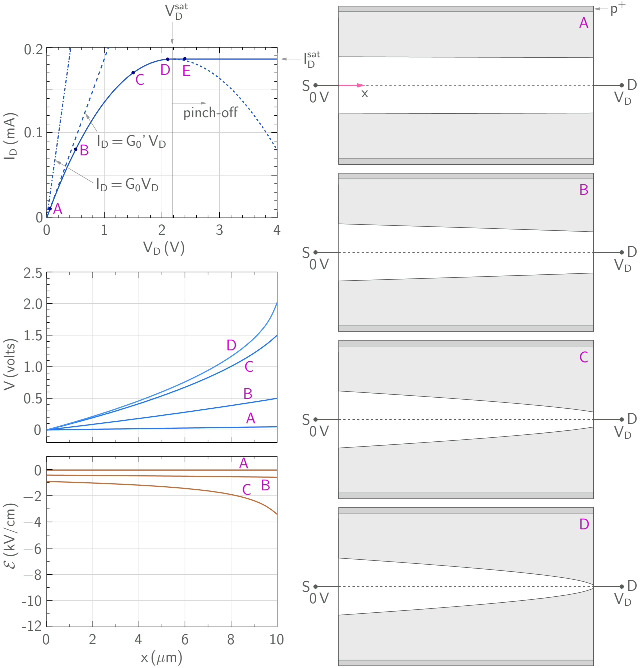

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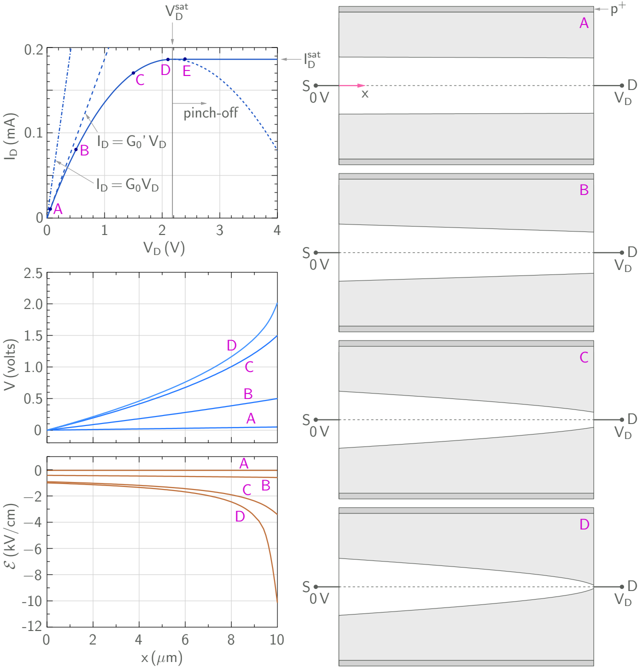

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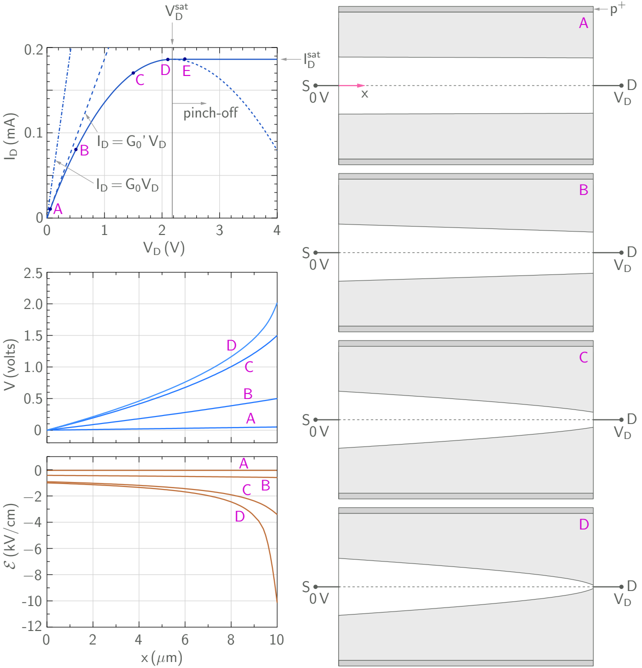
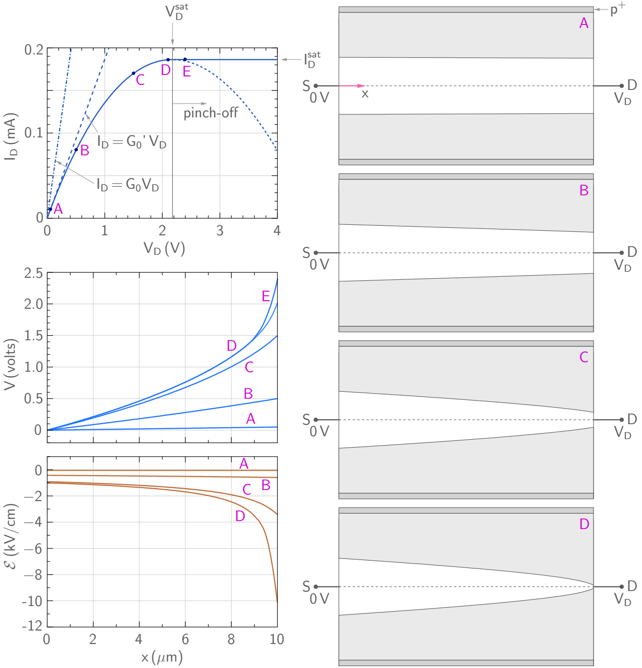
* At point D, as the current reaches its maximum value, the channel at the drain end is almost *pinched off* because the voltage across the p^+n junction at that point has become equal to the pinch-off voltage V_P, i.e., $V_G - V_D = V_P$.



M. B. Patil, IIT Bombay

JFET I-V relationship

What happens beyond punch-off?



JFET I-V relationship

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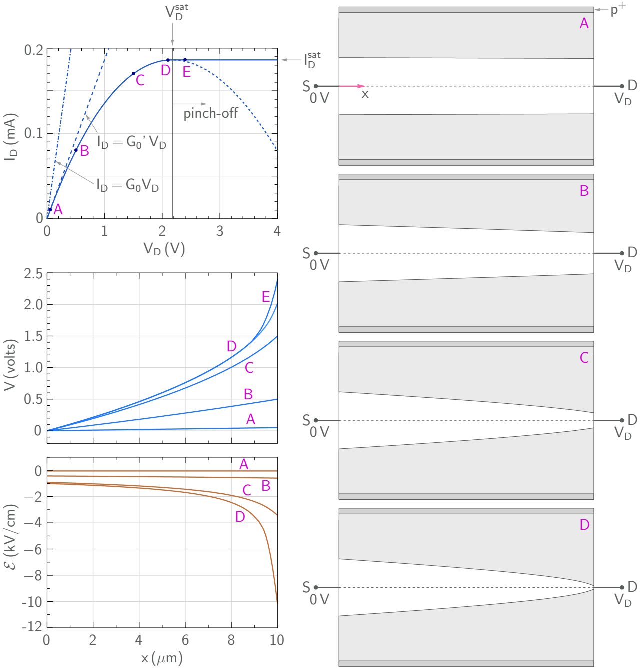
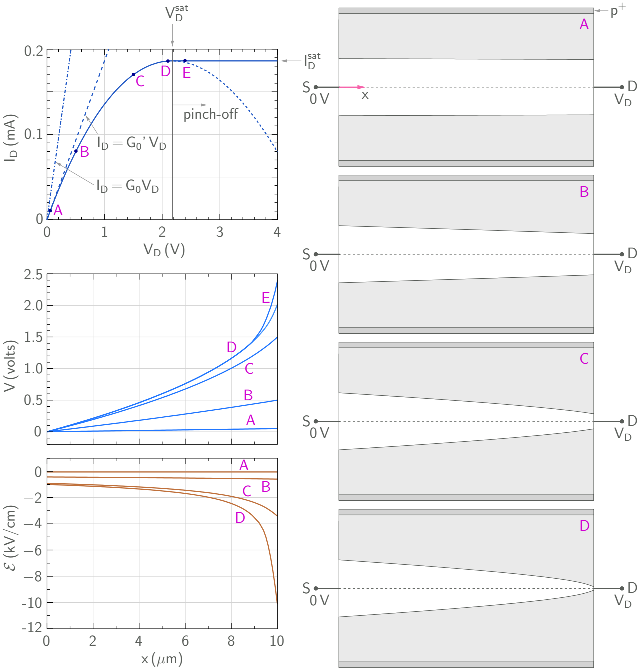


JFET I-V relationship

What happens beyond punch-off?

* Our I-V equation is not valid beyond pinch-off.
* What actually happens is that a narrow high-field region develops near the drain end, and the "excess" voltage (over and above V_D at point D) drops across this high-field region, leaving the conditions in the rest of the channel virtually the same as those at point D.



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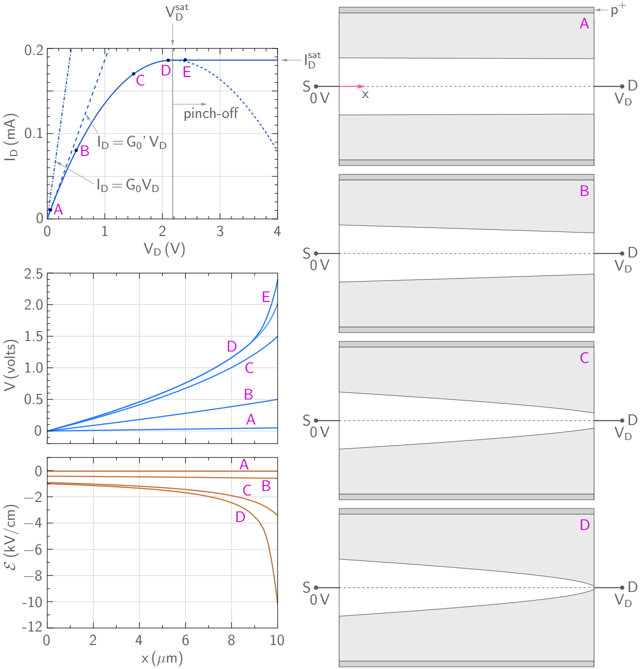
* Since the potential profile in most of the channel remains the same (as point D), $W(x)$, $h(x)$, $\mathcal{E}(x)$ also remain the same, and so does the current $\rightarrow$ the drain current saturates at I_D^{sat}.



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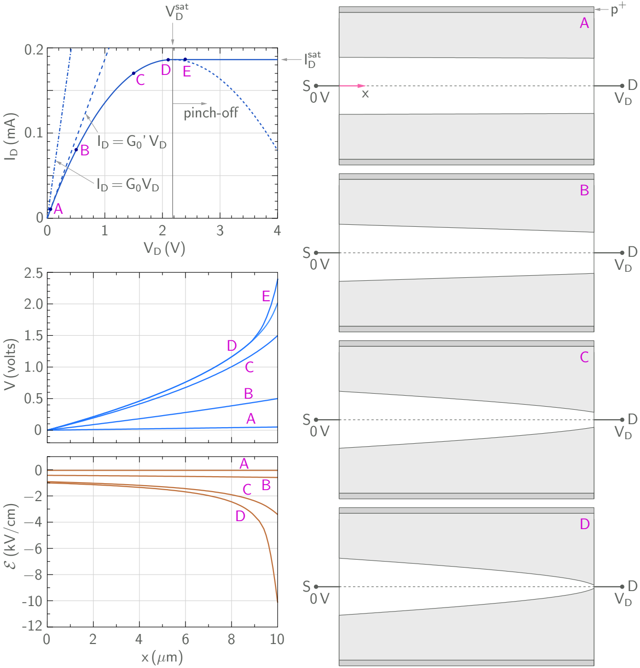
* The corresponding V_D is called the "drain saturation voltage" V_D^{sat}.



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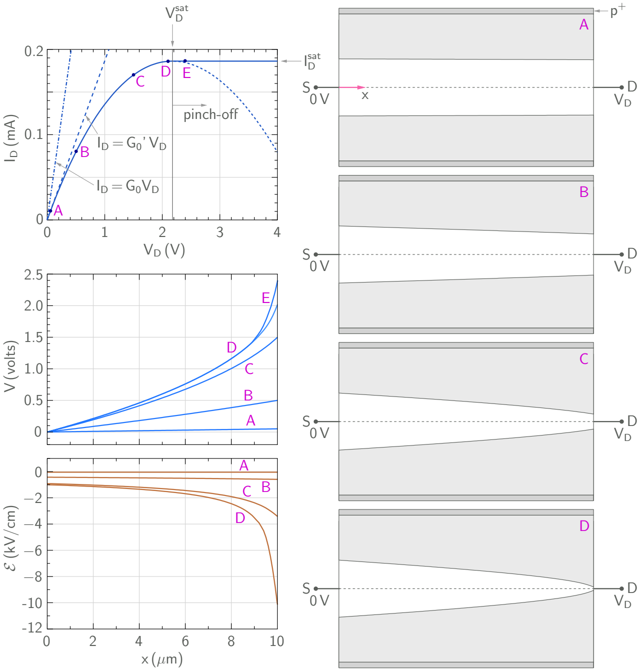
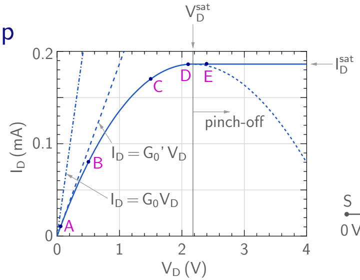
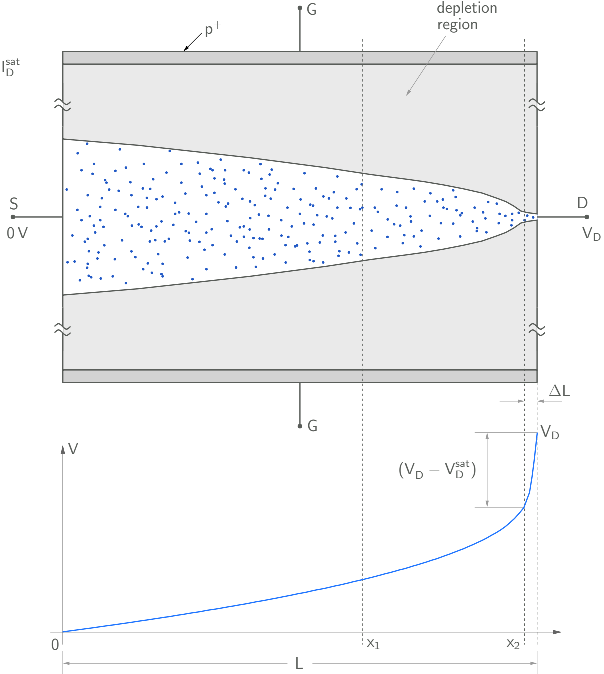
* The corresponding V_D is called the "drain saturation voltage" V_D^{sat}.
* $V_G - V_D^{sat} = V_P \rightarrow V_D^{sat} = V_G - V_P$. For example, if $V_P = -2.5\,V$, $V_G = -1\,V$, the drain current will saturate at $V_D^{sat} = -1 - (-2.5) = 1.5\,V$.



JFET I-V relationship





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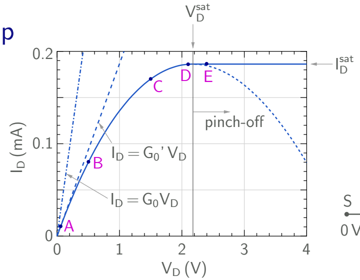
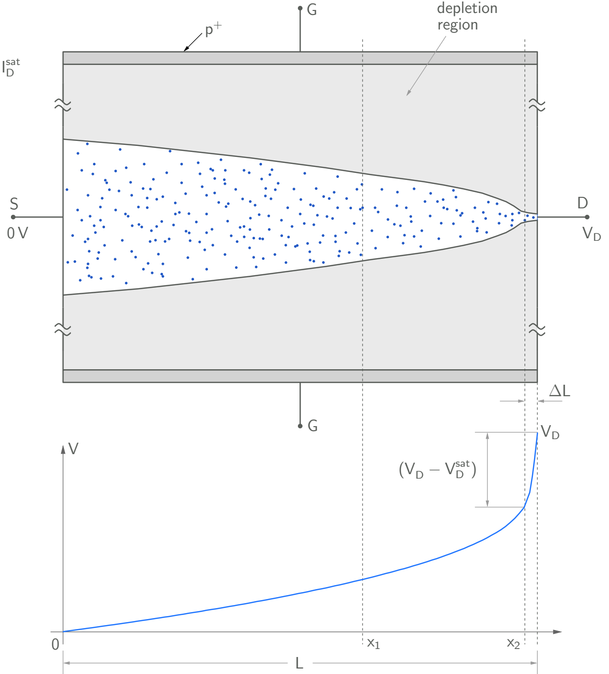
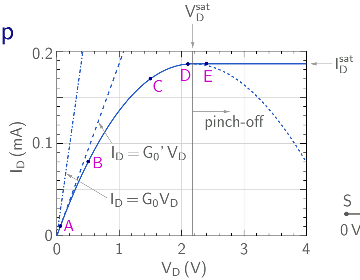
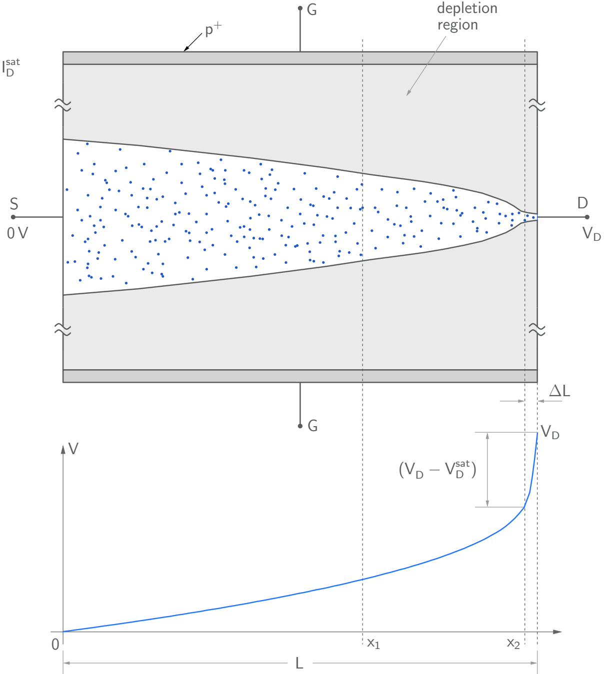




* In the region near the drain end (between $x = x_2$ and $x = L$), the electric field is larger than the rest of the channel. The "excess" voltage, $V_D - V_D^{sat}$, drops across this region.

JFET *I*-*V* relationship





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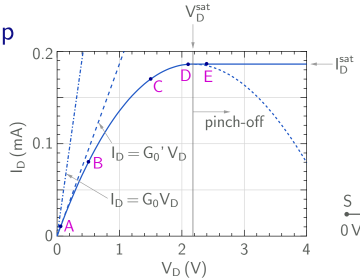
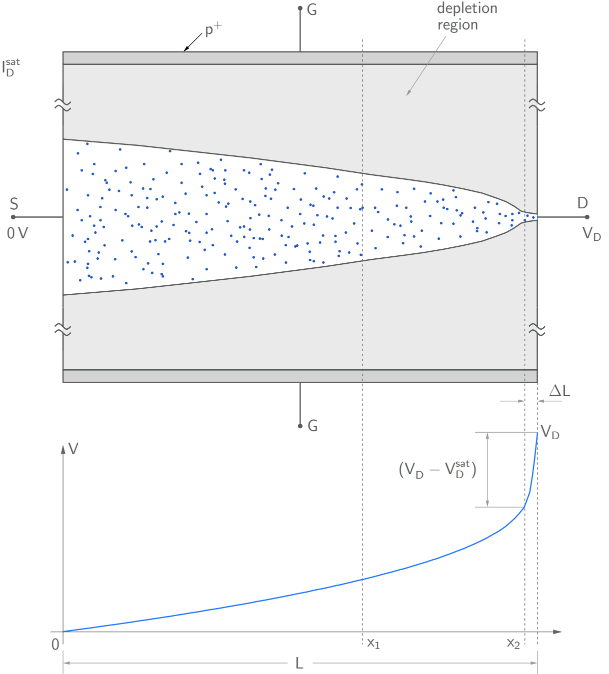
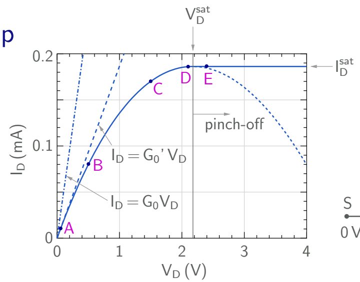
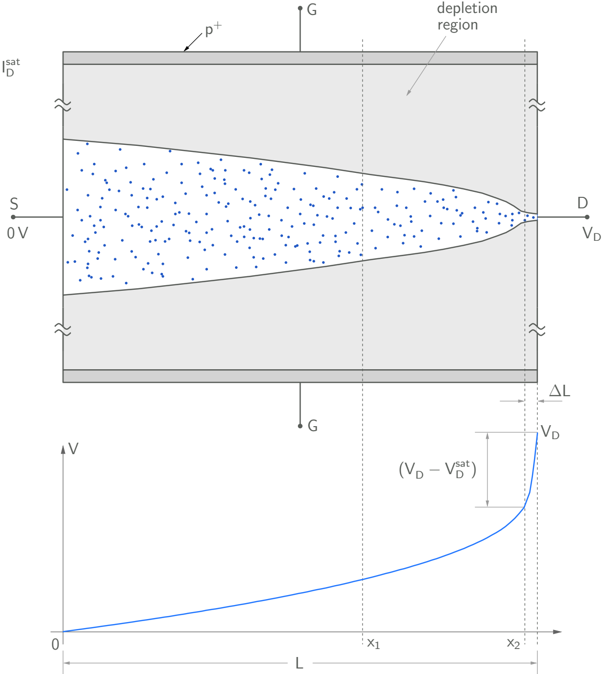




* In the region near the drain end (between $x = x_2$ and $x = L$), the electric field is larger than the rest of the channel. The "excess" voltage, $V_D - V_D^{sat}$, drops across this region.
* Any further increase in V_D causes a larger field in this high-field region, and the voltage drop across that region increases accordingly.
* The rest of the channel, "shielded" by the high-field region, does not experience any change as V_D is increased.

JFET I-V relationship





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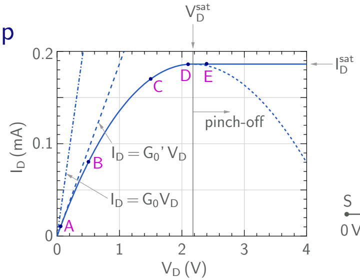
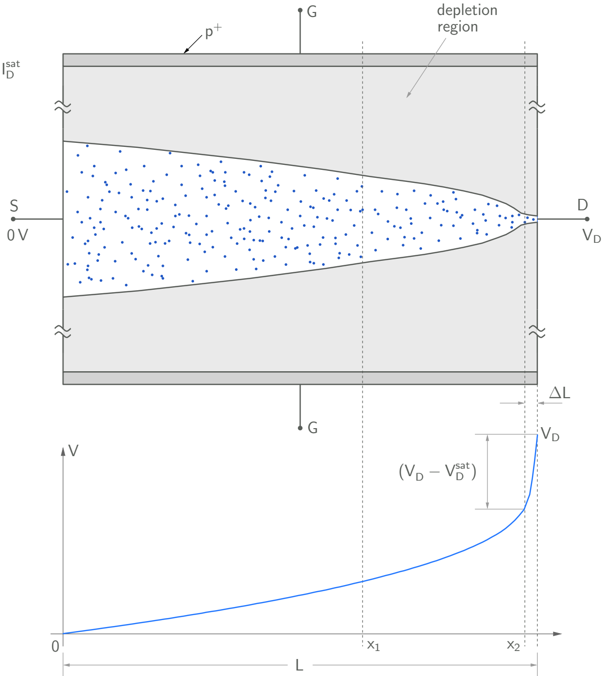
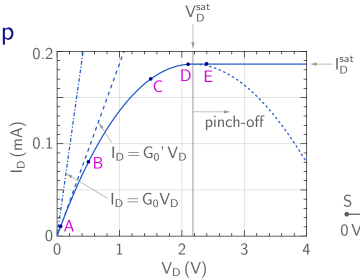
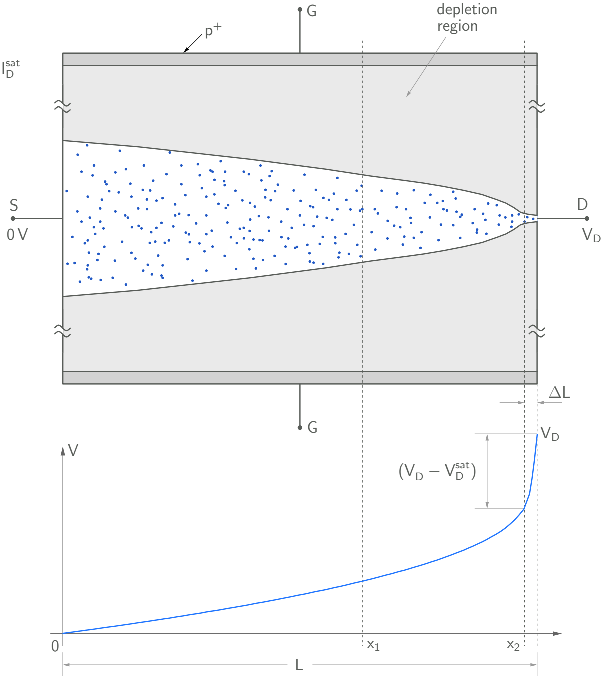




* At $x = x_1$ in the figure, for example, the channel potential as well as its derivative $\dfrac{dV}{dx}$ remain unaffected by the excess V_D, and therefore the current at x_1, which depends on $h(V)$ and $\dfrac{dV}{dx}$ remains constant. Since the current is the same throughout the device, I_D, the drain terminal current, remains constant.

JFET I-V relationship





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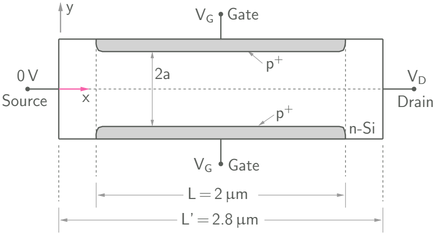
* Note that the high-field region near the drain is not completely devoid of electrons (otherwise, the current would be zero).

Simulation results



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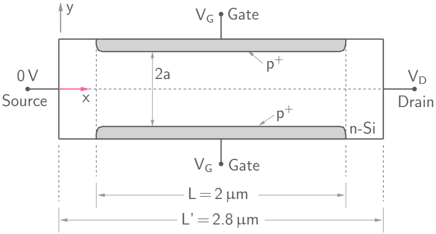

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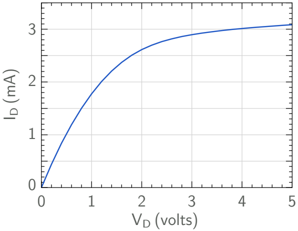

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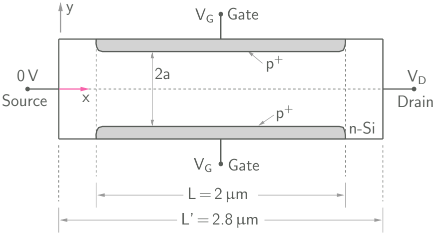

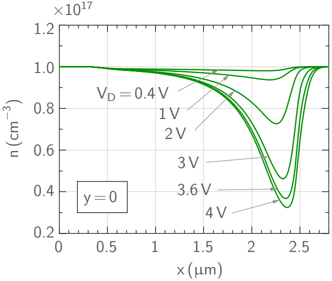

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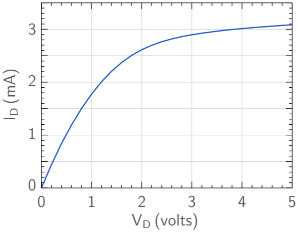

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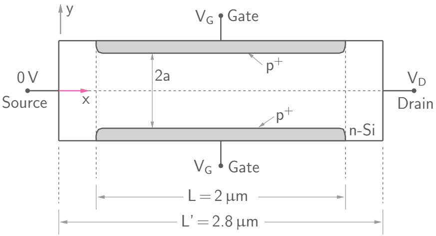

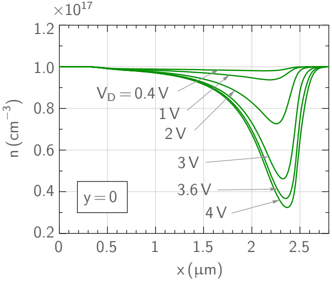

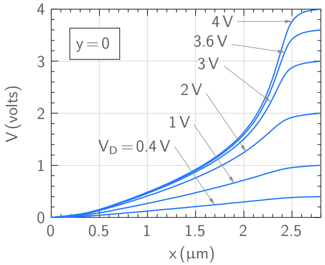

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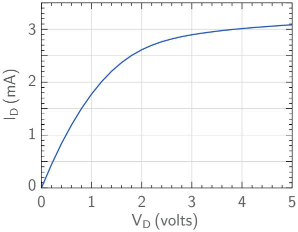

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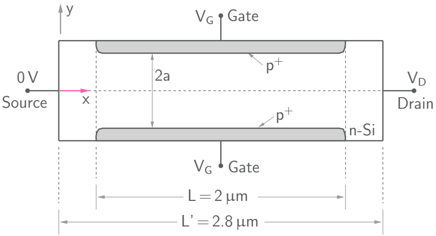

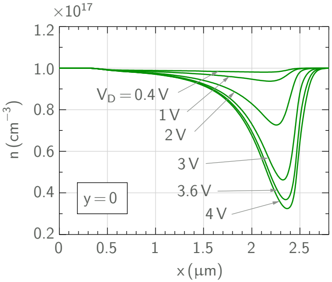

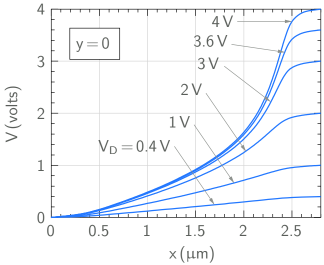

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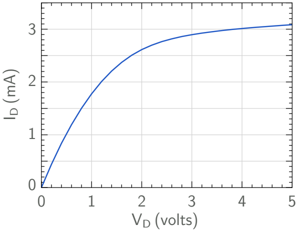

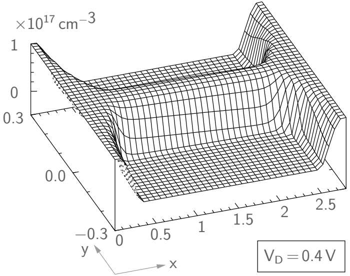

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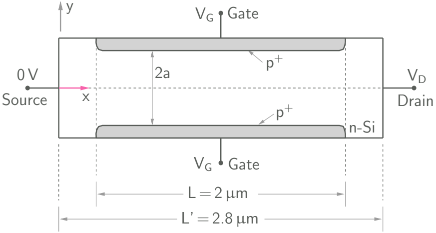

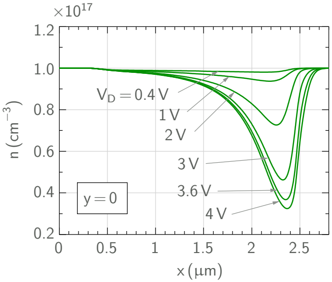

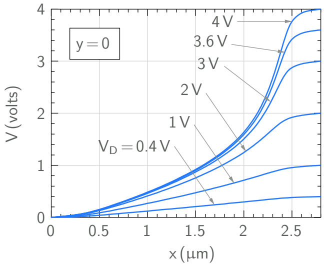

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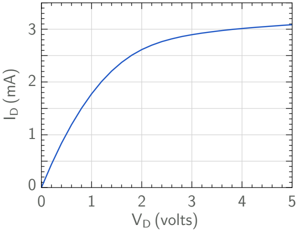

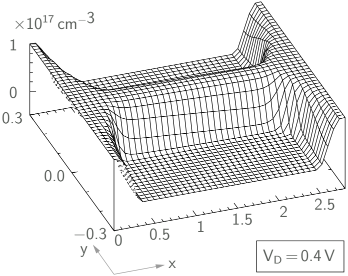

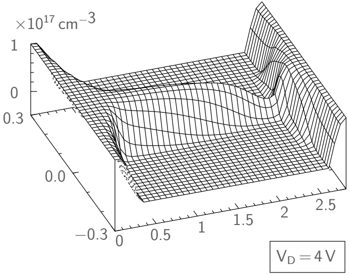

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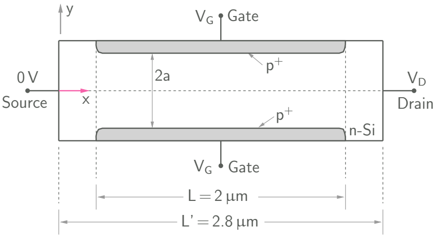
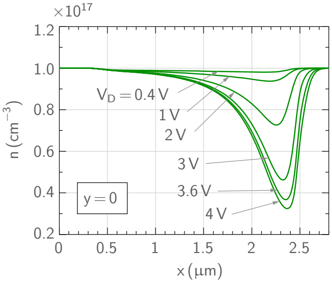
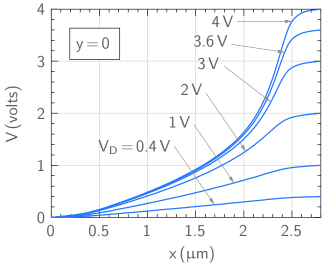
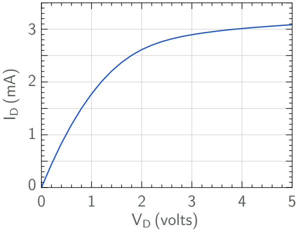
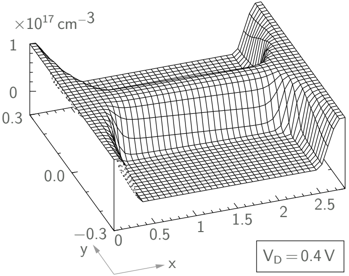


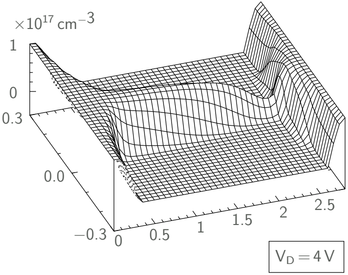




$V_G = -1$ V
$a = 0.2\,\mu m$
$L = 2\,\mu m$
$Z = 50\,\mu m$
$N_d = 10^{17}\ cm^{-3}$

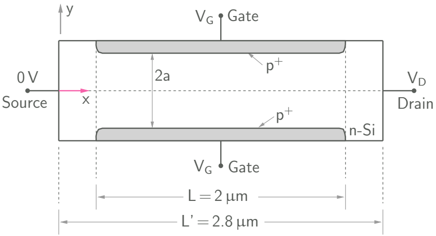


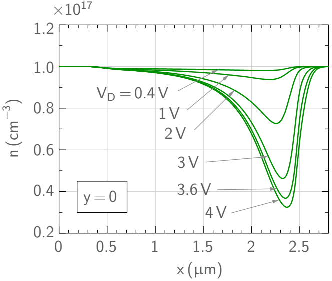


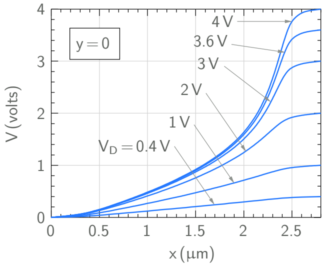


* The channel is uniform from S to D at low V_D and becomes narrower at the drain end at high V_D.

Simulation results







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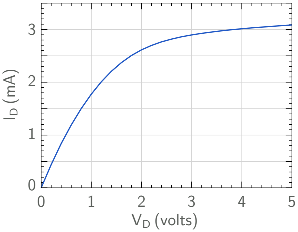
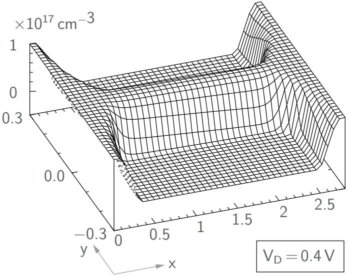
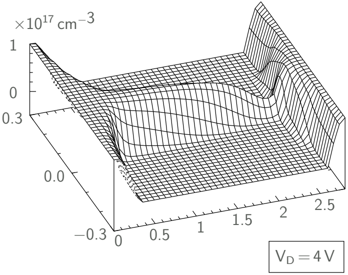
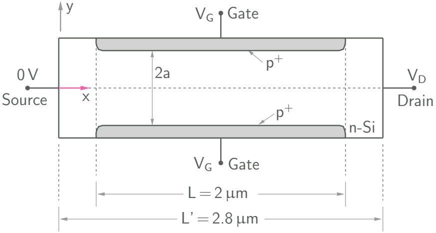


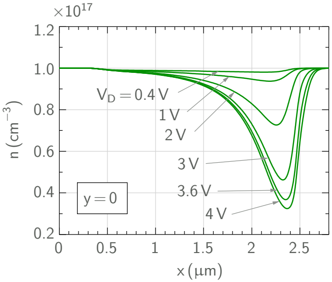


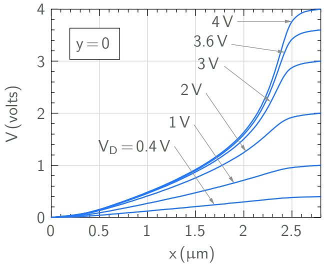


* The channel is uniform from S to D at low V_D and becomes narrower at the drain end at high V_D.
* An increase in V_D is accompanied by a decrease in n and an increase in $\mathcal{E}$.

Simulation results







$V_G = -1\,V$
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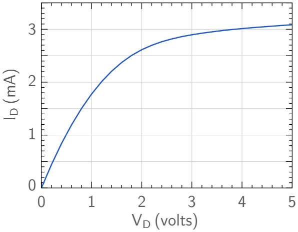
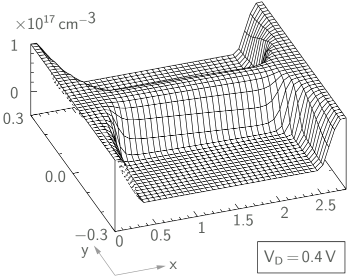
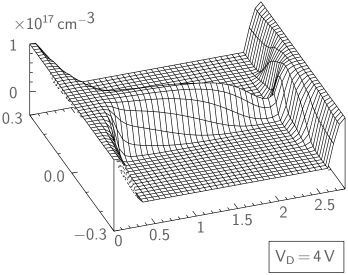
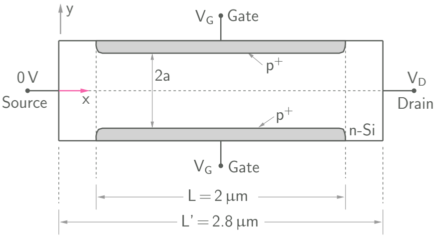
$L = 2\,\mu m$
$Z = 50\,\mu m$
$N_d = 10^{17}\,cm^{-3}$

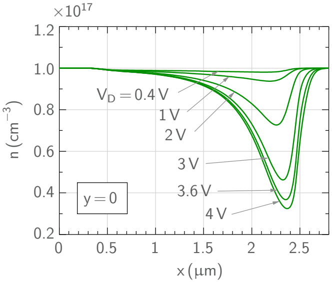


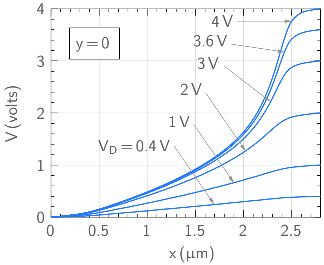




Simulation results







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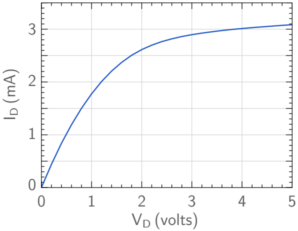
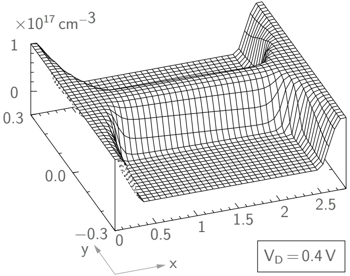
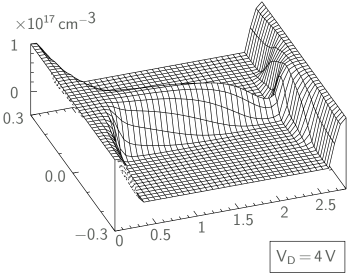
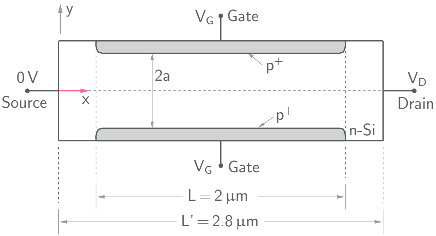


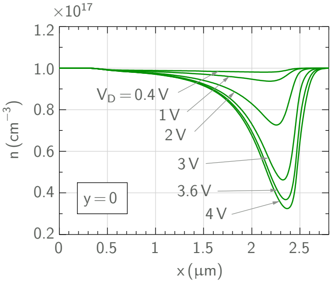


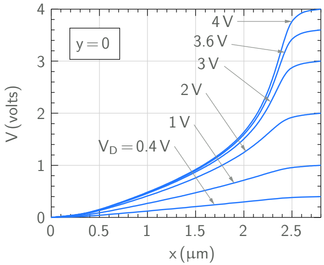


∗ Beyond saturation ($V_D \sim 3.6\,V$), $V(x)$ is almost constant except in the region close to the drain.

Simulation results







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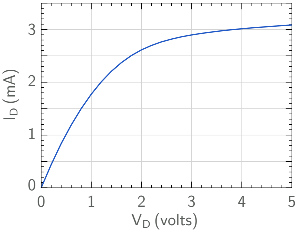

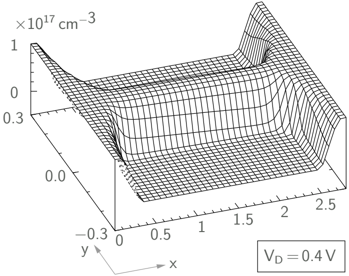

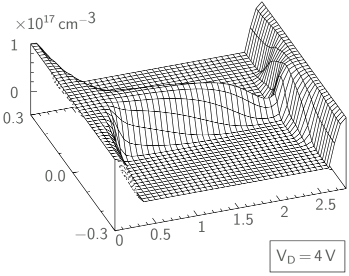

* Beyond saturation ($V_D \sim 3.6$ V), $V(x)$ is almost constant except in the region close to the drain.
* Note that the I_D versus V_D curve has a non-zero slope beyond saturation (to be discussed).

M. B. Patil, IIT Bombay