SEMICONDUCTOR DEVICES

MOS Transistors: Part 1

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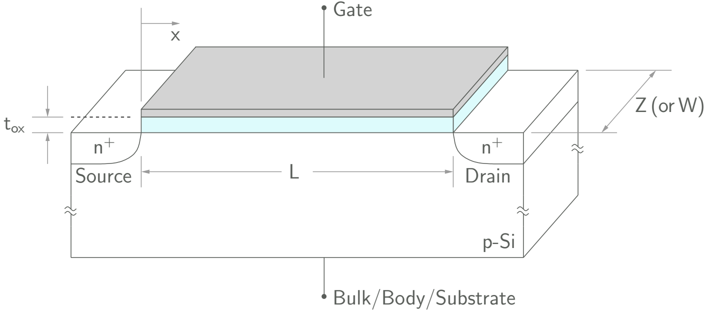
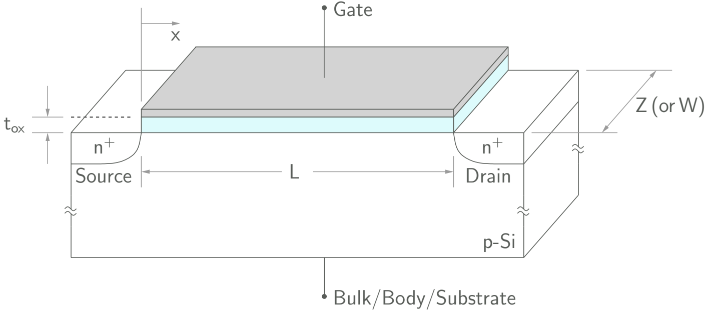
MOS transistors



MOS transistors



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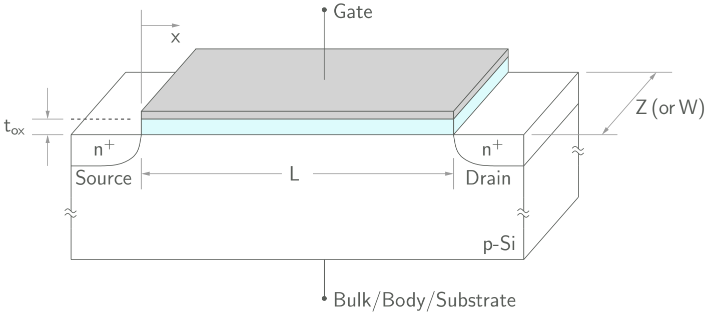
MOS transistors



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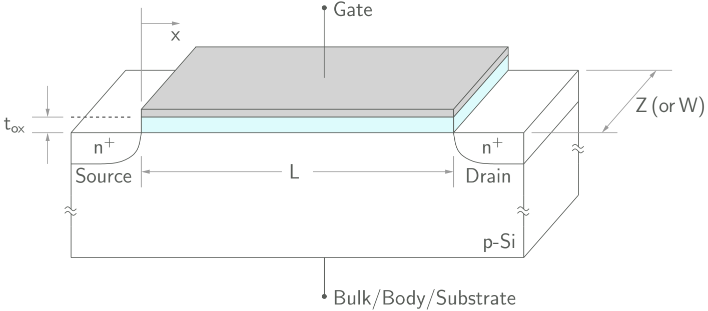

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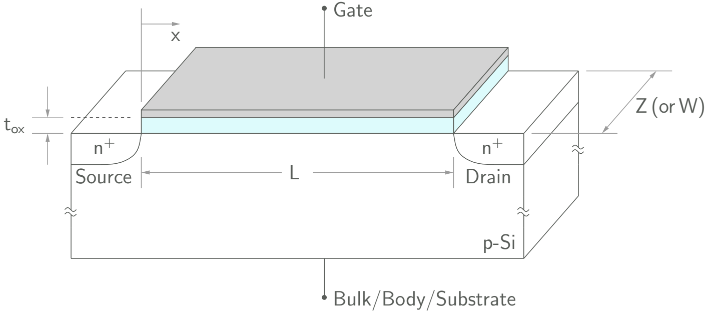

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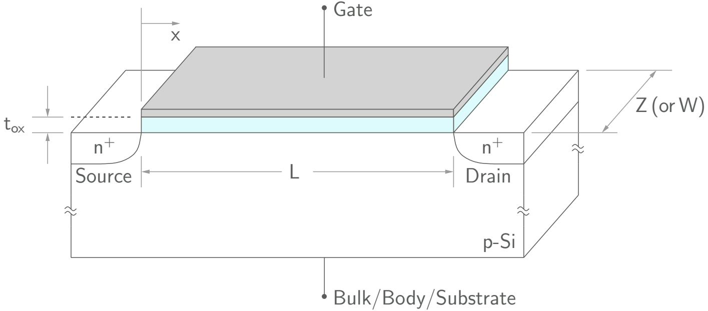

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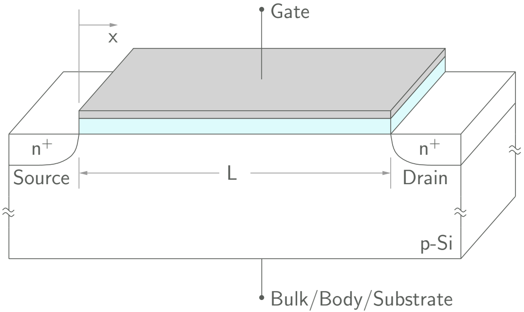
- We will consider the metal-SiO_2-Si transistor.
- Note that the substrate contact is not shown explicitly; it is assmued to be an ohmic contact.

MOS transistors



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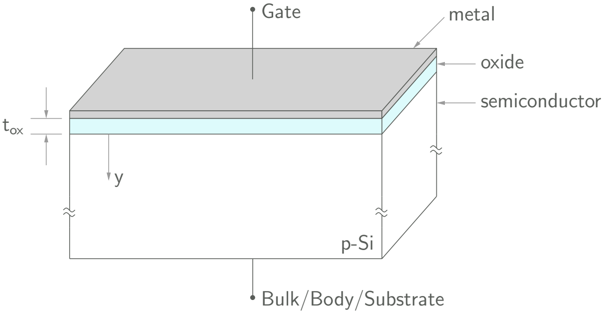
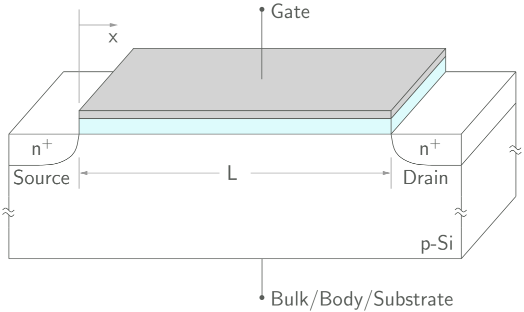


MOS capacitor

MOS transistors



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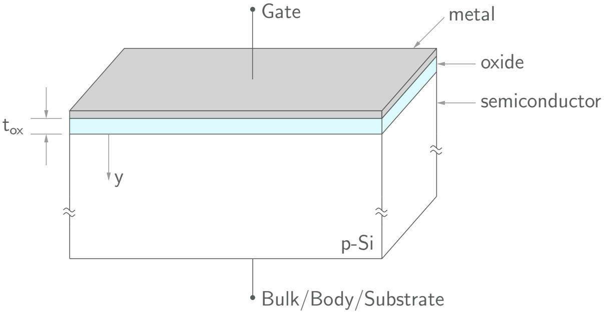

MOS capacitor

- The heart of a MOS transistor is the MOS capacitor which consists of an insulator (SiO_2), with a metal on one side and a semiconductor on the other.

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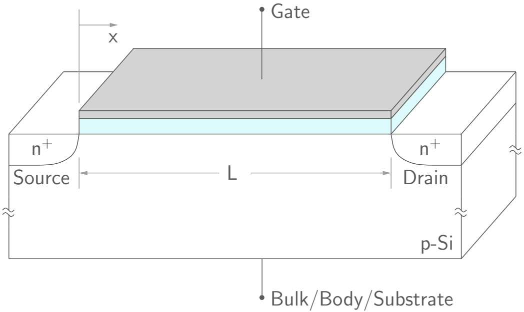

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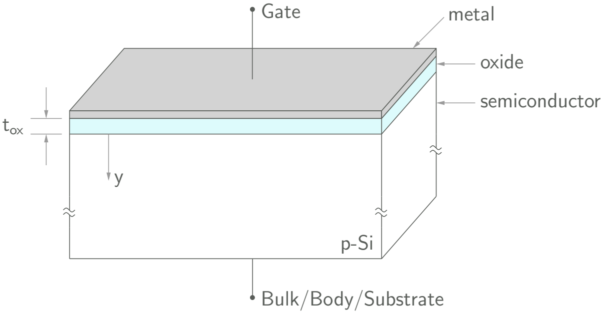

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- The oxide thickness t_{ox}, which is typically of the order of 100 Å (i.e., 0.01 μm), is crucial in determining the behaviour of the MOS capacitor.

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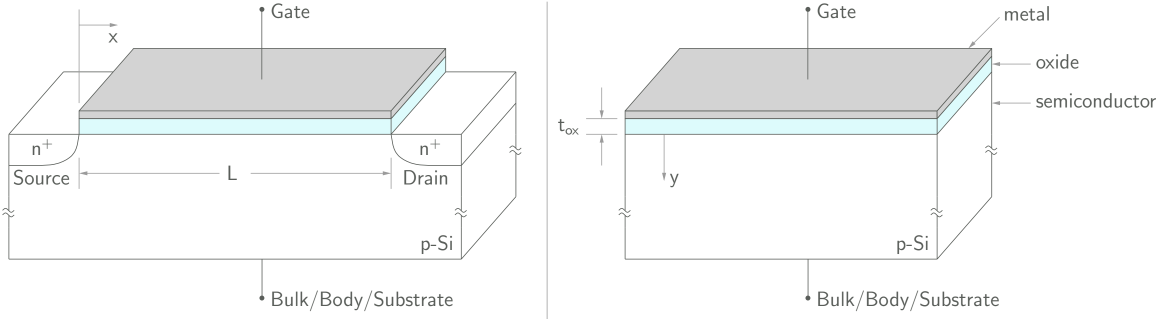

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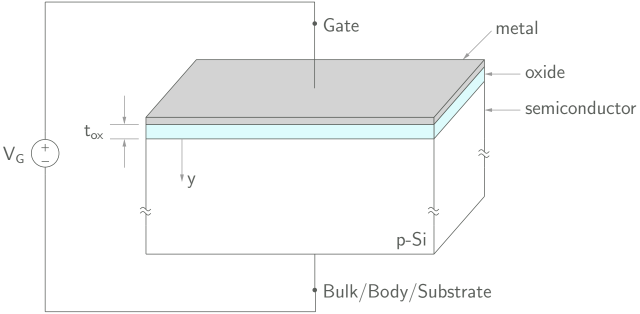
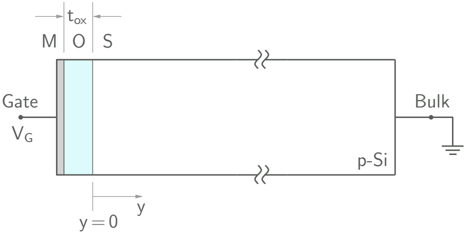
- The oxide thickness t_{ox}, which is typically of the order of 100 Å (i.e., 0.01 μm), is crucial in determining the behaviour of the MOS capacitor.
- The metal thickness — typically a few hundred nm — depends on technological considerations, but its exact value is not important.

MOS capacitor





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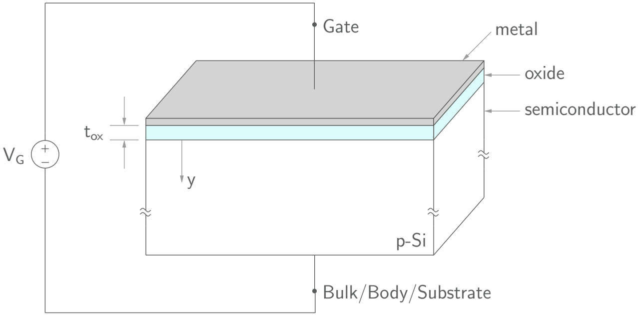
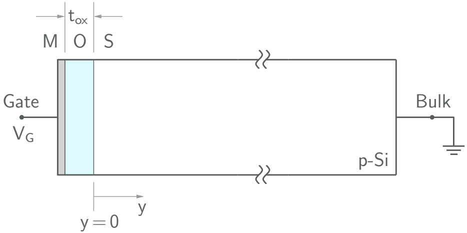
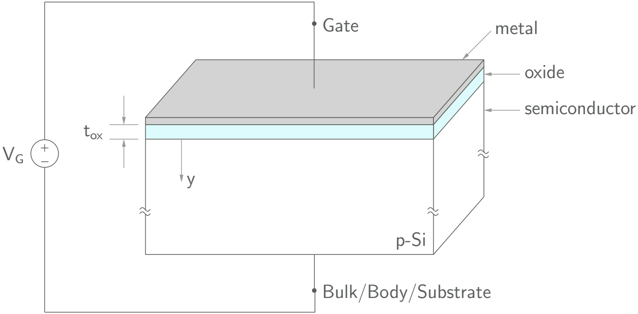
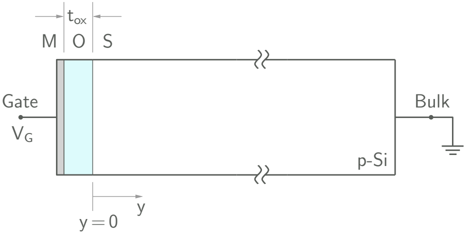




- ∗ A voltage V_G is applied to the “gate” (the metal layer) with respect to the bottom ohmic contact called “bulk” or “body” or “substrate” contact.

MOS capacitor





- ∗ A voltage V_G is applied to the “gate” (the metal layer) with respect to the bottom ohmic contact called “bulk” or “body” or “substrate” contact.
- ∗ We are interested in the charge distribution in the MOS structure for different V_G values.

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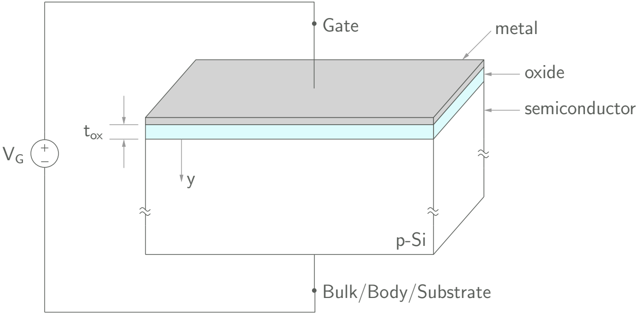

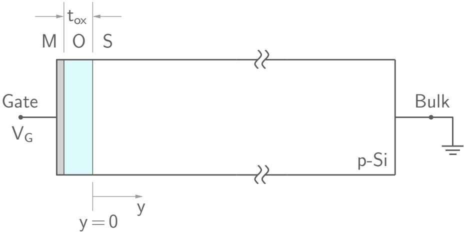

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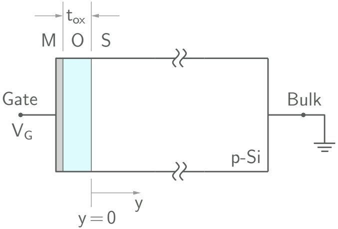
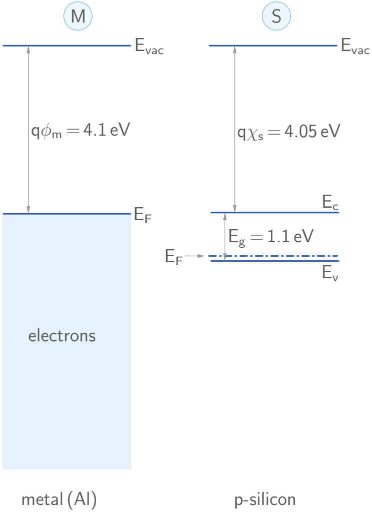
- ∗ We consider the structure to be one-dimensional, i.e., the variations in ψ, n, p are assumed to be only along the y direction.

MOS capacitor





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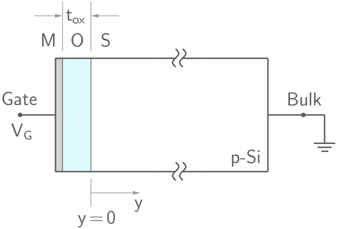
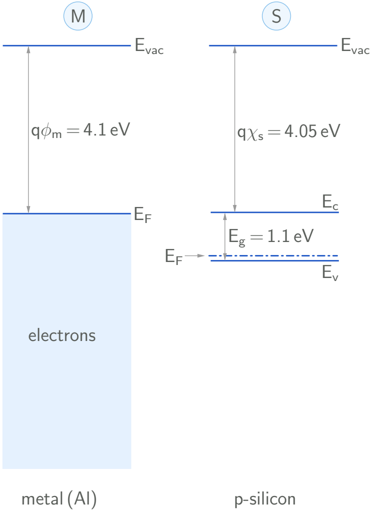
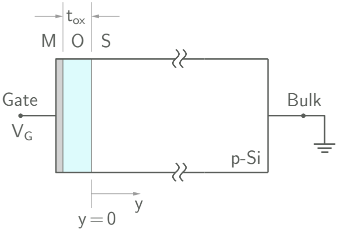
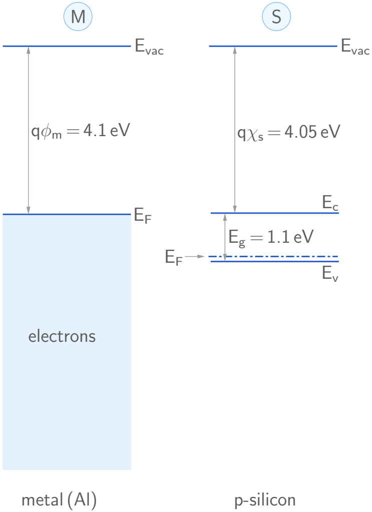




- Metal work function ϕ_m: An electron requires energy $q\phi_m$ to make a transition from the Fermi level to the vacuum level, i.e., to be free of the attractive forces it experiences inside the metal.

MOS capacitor





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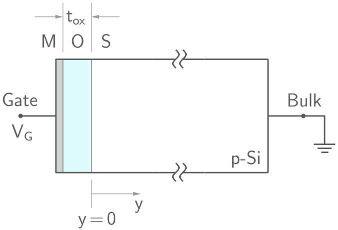
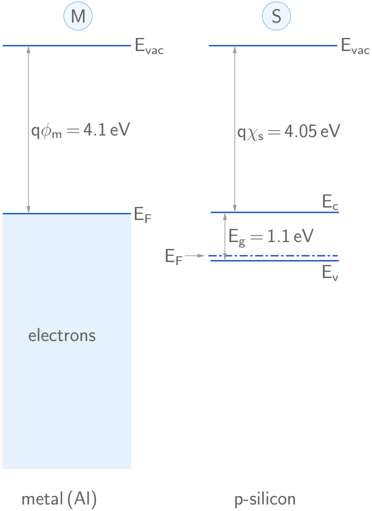
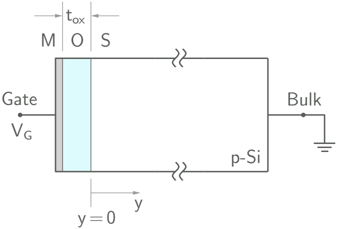
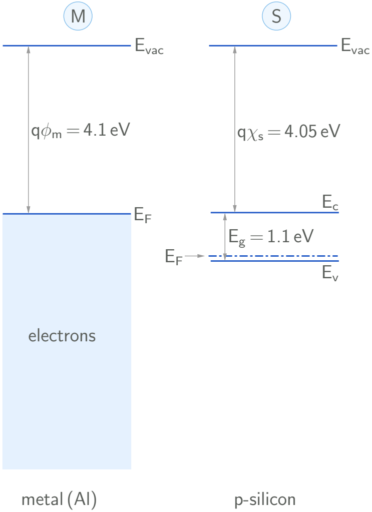




- ∗ Electron affinity χ_s: An electron at the edge of the conduction band in the semiconductor requires energy $q\chi_s$ to make a transition to the vacuum level, i.e., to be free of the attractive forces it experiences inside the semiconductor.

MOS capacitor





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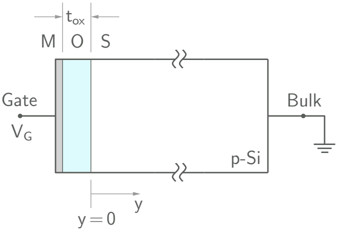

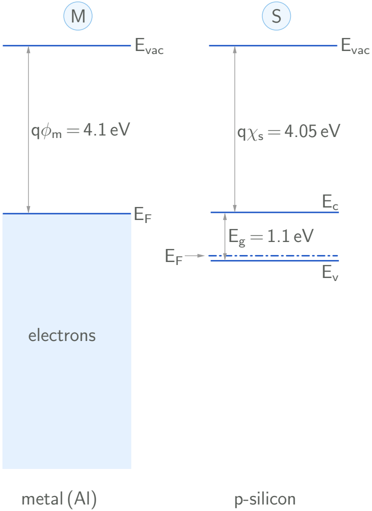

- In a MOS capacitor in equilibrium, the Fermi levels on both sides must be aligned, which requires a "built-in" potential difference between the M and S sides.

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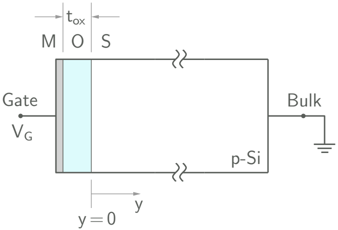

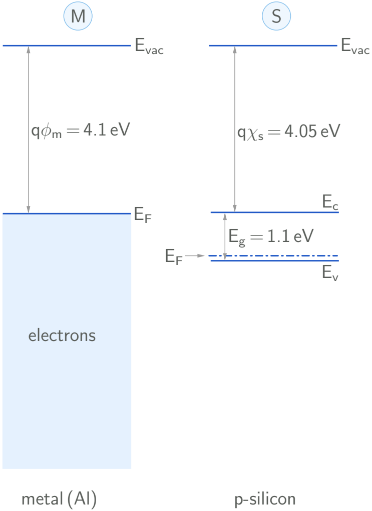

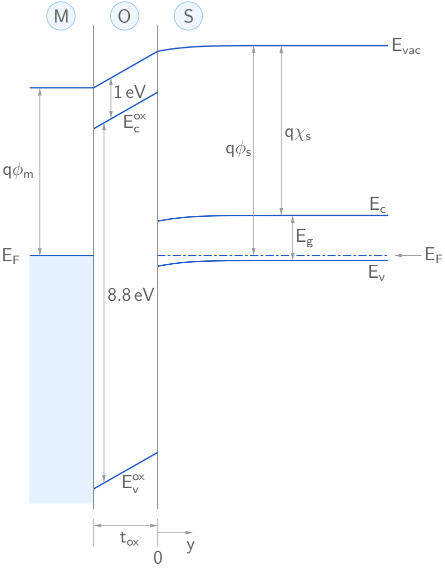

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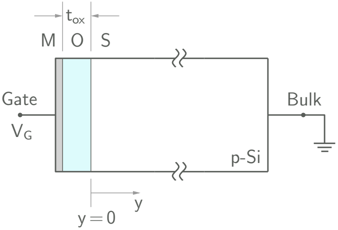

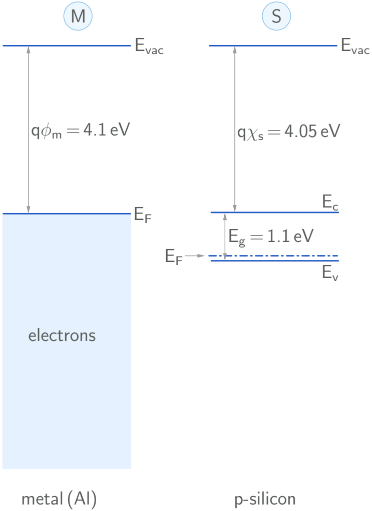

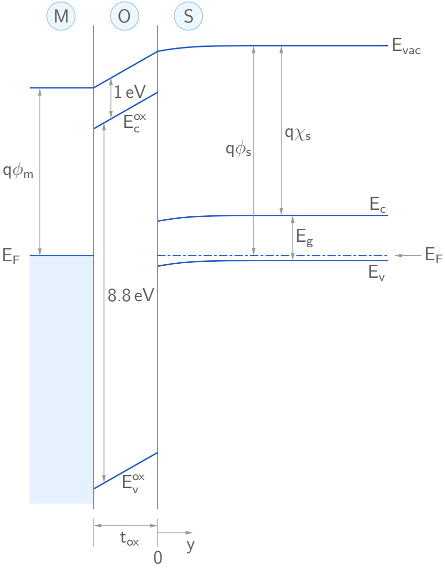

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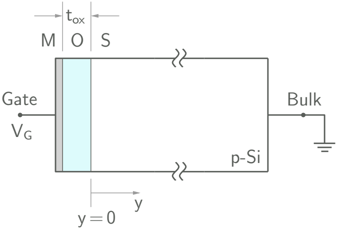

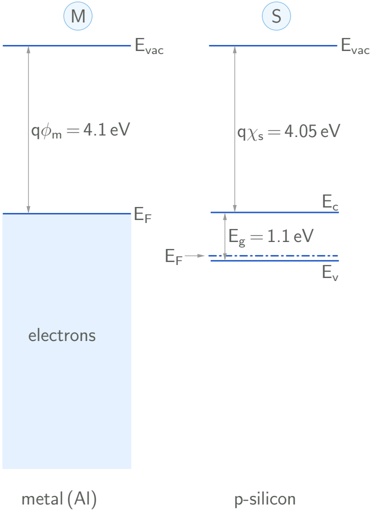

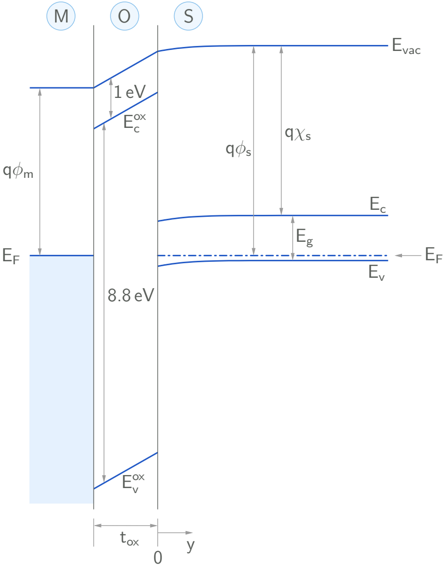

- In addition to the voltage drop on the semiconductor side, there is a voltage drop across the oxide layer. If there is no charge in the oxide layer, $\dfrac{d\mathcal{E}}{dy} = \dfrac{\rho}{\epsilon_{ox}} = 0 \rightarrow \mathcal{E} = \text{constant}$.

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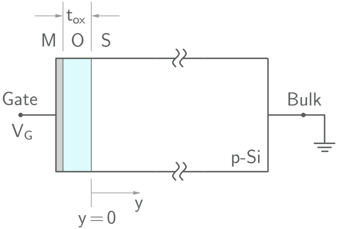

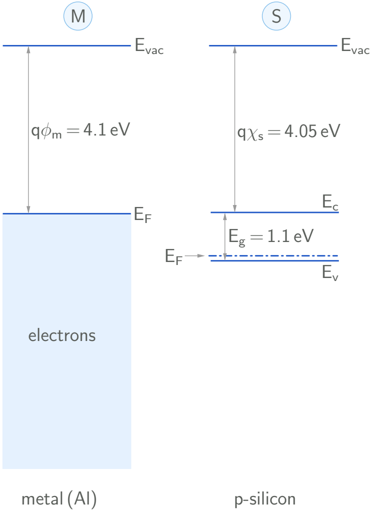

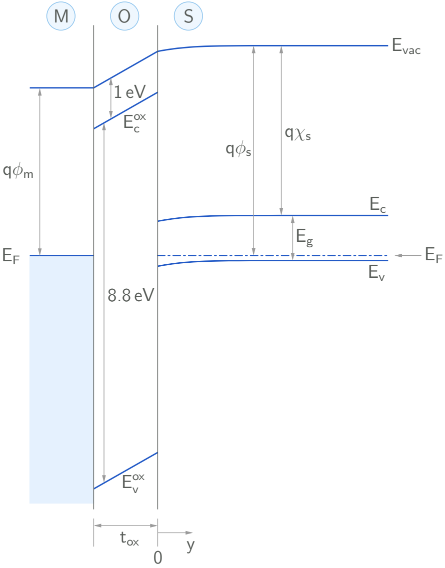

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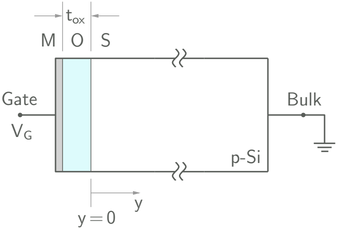

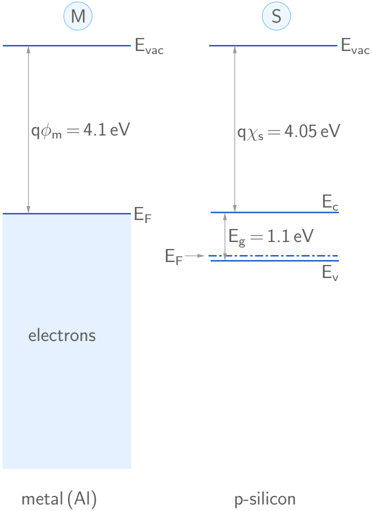

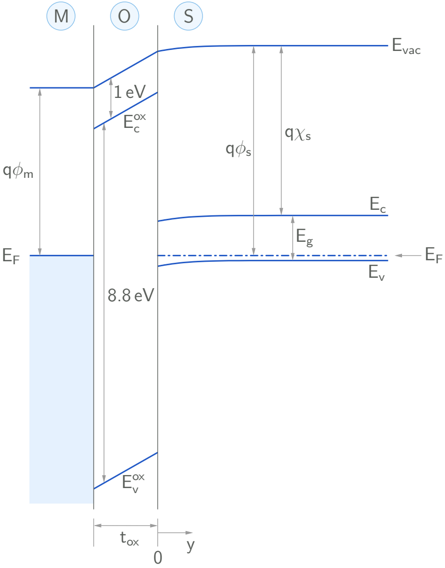

$$* \quad E_{\text{vac}}(-t_{\text{ox}}) - E_{\text{vac}}(\infty) = +q\phi_m - (E_c(\infty) - E_F) - q\chi_s$$

$$= q\phi_m - [E_g - (E_F - E_v(\infty))] - q\chi_s .$$

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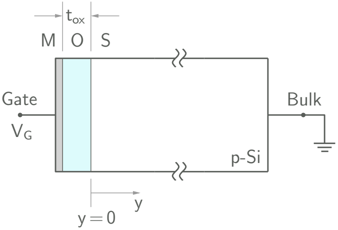

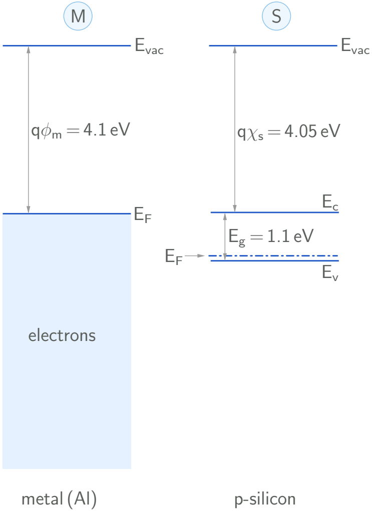

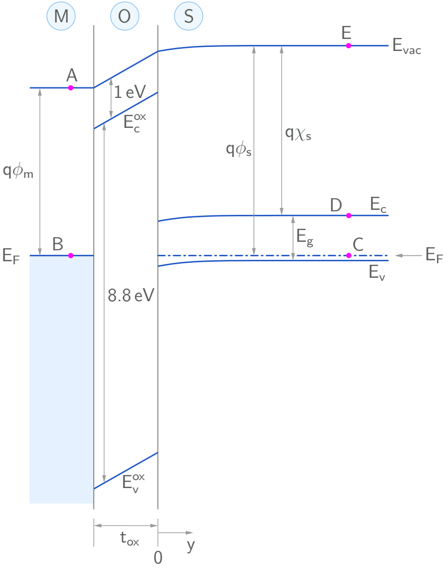

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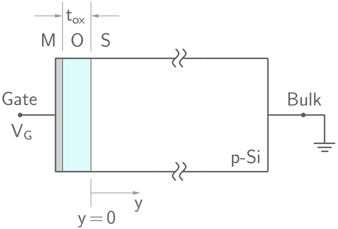

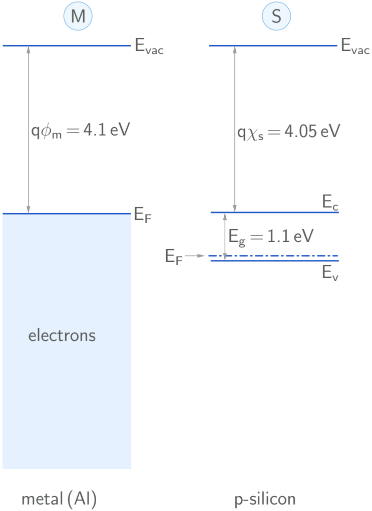

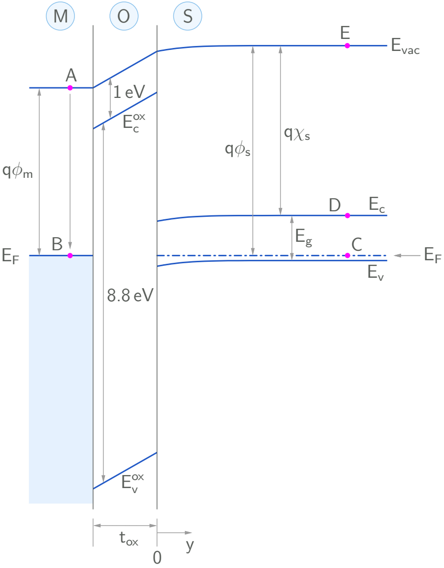

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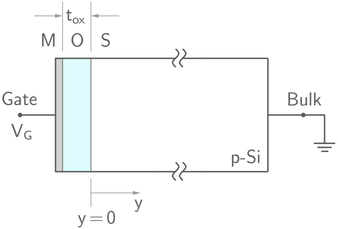

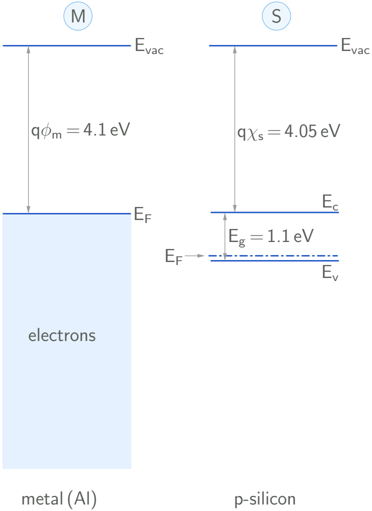

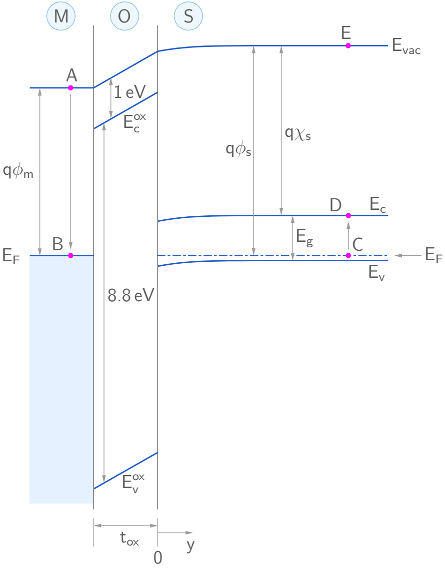

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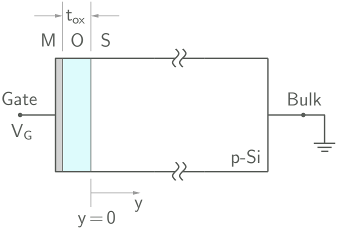
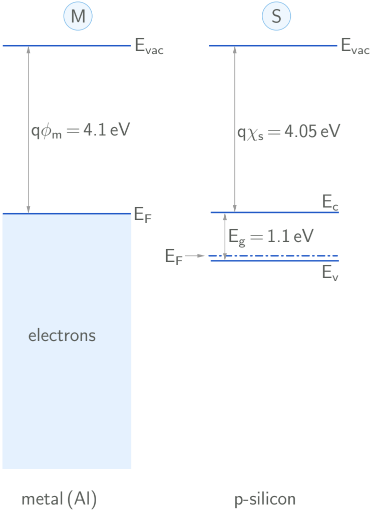
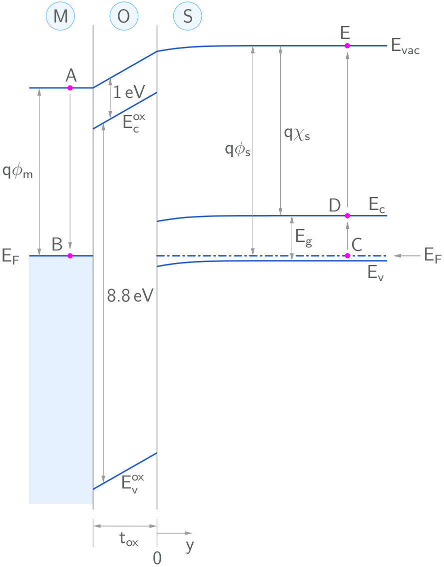


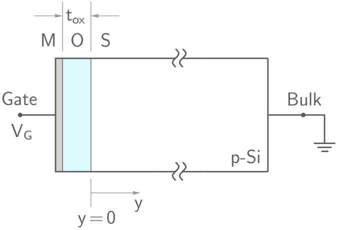


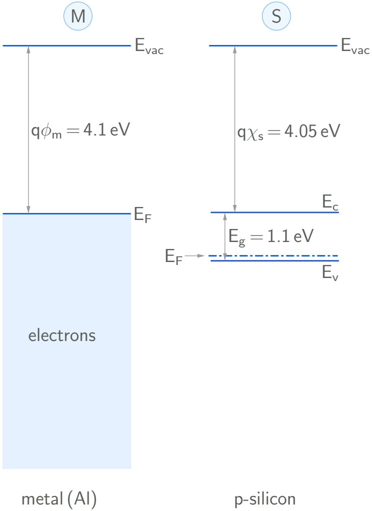


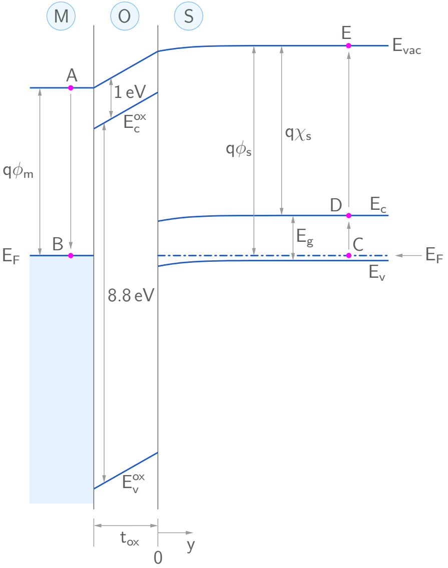
$$* \quad E_{vac}(-t_{ox}) - E_{vac}(\infty) = +q\phi_m - (E_c(\infty) - E_F) - q\chi_s$$

$$= q\phi_m - [E_g - (E_F - E_v(\infty))] - q\chi_s .$$

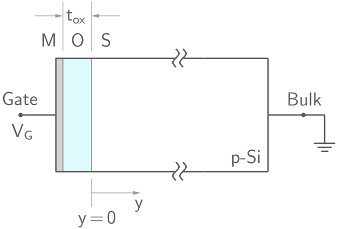
MOS capacitor

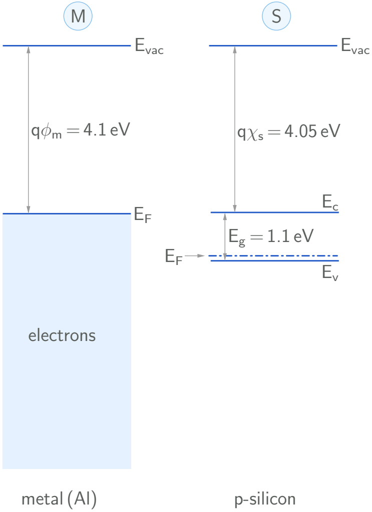


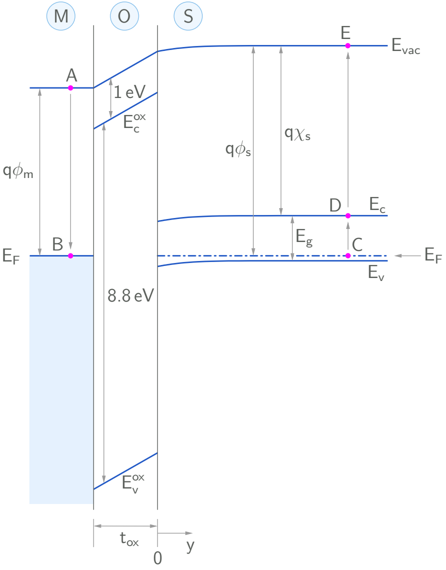




MOS capacitor



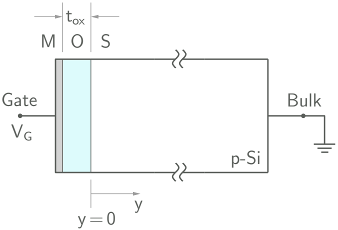


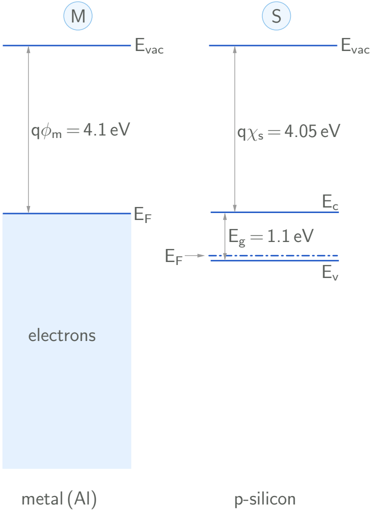


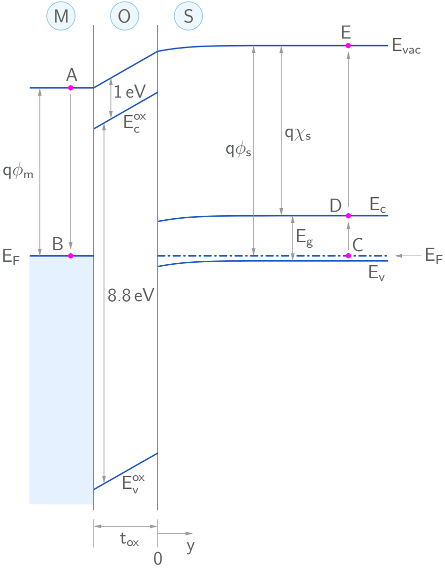
* $E_{\rm vac}(-t_{\rm ox}) - E_{\rm vac}(\infty) = q\phi_m - [E_g - (E_F - E_v(\infty))] - q\chi_s = q\phi_m - q\chi_s - E_g - k_B T \log\left(\dfrac{p_0}{N_v}\right)$.

$(E_{\rm vac} - E_F)/q$ (in equilibrium) is called the semiconductor work function ϕ_s.

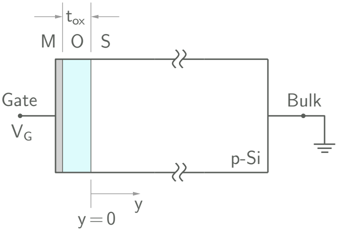
MOS capacitor

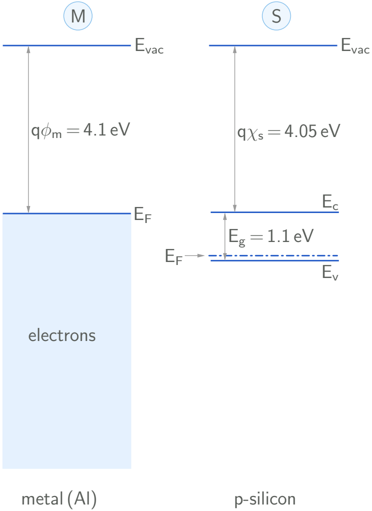


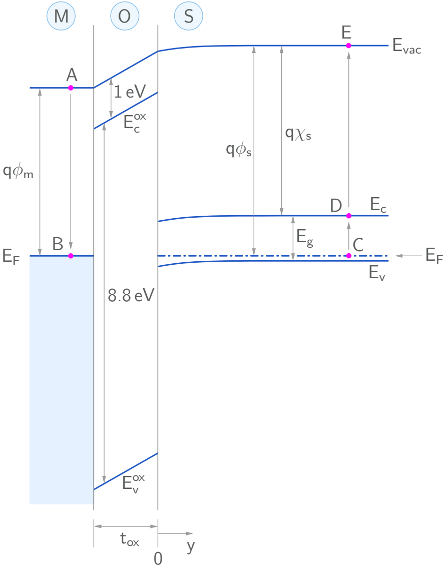




MOS capacitor







- The built-in potential difference can also be expressed as $E_{vac}(-t_{ox}) - E_{vac}(\infty) = q(\phi_m - \phi_s) \equiv q\phi_{ms}$. (Note that ϕ_s depends on the doping density.)

Example

Find the difference $E_{\text{vac}}(-t_{\text{ox}}) - E_{\text{vac}}(\infty)$ for a MOS capacitor in which the gate metal is aluminium ($\phi_m = 4.1\,\text{V}$), and the semiconductor is

(a) p-type silicon with $N_a = 1 \times 10^{17}\,\text{cm}^{-3}$,

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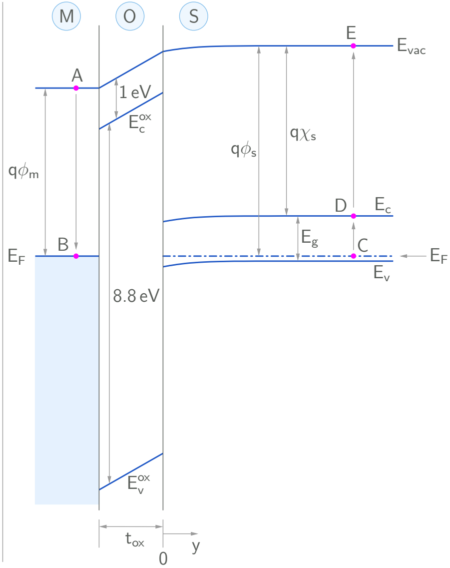
($T = 300\,\text{K}$)



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Solution:

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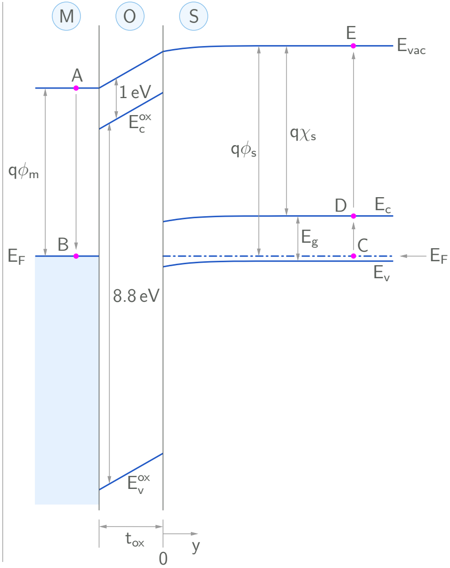

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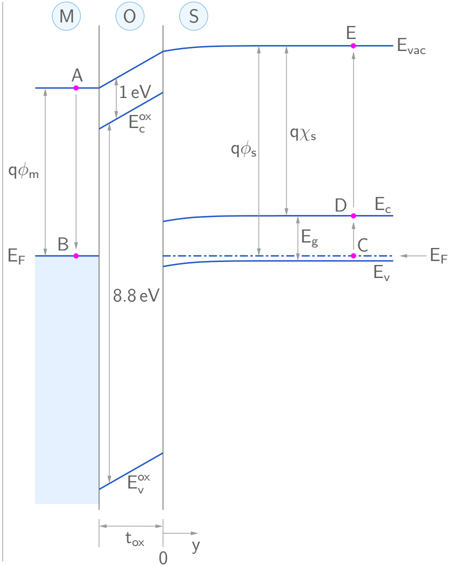
Solution:

$$\text{(a)}\quad q\phi_s = q\chi_s + \left[E_g + k_B T \log\left(\frac{p_0}{N_v}\right)\right]$$

$$= 4.05 + \left[1.12 + 0.0258 \times \log\left(\frac{10^{17}}{1.04 \times 10^{19}}\right)\right] = 5.05\,\text{eV}.$$



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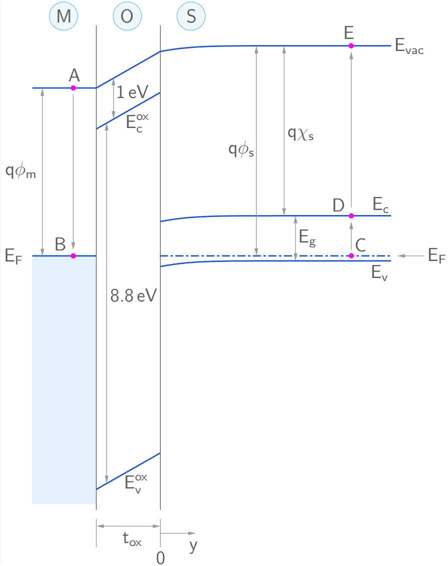
$$\rightarrow E_{\text{vac}}(-t_{\text{ox}}) - E_{\text{vac}}(\infty) = q(\phi_m - \phi_s) = -0.95\,\text{eV}.$$



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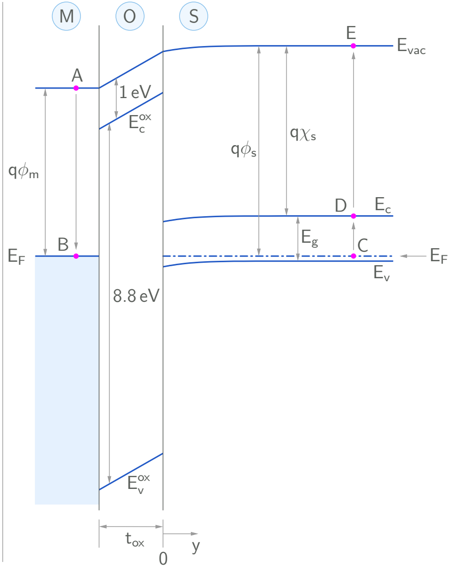
$$\text{(b)}\quad q\phi_s = q\chi_s + (E_c - E_F) = 4.05 - k_B T \log\left(\frac{n_0}{N_c}\right)$$



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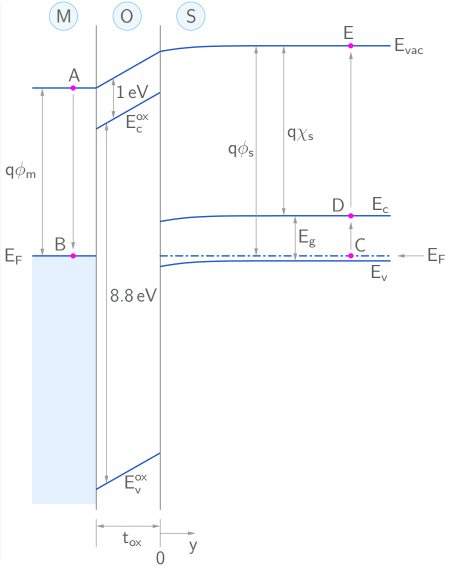
$$= 4.05 - 0.0258 \times \log\left(\frac{5 \times 10^{15}}{2.8 \times 10^{19}}\right) = 4.27\,\text{eV}.$$



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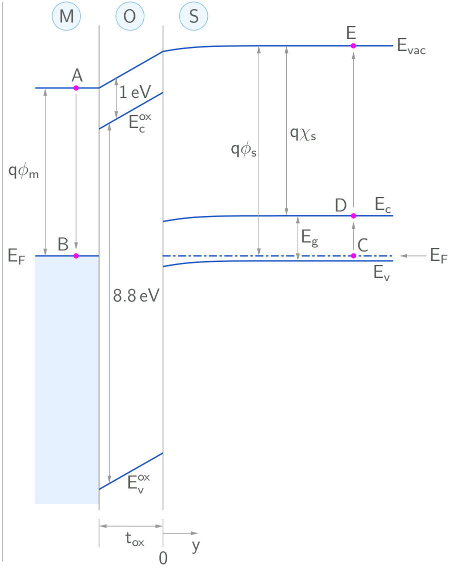
$$\rightarrow E_{\text{vac}}(-t_{\text{ox}}) - E_{\text{vac}}(\infty) = q(\phi_m - \phi_s) = -0.17\,\text{eV}.$$



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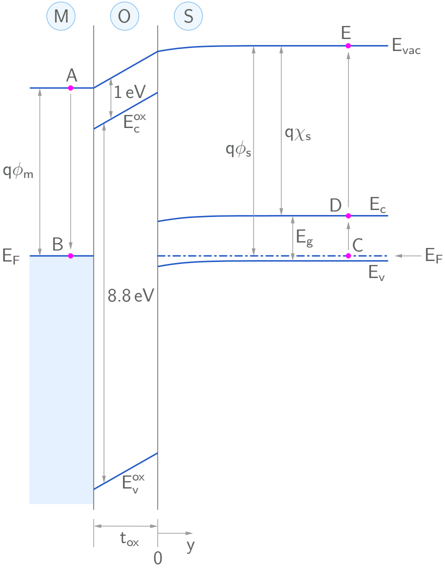
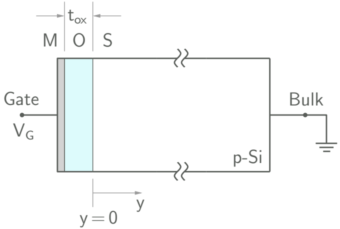
$$\rightarrow E_{\text{vac}}(-t_{\text{ox}}) - E_{\text{vac}}(\infty) = q(\phi_m - \phi_s) = -0.17\,\text{eV}.$$

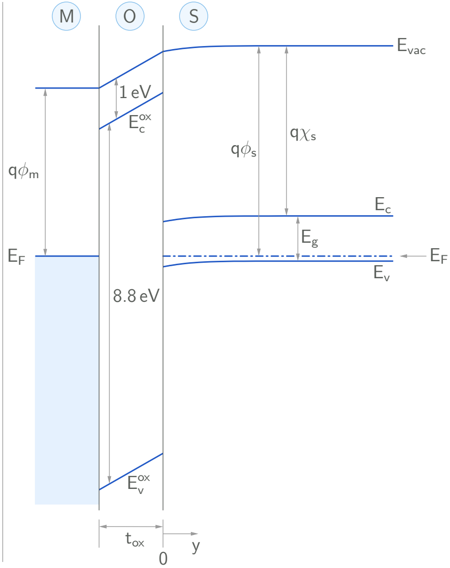
Home work: Draw the band diagram (to scale) for this case.



MOS capacitor: flat-band voltage



Given that there is a built-in band bending in a MOS capacitor, can we do something to make the bands flat?



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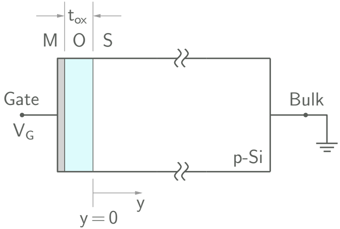
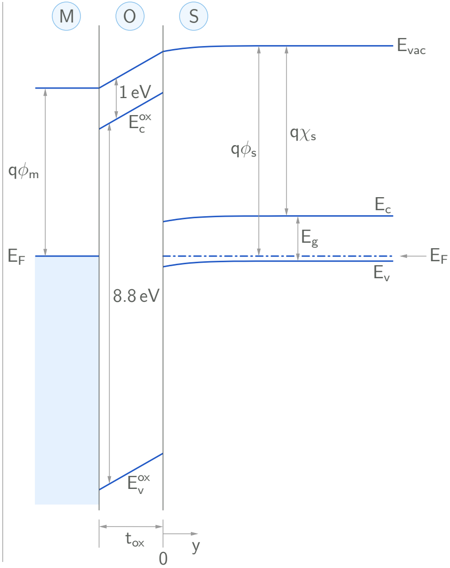


Given that there is a built-in band bending in a MOS capacitor, can we do something to make the bands flat?
→ Yes, we can apply a gate voltage.



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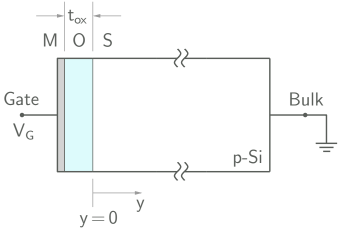

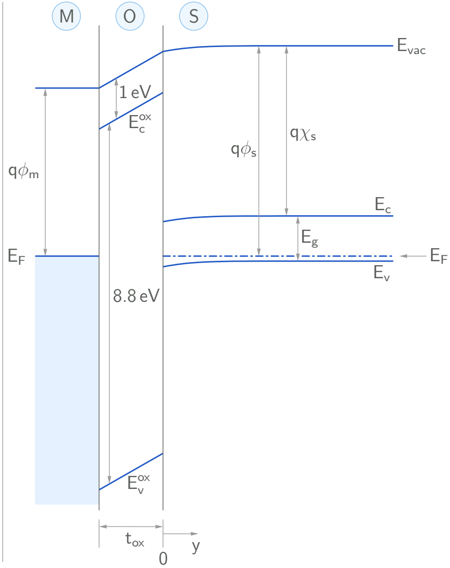

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→ Yes, we can apply a gate voltage.

- ∗ The flat-band voltage V_{FB} is equal to the gate voltage V_G (with respect to the body contact) which is required to make the band edges (E_c and E_v) flat.

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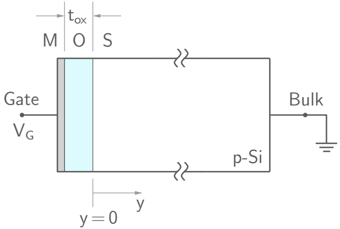

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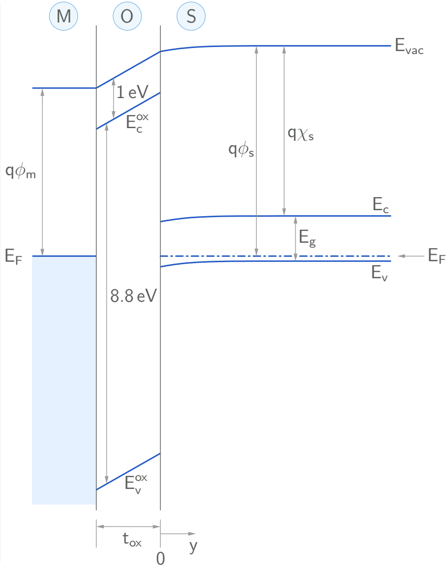
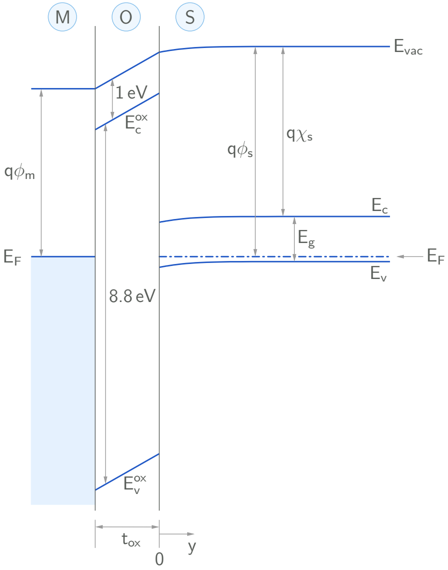
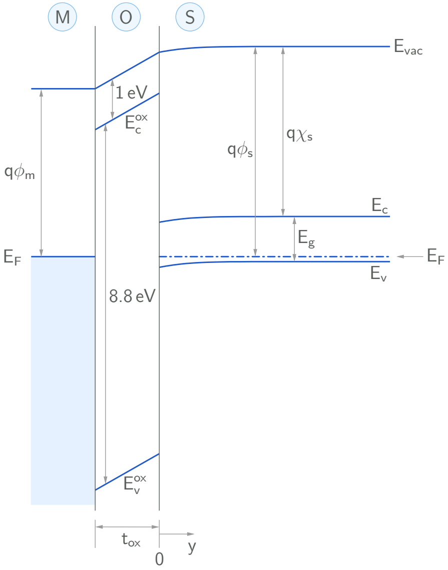
→ Yes, we can apply a gate voltage.

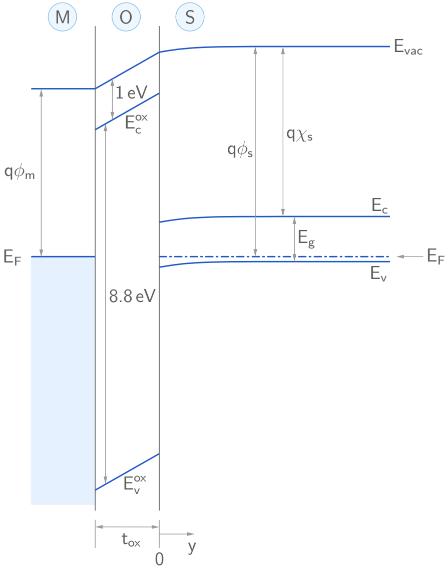
- ∗ The flat-band voltage V_{FB} is equal to the gate voltage V_G (with respect to the body contact) which is required to make the band edges (E_c and E_v) flat.
- ∗ The flat-band voltage serves as an important reference voltage in the study of MOS capacitors and transistors.

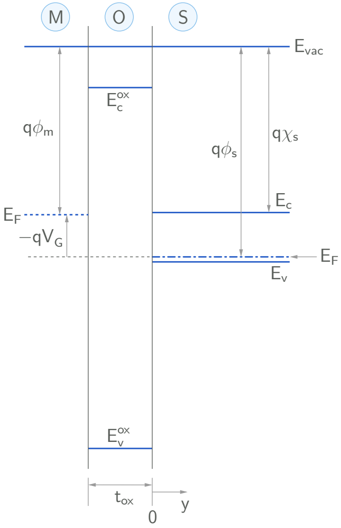



M
O
S
E_{vac}
1 eV
E_c^{ox}
$q\chi_s$
$q\phi_s$
$q\phi_m$
E_c
E_g
E_F
E_F
E_v
8.8 eV
E_v^{ox}
t_{ox}
0
y



- The flat-band condition can be achieved by making the vacuum level on the two sides coincide, which implies zero potential difference ($E_{\text{vac}} \sim -q\psi$).





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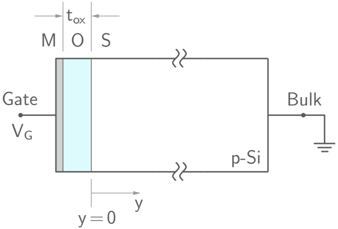

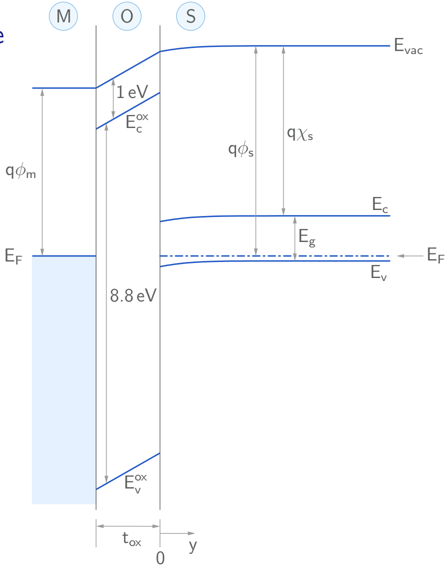

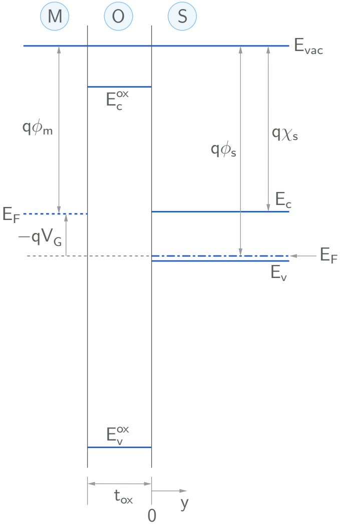

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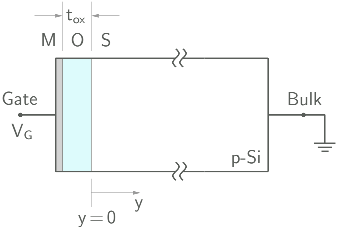
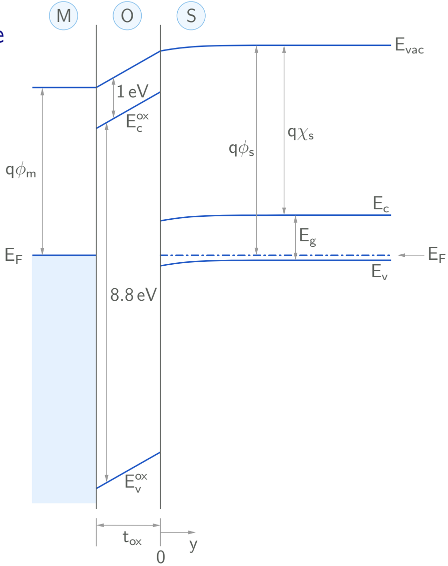
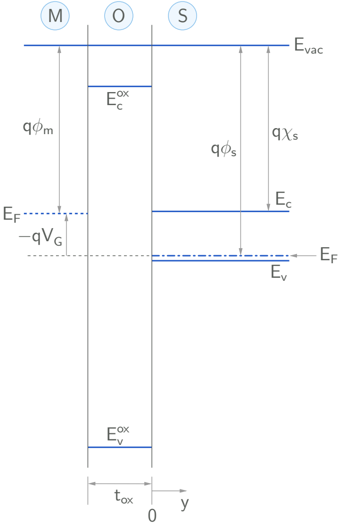
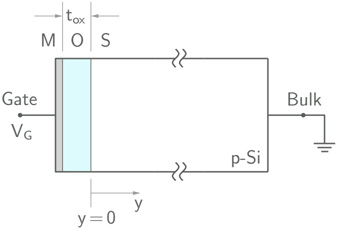


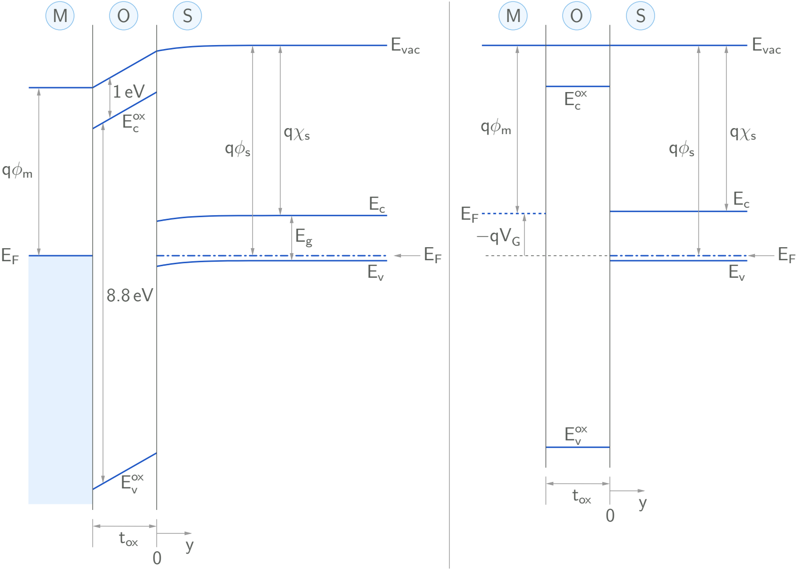




- Applying a *negative* V_G pushes E_F *up* on the metal side (since electron energy $\sim -q\psi$).

MOS capacitor: flat-band voltage

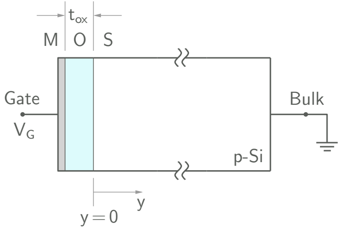


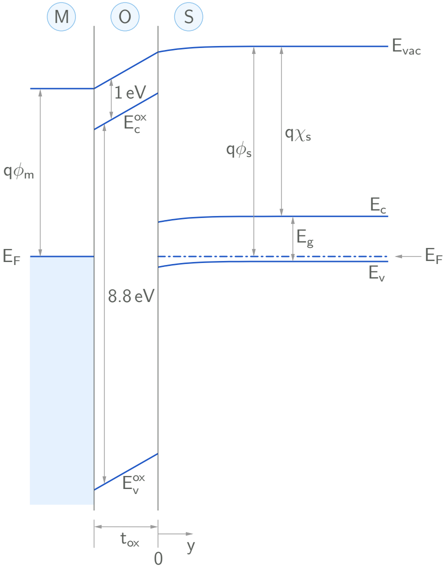


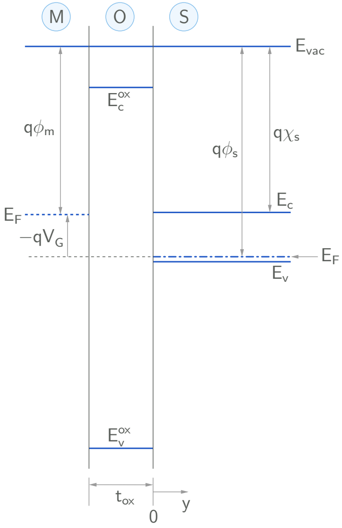
- ∗ Applying a *negative* V_G pushes E_F *up* on the metal side (since electron energy $\sim -q\psi$).
- ∗ $E_F(M) - E_F(S) = -qV_G$.

M. B. Patil, IIT Bombay

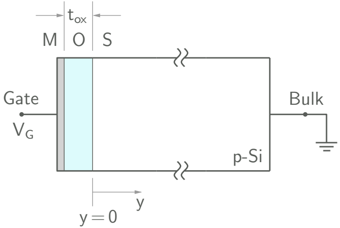
MOS capacitor: flat-band voltage

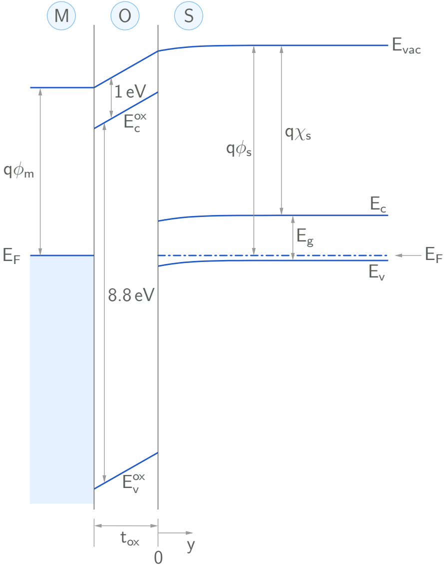


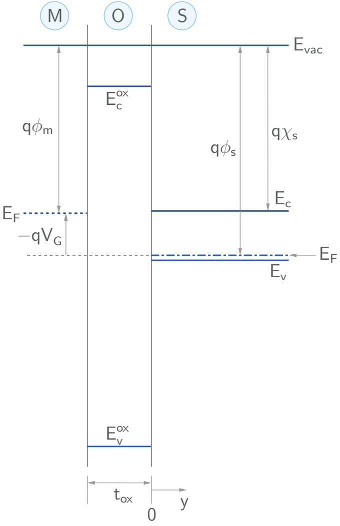




MOS capacitor: flat-band voltage

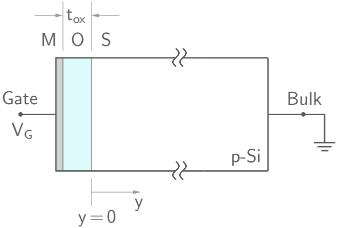




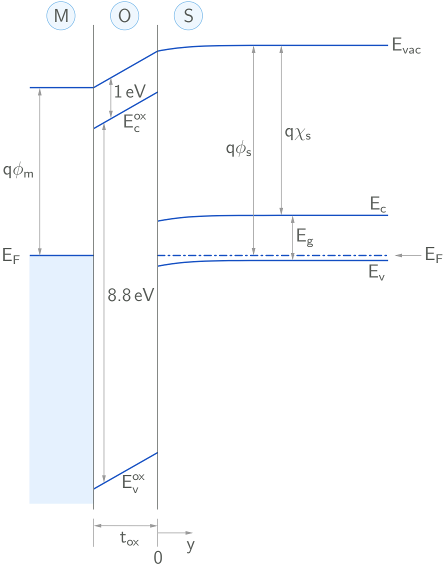


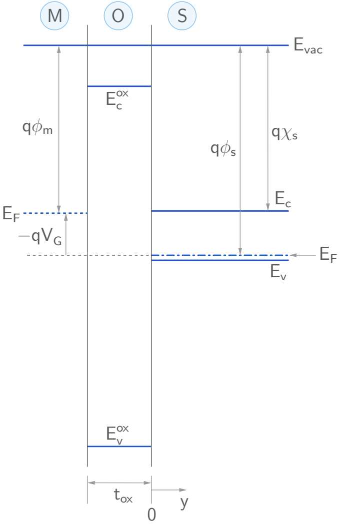
* The Fermi level in a metal is treated as a constant since the large number of electrons (which occupy states up to the Fermi level) available for conduction quickly nullify any cause of departure from equilibrium.

MOS capacitor: flat-band voltage

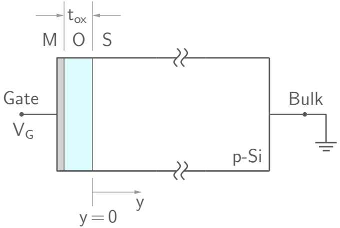


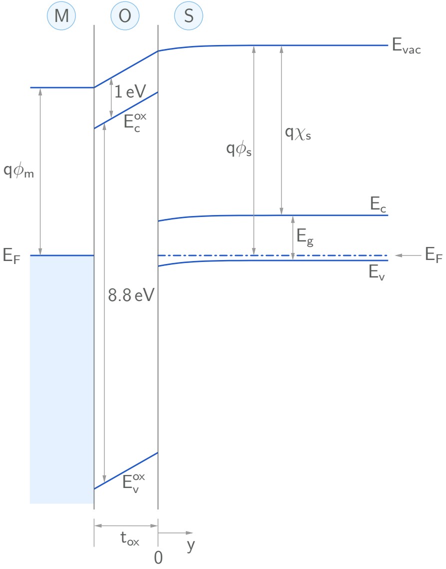
- ∗ The Fermi level in a metal is treated as a constant since the large number of electrons (which occupy states up to the Fermi level) available for conduction quickly nullify any cause of departure from equilibrium.
- ∗ The body (i.e., the material excluding the surface) of a metal is charge neutral, and a non-zero charge density can only exist at a metal surface such as the metal-oxide interface.

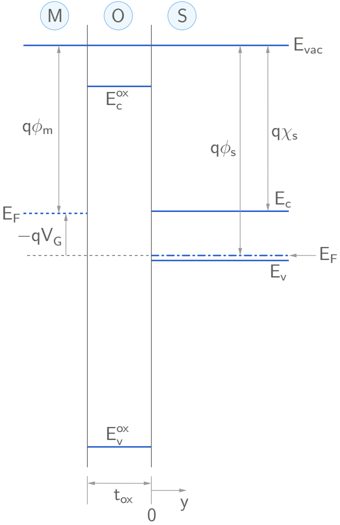




MOS capacitor: flat-band voltage

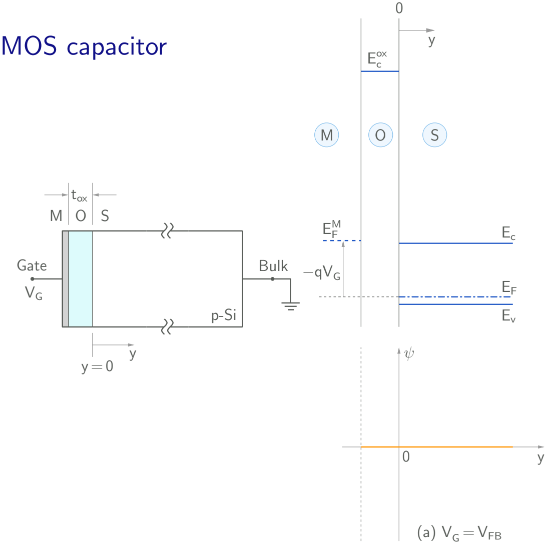






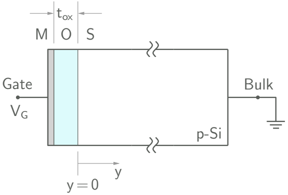
- * The Fermi level in a metal is treated as a constant since the large number of electrons (which occupy states up to the Fermi level) available for conduction quickly nullify any cause of departure from equilibrium.
- * The body (i.e., the material excluding the surface) of a metal is charge neutral, and a non-zero charge density can only exist at a metal surface such as the metal-oxide interface.
- * This is not an equilibrium situation. However, since the oxide layer blocks current flow, the semiconductor is in a quasi-equilibrium condition, and we can therefore draw a constant Fermi level.

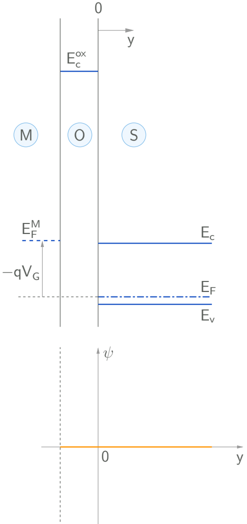
MOS capacitor



(a) $V_G = V_{FB}$

MOS capacitor

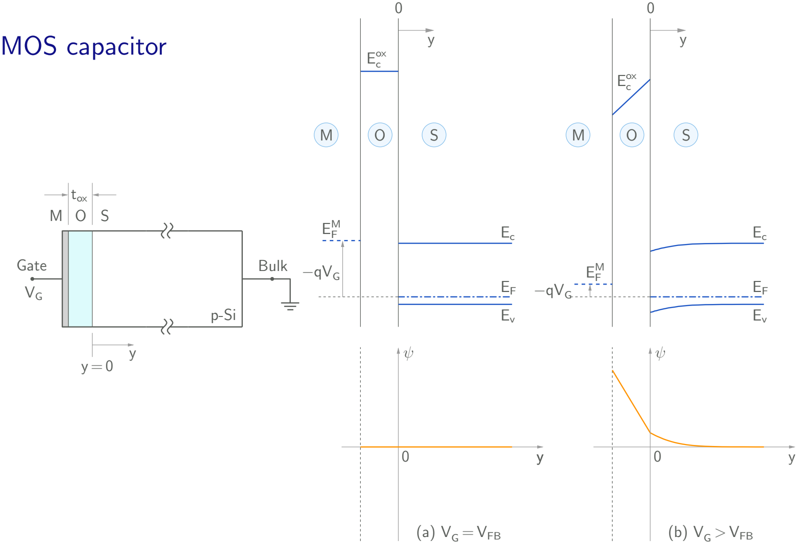




(a) $V_G = V_{FB}$

Suppose a voltage ΔV *in addition to* V_{FB} is applied, i.e., $V_G = V_{FB} + \Delta V$.

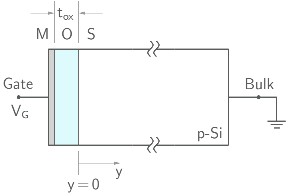
MOS capacitor

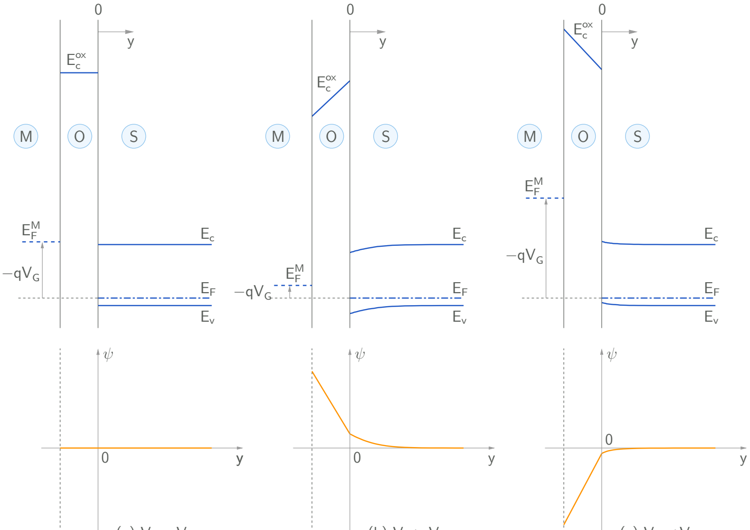


(a) $V_G = V_{FB}$ (b) $V_G > V_{FB}$

Suppose a voltage ΔV *in addition to* V_{FB} is applied, i.e., $V_G = V_{FB} + \Delta V$.

MOS capacitor

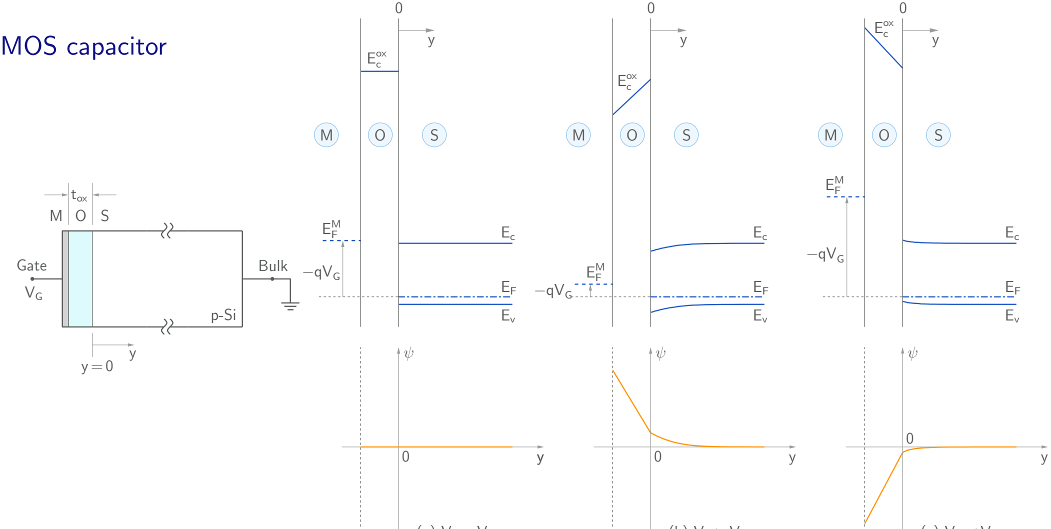




(a) $V_G = V_{FB}$ (b) $V_G > V_{FB}$ (c) $V_G < V_{FB}$

Suppose a voltage ΔV *in addition to* V_{FB} is applied, i.e., $V_G = V_{FB} + \Delta V$.

MOS capacitor

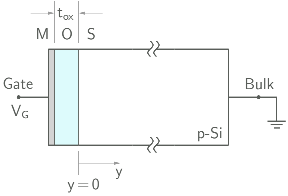


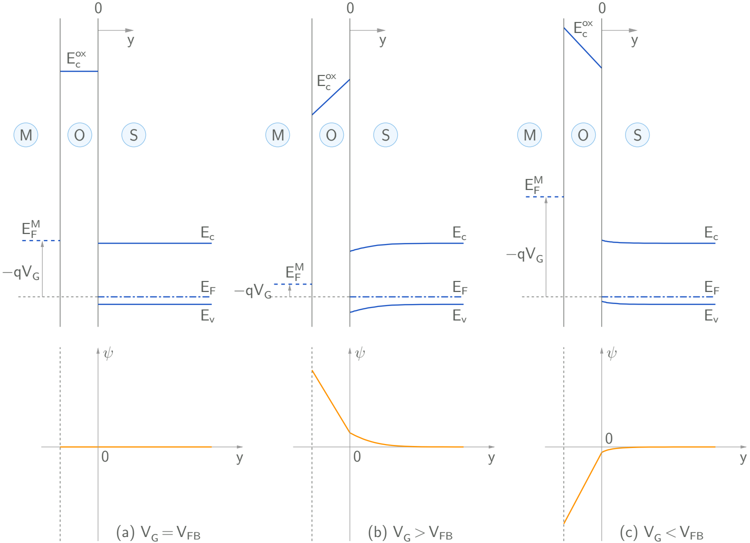
(a) $V_G = V_{FB}$ (b) $V_G > V_{FB}$ (c) $V_G < V_{FB}$

Suppose a voltage ΔV *in addition to* V_{FB} is applied, i.e., $V_G = V_{FB} + \Delta V$.

* The "excess" voltage ΔV appears partly across the oxide and partly across the semiconductor, i.e., $\Delta V = \Delta V_{ox} + \Delta V_{Si}$.

MOS capacitor



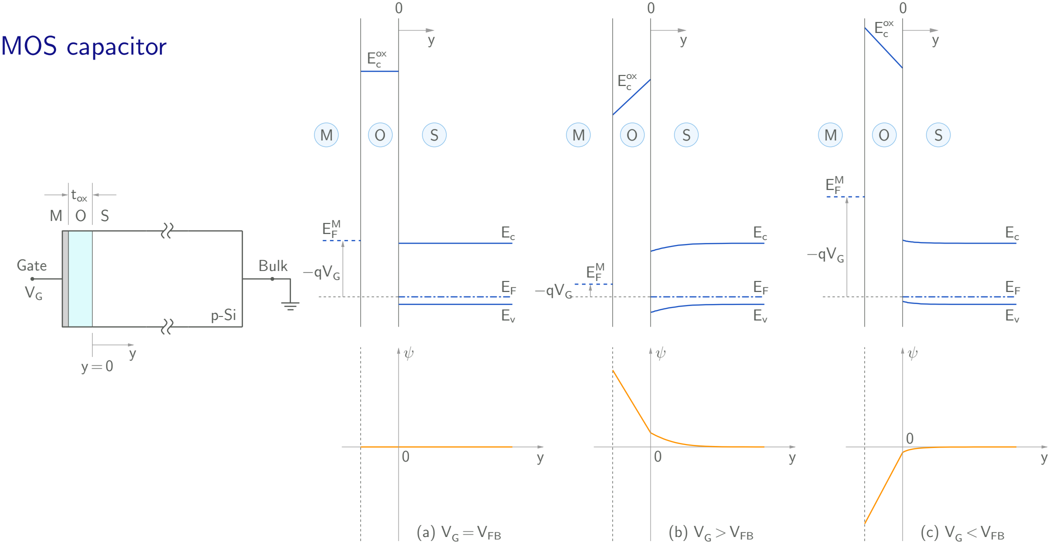


(a) $V_G = V_{FB}$

(b) $V_G > V_{FB}$

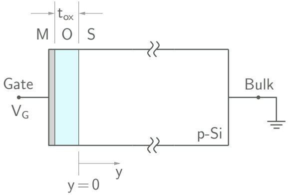
(c) $V_G < V_{FB}$

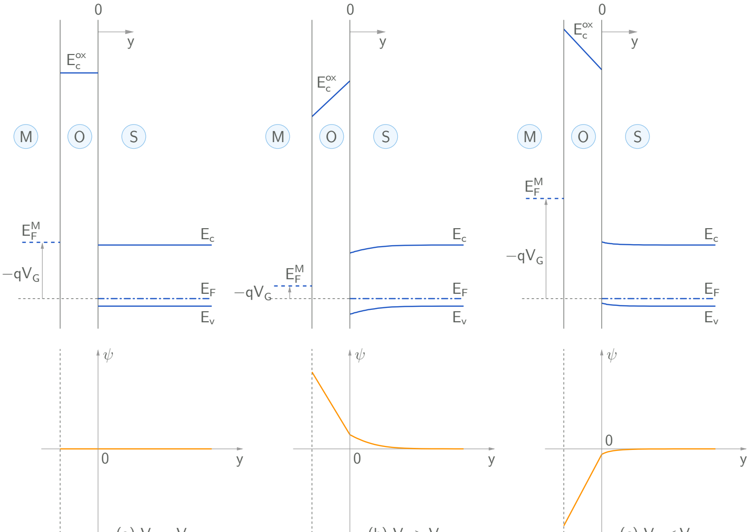
MOS capacitor


(a) $V_G = V_{FB}$ (b) $V_G > V_{FB}$ (c) $V_G < V_{FB}$

- * If $\Delta V > 0\,\text{V}$, the Fermi level E_F^M on the metal side goes *down* by $q\Delta V$, and the bands bend downward (with respect to the situation at $y \rightarrow \infty$).

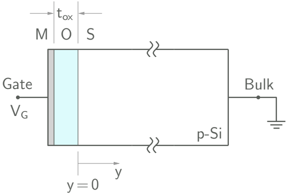
MOS capacitor

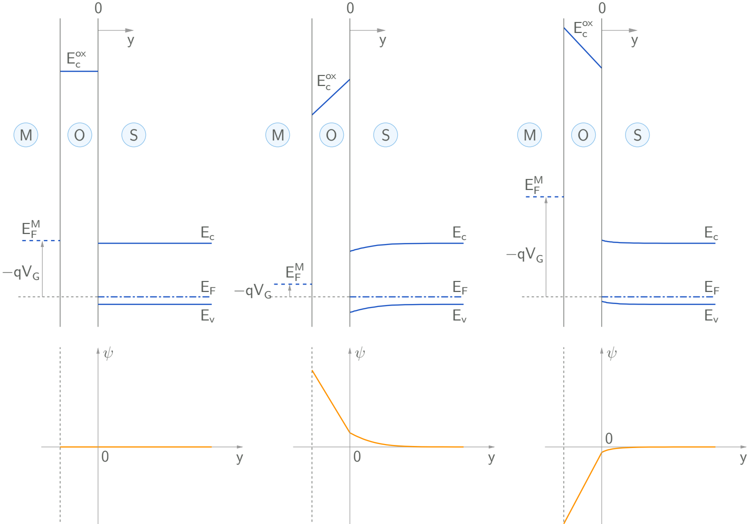




(a) $V_G = V_{FB}$ (b) $V_G > V_{FB}$ (c) $V_G < V_{FB}$

MOS capacitor

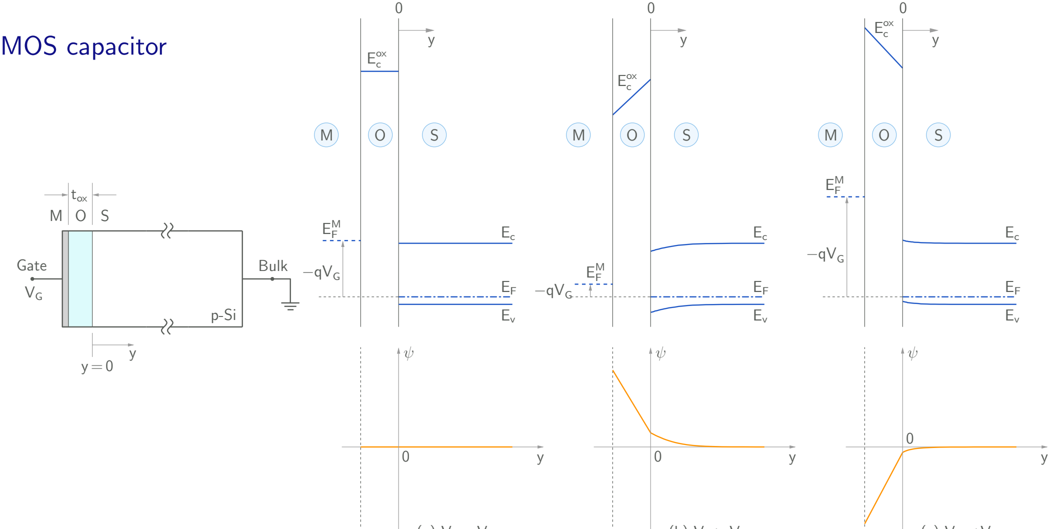




(a) $V_G = V_{FB}$ (b) $V_G > V_{FB}$ (c) $V_G < V_{FB}$

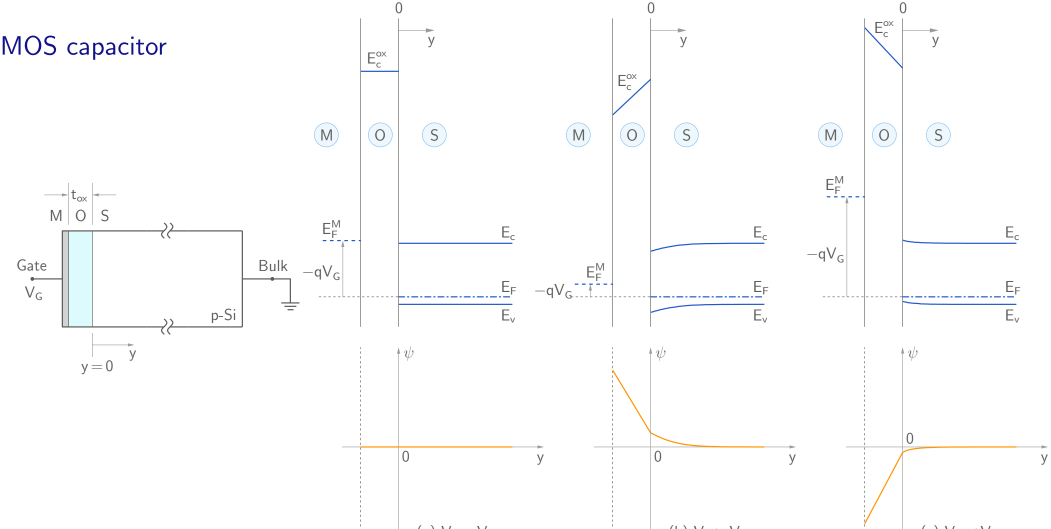
- ∗ If $\Delta V < 0\,\text{V}$, the Fermi level E_F^M on the metal side goes *up* by $-q\Delta V$, and the bands bend upward.

MOS capacitor



(a) $V_G = V_{FB}$ (b) $V_G > V_{FB}$ (c) $V_G < V_{FB}$

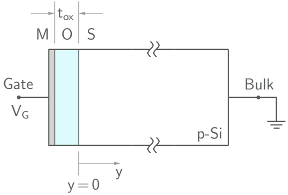
MOS capacitor

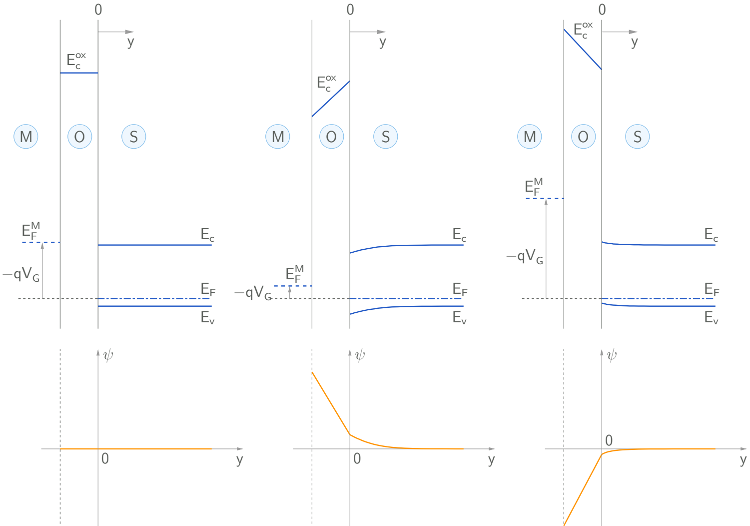


(a) $V_G = V_{FB}$ (b) $V_G > V_{FB}$ (c) $V_G < V_{FB}$

- $*$ Assuming that there is no surface charge at this interface or within the oxide layer, $\epsilon_{Si}\mathcal{E}_y(0^+) = \epsilon_{ox}\mathcal{E}_y(0^-)$, i.e., $\epsilon_{Si}\,\dfrac{d\psi}{dy}(0^+) = \epsilon_{ox}\,\dfrac{d\psi}{dy}(0^-)$, $|\Delta V_{ox}| = |\mathcal{E}_y(0^-)|\,t_{ox}$.

MOS capacitor



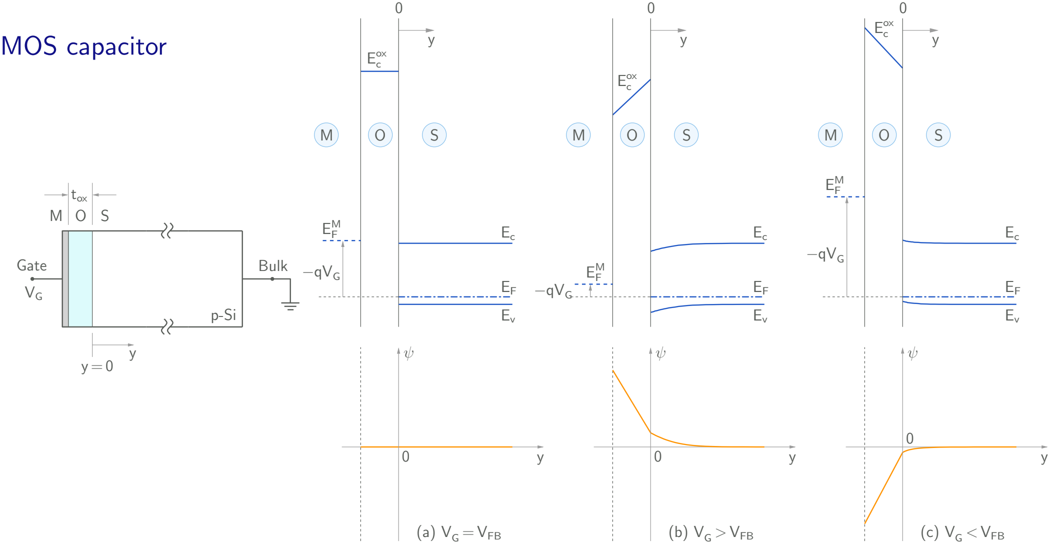


(a) $V_G = V_{FB}$

(b) $V_G > V_{FB}$

(c) $V_G < V_{FB}$

MOS capacitor



(a) $V_G = V_{FB}$

(b) $V_G > V_{FB}$

(c) $V_G < V_{FB}$

- In practice, there is always some charge at the Si-SiO$_2$ interface because of the abrupt interruption of the crystalline silicon structure caused by the oxide. The effect of the interface charge and any other fixed charge within the oxide layer can be clubbed into a shift in the flat-band voltage.

M. B. Patil, IIT Bombay

MOS capacitor: example

$q\phi_m = 4.1\,\mathrm{eV}$

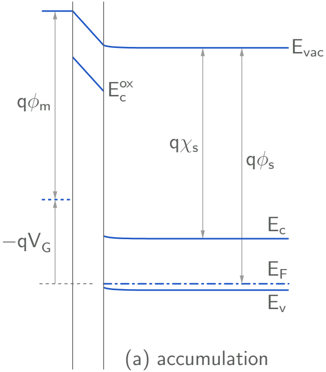
$q\chi_s = 4.05\,\mathrm{eV}$

$t_{ox} = 50\,\mathrm{nm}$

$N_a = 5 \times 10^{16}\,\mathrm{cm}^{-3}$

$V_{FB} \approx -1\,\mathrm{V}$

$V_G = -1.8\,\mathrm{V}$



(a) accumulation

MOS capacitor: example

$q\phi_m = 4.1\,\text{eV}$

$q\chi_s = 4.05\,\text{eV}$

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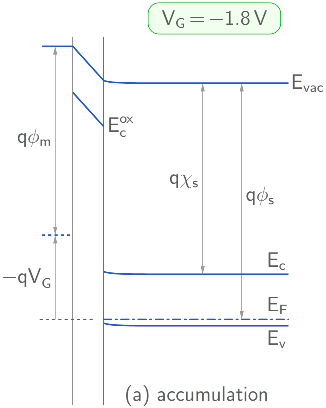

(a) accumulation

- $V_G = -1.8\,\text{V}$: accumulation of majority carriers (holes) near the interface

MOS capacitor: example

$q\phi_m = 4.1\,\mathrm{eV}$

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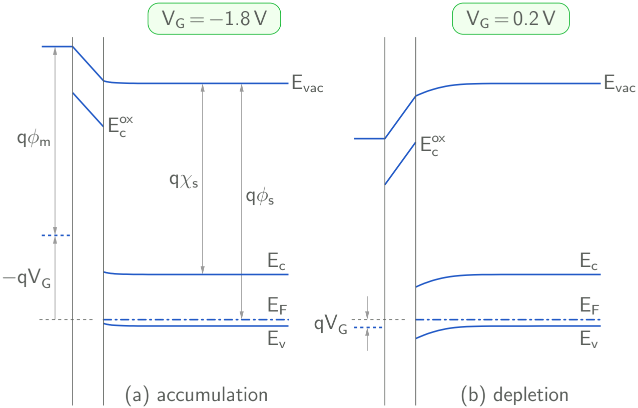


(a) accumulation

(b) depletion

- $V_G = -1.8\,\mathrm{V}$: accumulation of majority carriers (holes) near the interface

MOS capacitor: example

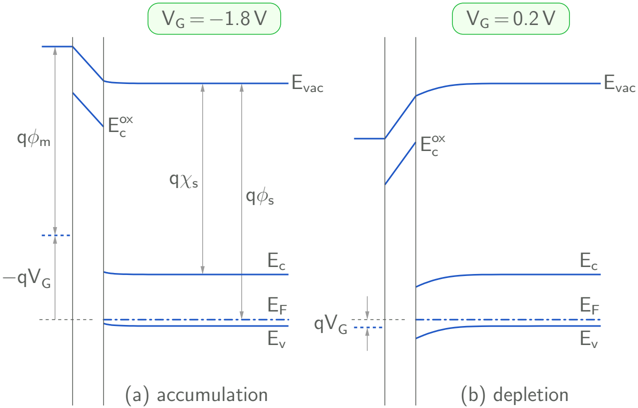
$q\phi_m = 4.1\,\text{eV}$

$q\chi_s = 4.05\,\text{eV}$

$t_{ox} = 50\,\text{nm}$

$N_a = 5 \times 10^{16}\,\text{cm}^{-3}$

$V_{FB} \approx -1\,\text{V}$



(a) accumulation (b) depletion

- $V_G = -1.8\,\text{V}$: accumulation of majority carriers (holes) near the interface
- $V_G = 0.2\,\text{V}$: depletion of majority carriers (holes) near the interface

MOS capacitor: example

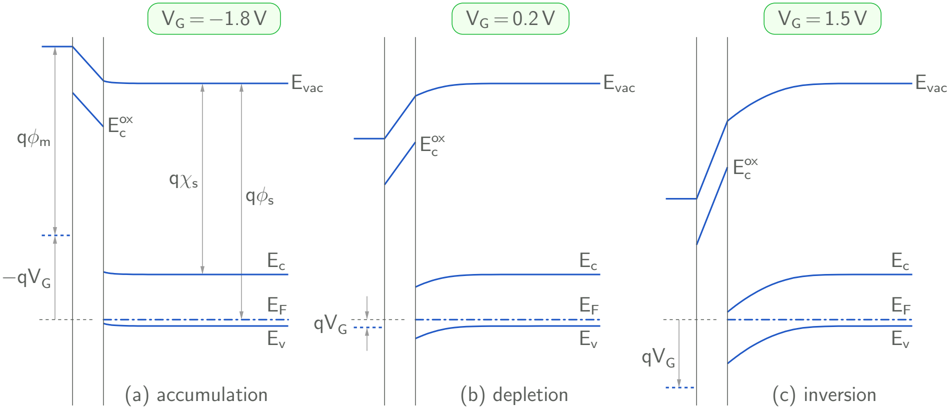
$q\phi_m = 4.1\,\text{eV}$

$q\chi_s = 4.05\,\text{eV}$

$t_{ox} = 50\,\text{nm}$

$N_a = 5 \times 10^{16}\,\text{cm}^{-3}$

$V_{FB} \approx -1\,\text{V}$



(a) accumulation (b) depletion (c) inversion

- $V_G = -1.8\,\text{V}$: accumulation of majority carriers (holes) near the interface
- $V_G = 0.2\,\text{V}$: depletion of majority carriers (holes) near the interface

MOS capacitor: example

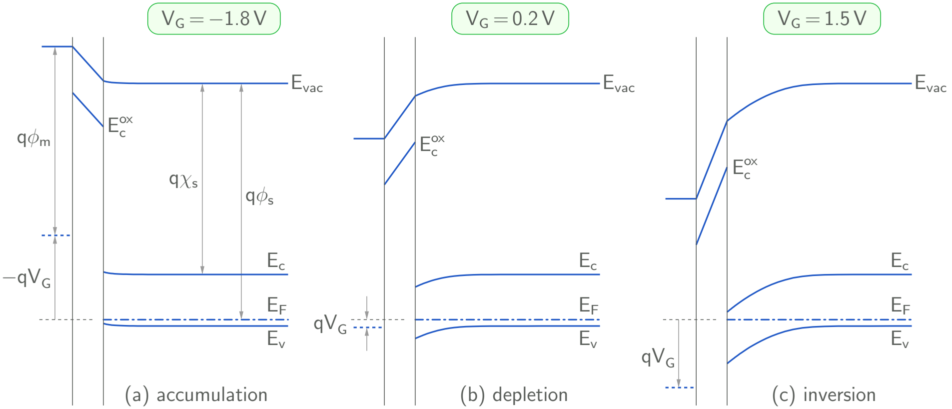
$q\phi_m = 4.1\,\text{eV}$

$q\chi_s = 4.05\,\text{eV}$

$t_{ox} = 50\,\text{nm}$

$N_a = 5 \times 10^{16}\,\text{cm}^{-3}$

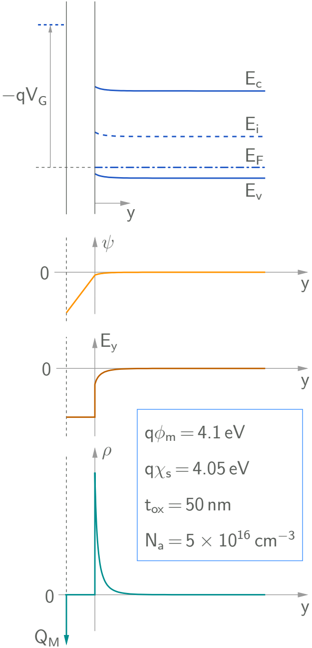
$V_{FB} \approx -1\,\text{V}$



(a) accumulation (b) depletion (c) inversion

- $V_G = -1.8\,\text{V}$: accumulation of majority carriers (holes) near the interface
- $V_G = 0.2\,\text{V}$: depletion of majority carriers (holes) near the interface
- $V_G = 1.5\,\text{V}$: depletion of majority carriers (holes) *and* a significant increase in minority carriers (electrons) near the interface

MOS capacitor: accumulation (*p*-type semiconductor)



$q\phi_m = 4.1\,\text{eV}$

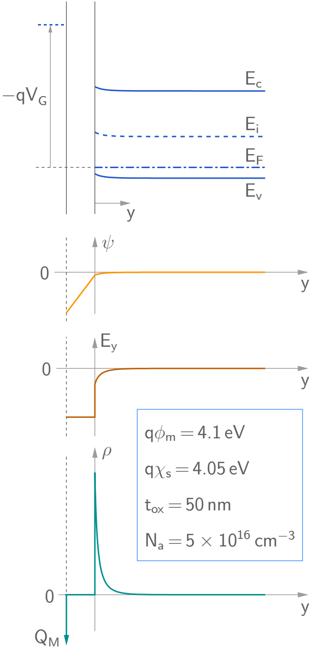
$q\chi_s = 4.05\,\text{eV}$

$t_{ox} = 50\,\text{nm}$

$N_a = 5 \times 10^{16}\,\text{cm}^{-3}$

MOS capacitor: accumulation (p-type semiconductor)

- $*$ When $V_G < V_{FB}$ is applied, the valence band edge E_v gets closer to the Fermi level E_F (as compared to the equilibrium situation), and we have $p > p_0$ near the surface ($y = 0$).

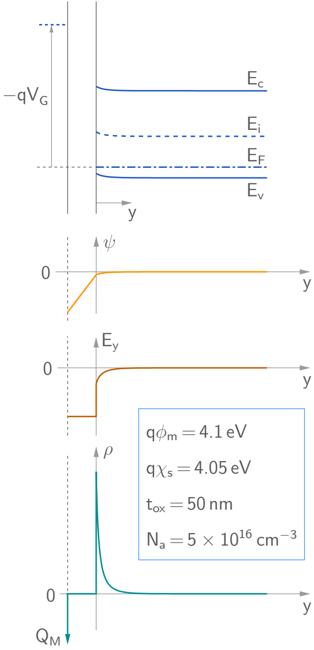


MOS capacitor: accumulation (p-type semiconductor)

- When $V_G < V_{FB}$ is applied, the valence band edge E_v gets closer to the Fermi level E_F (as compared to the equilibrium situation), and we have $p > p_0$ near the surface ($y = 0$).
- The total charge in the semiconductor (per unit area in the x-z plane),

  $$Q_s = \int_0^{\infty} \rho \, dy = q \int_0^{\infty} (N_d^+ - N_a^- + p - n) \, dy,$$

  is positive.



$q\phi_m = 4.1$ eV

$q\chi_s = 4.05$ eV

$t_{ox} = 50$ nm

$N_a = 5 \times 10^{16}$ cm^{-3}

MOS capacitor: accumulation (p-type semiconductor)

- When $V_G < V_{FB}$ is applied, the valence band edge E_v gets closer to the Fermi level E_F (as compared to the equilibrium situation), and we have $p > p_0$ near the surface ($y = 0$).
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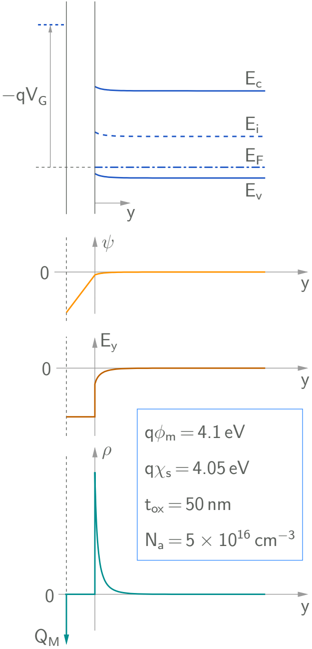
$$Q_s = \int_0^{\infty} \rho \, dy = q \int_0^{\infty} (N_d^+ - N_a^- + p - n) \, dy,$$
is positive.
- The electric field, $\mathcal{E}_y = \dfrac{1}{q} \dfrac{dE_c}{dy}$, is negative.



MOS capacitor: accumulation (p-type semiconductor)

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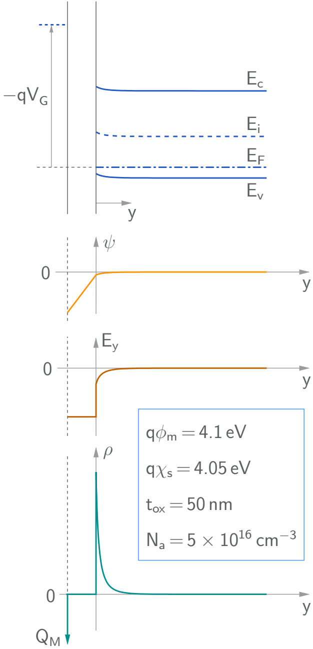
  $$Q_s = \int_0^{\infty} \rho \, dy = q \int_0^{\infty} (N_d^+ - N_a^- + p - n) \, dy,$$
  is positive.
- The electric field, $\mathcal{E}_y = \dfrac{1}{q} \dfrac{dE_c}{dy}$, is negative.
- There is a discontinuity in $\mathcal{E}$ at the interface;
  $$\epsilon_{\text{Si}} \mathcal{E}_{\text{Si}} = \epsilon_{\text{ox}} \mathcal{E}_{\text{ox}} \rightarrow \mathcal{E}_{\text{ox}} = \frac{\epsilon_{\text{Si}}}{\epsilon_{\text{ox}}} \mathcal{E}_{\text{Si}} = \frac{11.7 \, \epsilon_0}{3.9 \, \epsilon_0} \mathcal{E}_{\text{Si}} = 3 \mathcal{E}_{\text{Si}}.$$



$q\phi_m = 4.1$ eV

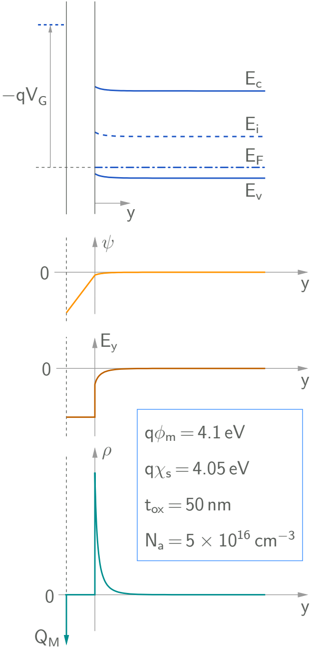
$q\chi_s = 4.05$ eV

$t_{ox} = 50$ nm

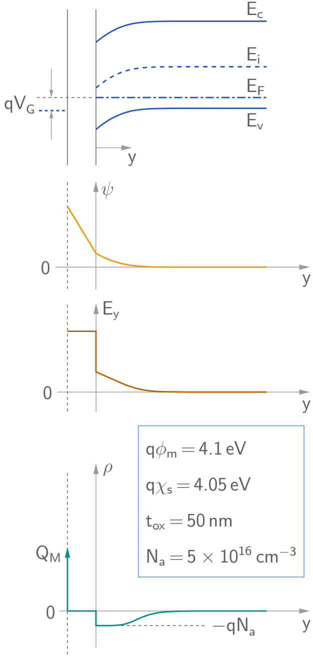
$N_a = 5 \times 10^{16}$ cm^{-3}

MOS capacitor: accumulation (p-type semiconductor)

- When $V_G < V_{FB}$ is applied, the valence band edge E_v gets closer to the Fermi level E_F (as compared to the equilibrium situation), and we have $p > p_0$ near the surface ($y = 0$).
- The total charge in the semiconductor (per unit area in the x-z plane),
$$Q_s = \int_0^\infty \rho\, dy = q \int_0^\infty (N_d^+ - N_a^- + p - n)\, dy,$$
is positive.
- The electric field, $\mathcal{E}_y = \dfrac{1}{q}\dfrac{dE_c}{dy}$, is negative.
- There is a discontinuity in $\mathcal{E}$ at the interface;
$$\epsilon_{\text{Si}}\mathcal{E}_{\text{Si}} = \epsilon_{\text{ox}}\mathcal{E}_{\text{ox}} \rightarrow \mathcal{E}_{\text{ox}} = \frac{\epsilon_{\text{Si}}}{\epsilon_{\text{ox}}}\mathcal{E}_{\text{Si}} = \frac{11.7\,\epsilon_0}{3.9\,\epsilon_0}\mathcal{E}_{\text{Si}} = 3\mathcal{E}_{\text{Si}}.$$
- There is a negative charge Q_M at the metal surface which is equal to $-Q_s$. The total charge in the MOS capacitor is zero.



MOS capacitor: depletion (*p*-type semiconductor)



$q\phi_m = 4.1\,\text{eV}$

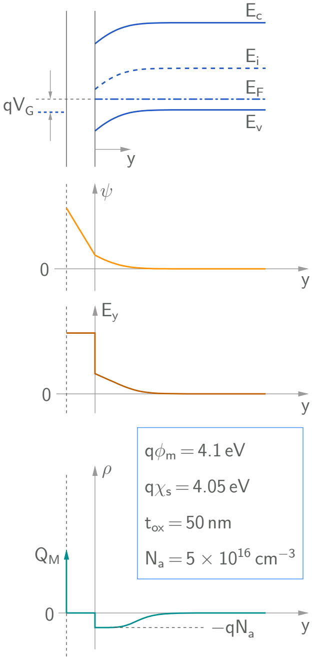
$q\chi_s = 4.05\,\text{eV}$

$t_{ox} = 50\,\text{nm}$

$N_a = 5 \times 10^{16}\,\text{cm}^{-3}$

MOS capacitor: depletion (p-type semiconductor)

- $*$ When $V_G > V_{FB}$ is applied, E_c comes closer to E_F near the interface.



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$q\chi_s = 4.05\,\text{eV}$

$t_{ox} = 50\,\text{nm}$

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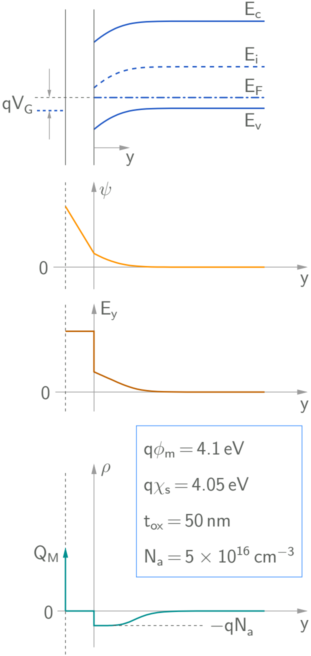

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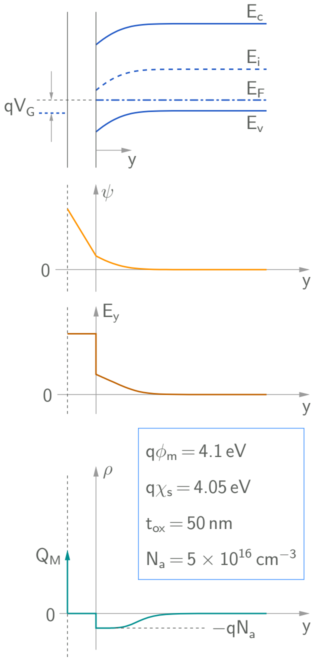

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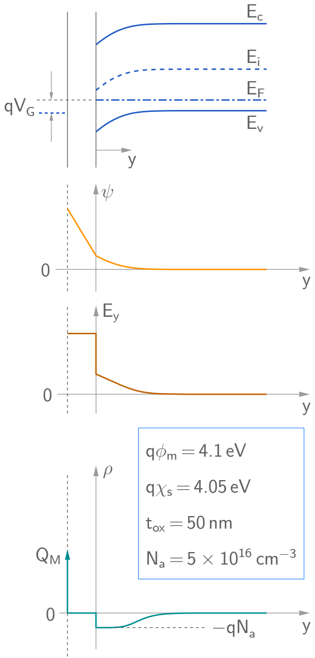

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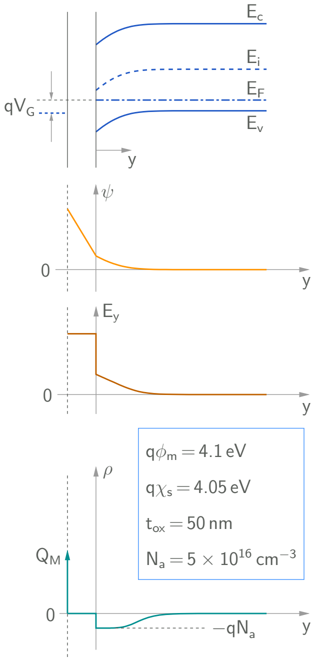

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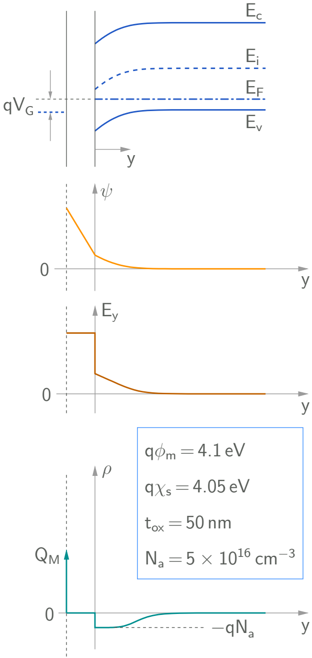
- There is a positive charge Q_M at the metal surface which is equal to $-Q_s$. The total charge in the MOS capacitor is zero.



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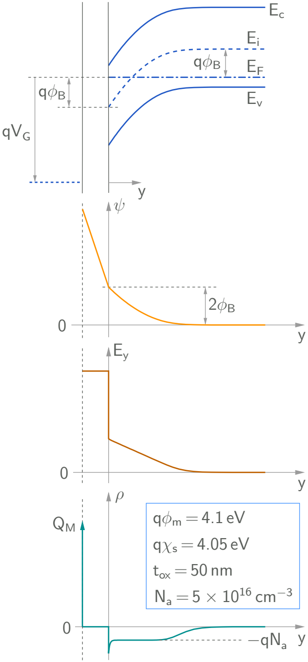

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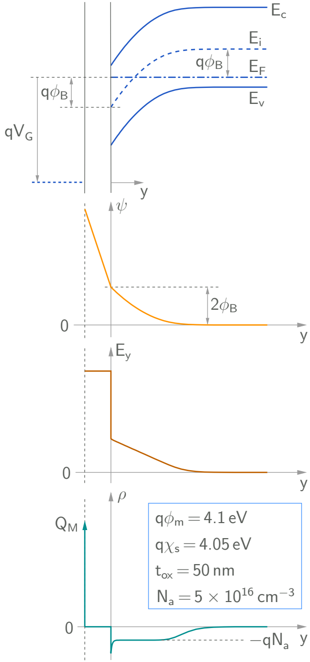

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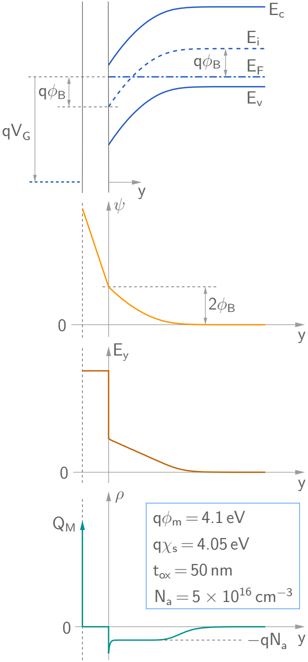

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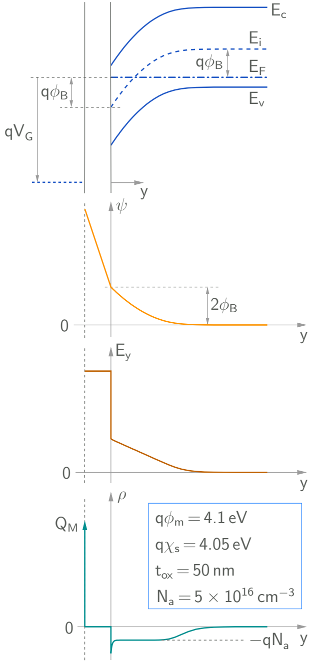

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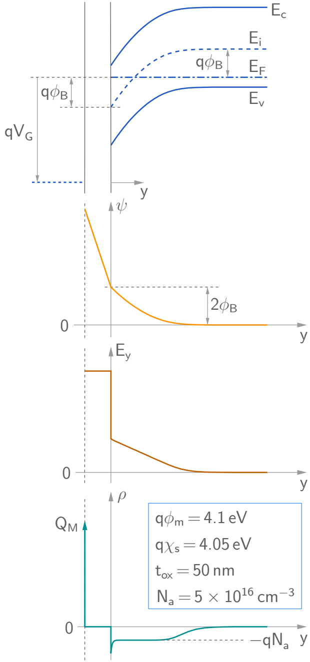

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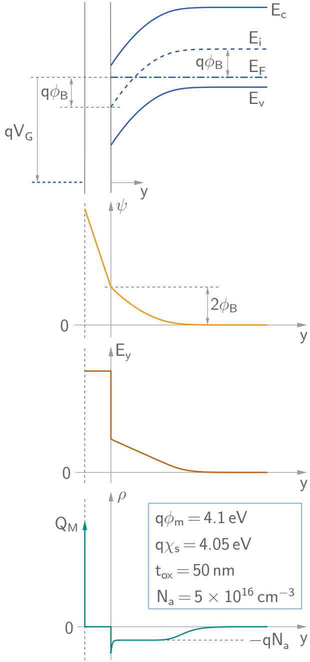

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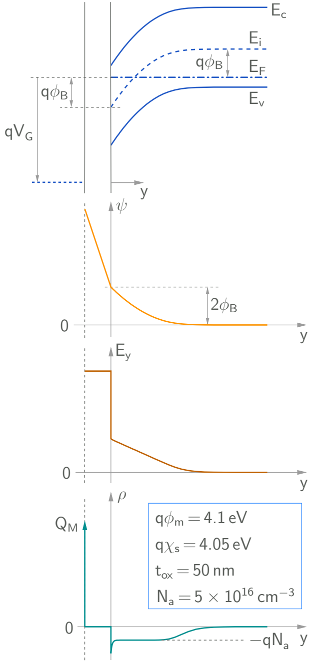
  In other words, the minority carrier density at the interface becomes as large as the majority carrier density in the "bulk" (i.e., sufficiently far from the interface).



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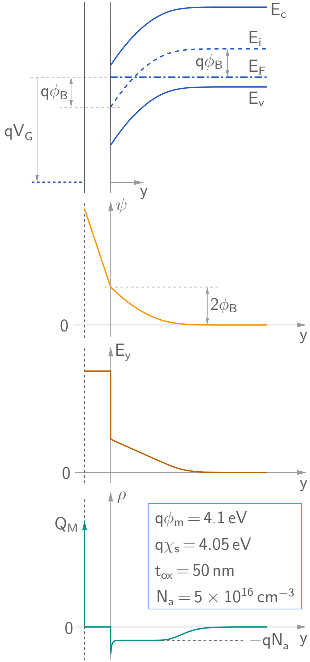

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- The condition $n(0) = p_0$ is considered to be the onset of the inversion regime.