Op Amp Circuits

Inverting and Non-inverting Amplifiers, Integrator, Differentiator

Introduction

An Operational Amplifier (Op Amp) is a versatile building block used in a variety of applications in electronics. Op amps make circuit design simple and robust. An op amp chip has a complex internal circuit (see Fig. 1), but from the user's perspective, it can be treated by a simple equivalent circuit, making the design process very simple and straightforward, as compared to using discrete transistors.

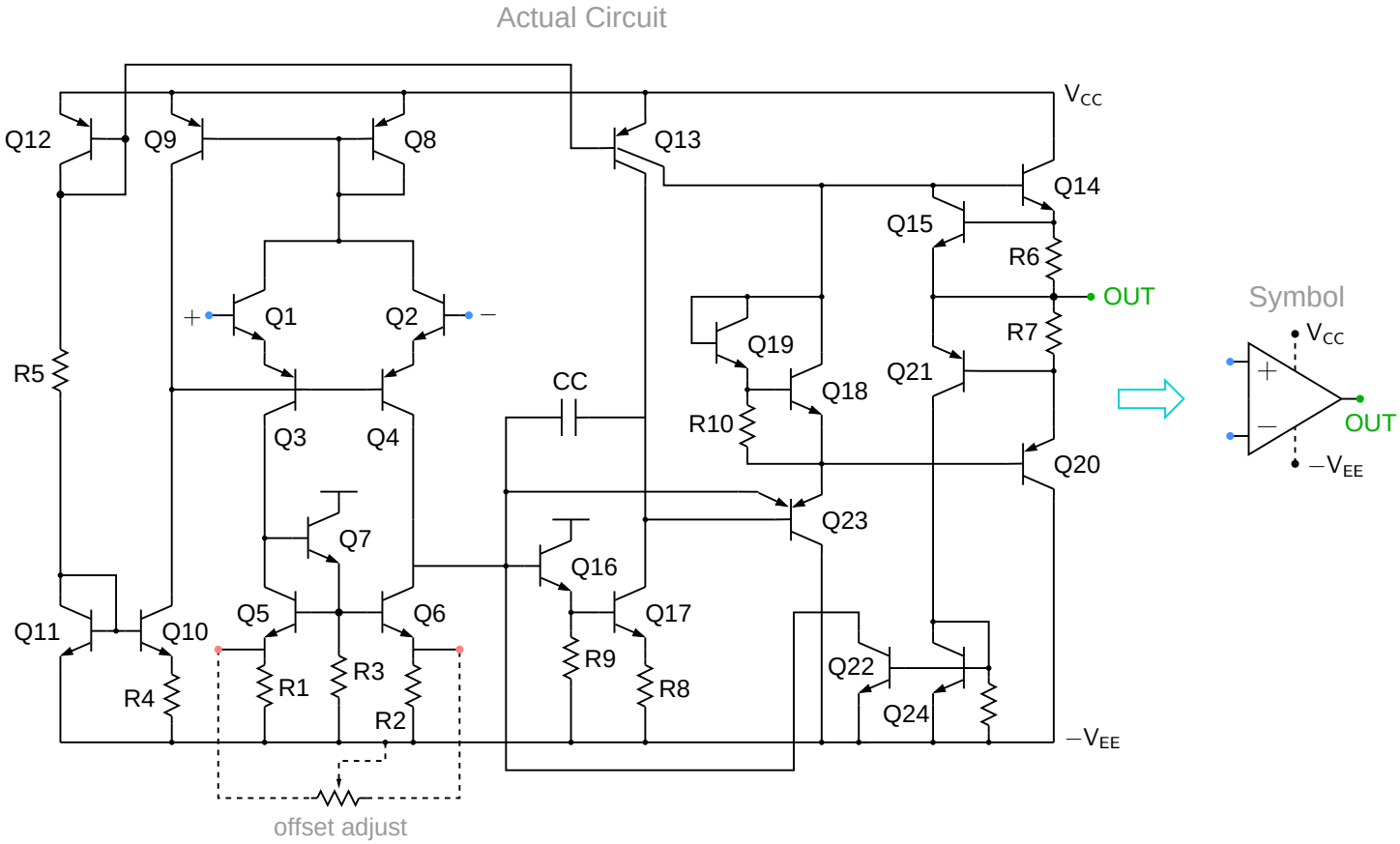

Figure 1: Internal circuit of Op Amp 741

Power supply

Fig. 2 shows the most commonly used configuration for providing power supply to an op amp. The $+V_{CC}$ and $-V_{CC}$ terminals of the op amp are connected to $+V_0$ and $-V_0$ where V_0 is typically 10 to 15 V. For example, the $+V_{CC}$ terminal may be connected to +15 V, and the $-V_{CC}$ terminal to −15 V. The voltages +15 V and −15 V here are with respect to the *ground* of the power supply which we will use in the lab. Note that the Op Amp 741 (see Fig. 1) does not have a ground terminal of its own.

In op amp circuit diagrams, the $\pm V_{CC}$ connections are often not shown explicitly, but we must always remember that an op amp circuit will not work if the power supply is not provided. While testing the circuit, it is a good idea to first check whether the $\pm V_{CC}$ terminals of the op amp are indeed getting $\pm V_0$.

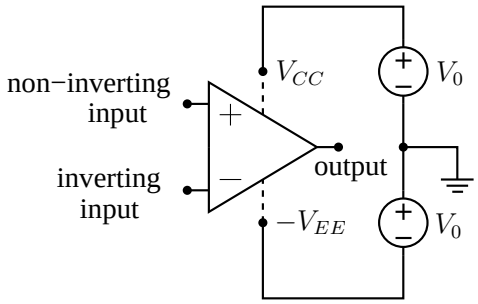

Figure 2: Connecting power supply to an op amp

Linear and saturation regions

An op amp exhibits a very large gain (of the order of 10^5) $A_V = \dfrac{V_o}{V_i}$, where $V_i = V_+ - V_-$. The maxmimum and minimum values of V_o are limited to $\pm V_{\text{sat}}$ (the saturation voltage), where V_{sat} is about 1 V smaller than V_{CC}. As an example, consider $V_{\text{sat}} = 10\,\text{V}$ (see Fig. 3 (a)). When

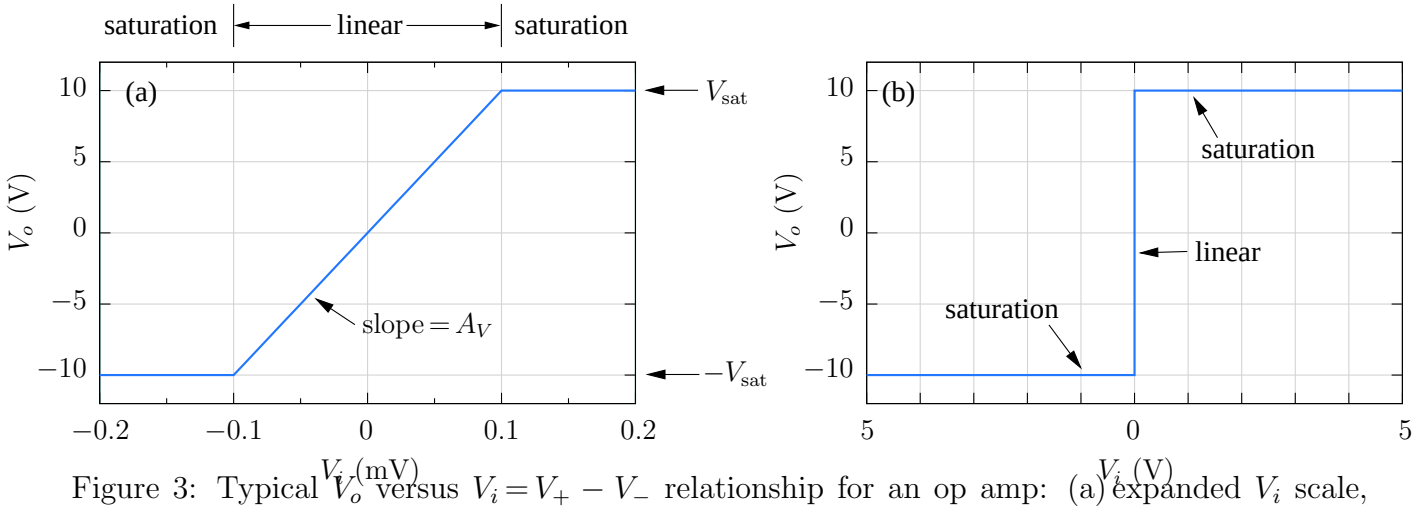

Figure 3: Typical V_o versus $V_i = V_+ - V_-$ relationship for an op amp: (a) expanded V_i scale, (b) compressed V_i scale.

$V_i > \dfrac{10\,\text{V}}{10^5} = 0.1\,\text{mV}$, $V_o = 10\,\text{V}$. Similarly, when $V_i < -\dfrac{10\,\text{V}}{10^5} = -0.1\,\text{mV}$, $V_o = -10\,\text{V}$. These two regions are referred to as "saturation." For an input voltage between these two limits, i.e., $-0.1\,\text{mV} < V_i < 0.1\,\text{mV}$, V_o changes linearly with V_i, and this region is referred to as the "linear" region. The exact values of these limits will of course change with V_{sat} and the gain A_V of the op amp, but it is clear that the linear region is very narrow indeed. When the V_o versus

V_i relationship is plotted on comparable scales, the linear region appears as a vertical line (see Fig. 3 (b)). In other words, when the op amp operates in the linear region, we can say that $V_+ - V_- \approx 0\,\text{V}$, i.e., $V_+ \approx V_-$.

Input resistance

From Fig. 1, we see that the current entering the inverting or the non-inverting terminal of the op amp is a base current of a BJT (or the gate current of an FET for op amps with FET input devices), which is generally small – much smaller than the other currents in the external circuit. To an excellent approximation, therefore, we can say that the input currents of the op amp can be neglected or that the op amp has an infinite input resistance.

To summarise, we can make the following assumptions for an op amp operating in the linear region.

(a) $V_+ \approx V_-$ or V_+ and V_- are *virtually* the same.

(b) $i_+ = i_- = 0$, where i_+ and i_- are the currents entering the non-inverting and inverting input terminals of the op amp, respectively.

In the following, we will consider op amp circuits in which the op amp operates in the linear region.

Inverting amplifier

Fig. 4 shows the inverting amplifier circuit.

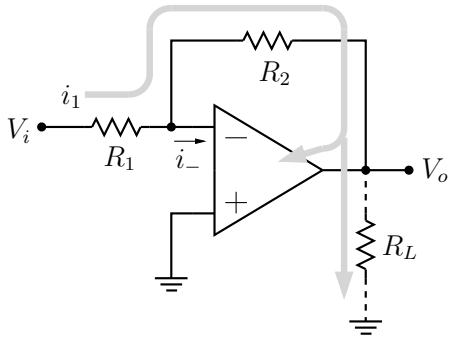

Figure 4: Inverting amplifier circuit

Since $V_+ = 0\,\text{V}$, $V_- \approx V_+ = 0\,\text{V}$, and $i_1 = \dfrac{V_i - 0}{R_1} = \dfrac{V_i}{R_1}$. Since the current entering the inverting terminal can be neglected, i_1 must flow through R_2, and therefore

$$V_o = V_- - i_1 R_2 = 0 - \frac{V_i}{R_1} R_2 \Rightarrow \frac{V_o}{V_i} = -\frac{R_2}{R_1}\,. \tag{1}$$

Since V_o and V_i are out of phase (because of the negative sign in Eq. 1), the circuit is called an *inverting* amplifier. The amplifier has a gain (magnitude) of R_2/R_1 which can be changed

simply by choosing appropriate values of R_1 and R_2, which is much simpler than designing a common-emitter or common-source amplifier, for example. Note also that Eq. 1 does not depend on whether or not a load resistance R_L is connected or its value, and that surely makes the amplifier design simpler.

We should keep in mind the following practical considerations (which may also apply to other op amp circuits).

(a) Saturation: Since the op amp output is limited to $\pm V_{\text{sat}}$, the output voltage waveform gets clipped if the expected output voltage (i.e., gain times the input voltage) exceeds these limits, as shown in Fig. 5.

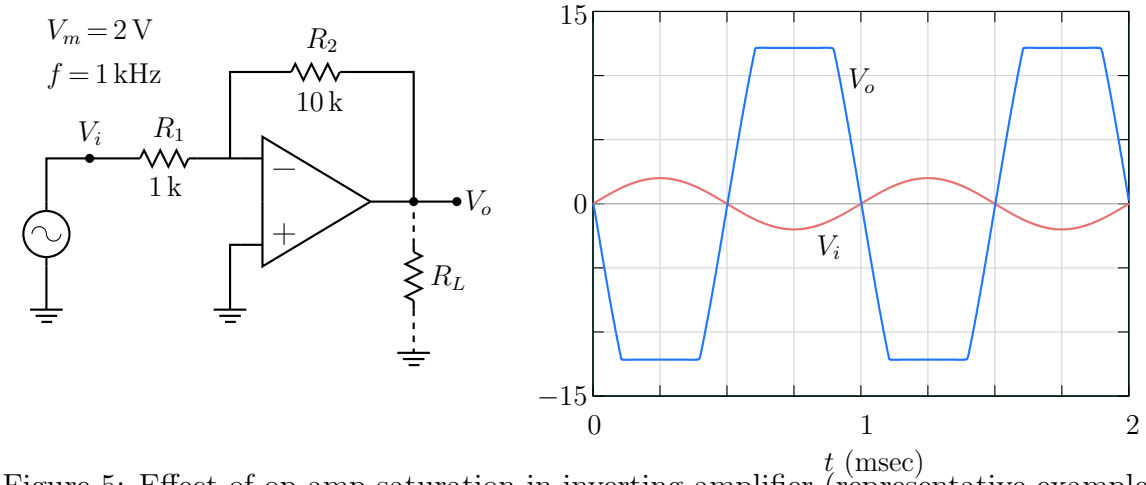

Figure 5: Effect of op amp saturation in inverting amplifier (representative example).

(b) Realistic R_i and R_o: In the above analysis, we have assumed the op amp to be ideal, with an infinite input resistance R_i and zero output resistance R_o. In practice, R_i could be of the order of a few MΩ, and R_o could be a few ohms. For Eq. 1 to hold, we require that R_1 and R_2 should be small compared to R_i and large compared to R_o. Keeping these limits in minds, R_1 and R_2 are typically chosen to be in the 1 kΩ to 50 kΩ range.

(c) Frequency response: Eq. 1 says nothing at all about the frequency response of the amplifier, implying that the amplifier will follow Eq. 1 for an input signal with very low frequencies (including DC) to very high frequencies. In reality, the frequency response of an op amp is limited and is given by

$$A(j\omega) = \frac{A_V^0}{1 + j\omega/\omega_c}\,. \tag{2}$$

For Op Amp 741, $A_V^0 \approx 10^5$, and $f_c = 10\,\text{Hz}$ ($\omega_c = 2\pi f_c$). With Eq. 2, we get the following expression for the gain of the inverting amplifier.

$$\frac{V_o(s)}{V_i(s)} = -\frac{R_2}{R_1}\,\frac{1}{1 + s/\omega_c'}\,, \quad \omega_c' = \frac{A_V^0 \omega_c}{1 + R_2/R_1}\,. \tag{3}$$

The gain now depends on the signal frequency, as shown in Fig. 6. Note that Eq. 1 holds only at low frequencies. At higher frequencies, the gain starts dropping. Higher the gain, lower is the cut-off frequency of the amplifier.

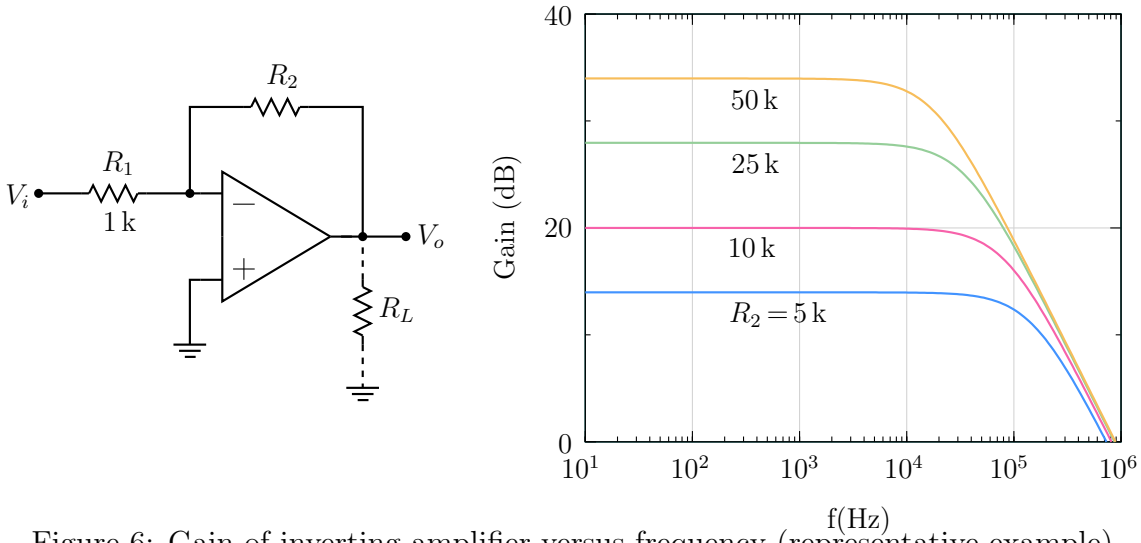

Figure 6: Gain of inverting amplifier versus frequency (representative example).

(d) Slew rate: In a real op amp, the maximum rate at which the output voltage can rise (or fall) is limited by the "slew rate." For Op Amp 741, the slew rate is $0.5\,\text{V}/\mu\text{sec}$. The slew rate limitation can casue distortion in the output voltage waveform. For example, with a sinusoidal input voltage to the inverting amplifier, we expect a sinusoidal output voltage. However, if the expected $\left|\frac{dV_o}{dt}\right|$ is larger than the slew rate, the output voltage waveform becomes triangular (see Fig. 7).

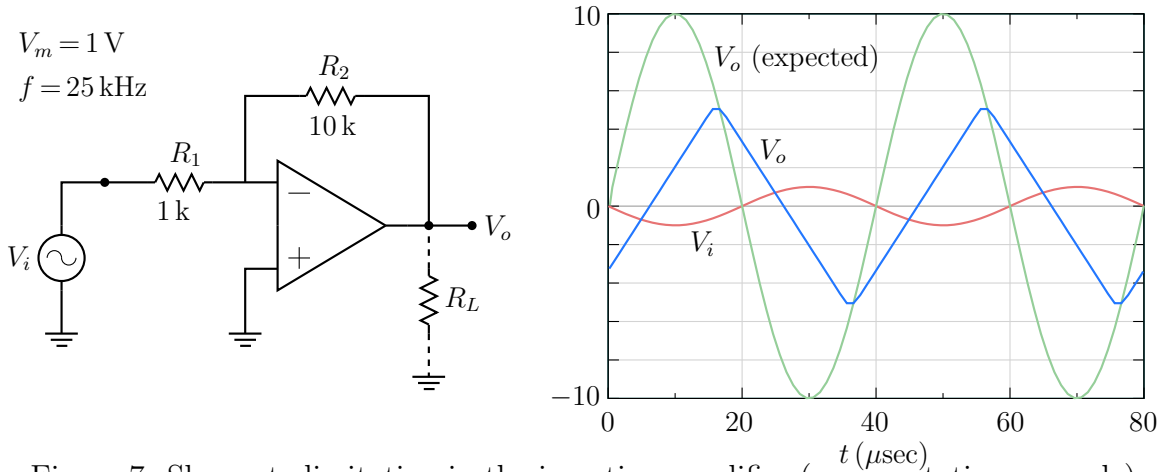

Figure 7: Slew rate limitation in the inverting amplifier (representative example).

If we want to plot gain versus frequency for the inverting amplifier, we must keep in mind the slew rate limitation and keep the magnitude of the input sinusoid sufficiently small in

the frequency range of interest. In other words, we need to check that the output waveform is sinusoidal at the highest frequency of interest.

Non-inverting amplifier

Fig. 8 shows the non-inverting amplifier circuit.

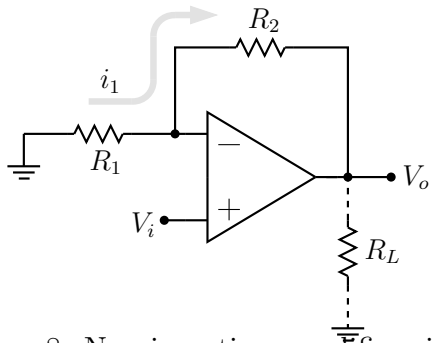

Figure 8: Non-inverting amplifier circuit

Since $V_+ = V_i$, we have $V_- \approx V_+ = V_i$. The current i_1 is therefore $i_1 = \dfrac{0 - V_i}{R_1} = -\dfrac{V_i}{R_1}$. Since the input current of the op amp is negligibly small, the current through R_2 is also equal to i_1. The output voltage is given by

$$V_o = V_- - i_1 R_2 = V_i - \left(\frac{-V_i}{R_1}\right) R_2 \Rightarrow \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}\,. \tag{4}$$

The output voltage V_o is in phase with the input voltage V_i, and the circuit is therefore known as the non-inverting amplifier, its gain being $1 + R_2/R_1$.

Integrator

Fig. 9 shows the integrator circuit.

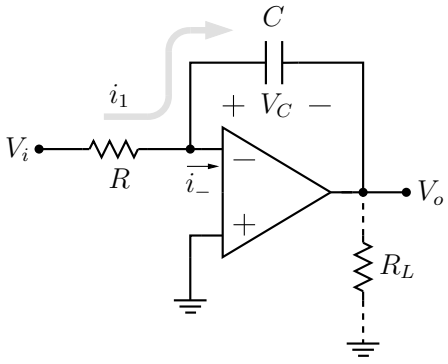

Figure 9: Integrator circuit

As in the inverting amplifier, we have a virtual ground at V_- since $V_- \approx V_+ = 0\,\mathrm{V}$. The current i, which also flows through the capacitor, is $\dfrac{V_i - 0}{R} = \dfrac{V_i}{R}$. Since $i = \dfrac{dV_C}{dt}$, we have

$$\frac{dV_C}{dt} = \frac{i}{C} = \frac{V_i}{RC} \Rightarrow V_C = \frac{1}{RC}\int V_i dt\,. \tag{5}$$

Finally, the output voltage can be related to the input voltage as

$$V_o = V_- - V_C = 0 - V_C = -\frac{1}{RC}\int V_i dt\,. \tag{6}$$

Integrator: Practical implementation

Fig. 10 shows the integrator circuit with a more realistic op amp model, including the bias currents [i.e., the base currents of transistors Q_1 and Q_2 (see Fig. 1) in Op Amp 741].

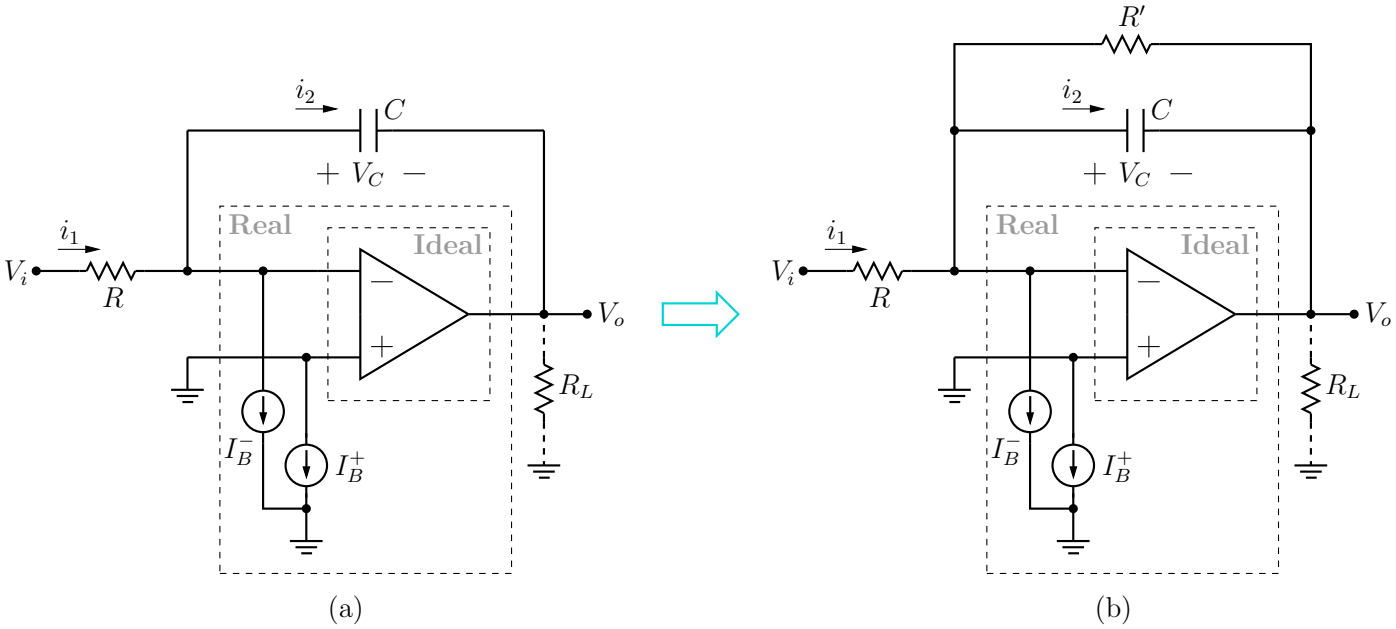

Figure 10: (a) An integrator with a realistic op amp model, (b) improved integrator circuit.

As mentioned earlier, the bias currents are generally small and can be neglected, as we have done for the inverting and non-inverting amplifier circuits. In the integrator, however, the bias currents are a cause for concern for the following reason.

Consider $V_i = 0$ in the circuit of Fig. 10 (a). Let the capacitor voltage be initially zero. In this situation, we would expect the output voltage to remain 0 V. However, the bias current I_B^- flows through the capacitor, and it charges the capacitor. Even though I_B^- is a small current, it results in a continuous increase in the capacitor voltages, eventually driving the op amp into saturation.

To prevent this undesirable situation, we can provide a DC path to the bias current in the form of the resistor R' shown in Fig. 10 (b). In steady state, the bias current causes a voltage drop $I_B^- R'$ across the resistor. The output voltage is now $V_o = V_- - V_{R'} = -I_B^- R'$ which can be made negligibly small by choosing an appropriate value of R'. Note that R' should not be made so small that it interferes with the functioning of the circuit as an integrator. In other words, R' must be large as compared to $1/j\omega C$ (in magnitude) at the frequency of interest.

Differentiator

Fig. 11 (a) shows the differentiator circuit.

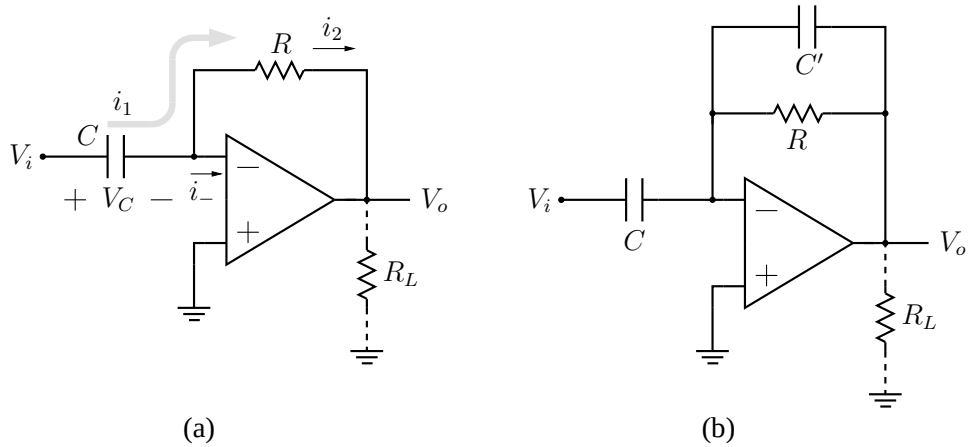

Figure 11: Differentiator circuit: (a) basic operation, (b) practical configuration

As in the inverting amplifier, we have $V_- \approx V_+ = 0\,\text{V}$. The voltage across the capacitor is $V_C = V_i - 0 = V_i$, and the capacitor current i_1 is $C\,\dfrac{dV_C}{dt}$. Since the current i_- can be neglected, we have

$$i_2 = i_1 = C\,\frac{dV_C}{dt} = C\,\frac{dV_i}{dt}\,. \tag{7}$$

The output voltage V_o is

$$V_o = V_- - i_2 R = 0 - RC\,\frac{dV_i}{dt} = -RC\frac{dV_i}{dt}\,, \tag{8}$$

and the circuit works as a differentiator.

There is a practical difficulty in using a differentiator in the above form. The AC gain of the circuit is $A = -R/(1/j\omega C) = -j\omega RC$, which keep increasing with increasing frequency and makes the circuit oscillate. The high-frequency gain can be reduced by adding a small capacitance C' in the feedback path (see Fig. 11 (b)). The gain now becomes $A = -\dfrac{j\omega RC}{1 + j\omega RC'}$ and is limited at high frequencies[1], thus stabilising the circuit operation.

References

1. R. A. Gayakwad, "Op-amps and linear integrated circuits,"
Prentice Hall, 2000.

[1]In addition, we also need to consider the frequency response of the op amp, see [1].