Contents

Chapter 1

Semiconductor (p-n junction) diode and its cousins

We start with the basic functionality of semiconductor (p-n junction) diodes, i.e., their current-voltage (I-V) behaviour, considering both the ideal scenario and real diodes. We then analyse a simple diode circuit. Thereafter, we discuss some special types of diodes, viz., Zener diode, light emitting diode, photodiode, and solar cell. For each device, we briefly point out typical applications where it may be used.

1.1 Diode I-V relationship

A "p-n junction diode" (called simply as "diode" from now on) involves a junction of p-type and n-type semiconductor regions. In terms of basic functionality, a diode is like a check valve (see Fig. 1.1). Pressure and flow in the check valve are analogous to voltage and current, respectively, in a

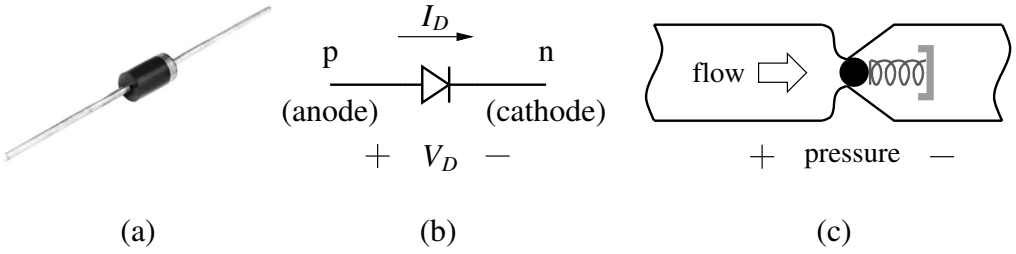


Figure 1.1: (a) typical semiconductor diode (image taken from: `stock.adobe.com`) (b) diode symbol, (c) a check valve

diode. A check vale allows water to flow if the pressure is positive and blocks flow if the pressure is negative. Similarly, a diode allows current to flow when V_D ($= V_p - V_n$ in Fig. 1.1 (b)) is positive, but blocks current (i.e., allows a negligibly small current) if V_D is negative. Note that the p and n terminals of a diode are also called anode and cathode, respectively, as shown in Fig. 1.1 (b).

A simple model which captures the basic diode behaviour is shown in Fig. 1.2 (a). When V_D is positive, the diode behaves like a small resistance R_{on}, and when it is negative, it behaves like a large resistance R_{off}. Fig. 1.2 (b) shows the I-V relationship obtained with this simple model for $R_{\text{on}} = 5\,\Omega$ and $R_{\text{off}} = 500\,\Omega$. As R_{on} is made smaller and R_{off} larger, we get the "ideal" diode behaviour (see Fig. 1.2 (c)). If V_D is negative, the diode conducts hardly any current. If V_D is positive, it allows a forward current ($I_D > 0$) with a negligible voltage drop across the device.

A more realistic diode I-V curve is shown in Fig. 1.3 (a). It is represented by the analytic

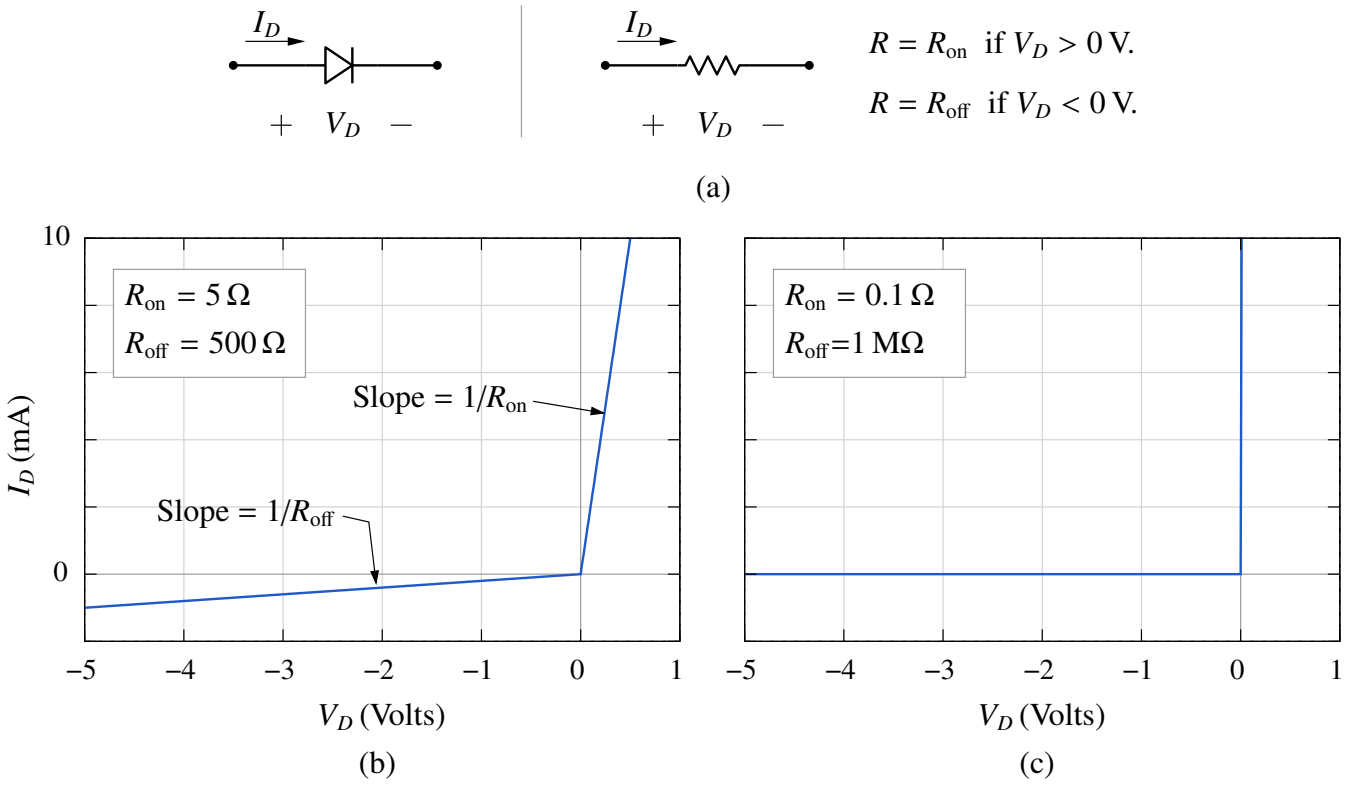


Figure 1.2: (a) R_{on}/R_{off} diode model, (b) I-V relationship for $R_{on} = 5\,\Omega$ and $R_{off} = 500\,\Omega$, (c) I-V relationship for $R_{on} = 0.1\,\Omega$ and $R_{off} = 1\,\text{M}\Omega$.

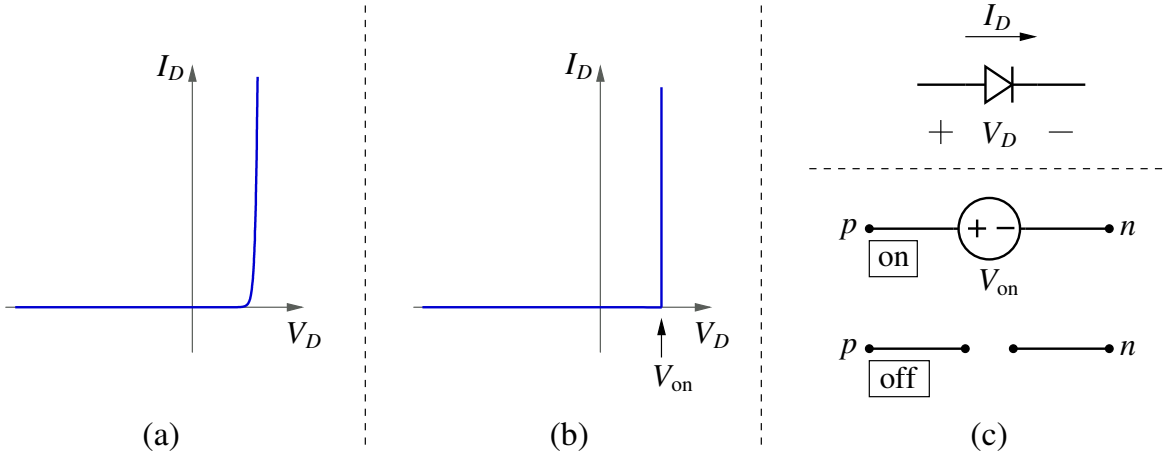


Figure 1.3: (a) I-V curve for a practical diode, (b) approximate I-V curve, (c) approximate diode model.

expression,

$$I_D = I_s\,[\exp(V_D/V_T) - 1]\,, \tag{1.1}$$

where I_s is the "saturation current" (typically about 10^{-13} A for a low-power silicon diode), and V_T is the "thermal voltage" (about 25 mV at room temperature). For a voltage of about 0.7 V, the exponential factor in Eq. 1.1 is $\exp(0.7/0.025) \approx 10^{12}$. Thus, although I_s is a very small current, the

resulting diode current at 0.7 V is in the mA range. On the other hand, for negative V_D, $\exp(V_D/V_T) \ll 1$, and Eq. 1.1 gives $I_D \approx -I_s$, which is negligibly small compared to the forward currents that the diode can carry.

As an approximation, we can replace the forward current part of the I-V curve in Fig. 1.3 (a) by a vertical line $V_D = V_{\text{on}}$ (see Fig. 1.3 (b)). For any voltage smaller than V_{on}, we can write $I_D = 0$, which gives the horizontal line in Fig. 1.3 (b). This approximation leads to the simple diode model shown in Fig. 1.3 (c).

One important point needs to be made about diode connections in a circuit. Although we have been plotting the current I_D through a diode as a function of the voltage V_D across it, a diode is never connected directly across a voltage source. This is because, for any voltage larger than V_{on} across the diode, the current I_D (see Eq. 1.1) can become so large that the diode would get excessively heated and even destroyed. Instead, we connect the diode to the voltage source through a series resistance (see Fig. 1.4) such that the current gets automatically limited. For example, if $V_{\text{on}} \approx 0.7$ V, $V_s = 5$ V, and $R = 1$ kΩ in Fig. 1.4 (b), then the current gets limited to $\dfrac{(5 - 0.7)\text{ V}}{1\text{ k}\Omega} = 4.3$ mA.

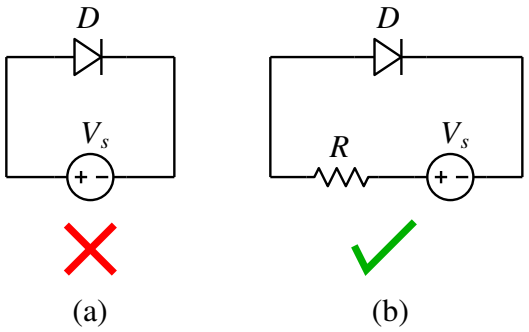


Figure 1.4: Diode connected to a voltage source directly and through a resistor.

1.2 Diode circuit example

Consider the circuit shown in Fig. 1.5. We want to find the current i_1, given $V_{\text{on}} = 0.7$ V for the diode.

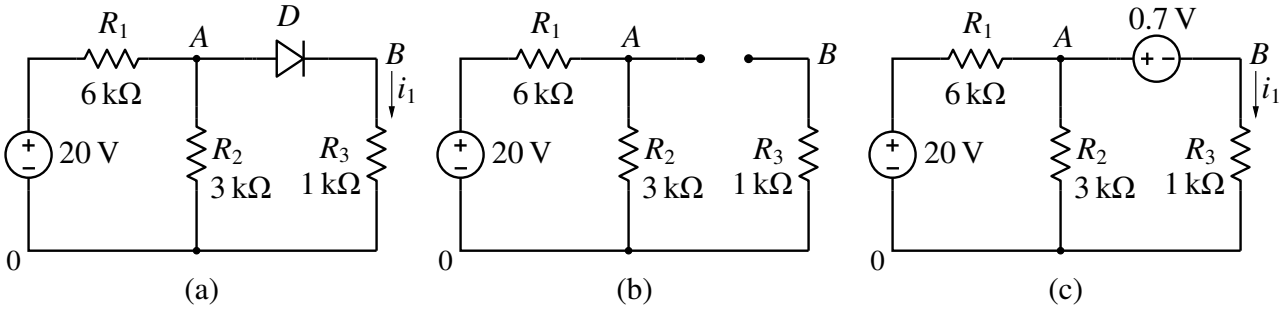


Figure 1.5: (a) Diode circuit example, (b) circuit with diode off, (c) circuit with diode on.

We first need to determine whether the diode is conducting. Let us start with the assumption that it is not conducting which means that it can be replaced with an open circuit, as shown in Fig. 1.5 (b). In this case, R_3 does not carry any current, and $V_D = V_{AB}$, the voltage across the diode is

simply the drop across R_2, viz., $V_{AB} = \dfrac{R_2}{R_1 + R_2} \times 20\,\text{V} = 6.67\,\text{V}$, a positive V_D which is larger than $V_{\text{on}} = 0.7\,\text{V}$. However, our assumption of D not conducting would imply that $V_D < V_{\text{on}}$. Clearly, this is an inconsistency, and therefore the assumption that D is off is incorrect.

Let us now try the other case in which D is on and is replaced with a voltage source $V_{AB} = V_{\text{on}} = 0.7\,\text{V}$, as shown in Fig. 1.5 (c). We can use the "nodal analysis" method, with the node marked 0 as the reference node (i.e., its node voltage is zero). We write KCL at node A as,

$$\frac{V_A - 20}{R_1} + \frac{V_A}{R_2} + \frac{V_A - 0.7}{R_3} = 0\,, \tag{1.2}$$

giving $V_A = 2.7\,\text{V}$, and $i_1 = \dfrac{V_A - 0.7}{R_3} = 2\,\text{mA}$. This is a *forward* current since its direction is from the p terminal to the n terminal of the diode. In other words, the current we have obtained is consistent with the assumption that D is conducting.

1.3 Breakdown voltage

In our discussion so far, we have assumed that a diode can block arbitrarily large reverse voltages (negative V_D), i.e., it conducts a negligibly small current for any negative voltage. A practical diode, however, "breaks down" at some point as the reverse voltage is increased, i.e., it conducts significantly large currents limited only by the external circuit. A diode I-V curve with reverse breakdown is shown in Fig. 1.6. The breakdown voltage V_{BR} is generally expressed as a positive number. For example, a diode that breaks down at an applied voltage $V_D = -10\,\text{V}$ is said to have $V_{BR} = 10\,\text{V}$.

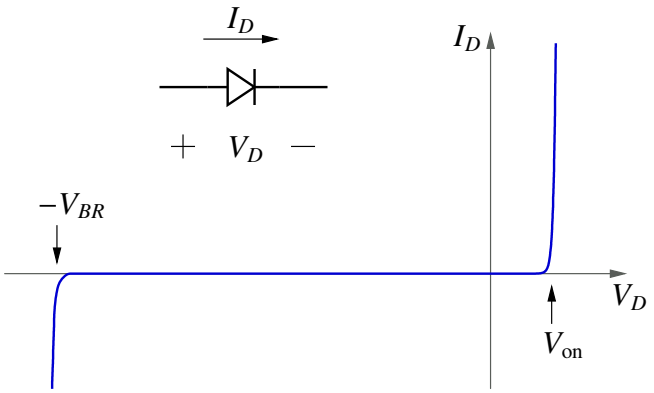


Figure 1.6: Diode I-V curve showing reverse breakdown.

In a large number of application – with some exceptions to be discussed shortly – diode circuits are designed such that the reverse voltage across the diode is less than its V_{BR} rating. Diodes with a wide range of V_{BR} rating, from a few Volts (in low-power electronics) to thousands of Volts (in power electronics), are commercially available.

A "Zener diode" (see Fig. 1.7) is designed for a certain breakdown voltage, denoted by V_Z, and it is generally operated in the reverse breakdown region of the I_D-V_D curve, with $V_D = -V_Z$.

Fig. 1.7 (b) shows a simple voltage regulator using a Zener diode. An input voltage $V_{\text{in}} > V_Z$ is applied to the regulator. A load resistance R_L is connected at the output, which draws a "load

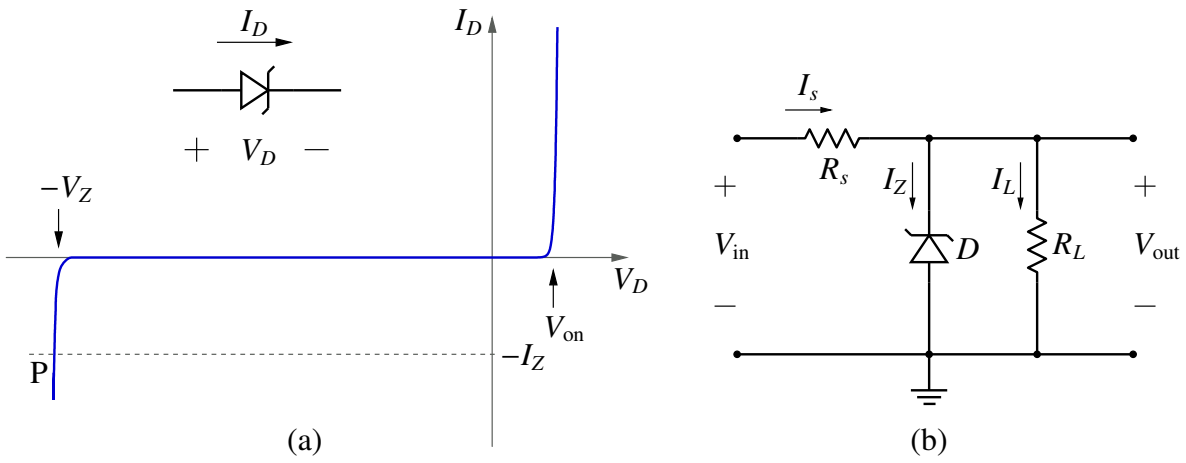


Figure 1.7: (a) Zener diode I-V curve, (b) a simple regulator circuit using a Zener diode.

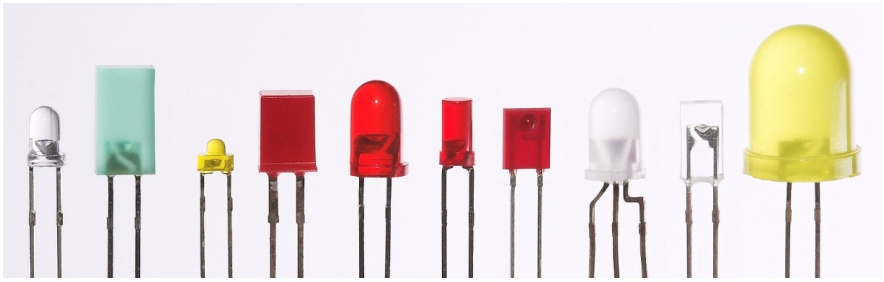
current" I_L. The purpose of a voltage regulator is to maintain a constant (dc) output voltage V_{out} even if there are some variations in V_{in} and I_L. As long as we ensure that the Zener diode operates in the breakdown region, we can say that it has a drop of $V_D = -V_Z$ across it, and $V\text{out} \approx V_Z$ is maintained. Note that the current I_Z represents a *reverse* current through the diode. In other words, the operating point for the Zener diode in the V_D-I_D plane (see Fig. 1.7 (a)) is P given by $(-V_Z, -I_Z)$. Since the Zener diode maintains the same voltage ($V_D = -V_Z$) for a wide range of I_Z, the output voltage remains equal to V_Z even if V_{in} or I_L changes, as long as $I_Z = \left(\dfrac{V_{\text{in}} - V_Z}{R_s}\right) - I_L$ remains positive.

1.4 Light emitting diodes (LEDs)

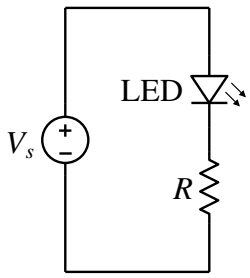
LEDs (see Fig. 1.8) are p-n junction diodes made from semiconductors such as GaAs, AlGaAs, InP, GaN, which can emit light with a wavelength specific to that semiconductor. For an LED to emit light, it must be biased in forward conduction. A larger forward current gives a higher intensity of the emitted light. The I-V curve of an LED would be similar to that of a diode (see Fig. 1.6). However, V_{on} for an LED would be different than that of a silicon diode. Consider the circuit shown in Fig. 1.8 (b) with $V_s = 5$ V. If the LED has $V_{\text{on}} = 2$ V, then to drive a current of 1 mA through the LED, we will choose $R = \dfrac{(5-2)\text{ V}}{1\text{ mA}} = 3\,\text{k}\Omega$.

LEDs are used for several applications:

1. Display: In this category, we have
   (a) single LED indicators of various colours and shapes (see Fig. 1.8 (a))
   (b) 7-segment LED numeric displays
   (c) alphanumeric displays in laboratory instruments
2. White LEDs for lighting: LED bulbs (see Fig. 1.8 (c)) are attractive in terms of efficiency. A typical LED bulb operates at a light conversion efficiency of 60%. In comparison, incandescent bulbs are only 5 to 12% efficient, and compact fluorescent bulbs are 27% efficient.
3. video displays (laptop, PC), and large LED display screens (see Fig. 1.8 (d)).



(a)



(b)

(c)

(d)

Figure 1.8: (a) LEDs in different packages (source: wikipedia), (b) circuit to drive an LED, (c) LED lamp with internal details (source: wikipedia), (d) LED display (image taken from: `metabranding.in`)

1.5 Photodiodes and solar cells

The principle of operation of photodiodes and solar cells is illustrated in Fig. 1.9. Light incident on the photodiode or solar cell results in a downward shift of the I-V curve. Higher the light intensity, larger this shift. In a photodiode, our interest is in detecting this current shift, whereas in a solar cell, we are interested in getting power out of the device.

1.5.1 Photodiodes

A photodiode (see Fig. 1.10) operates in the third quadrant of the I_D-V_D plot of Fig. 1.9. In other words, it is biased with a negative V_D (see Fig. 1.10 (b)). Light shines on the device through the transparent window of the package and causes a change in I_D, thus a light signal is converted into an electrical signal. A photodiode is used in the following applications:

1. Optical fibre communications: A photodiode is used at the receiver side for detecting optical signals arriving from the fibre.

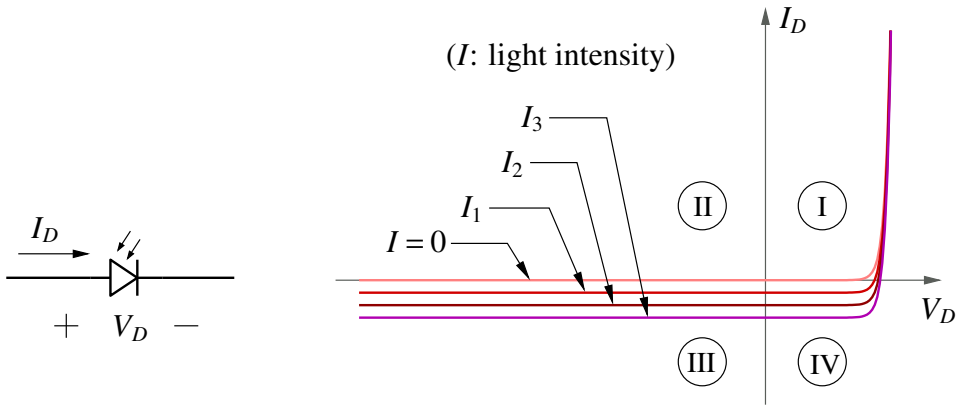
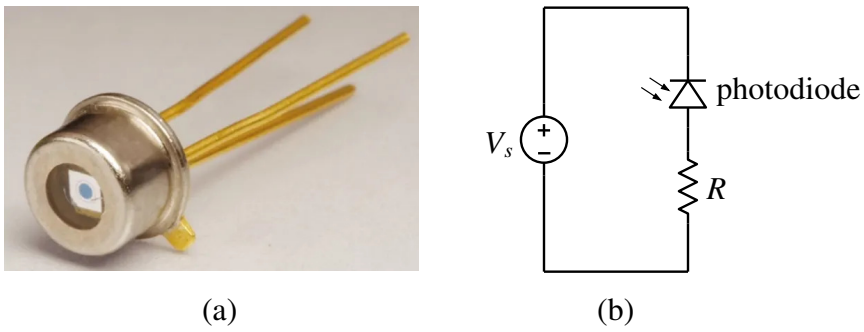


Figure 1.9: *I*-*V* characteristics for photodiodes and solar cells for different values of light intensity: $0 < I_1 < I_2 < I_3$.



(a) (b)

Figure 1.10: (a) a photodiode (image taken from: `uk.rs-online.com`) (b) simple circuit to show how a photodiode is biased.

2. Remote control of appliances: A combination of LED (on the TV remote, for example) and a photodiode (on the TV panel) is used for remote control.

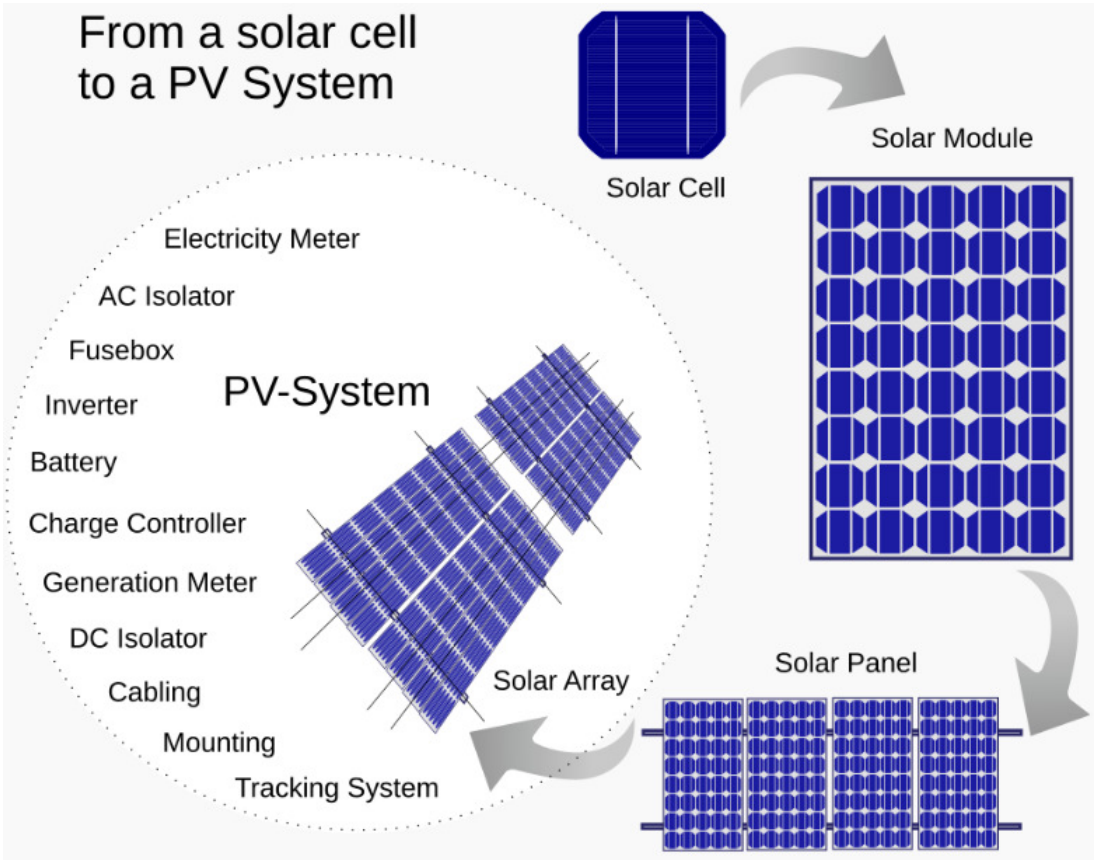
3. Obstacle detection: An LED/photodiode pair is used to detect if the path of light from the LED to the photodiode is blocked by an object, e.g., in a lift door.

Photodiodes can be characterised in terms of sensitivity (what is the smallest light intensity it can detect?), switching speed (how fast can it respond?), and spectral bandwidth (which light wavelengths does it detect?). The figure of merit for a photodiode depends on the application. In a burglar alarm, the photodiode does not need to switch in a nanosecond, so speed is not as important as sensitivity. In optical communications, on the other hand, a photodiode is called upon to detect signals with frequencies in the GHz range, so its switching speed is very important.

1.5.2 Solar cells

A solar cell (see Fig. 1.11) operates in the fourth quadrant of the I_D-V_D plot of Fig. 1.9, the reason being simple – in the fourth quadrant, $I_D < 0$ and $V_D > 0$ (i.e., a forward bias), and the power consumed by the device $P = V_D \times I_D$ is negative. In other words, a solar cell *generates* power, and that is exactly what we want. Solar cells are generally made from silicon due to its low cost.

However, when a higher efficiency is a priority, as in space applications, solar cells made from compound semiconductors may be used.



(a)

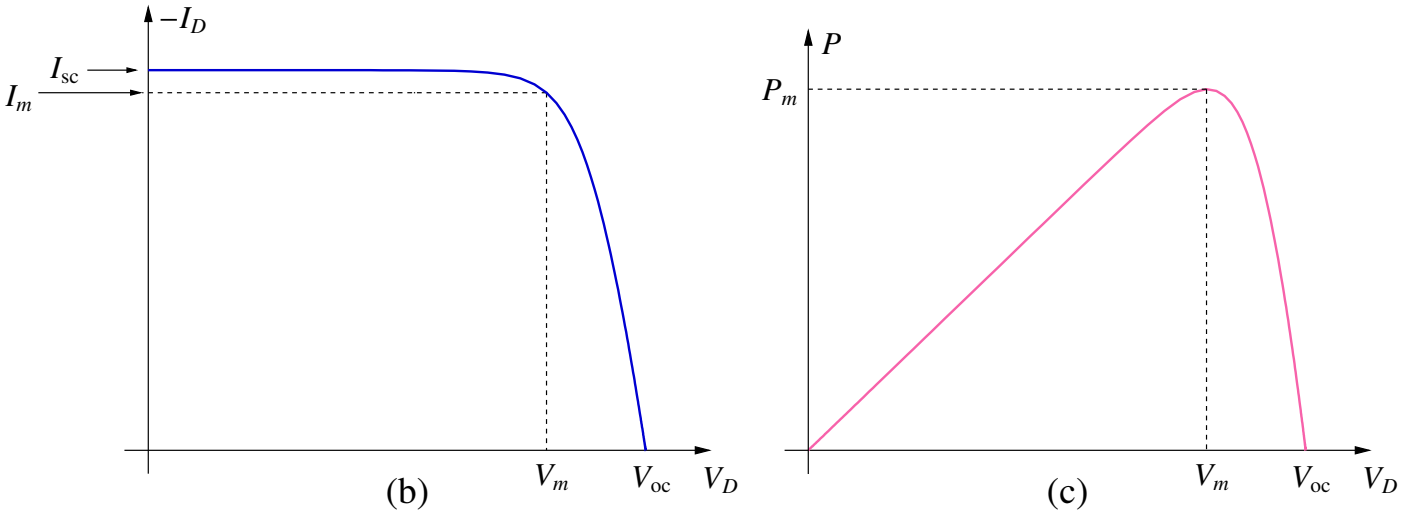


Figure 1.11: (a) Making up a PV (photovoltaic) system (image from wikipedia) (b) *I*-*V* curve and (c) *P*-*V* curve of a solar cell

It is customary to plot the I-V curve of a solar cell with the reverse current (i.e., $-I_D$) taken as positive, as shown in Fig. 1.11 (b). With this change, the fourth quadrant of Fig. 1.9 gets mapped to the first quadrant of Fig. 1.11 (b). When the voltage across the cell is zero, the current it carries is denoted by I_{sc} (short-circuit current). When the current through the cell is zero, the voltage across it is denoted by V_{oc} (open-circuit voltage). The product $P = V \times I$ gives the power generated by the solar cell. P is zero when V or I is zero (see Fig. 1.11 (c)), and at $V = V_m$, it reaches its maximum value $P_{\max}$. As specifications of the solar cell, manufacturers provide I_{sc}, V_{oc}, V_m, $P_{\max}$ at certain atmospheric conditions and temperature. A typical polycrystalline solar cell of size $15.6\,\text{cm} \times 15.6\,\text{cm}$ has $P_{\max}$ of about 4 W.

Chapter 2

Diode rectifiers

For several electronic circuits, a DC power supply typically in the range 5 V to 20 V (sometimes with both polarities, e.g., ±15 V) is required. Since the domestic supply available is an AC voltage (230 V rms, 50 Hz), a conversion from AC to DC is necessary. A diode rectifier can be used for this conversion. [1] In a diode rectifier (see Fig. 2.1), a step-down transformer is used to convert the AC mains voltage from 230 Vrms to a suitable low level, giving, for example, $V_{AB} = 10 \sin \omega t$ V. A

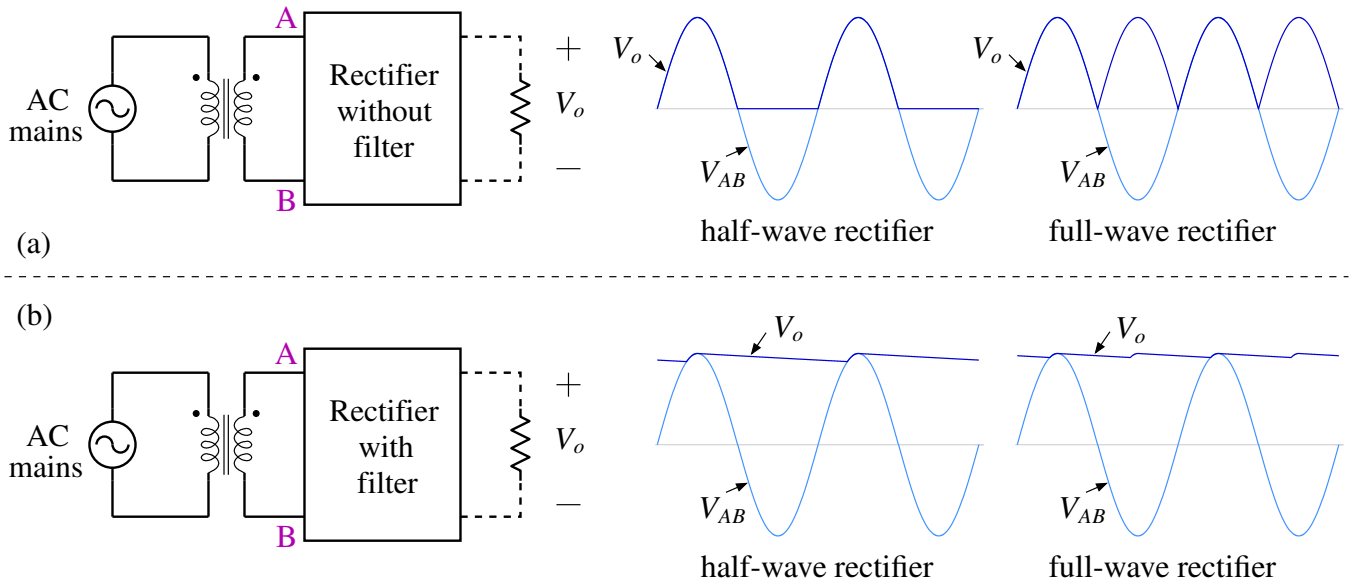


Figure 2.1: Schematic diagram illustrating the functioning of a rectifier: (a) without filter and (b) with filter.

rectifier without a filter (see Fig. 2.1 (a)) either removes the negative half of the stepped-down AC voltage or inverts it (i.e., makes it positive), thus resulting in an output voltage that has a positive average value. Our final goal of course is *not* a time-varying voltage with a positive average value but a *constant* (DC) voltage. With an appropriate filter, a DC output voltage can be produced, as shown in Fig. 2.1 (b). A close examination of Fig. 2.1 (b) reveals that there is a small "ripple" in the output voltage, which is undesirable. This ripple can be eliminated by using a "voltage regulator" circuit. Later in this chapter, we will look at a commercial voltage regulator IC.

[1] Apart from diode rectifiers, switched-mode power supplies (SMPS) are also used to obtain a DC voltage from the AC mains supply (e.g., in a PC). However, we will not discuss SMPS's in this course.

2.1 Rectifier circuits without a filter

A rectifier circuit without a filter can be used to convert a sinusoidal input voltage (with average value zero, such as V_{AB} in Fig. 2.1) into an output voltage with a positive average value. We have two type of circuits in this category: half-wave and full-wave.

2.1.1 Half-wave rectifier

Fig. 2.2 (a) shows the circuit diagram for a half-wave rectifier. The AC mains voltage is stepped down through the transformer, leading to the simplified circuit of Fig. 2.2 (b). The turn-on voltage of the diode is denoted by V_{on}. Fig. 2.2 (c) shows how V_o varies with V_s. If $V_s < V_{\text{on}}$, the diode is off, there is no current through the resistor, and we have $V_o = 0$ V. If $V_s > V_{\text{on}}$, the diode conducts, with $V_D = V_{\text{on}}$, and we have $V_o = V_s - V_{\text{on}}$, a straight line in the V_s-V_o plane with slope equal to 1.

Fig. 2.2 (d) shows V_s and V_o versus time. Note that, when the diode is on, $V_o(t)$ is displaced from $V_s(t)$ by V_{on} as we would expect since, during this interval, we have $V_o = V_s - V_{\text{on}}$. As can be seen from the figure, only half of the AC cycles result in a positive output voltage; hence, the name "half-wave" rectifier.

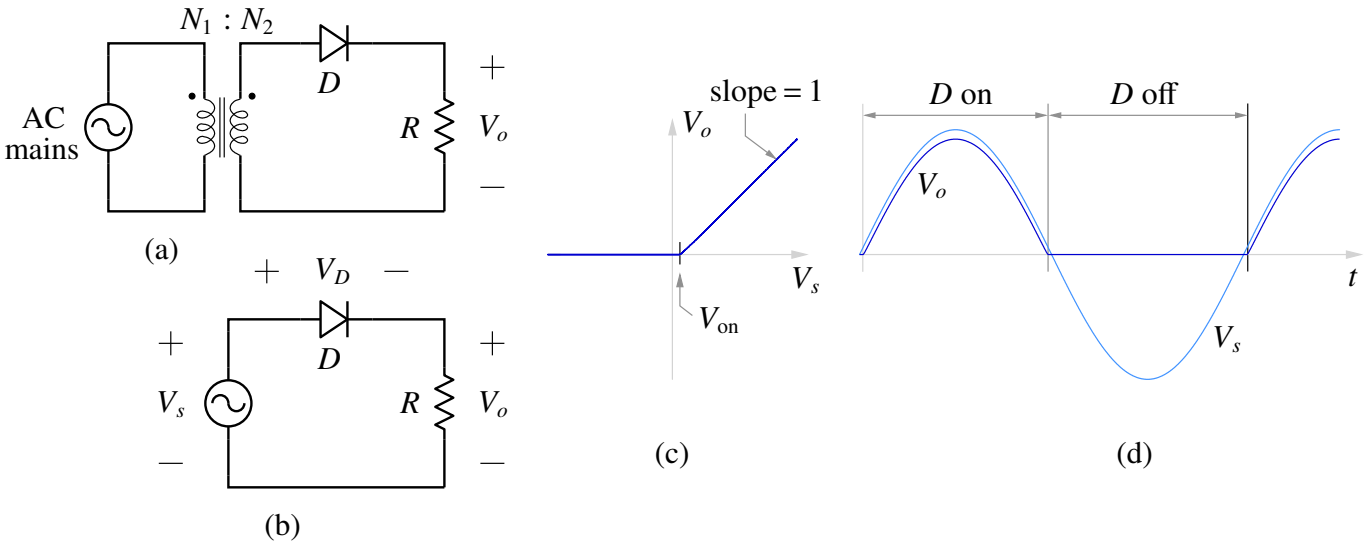


Figure 2.2: (a) Circuit diagram of a half-wave rectifier, (b) simplified circuit diagram, (c) V_o versus V_s, and (d) V_s (light blue) and V_o (dark blue) versus time.

2.1.2 Full-wave (bridge) rectifier

The bridge rectifier, shown in Fig. 2.3 (a), is a full-wave rectifier, i.e., it produces an output voltage with a positive average value in both half cycles of the input AC voltage. The circuit of Fig. 2.3 (a) is redrawn in Figs. 2.3 (b) and 2.3 (c) to illustrate the functioning of the bridge rectifier.

When $V_s > 2\,V_{\text{on}}$ (see Fig. 2.3 (b)), diodes D_1 and D_2 conduct (with $V_D = V_{\text{on}}$ for each of them), and the current through the load resistance flows from P to Q. The output voltage is $V_o(t) = V_s(t) - 2\,V_{\text{on}}$. During this time, diodes D_3 and D_4 see a reverse bias and therefore do not conduct.

When $V_s < -2\,V_{\text{on}}$ (see Fig. 2.3 (c)), diodes D_3 and D_4 conduct (with $V_D = V_{\text{on}}$ for each of them). The current through the load resistance flows from P to Q in this case as well. The output voltage is $V_o(t) = -V_s(t) - 2\,V_{\text{on}}$, which is positive. Since the output voltage is positive in both half cycles, the circuit is called a "full-wave" rectifier.

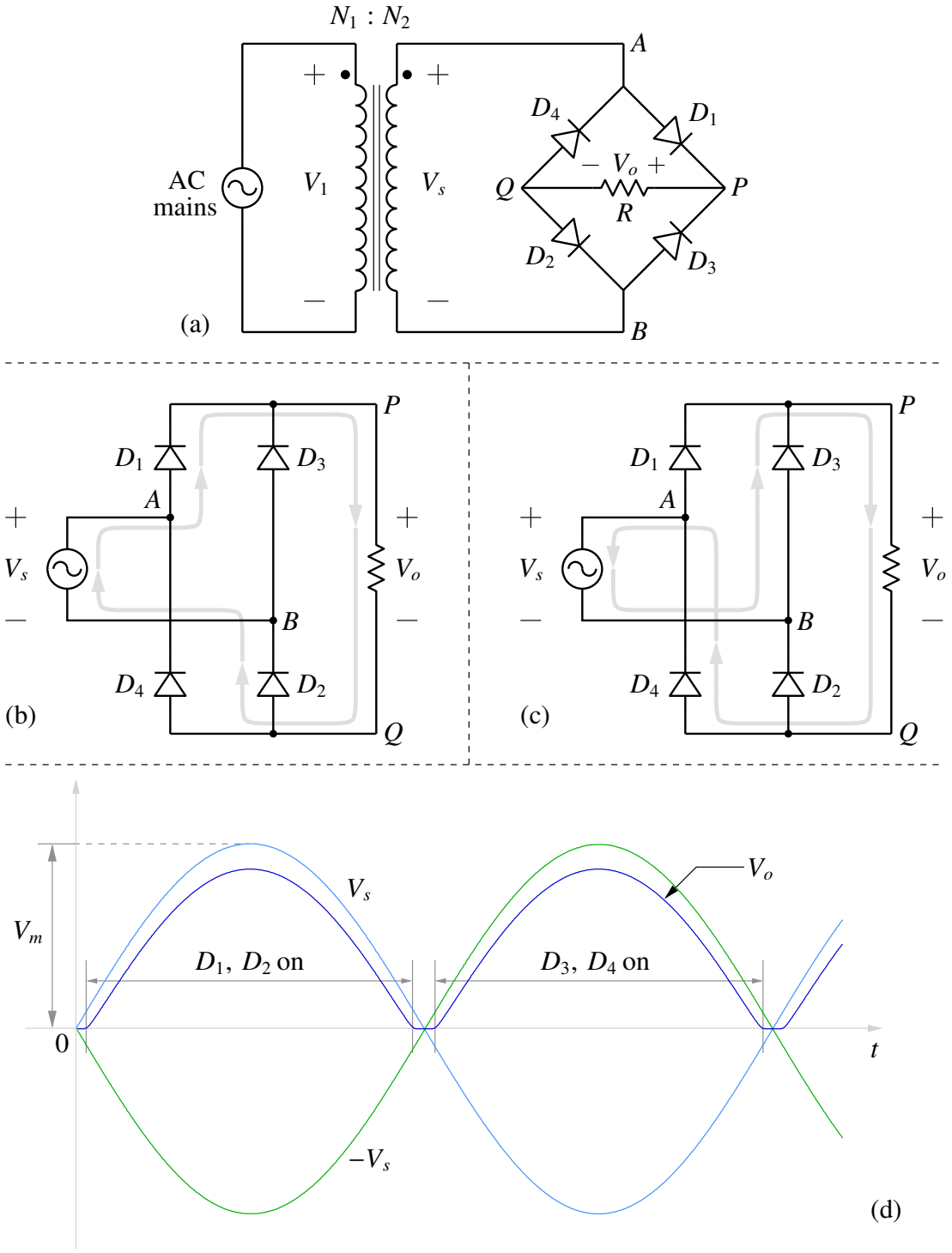


Figure 2.3: (a) Circuit diagram of a full-wave bridge rectifier, (b) current path in the positive half cycle ($V_A > V_B$), (c) current path in the negative half cycle ($V_A < V_B$), and (d) V_s, $-V_s$, and V_o versus time.

2.2 Rectifier circuits with a capacitor filter

The half-wave and full-wave rectifier circuits of Sec. 2.1 produce a time-varying output voltage with an average positive value; however, for a dc power supply, what we need is a *constant* (dc) voltage. The circuits described in this section represent one step in that direction. They produce an output voltage which is *almost* constant, as we will see.

Let us begin with the "peak detector" circuit shown in Fig. 2.4 (a), with $V_s(t) = V_m \sin \omega t$. For

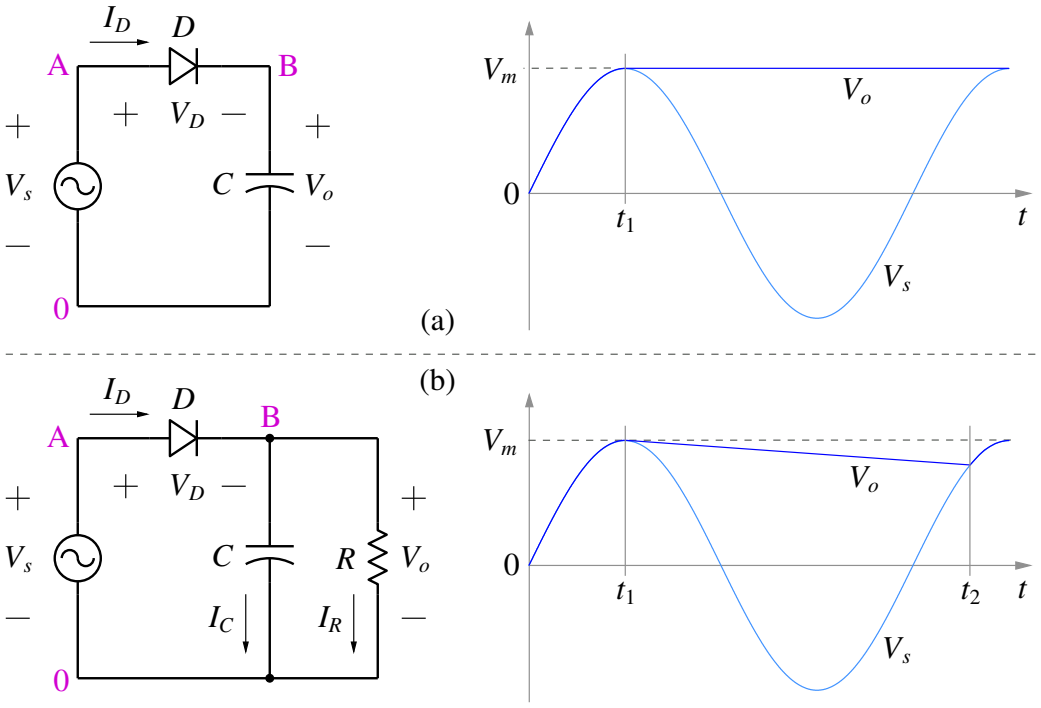


Figure 2.4: Peak detector circuit and associated waveforms: (a) with no load, (b) with a resistor load. The diode is assumed to be ideal, with $V_{\text{on}} = 0$ V.

simplicity, we will consider V_{on} to be 0 V for the diode. Let the capacitor voltage $V_C = V_o = 0$ V initially. Treating the node marked "0" as the reference node, with node voltage of 0 V, we have $V(p) = V_A = V_s$, and $V(n) = V_B = V_o$ at the two ends of the diode. As V_s starts increasing at $t = 0$, $V(p)$ increases, thus making $V(p)$ greater than $V(n)$ for the diode, and the diode starts conducting. The capacitor gets charged. The time constant of this charging process is given by $R_{\text{on}} C$ where R_{on} is the on resistance of the diode, a very small resistance. The charging process is therefore almost instantaneous, which means that $V_o(t)$ simply follows $V_s(t)$, without any delay, as shown in Fig. 2.4 (a).

At $t = t_1$, $V(n) = V_o$ has reached V_m, the maximum value of $V_s(t)$. Subsequently, $V(p) = V_s$ falls below V_m. Since $V(p) - V(n)$ is now negative, the diode sees a reverse bias and stops conducting. Since there is no current in the circuit, the capacitor charge remains constant at its value at $t = t_1$, and V_o remains equal to V_m. The circuit has detected the peak (V_m) of the input waveform and is therefore called the "peak detector."

Although the peak detector of Fig. 2.4 (a) produces a constant output voltage, it is not useful as a power supply. What we want a power supply to do is to provide current to a load (e.g., a resistor).

When a resistive load is connected to the peak detector (see Fig. 2.4 (b)), the circuit operation changes considerably. As with the peak detector, V_o reaches V_m at $t = t_1$, and the diode turns off subsequently since it gets reverse biased. However, the capacitor does have a discharge path available in this case, viz., the resistor. As a result, the capacitor charge – and therefore the capacitor voltage V_o – starts decreasing, as shown in the figure. This goes on up to $t = t_2$ at which point $V(p)$ of the diode becomes greater then $V(n)$, and the capacitor gets charged again through the diode. The circuit of Fig. 2.4 (b) is our half-wave rectifier with a capacitor filter, which we now look at in more detail.

2.2.1 Half-wave rectifier with capacitor filter

Fig. 2.5 shows the half-wave rectifier circuit with a capacitor filter, along with the associated voltage and current waveforms in the (periodic) steady state, assuming the diode to be ideal, with $V_{\text{on}} = 0$ V. Let $V_s(t) = V_m \sin \omega t$. In the interval marked T_c, the diode conducts, and the capacitor gets charged. In the rest of the period (of duration $T - T_c$), the diode is off, and the capacitor discharges through the load resistor, making the capacitor current negative in this interval, as seen in Fig. 2.5 (c). The charging interval is much smaller than the discharging interval. During any given period T, the amount of charge gained by the capacitor must be equal to the amount of charge lost. Because the charging process has a much shorter duration as compared to the discharging process, it follows that the charging current would be much larger than the discharging current.

Since the output voltage (V_o) decreases due to capacitor discharge, the V_o waveform in Fig. 2.5 (c) shows a "ripple" voltage given by

$$V_R = V_m \frac{T}{RC}, \tag{2.1}$$

where V_m is the amplitude of the AC voltage V_s. The ripple voltage can be reduced by increasing C. However, this would increase the size and cost of the capacitor. In addition, it makes the peak diode current substantially larger.

The average diode current is $I_D^{\text{avg}} \approx \frac{V_m}{R}$. The maximum reverse bias that appears across the diode is about $2\,V_m$ (see Fig. 2.5 (c)). The diode for this circuit must be selected such that its ratings like average current, peak current, and peak inverse voltage are not exceeded when connected in the circuit.

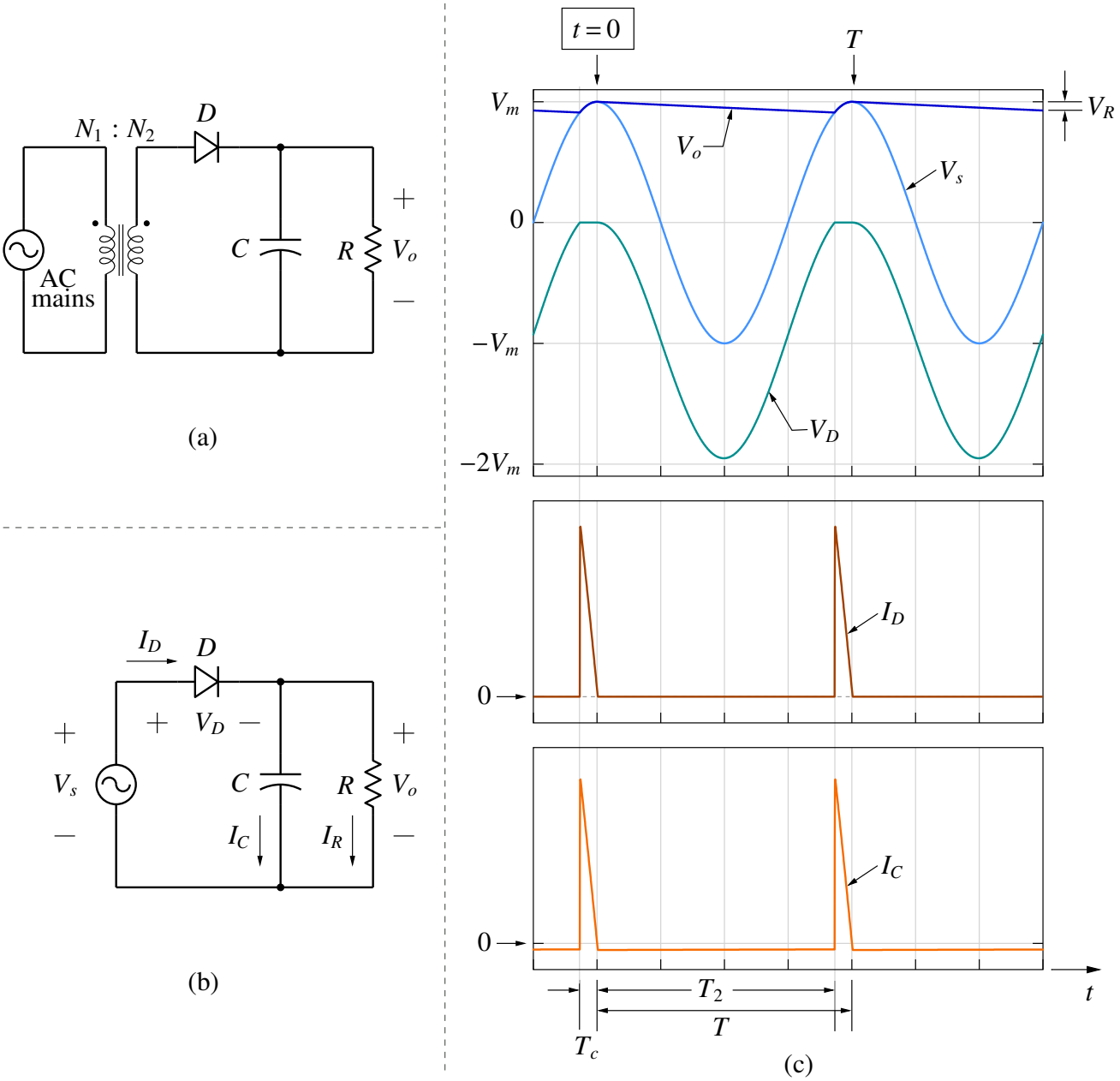


Figure 2.5: (a) Circuit diagram of a half-wave rectifier with a capacitor filter, (b) simplified circuit diagram, (c) voltage and current waveforms. ($V_{\text{on}} \approx 0$ is used for the diode.)

2.2.2 Full-wave (bridge) rectifier with capacitor filter

Fig. 2.6 shows the full-wave bridge rectifier circuit with a capacitor filter, along with the associated voltage and current waveforms in the (periodic) steady states. The diodes are assumed to be ideal, with $V_{\text{on}} = 0$ V. In the interval marked T_{c1}, diodes D_1 and D_2 conduct, with the current path shown in Fig. 2.6 (a). In the interval marked T_{c2}, diodes D_3 and D_4 conduct, with the current path shown in Fig. 2.6 (b). During the remaining time interval (of duration $T - T_{c1} - T_{c2}$ in one period), none of the diodes conduct, and the capacitor discharges through the load resistor, thus causing a droop in V_o. In many ways, the circuit operation is similar to that of the half-wave rectifier of Sec. 2.1.1; the main

difference is that the charging and discharging of the capacitor happens *twice* in each cycle in the full-wave rectifier.

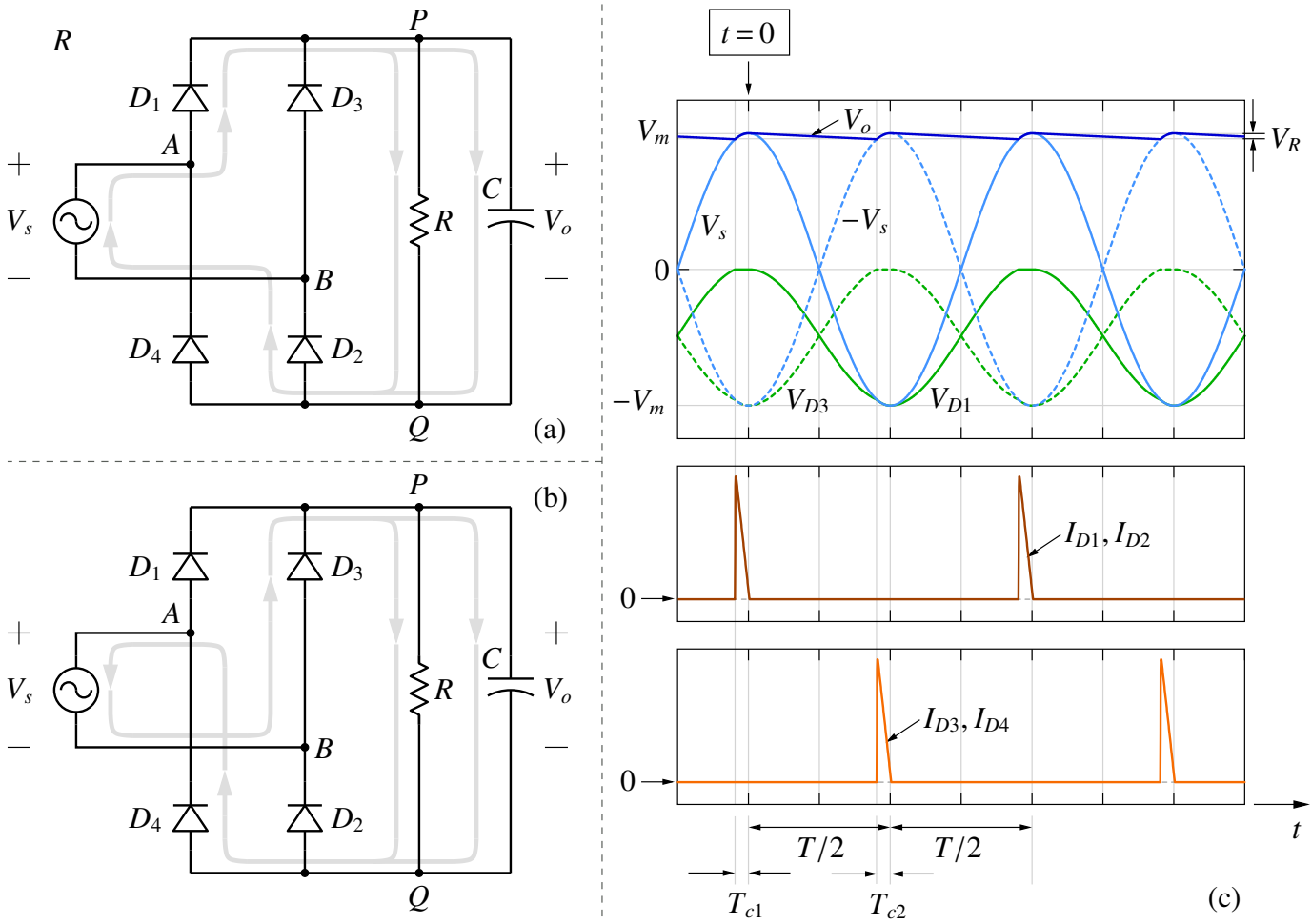


Figure 2.6: Bridge rectifier with a capacitor filter: (a) circuit diagram with D_1 and D_2 conducting, (b) circuit diagram with D_3 and D_4 conducting, (c) voltage and current waveforms. ($V_{on} = 0$ is used for the diodes.)

For the same dc value of the output voltage V_{DC}, ripple voltage V_R, and load resistance R, Table 2.1 compares the capacitance, average diode current rating, and peak inverse voltage rating for the diode. The advantage of using the bridge rectifier can be clearly seen from this table.

Table 2.1: Comparison of rectifier configurations

	Half-wave	Bridge
C	$\frac{V_{DC}}{V_R}\frac{T}{R}$	$\frac{1}{2}\frac{V_{DC}}{V_R}\frac{T}{R}$
I_D^{av}	$\frac{V_{DC}}{R}$	$\frac{1}{2}\frac{V_{DC}}{R}$
PIV	$2V_{DC}$	V_{DC}

2.3 Regulated power supply

The rectifier circuits discussed in Sec. 2.2 have the following limitations:

1. Any change in the amplitude of the input voltage (V_m) causes the output voltage to change.
2. The output voltage also changes with the load current. For example, if the load resistance R in Fig. 2.6 is reduced, it draws a larger load current, thus causing the ripple voltage to change.
3. The ripple in the output voltage can be reduced by increasing the filter capacitance. However, that causes a large change in the peak diode current. If the peak current rating of the diode is exceeded, the diode can get damaged.

To address the above limitations, a "voltage regulator" is used, as shown in the block diagram of Fig. 2.7. As input, the voltage regulator takes the output voltage of the rectifier and produces a constant (dc) voltage at its output (where the load is connected). For proper operation, the input voltage of the regulator is expected to be larger (typically by 2 to 3 V) than its output voltage. A capacitor (C in Fig. 2.7), typically about 1 μF, is connected at the output of the voltage regulator for stability, i.e., to prevent oscillations which can potentially arise because of negative feedback employed within the regulator IC.

The following figures of merit[2] are used to describe voltage regulators.

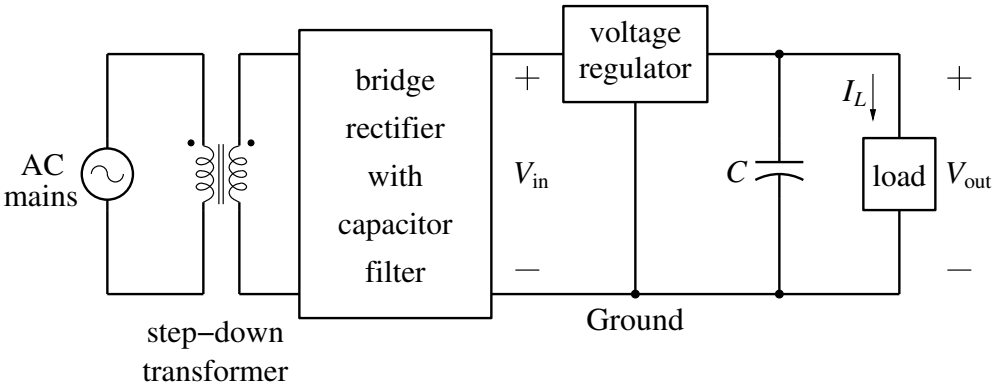


Figure 2.7: Schematic diagram of a regulated power supply.

[2] source: wikipedia

1. "Line regulation" is the ability of a power supply to maintain a constant output voltage despite changes to the input voltage, with the output current drawn from the power supply remaining constant. In the datasheets for voltage regulators, line regulation is expressed as,

$$\text{Line Regulation} = \frac{1}{V_o}\frac{\Delta V_o}{\Delta V_i} \times 100\% \ /\text{V}, \tag{2.2}$$

   where ΔV_o is the change in the output voltage of the regulator when the input voltage changes by ΔV_i. Typically, Line Regulation of voltage regulator ICs is about 0.05%/V.

2. "Load regulation" is the ability of a power supply to maintain a constant output voltage despite changes in the load (such as a change in load resistance) and is expressed as,

$$\text{Load Regulation} = \frac{V_o^{\text{min-load}} - V_o^{\text{max-load}}}{V_o^{\text{nom-load}}} \times 100\%, \tag{2.3}$$

   where

   (a) $V_o^{\text{max-load}}$ is the output voltage when the load current is maximum.

   (b) $V_o^{\text{min-load}}$ is the output voltage when the load current is minimum.

   (c) $V_o^{\text{nom-load}}$ is the output voltage when the load current is equal to the nominal (typical) value specified by the manufacturer.

Fig. 2.8 shows the circuit connections, pin diagram, and the internal circuit of the voltage regulator IC 7812, which is used to get a constant 12 V output voltage. Its input voltage can be in the range 14.5 V to 30 V, and it can supply a load current of up to 1 A.

Some other commonly used voltage regulators are

(a) Positive voltage output: 7805 (5 V), 7806 (6 V), 7809 (9 V).

(b) Negative voltage output: 7905 (−5 V), 7906 (−6 V), 7909 (−9 V). 7912 (−12 V).

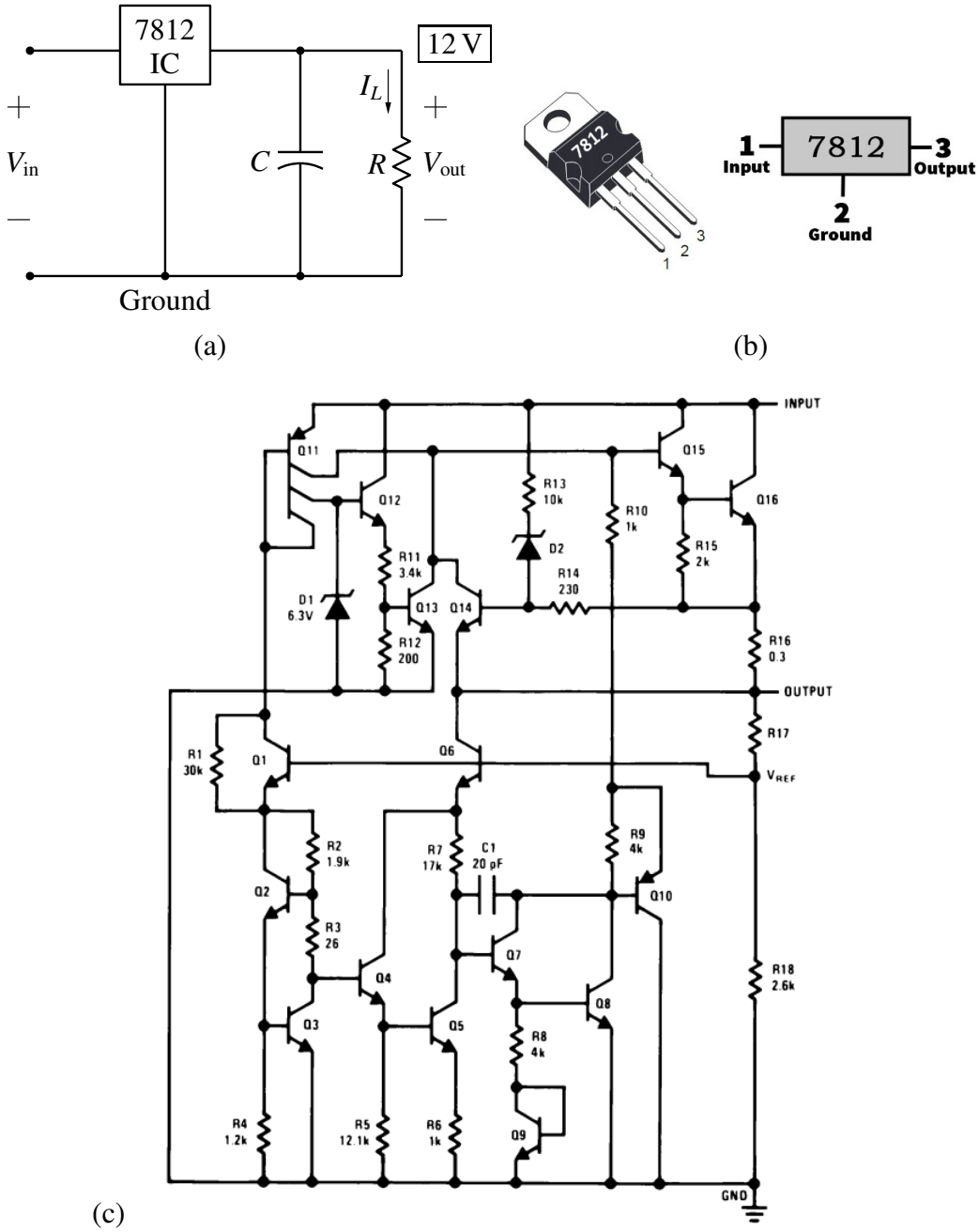


Figure 2.8: Voltage regulator IC 7812: (a) circuit connections, (b) package and pin diagram, (c) internal details of the IC.

Chapter 3

Op-Amp Circuits

3.1 Introduction

The Operational Amplifier (op-amp) is a versatile building block useful for implementing various functions, such as addition or subtraction of voltages, integration, conversion of a current signal to a voltage signal, etc. Fig. 3.1 (a) shows the commonly used "741" op-amp dual-in-line package (DIP). The notch at one end of the package serves as a reference for pin 1 which is on the left of the notch in the top view. Fig. 3.1 (b) shows the pin diagram for op-amp 741. In your experiments, the following pins are used: non-inverting input (3), inverting input (2), output (6), V^+ (7), and V^- (4). Note that there is no "ground" pin. Fig. 3.1 (c) shows the op-amp symbol with the power supply connections V^+ and V^-. Typically, the power supply connections are not shown explicitly in circuit diagrams – to avoid clutter – and the simplified symbol shown in Fig. 3.1 (d) is used.

The internal circuit of op-amp 741 is shown in Fig. 3.1 (e). Although the op-amp is very complex internally, it can be represented with a simple equivalent (to be discussed in Sec. 3.2). This means that the user can generally carry out circuit design without a thorough knowledge of the intricate details of an op-amp. This makes the design process simple.

We note the following points about Fig. 3.1 (e) which are relevant in understanding how op-amp circuits work.

1. The input terminals of the op-amp (marked as "non-inverting input" and "inverting input" in Fig. 3.1 (e)) are connected to base terminals of transistors Q1 and Q2. The base currents are generally negligibly small compared to other relevant currents in op-amp circuits, thus allowing us to treat them as zero.

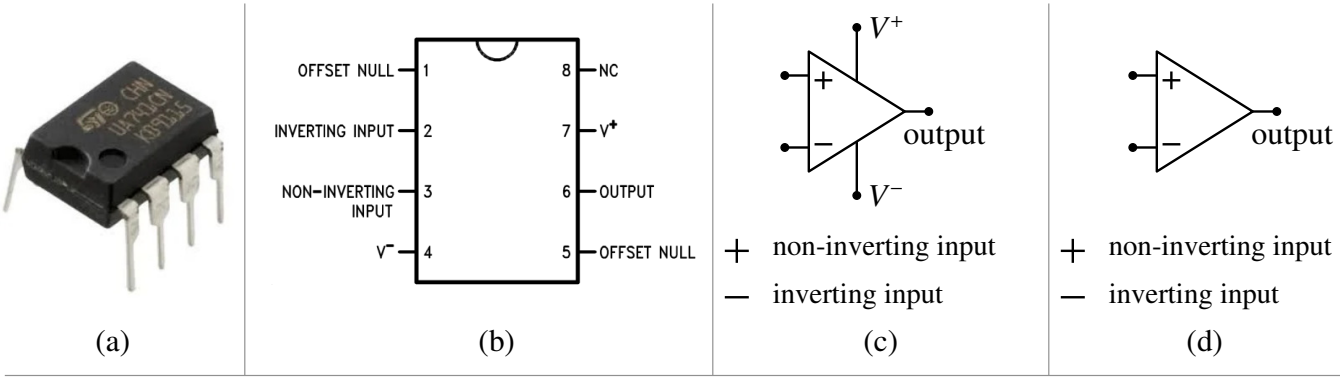
2. When a current flows from the op-amp into an external component connected to the "output" pin, it is carried by transistor Q14. In this case, we say that the op-amp is "sourcing" a current.

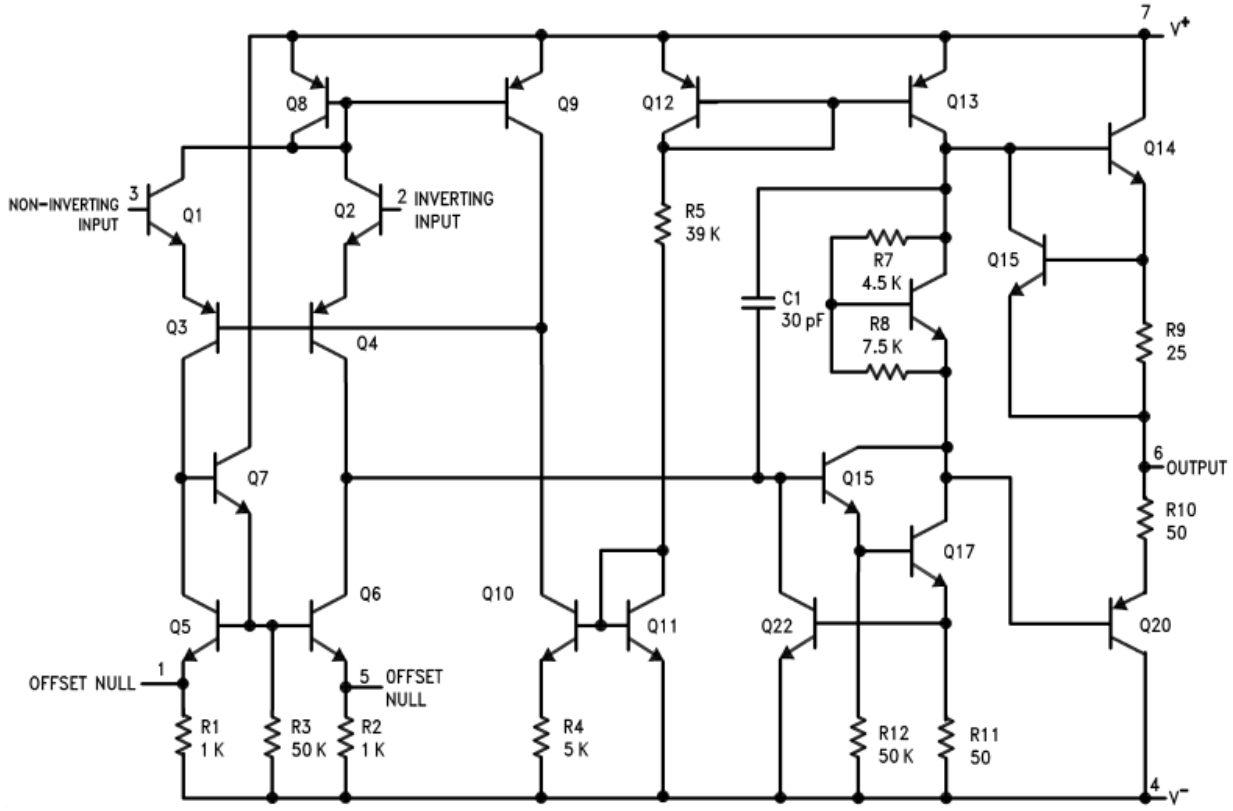
3. When a current flows into the op-amp from the "output" pin, it is carried by transistor Q20, and we say that the op-amp is "sinking" a current.

   Op-amp 741 can source or sink up to 25 mA.

4. All ICs require one or more power supplies to be externally connected. For op-amp 741, two voltage sources need to be connected to the V^+ and V^- terminals, as shown in Fig. 3.2 (a), with V_{CC} and V_{EE} both being positive. What it means is that, with respect to ground, the V^+ pin would be at $+V_{CC}$, and the V^- pin at $-V_{EE}$.

Typically ±15 V supplies are used with 741; however, the 741 specs allow ±10 V to ±18 V.[1]





(e)

Figure 3.1: Op-Amp 741: (a) package (from `www.makestore.in`), (b) pin diagram (from `www.ti.com`), (c) symbol with power supply connections included, (d) simplified symbol, (e) internal circuit (from `www.ti.com`).

3.2 Op-amp equivalent circuit

Fig. 3.2 (b) shows the equivalent circuit of the op-amp, assuming that power supply connections are made, as shown in Fig. 3.2 (a). Between the inverting and non-inverting input terminals, we have a

[1] Some op-amps work with a single supply, e.g., 5 V.

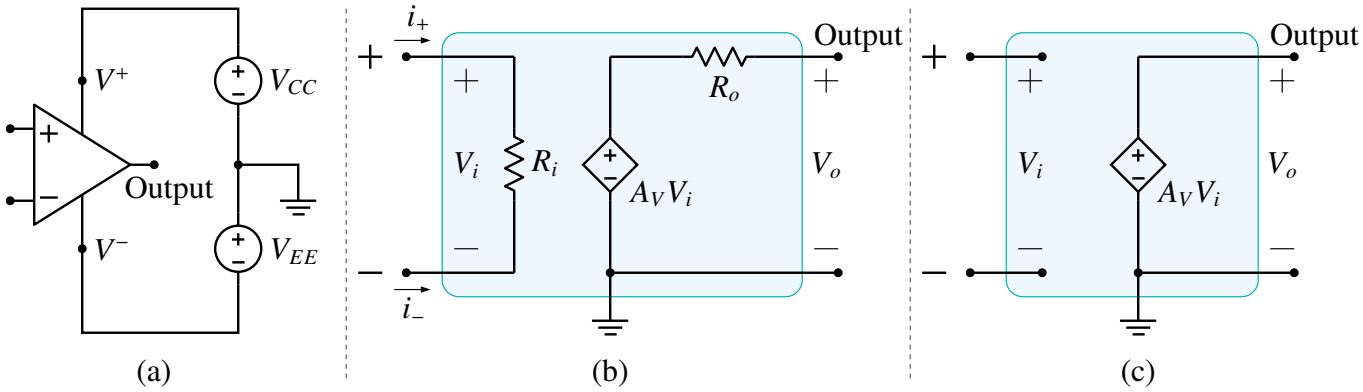


Figure 3.2: (a) Op-amp power supply connections, (b) equivalent circuit with R_i and R_o, (c) equivalent circuit with $R_i \to \infty$, $R_o \to 0$. "+" and "−" terminals correspond to the non-inverting and inverting inputs of the op-amp, respectively.

resistance called the "input resistance" of the op-amp, denoted by R_i in the figure. The voltage appearing between the input terminals $V_i = V_+ - V_-$ is amplified by the "op-amp gain" A_V and is represented by a VCVS on the output side. In series with the VCVS, we have the op-amp "output resistance" R_o. An op-amp can be treated in most applications like an "ideal" block, with $A_V \to \infty$, $R_i \to \infty$, $R_o \to 0$. For the 741 op-amp, A_V is 10^5, a very large gain. R_i and R_o are, respectively, 2 MΩ and 75 Ω. Since typical values of resistances used externally in op-amp circuits are a few kΩ to tens of kΩ, we can consider R_i to be large (like an open circuit) and R_o to be small (like a short circuit). With these simplifications, we get the approximate equivalent circuit of Fig. 3.2 (c). A large R_i implies that the currents i_+ and i_- entering the input terminals of the op-amp (see Fig. 3.2 (b)) are negligibly small, and in analysing op-amp circuits, we can say

$$i_+ \approx i_- \approx 0. \tag{3.1}$$

The equivalent circuit of Fig. 3.2 (c) implies that $V_o = A_V \times V_i$, i.e., $A_V\,(V_+ - V_-)$. A plot of V_o versus V_i would therefore be a straight line with slope A_V. However, the output voltage of the op-amp (V_o) is limited by the supply voltage. On the positive side, V_o cannot be greater than $+V_{\text{sat}}$ ("saturation" voltage), and on the negative side, it cannot be smaller than $-V_{\text{sat}}$. The value of V_{sat} depends on the supply voltage and is typically smaller than V_{CC} by about 1 V.

Fig. 3.3 (a) shows the V_o versus V_i relationship with $A_V = 10^5$ and $V_{\text{sat}} = 10$ V. When $V_i = 10\text{ V}/10^5$, i.e., +0.1 mV, V_o saturates to +10 V. Similarly when $V_i = -10\text{ V}/10^5$, i.e., −0.1 mV, V_o saturates to −10 V. The op-amp is said to be operating in the "linear" region if $-V_{\text{sat}} < V_o < +V_{\text{sat}}$, i.e., for $-0.1\text{ mV} < V_i < 0.1$ mV in Fig. 3.3 (a). Since V_i is restricted to very small values, we have

$$V_+ \approx V_-\,, \tag{3.2}$$

if the op-amp is operating in the linear region. In other words, we can say that V_+ and V_- are "virtually" the same.

Note that the V_i and V_o scales are very different in Fig. 3.3 (a). If similar scales are used for V_i and V_o, we get the plot shown in Fig. 3.3 (b). In this plot, the linear region appears almost like a vertical line segment.

Eqs. 3.1 and 3.2 are our "golden rules" for analysing op-amp circuits in which the op-amp is operating in the linear region. In Sec. 3.3, we will use them to understand circuits which you will study in your experiments.

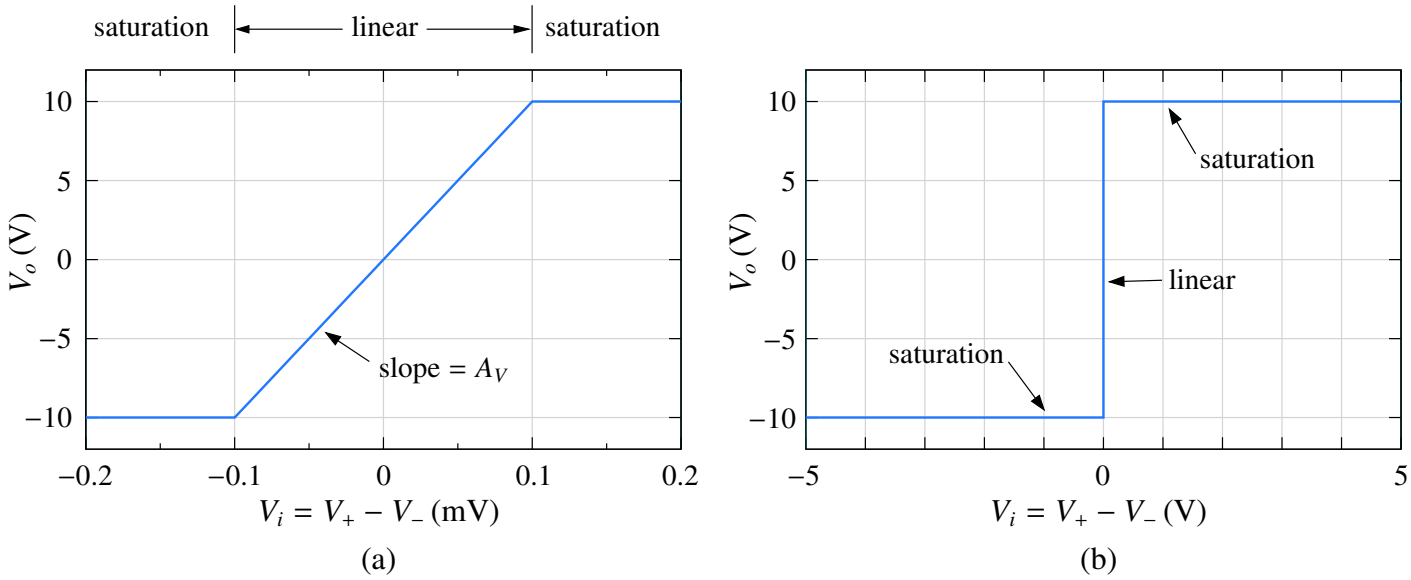


Figure 3.3: Op-amp V_o versus V_i relationship, with $A_V = 10^5$ and $\pm V_{\text{sat}} = \pm 10$ V. Note that the V_i-axis scales are different in (a) and (b).

3.3 Op-amp circuit examples

Op-amp circuits can be divided into two broad types: (i) op-amp operating in the linear region, (ii) op-amp operating in the saturation region. In a given circuit, whether the op-amp(s) will operate in the linear region depends on the type of feedback involved in that circuit. Circuits with negative feedback are "stable", leading to op-amp operation in the linear region. Analysis of feedback is outside the scope of this document. In the following, we will assume that the op-amp is working in the linear region, thus allowing us to use Eqs. 3.1 and 3.2 in analysing the circuits.

3.3.1 Inverting amplifier

Fig. 3.4 (a) shows the inverting amplifier circuit. Since $V_- \approx V_+$, we conclude that $V_- \approx 0$ V. The inverting input terminal of the op-amp in this case is at nearly 0 V although it is not physically connected to ground. It is therefore called "virtual ground."

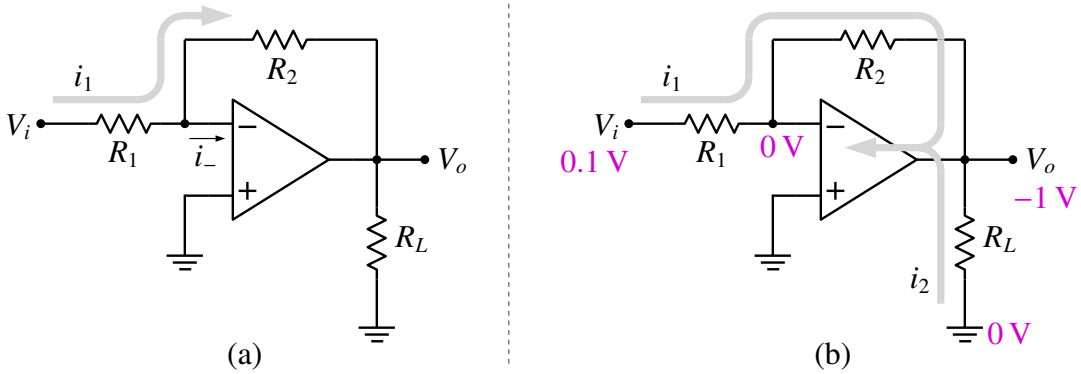


Figure 3.4: (a) Inverting amplifier circuit, (b) Current flow with $V_i = 0.1$ V, and $R_2/R_1 = 10$.

Having established that $V_- \approx 0$ V, we can write the current i_1 in terms of the input voltage V_i as

$$i_1 = \frac{V_i - 0}{R_1} = \frac{V_i}{R_1}. \tag{3.3}$$

We can now use the fact that the op-amp input currents are zero. In particular, since $i_- = 0$, we know that i_1 also flows through R_2, and we can write

$$V_o = V_- - i_1 R_2 = 0 - \frac{V_i}{R_1} R_2 = -\frac{R_2}{R_2} V_i. \tag{3.4}$$

Note that the load resistance R_L is not involved in the expression for the gain.

The gain of the inverting amplifier is $-R_2/R_1$. Fig. 3.5 (a) shows $V_o(t)$ when a sinusoidal input voltage $V_i(t) = V_m \sin \omega t$, with $V_m = 0.5$ V and $f = 1$ kHz, is applied to an inverting amplifier with gain -10 (i.e., $R_2/R_1 = 10$). Since the gain is negative, the output waveform is an inverted (and amplified) version of the input; hence the name "inverting amplifier."

It is instructive to trace the current path in the inverting amplifier by taking a specific example. Consider $V_i = 0.1$ V (constant), and $R_2/R_1 = 10$. The gain is therefore -10, and the output voltage would be $V_o = -1$ V, as shown in Fig. 3.4 (b). The directions of currents through R_1, R_2, R_L are shown in the figure. The currents i_{R2} and i_{RL} combine and flow into the op-amp output terminal, i.e., the op-amp is "sinking" a current in this case.

The gain of the inverting amplifier can be adjusted by simply changing R_1 or R_2, and it does not require an in-depth knowledge of the internal circuit of the op-amp. This feature of simple design process is common to op-amp circuits, making them attractive. However, we should be aware of some performance limitations, as illustrated in the following examples.

1. For the waveforms shown in Fig. 3.5 (a), we have $V_m = 0.5$ V and $f = 1$ kHz. If V_m is increased to 2 V, keeping the frequency the same, we would expect V_o to have an amplitude of $10 \times 2 = 20$ V. However, in this example, the saturation voltage V_{sat} of the op-amp is about 12.5 V, thus causing the output to saturate at $\pm V_{\text{sat}}$, as shown in Fig. 3.5 (b).

2. For $V_m = 1$ V and $f = 25$ kHz, we would expect V_o to have an amplitude of $1 \times 10 = 10$ V, shown as the curve marked "V_o (expected)" in Fig. 3.5 (c). However, the actual V_o looks very different; it is not sinusoidal. This behaviour arises because of the finite "slew rate" of the op-amp, which is the maximum rate at which V_o can rise or fall. For the 741 op-amp, it is 0.5 V/μsec. We expect the maximum $\left|\frac{dV_o}{dt}\right|$ to be $(R_2/R_1) \times \left|\frac{dV_i}{dt}\right|_{\text{max}}$, i.e., $10 \times \max(\omega V_m \cos \omega t)$, which is 1.57×10^6 V/sec or 1.57 V/μsec. Since the op-amp output cannot rise or fall faster than 0.5 V/μsec, the $V_o(t)$ waveform gets distorted.

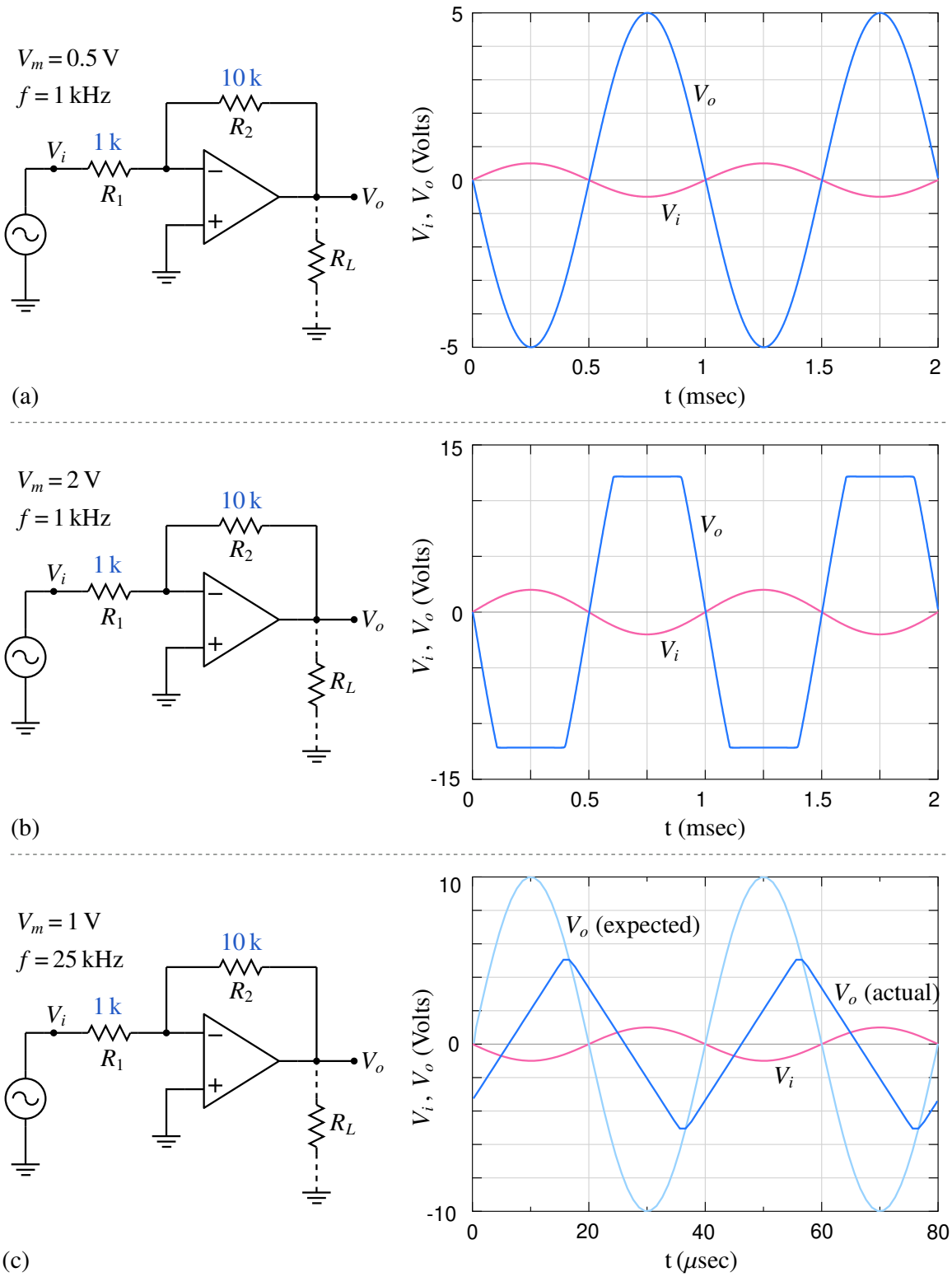


Figure 3.5: Inverting amplifier circuit with input $V_i(t) = V_m \sin \omega t$: (a) $V_m = 0.5$ V, $f = 1$ kHz (normal operation), (b) $V_m = 2$ V, $f = 1$ kHz (output limited by $\pm V_{\text{sat}}$), (c) $V_m = 1$ V, $f = 25$ kHz (output affected by slew rate). The 741 op-amp model has been used to obtain the waveforms in all three cases.

3.3.2 Difference amplifier

In some applications, we want $V_o = K\,(V_{i1} - V_{i2})$, an amplified form of the *difference* between two input voltages. The difference amplifier, shown in Fig. 3.6, can be used for this purpose. To analyse this circuit, we first note that $i_+ = 0$, and we can get the voltage at the non-inverting terminal (with

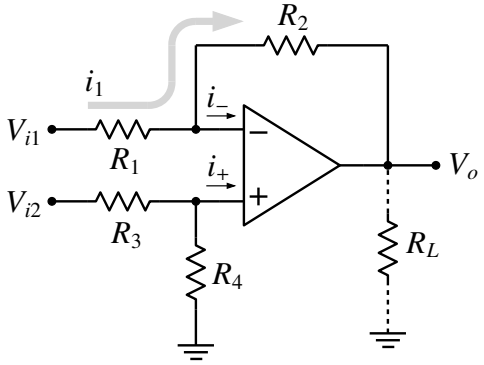


Figure 3.6: Difference amplifier.

respect to ground) using voltage division:

$$V_+ = V_{i2}\,\frac{R_4}{R_3 + R_4}. \tag{3.5}$$

For i_1, which also flows through R_2 (since $i_- = 0$), we have

$$i_1 = \frac{V_{i1} - V_-}{R_1}. \tag{3.6}$$

The output voltage is

$$V_o = V_- - i_1 R_2 = V_- - \left(\frac{V_{i1} - V_-}{R_1}\right) R_2 = V_- \left(1 + \frac{R_2}{R_1}\right) - \frac{R_2}{R_1}\,V_{i1}. \tag{3.7}$$

Using $V_- \approx V_+$ and Eq. 3.5, we get

$$\begin{aligned} V_o &= V_{i2}\left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) - \frac{R_2}{R_1}\,V_{i1} \\ &= V_{i2}\left(\frac{R_4/R_3}{1 + R_4/R_3}\right)(1 + R_2/R_1) - \frac{R_2}{R_1}\,V_{i1} \\ &= \frac{R_2}{R_1}\,(V_{i2} - V_{i1}) \quad \text{if } \frac{R_4}{R_3} = \frac{R_2}{R_1}. \end{aligned} \tag{3.8}$$

3.3.3 Current-to-voltage converter

A current I_s can be converted to a voltage by simply passing it through a resistor R, as shown in Fig. 3.7 (a)[2] (with $R_L \to \infty$), giving $V_o = I_s \times R$. However, when a load is connected to the circuit,

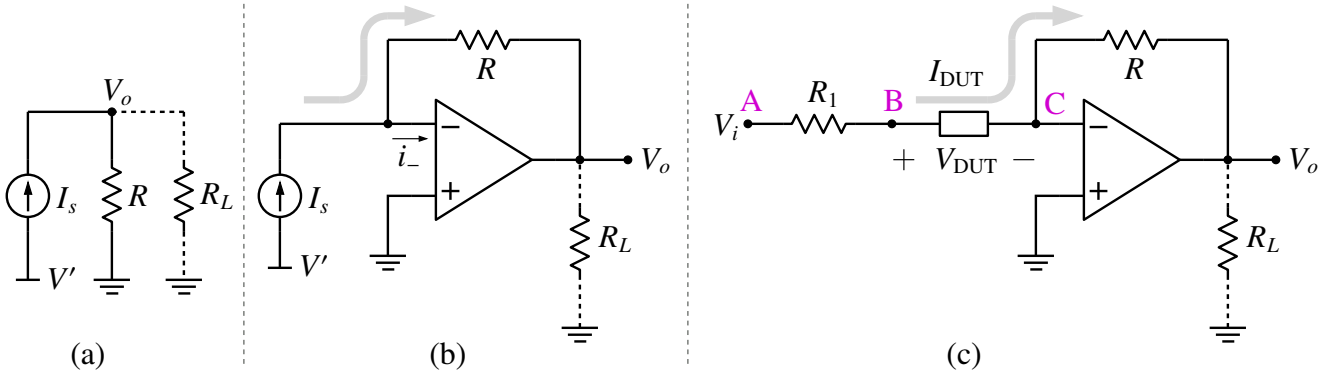


Figure 3.7: (a) Simple current-to-voltage converter, (b) op-amp based current-to-voltage converter, (c) measurement of the I-V curve of a Device Under Test (rectangular box).

such as the resistance R_L in the figure, V_o changes to $I_s \times (R \parallel R_L)$, i.e., the output of our current-to-voltage converter depends on what it drives, and that is not desirable.

An op-amp based current-to-voltage converter (see Fig. 3.7 (b)) makes the output independent of the load. The current I_s also flows through R since $i_- = 0$. Since $V_- \approx V_+ = 0$ V, the output voltage is

$$V_o = V_- - I_s R = 0 - I_s R = -I_s R, \tag{3.9}$$

which is independent of R_L.

The op-amp current-to-voltage converter can be used to measure the I-V curve of a "device under test" (DUT) using the circuit shown in Fig. 3.7 (c). When the input voltage V_i is varied, V_{DUT} and I_{DUT} change. The voltage across the DUT is

$$V_{\text{DUT}} = V_B - V_C = V_B, \tag{3.10}$$

since node C remains at virtual ground. The output voltage is

$$V_o = V_C - I_{\text{DUT}} R = -I_{\text{DUT}} R. \tag{3.11}$$

The I-V curve for the DUT can be plotted in two ways.

1. Use a dc source for V_i and take readings for $V_i = V_1$, V_2, etc. For each V_i, measure V_B and V_o, which give V_{DUT} and I_{DUT}, respectively.

2. Apply a triangular wave as $V_i(t)$. Connect node B to CH1 of the oscilloscope, V_o to CH2, and use the X-Y mode of the scope to view the I-V curve. Note the following points.

   (a) CH2 needs to be used in the "invert" mode because of the negative sign in Eq. 3.11.

   (b) The DUT current gets scaled by R (see Eq. 3.11).

[2]The voltage V' in the figure could be 0 V or a constant (dc) voltage, depending on what the current source represents.

The purpose of R_1 is to limit the current drawn from the input source. This is particularly important in diode I-V measurements where a forward bias of a few Volts would cause a very large current. With R_1 in place, a large current would cause most of the voltage to drop across R_1, thus limiting V_{DUT} and hence the current.