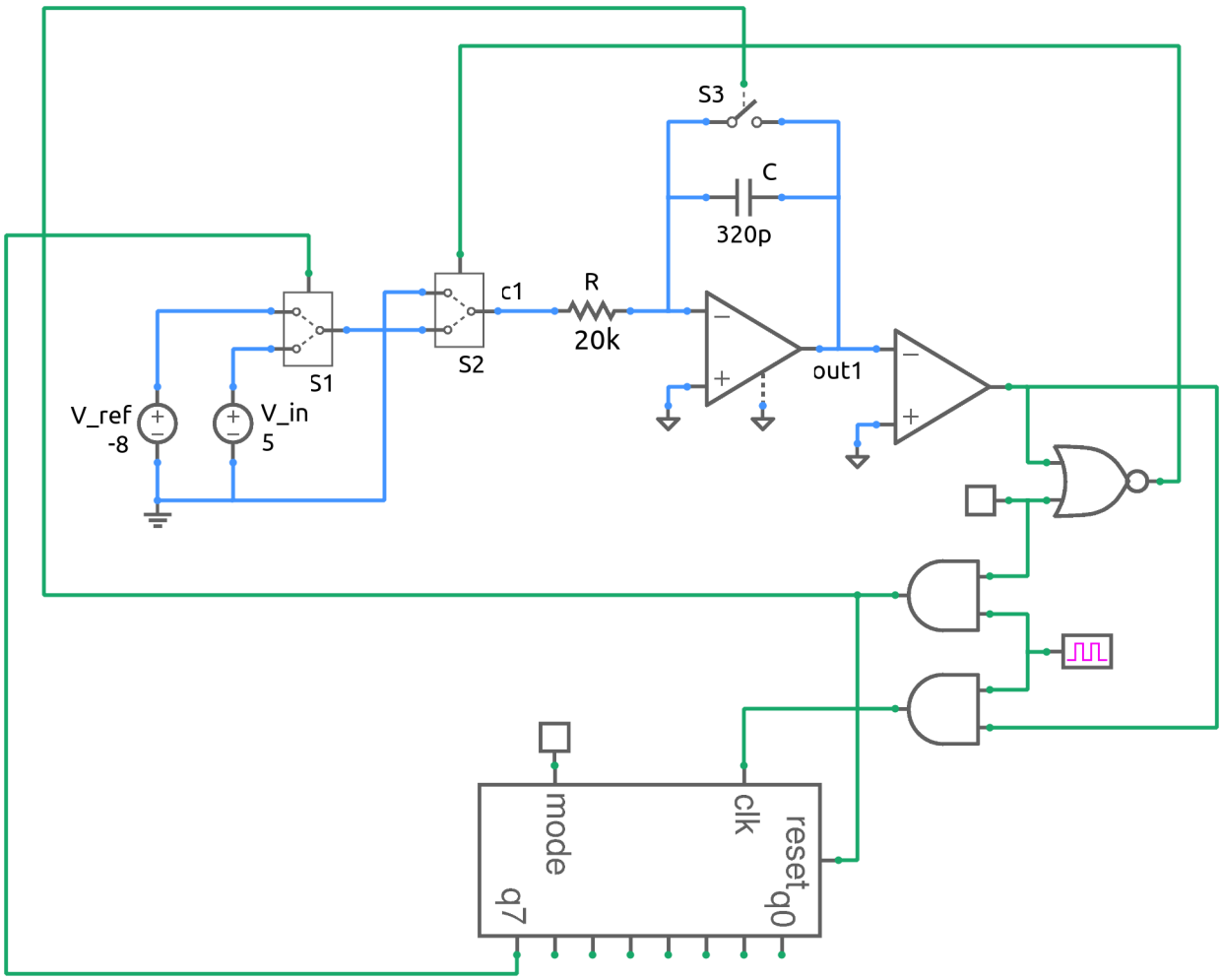
adc_dual_slope.sqproj



Consider an analog voltage V_A (denoted by `v_in` in the figure) to be converted to the digital format. In a dual-slope ADC, conversion starts by connecting V_A to the input of the integrator and starting the counter. When the counter exceeds 2^N, an overflow is generated by the counter[1]. By this time, the integrator output has reached $-V_A\, 2^N\, T_c/RC$ (a negative voltage, assuming V_A to be positive), where T_c is the period of the clock driving the counter. The overflow signal causes the integrator input to switch from V_A to V_R, a reference voltage (which is negative and larger in magnitude than V_A). The integrator output now starts going

[1]Note that, in the figure, an 8-bit counter is used to serve as a 7-bit counter (bits `q0`-`q6` and an overflow in the form of `q7`.

back to 0 V. When it crosses 0 V, the comparator output changes, and the counter stops counting. The counter output at this stage is the desired digital representation of V_A.

Exercise Set

1. For $V_A = 5$ V, $V_R = -8$ V, and the other parameters as specified in the figure, what would be the ADC output? Verify with simulation.

2. What would be the ADC output for the following values of V_A: 1 V, 1.5 V, 1.8 V, 2.3 V, 6 V? Verify with simulation.

3. Will the ADC output for a given V_A (say, 1 V) change if the integrator R is doubled? Verify with simulation.

4. Will the ADC output for a given V_A (say, 1 V) change if the clock frequency is doubled? Verify with simulation.

References

1. K. Gopalan, *Introduction to Digital Microelectronic Circuits*, Tata McGraw-Hill, New Delhi, 1978.

2. H. Taub and D. Schilling, *Digital Integrated Electronics*, McGraw-Hill, 1977.