`bjt_diff_pair.sqproj`

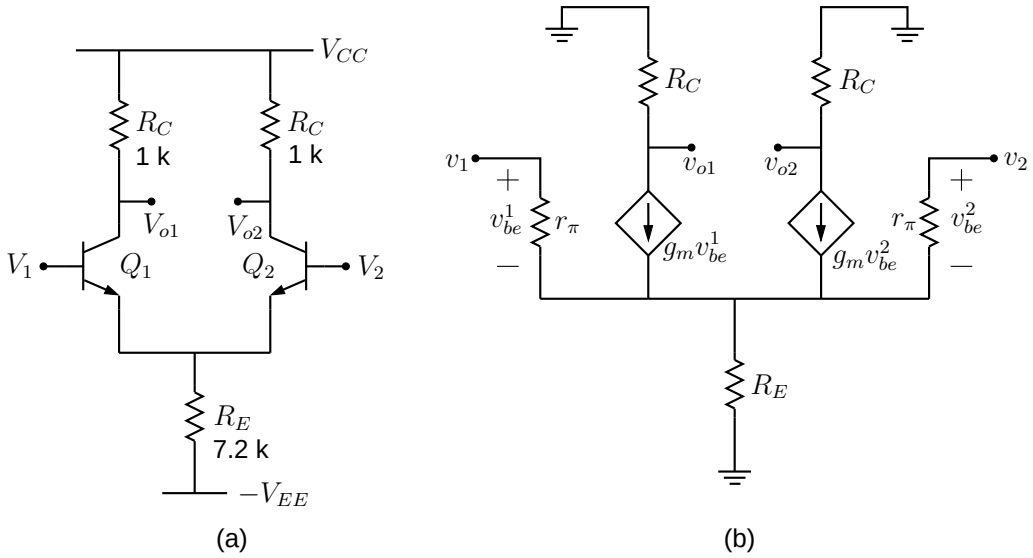

Figure 1: (a) BJT differential pair, (b) small-signal equivalent circuit.

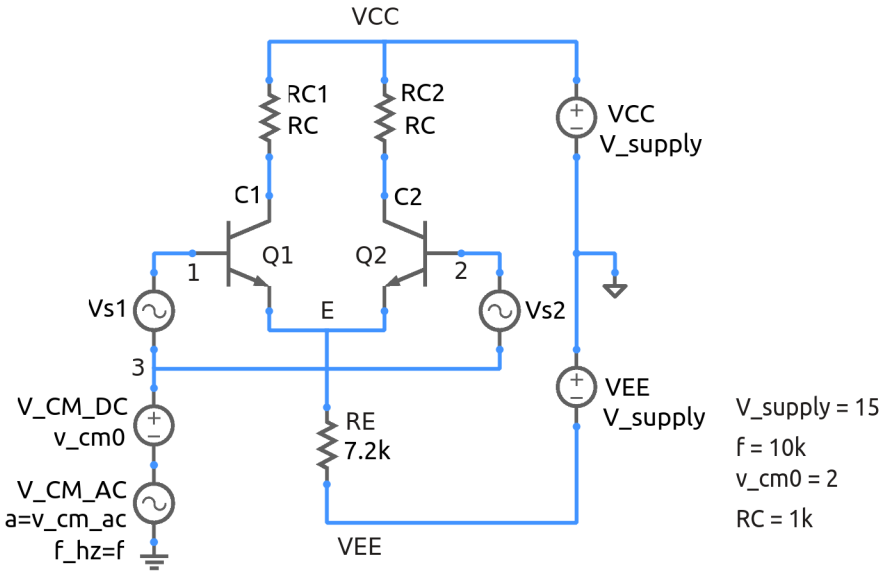

Figure 2: SEQUEL implementation of a BJT differential pair.

In a differential amplifier, the output V_o is given by,

$$V_o = A_d\, v_d + A_c\, v_c\,, \tag{1}$$

where v_d and v_c, the differential- and common-mode input voltages, are given by (with V_1 and V_2 as the two input voltages of the amplifier),

$$v_d = V_1 - V_2 \,, \tag{2}$$

$$v_c = \frac{1}{2}\,(V_1 + V_2)\,. \tag{3}$$

Ideally, we would like to have $A_c = 0$. In practice, A_c is small but finite. The common-mode rejection ratio (CMRR) is used as a figure of merit to describe the differential amplifier:

$$\text{CMRR} = \frac{A_d}{A_c}\,. \tag{4}$$

Consider the differential amplifier shown in Fig. 1(a). The small-signal equivalent circuit for this differential amplifier is shown in Fig. 1(b). The differential-mode gain for single-ended output (i.e., $V_o = V_{o1}$ or V_{o2}) is given by

$$A_d = \frac{1}{2}\,g_m R_c\,, \tag{5}$$

where $g_m = I_C/V_T$ is the BJT transconductance.

Regarding the common-mode output voltage, if the output is taken in a double-ended manner (i.e., $V_o = V_{o1} - V_{o2}$), the common-mode gain A_c is zero. However, if it is taken in a single-ended manner ($V_o = V_{o1}$ or V_{o2}), the common-mode gain is finite and is given by,

$$A_c = -\frac{\alpha R_c}{2R_E}\,. \tag{6}$$

The SEQUEL implementation of the BJT differential pair is shown in Fig. 2, giving

$v_{B1}(t) = V_{CM}(t) + V_m \sin\omega t$, and

$v_{B2}(t) = V_{CM}(t) - V_m \sin\omega t$.

For convenience, three solve blocks have been set up which can be used as follows.

1. Solve block 1: This block performs the DC bias computation for the amplifier.

2. Solve block 2: Here, a constant common-mode voltage is used (i.e., $V_{CM}(t) = V_0$, a constant), and a small value of V_m is used to ensure that the output is not distorted.

3. Solve block 3: This block is similar to the first block except that a larger value of V_m is used.

4. Solve block 4: Here, V_m is made zero (i.e., the difference-mode input voltage v_d is made zero), and a common-mode voltage of the form $v_{CM}(t) = V_0 + V'_m \sin \omega t$ is applied.

Exercise Set

1. Derive the results given above from the small-signal equivalent circuit shown in Fig. 1(b).

2. With $V_1 = V_2 = 2\,V$, what is the DC collector current for $Q1$ and $Q2$?

3. Find the value of g_m for each transistor.

4. What is the expected value of A_d? Compare with simulation results. (Use solve block 2).

5. Plot i_{C1} and i_{C2} versus the input voltage v_{B1} when V_m is relatively large (200 mV for this circuit). Comment on your observations. (Use solve block 3).

6. Calculate the common-mode gain A_c. Apply a time-varying common-mode voltage with $v_d = 0$, and simulate the circuit to find A_c (Use solve block 4). Compare your expected value of A_c with the simulation result.

References

1. A. S. Sedra, K. C. Smith, and A. N. Chandorkar, *Microelectronic Circuits: Theory and Applications*, Fifth edition, Oxford University Press, 2009.