`bjt_diff_pair_1.sqproj`

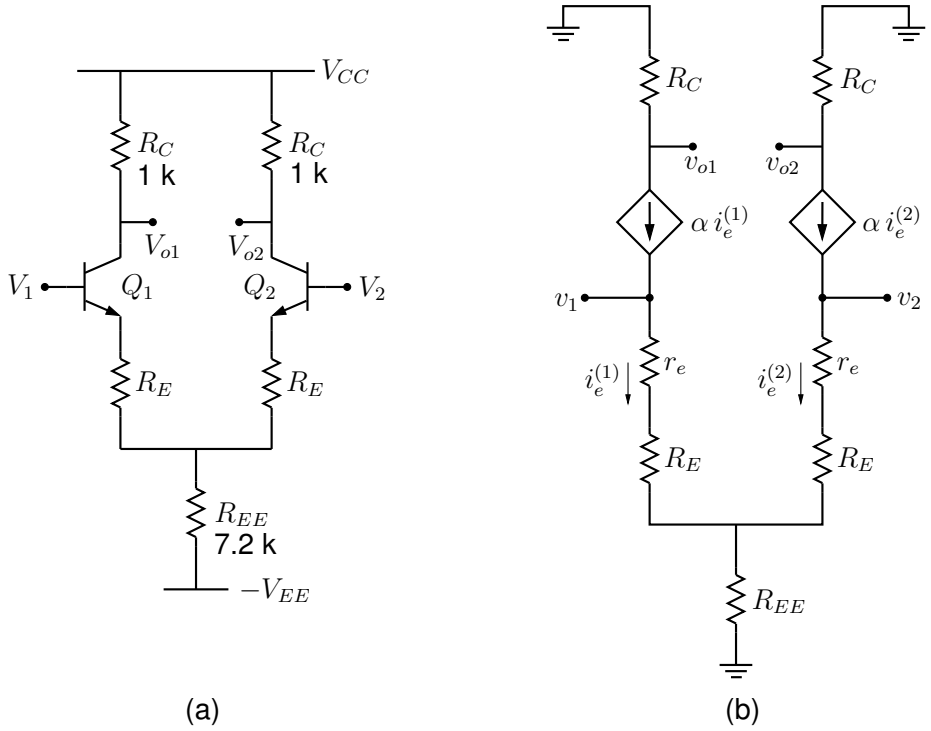

Figure 1: (a) BJT differential pair with emitter resistances, (b) small-signal equivalent circuit.

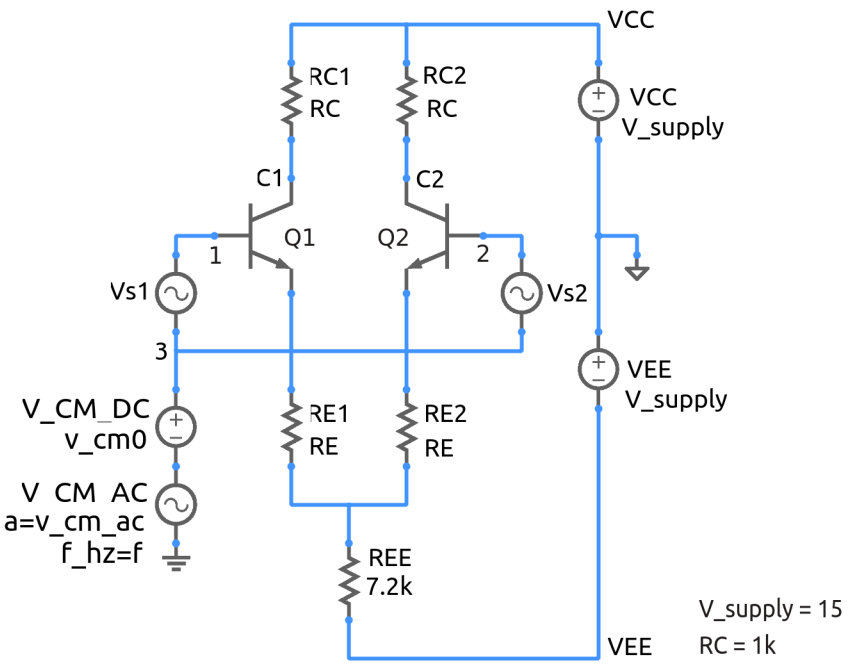

Figure 2: SEQUEL implementation of a BJT differential pair with emitter resistances.

In a differential amplifier, the output V_o is given by,

$$V_o = A_d\, v_d + A_c\, v_c\,, \tag{1}$$

where v_d and v_c, the differential- and common-mode input voltages, are given by (with V_1 and V_2 as the two input voltages of the amplifier),

$$v_d = V_1 - V_2\,, \tag{2}$$

$$v_c = \frac{1}{2}\,(V_1 + V_2)\,. \tag{3}$$

Ideally, we would like to have $A_c = 0$. In practice, A_c is small but finite. The common-mode rejection ratio (CMRR) is used as a figure of merit to describe the differential amplifier:

$$\text{CMRR} = \frac{A_d}{A_c}\,. \tag{4}$$

Consider the differential amplifier shown in Fig. 1(a). The small-signal equivalent circuit for this differential amplifier is shown in Fig. 1(b). The differential-mode gain for single-ended output (i.e., $V_o = V_{o1}$ or V_{o2}) is given by

$$A_d = \frac{1}{2}\,\frac{\alpha\, R_C}{R_E + r_e}\,, \tag{5}$$

where $r_e = \dfrac{r_\pi}{\beta + 1}$, and r_π and g_m are given by $r_\pi = \beta/g_m$, $g_m = I_C/V_T$.
Regarding the common-mode output voltage, if the output is taken in a double-ended manner (i.e., $V_o = V_{o1} - V_{o2}$), the common-mode gain A_c is zero. However, if it is taken in a single-ended manner ($V_o = V_{o1}$ or V_{o2}), the common-mode gain is finite and is given by,

$$A_c = -\frac{\alpha R_c}{R_E + r_e + 2R_{EE}} \approx -\frac{\alpha R_c}{2R_{EE}}\,. \tag{6}$$

The SEQUEL implementation of the BJT differential pair is shown in Fig. 2, giving
$v_{B1}(t) = V_{CM}(t) + V_m \sin \omega t$, and
$v_{B2}(t) = V_{CM}(t) - V_m \sin \omega t$.
For convenience, three solve blocks have been set up which can be used as follows.

1. Solve block 1: This block performs the DC bias computation for the amplifier.

2. Solve block 2: Here, a constant common-mode voltage is used (i.e., $V_{CM}(t) = V_0$, a constant), and a small value of V_m is used to ensure that the output is not distorted.

3. Solve block 3: This block is similar to the first block except that a larger value of V_m is used.

4. Solve block 4: Here, V_m is made zero (i.e., the difference-mode input voltage v_d is made zero), and a common-mode voltage of the form $v_{CM}(t) = V_0 + V_m' \sin \omega t$ is applied.

Exercise Set

1. Derive the results given above from the small-signal equivalent circuit shown in Fig. 1(b).

2. With $V_1 = V_2 = 2\,V$, what is the DC collector current for $Q1$ and $Q2$?

3. Find the value of g_m and r_e for each transistor.

4. What is the expected value of A_d with $R_E = 1\,\Omega$? Compare with simulation results. (Use solve block 2).

5. Repeat for the following values of R_E: $10\,\Omega$, $20\,\Omega$, $50\,\Omega$, $100\,\Omega$. Compare with simulation results in each case. (Use solve block 2).

6. Plot v_{C1} and v_{C2} (together) versus the input voltage v_{B1} when V_m is relatively large (200 mV for this circuit). Do this for different values of R_E as mentioned above, superimposing on the previous plot every time. Comment on your observations. (Use solve block 3).

7. Calculate the common-mode gain A_c. Apply a time-varying common-mode voltage with $v_d = 0$, and simulate the circuit to find A_c (Use solve block 4). Compare your expected value of A_c with the simulation result.

8. Let $R_E = 1\Omega$, $V_{\rm CM} = 2\,{\rm V}$. If R_{EE} is changed from $7.2\,{\rm k}\Omega$ to $10\,{\rm k}\Omega$, how will A_d and A_c change? Verify with simulation.

References

1. A. S. Sedra, K. C. Smith, and A. N. Chandorkar, *Microelectronic Circuits: Theory and Applications*, Fifth edition, Oxford University Press, 2009.