

bjt_mirror_1.sqproj

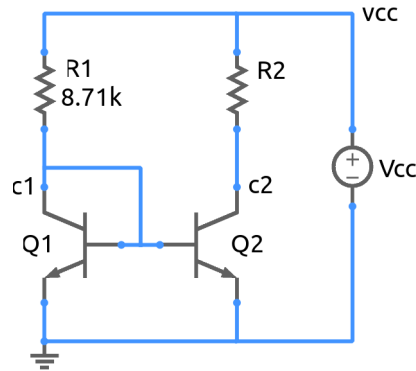


Figure 1: Circuit schematic for simple current mirror.

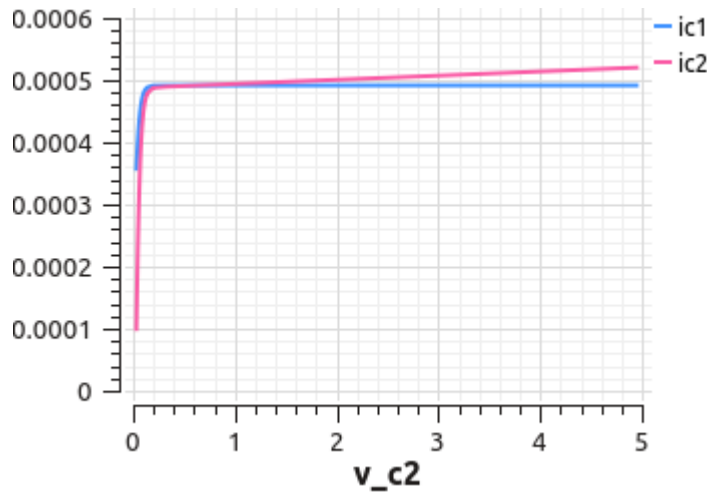


Figure 2: I_{C1} and I_{C2} versus V_{C2} for the current mirror of Fig. 1.

Shown in Fig. 1 is a simple current mirror. Assume that the two transistors are identical, i.e., their device parameters as well as operating temperatures are the same. Since the base-emitter voltage (V_{BE}) for the two BJTs is the same, the reference current I_{C1} of Q_1 is “mirrored” on the transistor Q_2 , i.e., I_{C2} is made equal to I_{C1} (if we ignore the base currents). This allows us to change I_{C2} *irrespective* of the voltage V_{C2} by simply changing the resistance R_1 , since

$$I_{C1} \approx \frac{V_{CC} - 0.7 V}{R_1}. \quad (1)$$

If the base currents I_{B1} and I_{B2} are taken into account, we get

$$I_{C2} = \frac{I_{C1}}{1 + (2/\beta)}. \quad (2)$$

In practice, the output current I_{C2} is not quite independent of V_{C2} because the transistor Q_2 has a finite output resistance due to the Early effect. Thus, I_{C2} is found to increase slightly with V_{C2} (see Fig. 2). We can think of the slope $\partial I_{C2}/\partial V_{C2}$ as an important figure of merit (smaller the better) for a current mirror. The behaviour of I_{C2} with respect to V_{C2} can be described in terms of the Early voltage as

$$I_{C2} = I_s e^{V_{BE2}/V_T} \left(1 + \frac{V_{CE2}}{V_A} \right), \quad (3)$$

where V_A is the Early voltage. Equivalently, we can say that the output resistance of the current mirror is

$$R_o = \frac{V_A}{I_{C2}}, \quad (4)$$

which is the same as r_{o2} , the output resistance of Q_2 .

Finally, for the current mirror to work as desired, the transistors must remain in the active region. When V_{C2} is not sufficiently large, this condition does not hold any more, resulting in a drop in I_{C2} , as seen in Fig. 2.

Exercise Set

1. What do you expect to happen if R_1 is reduced by a factor of 2? Verify with simulation.
2. How would the I_{C2} versus V_{C2} plot change if the value of the Early voltage (V_A) of Q_2 is doubled. Verify with simulation.

References

1. A. S. Sedra, K. C. Smith, and A. N. Chandorkar, *Microelectronic Circuits: Theory and Applications*, Fifth edition, Oxford University Press, 2009.
2. P. R. Grey and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley and Sons, 1995.