bjt_schmitt.sqproj

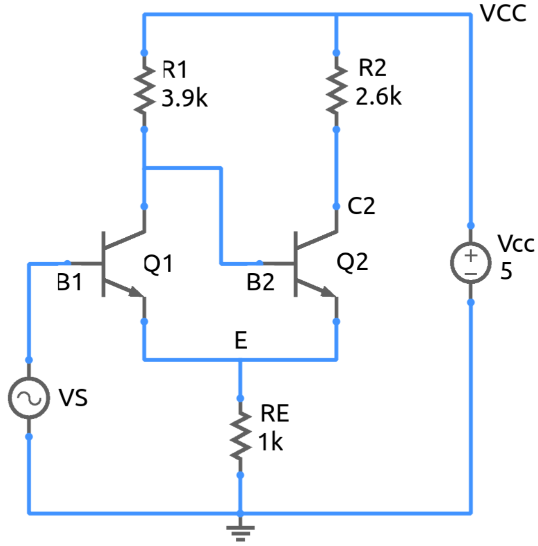

Figure 1: Emitter-coupled Schmitt circuit.

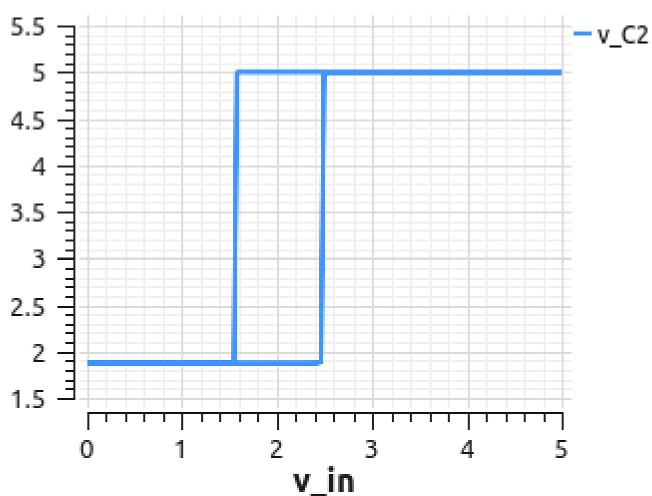

Figure 2: V_{out} $(= V_{C2})$ versus V_s $(= V_{B1})$ for the circuit of Fig. 1.

An emitter-coupled Schmitt trigger circuit is shown in Fig. 1. The V_o-V_i plot for the circuit is shown in Fig. 2. The circuit works as a comparator, i.e., it compares the input voltage with a threshold voltage and produces a high or low output voltage, depending on the result of the comparison. The threshold voltage V_T depends on the "state" of the circuit: If V_i is increased from the left, $V_T \equiv V_T^+ \approx 2.5\,\text{V}$. If V_i is decreased from the right, $V_T \equiv V_T^- \approx 1.6\,\text{V}$. The two threshold values can be seen in Fig. 2. Let us try to understand where this "memory" feature is coming from.

Consider $V_i = 5\,\text{V}$. In this condition, Q_1 is conducting and in saturation, with $V_{CE1} \approx 0.1\,\text{V}$. Since $V_{BE2} = V_{CE1}$, Q_2 does not conduct, and the output V_{C2} is pulled up to V_{CC}. As V_{in} is reduced, at some point, Q_1 comes out of saturation, and V_{CE1} starts increasing. When V_{CE1} becomes equal to $0.7\,\text{V}$, Q_2 turns on. At this point, neglecting I_{B1}, we have

$$I_{C1} = \frac{5 - 0.7}{3.9\,\text{k}\Omega + 1\,\text{k}\Omega} = 0.88\,\text{mA}, \tag{1}$$

and $V_E \approx I_{C1} R_E = 0.88\,\text{V}$. The input voltage which makes this transition happen is $V_{\text{in}} = V_T^- = V_E + 0.7\,\text{V}$, about $1.6\,\text{V}$. A further decrease in V_i makes Q_1 turn off.

Now consider $V_i = 0\,\text{V}$. In this condition, Q_1 is off, and Q_2 is in saturation with the base current I_{B2} being supplied through R_1. In this condition, $I_{E2} = I_{C2} + I_{B2}$ gives

$$\frac{V_E}{R_E} = \frac{V_{CC} - (V_E + 0.1)}{R_2} + \frac{V_{CC} - (V_E + 0.8)}{R_1}. \tag{2}$$

Solving for V_E, we get $V_E = 1.8\,\text{V}$. As V_{in} is made larger than $V_T^+ = 1.8 + 0.7$, i.e., $2.5\,\text{V}$, Q_1 turns on, V_{C1} drops, and Q_2 turns off. The output voltage V_{C2} is now $1.8 + 0.1$, i.e., $1.9\,\text{V}$.

Exercise Set

1. Simulate the circuit. Plot I_{C1}, I_{C2} (together) and V_{CE1}, V_{CE2} (together) versus V_{in} to verify that the above description of transistors Q_1 and Q_2 being on/off is correct. Plot also V_E versus V_{in}, and verify that the values obtained above at the thresholds V_T^- and V_T^+ are reasonable estimates.

2. How would the V_o-V_i plot change if R_E is changed to $1.5\,\text{k}\Omega$, with all other parameters the same? Verify with simulation.

References

1. D. A. Hodges and H. G. Jackson, *Analysis and Design of Digital Integrated Circuits,* McGraw-Hill, 1983.