bjt_ttl_dc_1.sqproj

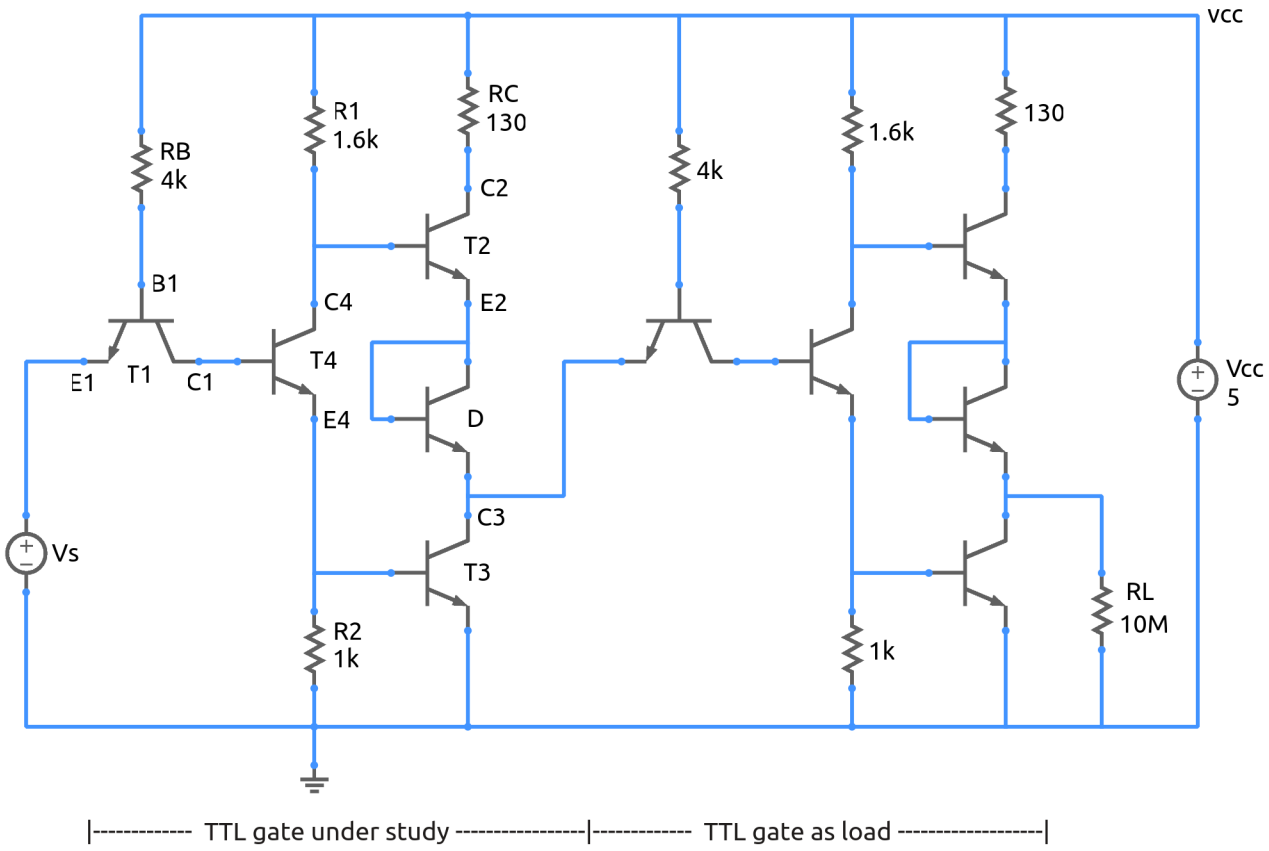

Figure 1: TTL inverter circuit.

Fig. 1 shows the circuit diagram of a TTL inverter driving another TTL inverter. When the input voltage is 0 V, the B-E diode of T1 conducts, T4 is off, and node $C4$ is pulled up to V_{CC}. The output voltage is $V_{CC} - V_{BE2} - V_D$, i.e., about 3.5 V.

When the input voltage is 5 V, T1 is in the inverse active mode, T4 conducts, making V_{E4} large enough to turn T3 on. T3 works in the saturation mode, and the output voltage, which is equal to V_{CE3}, is about 0.1 V.

Between these two extremes, there is a region in which T4 begins to conduct and remains in the active region before finally entering the saturation region, as V_{in} increases. Simulation helps us to understand these transitions.

Note that this project is similar to `bjt_ttl_dc_2.sqproj` except that the transfer curve is obtained here by applying a ramp as input.

Exercise Set

1. In the SEQUEL project file, a ramp input is applied to the TTL inverter. The input voltage variation is slow enough to ensure DC-like operation of the gate[1].

   Run the simulation, and plot V_{out} (the output of the first TTL gate) versus V_{in}.

2. Plot I_{C1}, I_{B1}, I_{E1} versus V_{in}. From this plot, determine the region of operation of T1 as V_{in} changes.

3. Repeat the above exercise for T2, T3, T4.

4. Plot V_{B1}, V_{C1}, V_{C4}, V_{E4} versus V_{in}. Explain the important features of these graphs.

References

1. H. Taub and D. Schilling, *Digital Integrated Electronics,* McGraw-Hill, 1977.

2. K. Gopalan, *Introduction to Digital Microelectronic Circuits,* Tata McGraw-Hill, 1998.

[1] In other words, the device capacitances do not contribute to the waveforms here.