decade_sync_counter.sqproj

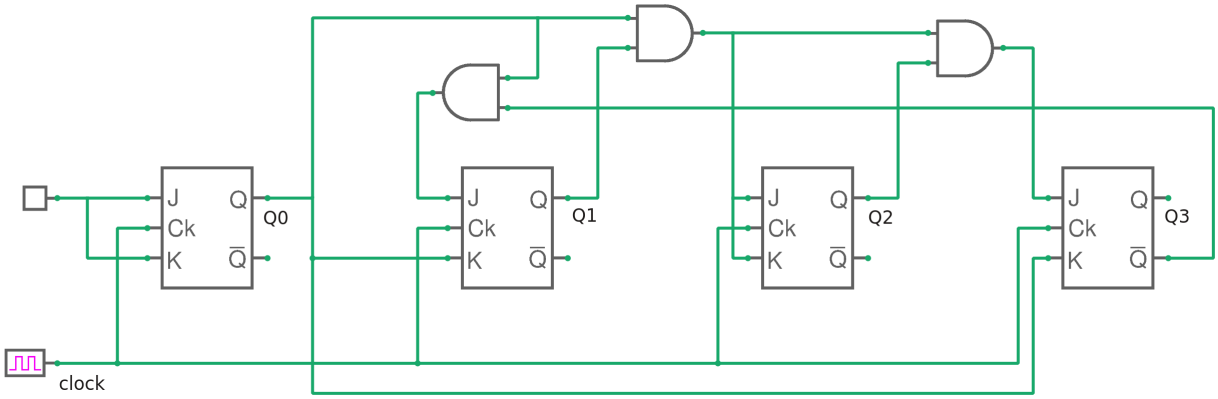

Figure 1: Circuit schematic for synchronous decade counter.

In a synchronous counter, all flip-flops receive the same clock signal. Design of a synchronous counter is based on the following state transition tables:

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Table A

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Table B

From the required sequence of counter states, logical functions for J and K of each flip-flop are constructed and then minimized using the Karnaugh map technique. Finally, the design is implemented with gates. Fig. 1 shows the design obtained for a decade counter with the sequence `0000`, `0001`, $\cdots$, `1001`, and then `0000` again.

Exercise Set

1. Design the decade counter using the procedure above, and verify that the connections given in Fig. 1 are appropriate.

2. Starting with the initial state `0000`, work out the counter sequence using Table A above, and verify (on paper) that it will count as desired. Verify with simulation.

3. Design a synchronous counter with the sequence given below.

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	0	0	0

4. Simulate the counter designed in (a), and verify its operation.