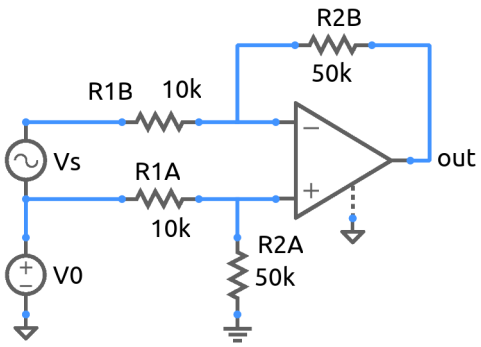
difference_amp_1.sqproj



Shown in the figure is a difference amplifier. In this circuit file, an idealised Op Amp model is used which is adequate for looking at the basic functionality of the circuit. In the arrangement shown in the figure, the input differential mode voltage is v_s, and the input common-mode voltage is approximately V_0 (since V_0 is much larger in magnitude than v_s).

Exercise Set

1. Assuming that the Op Amp is working in the linear regime, calculate the differential gain (A_d) of the circuit (V_{out}/V_s). Verify with simulation.

2. What would be the common-mode gain of the circuit if there is a mismatch of 1 % in the values of R_{1A} and R_{1B}? Verify with simulation.

References

1. A. S. Sedra, K. C. Smith, and A. .N. Chandorkar, *Microelectronic Circuits*, Oxford University Press, 2004.