ee101_bjt_amp1.sqproj



This simulation can be used to illustrate a simple BJT amplifier configuration. Assuming the BJT to be operating in the active region, we have

$$V_C = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C = V_{CC} - \beta \frac{V_{BB} - V_{BE}}{R_B} R_C,$$
(1)

where V_{BE} is approximately 0.7 V for a silicon BJT. Eq. 1 can be used to find the bias point (I_C, V_{CE}) and to estimate the gain v_c/v_{bb} of the amplifier.

The simulation file has two solve blocks: The first block performs transient simulation which can be used to plot I_C and V_C versus time. The second solve block performs DC analysis for different values of the input bias voltage, using a vary_parm statement.

To get a complete picture of the amplifier operation, the reader could first plot V_o versus V_i (i.e., V_C versus V_{BB}) with the second solve block and figure out the ideal bias point. After that, using the first solve block with different input bias voltages, the effect of the input bias voltage on the output waveforms can be observed.

Additional insight can be obtained by doing the following exercises.

Exercise Set

- 1. Compute the DC bias condition $(I_C \text{ and } V_C)$ for an input bias voltage of 1 V, and compare with simulation results. Explain the differences, if any.
- 2. Calculate the expected gain of the amplifier (v_c/v_{bb}) . Plot V_{BB} versus time and V_C versus time in separate plots, and verify your gain calculation. Assume $\beta = 100$.

- 3. Plot V_C versus V_{BB} and calculate the gain from this plot as well.
- 4. If R_C is changed from 1 k to 1.5 k, how are the bias conditions and the gain expected to change? Verify with simulation.
- 5. If R_B is changed from 10 k to 20 k, how are the bias conditions and the gain expected to change? Verify with simulation.