

Figure 1: Graphic equalizer circuit (one section).

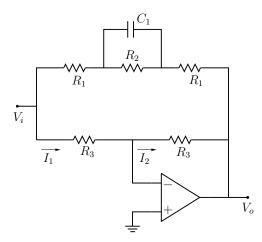


Figure 2: Circuit of Fig. 1 at low frequencies (at which C_2 can be considered an open circuit).

Fig. 1 shows a section¹ of a graphic equalizer [1] which provides "boost" (increased gain) and "cut" (reduced gain) controls in a certain frequency band. At sufficiently low frequencies (see Fig. 2), the capacitor C_2 can be considered an open circuit, and we have

$$I_1 = I_2 = \frac{V_i}{R_3}, \quad V_o = -I_2 R_3 = -V_i,$$
 (1)

since V_{-} is at virtual ground. The gain is therefore 1 in magnitude.

¹In a real graphic equalizer, an array of these circuits is employed each designed for a range of frequencies.

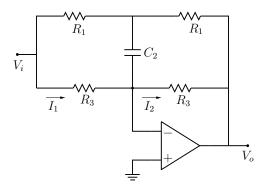


Figure 3: Circuit of Fig. 1 at high frequencies (at which C_1 can be considered a short circuit).

At sufficiently high frequencies, the capacitor C_1 may be considered a short circuit (see Fig. 3), and we then have a balanced Wheatstone bridge situation, which means that C_2 does not draw any current. The gain is once again -1,following the above reasoning. Between these two extremes, the gain is either larger or smaller than 1, depending on the pot setting. If the component values are such that $R_3 \gg R_1$, $R_3 = 10 R_2$, $C_1 = 10 C_2$, then the centre of the band is [1]

$$f_0 = \frac{\sqrt{2 + R_2/R_1}}{20 \,\pi R_2 C_2} \,, \tag{2}$$

and the gain (magnitude) can be varied (by changing the pot setting) at f_0 over the range $3R_1 = 3R_2 \pm R_1$

$$\frac{3R_1}{3R_1 + R_2} \le A_0 \le \frac{3R_1 + R_2}{3R_1}$$

Exercise Set

- Plot the magnitude frequency response (log-log plot) and verify the circuit functionality. Change the pot setting (a in the circuit file) and note the difference in the frequency response between a < 0.5 and a > 0.5. (Note: It is convenient to superimpose plots for different a values for easy comparison.)
- 2. Using $a \approx 0$, $a \approx 1$, and some values in between, verify that the gain varies between the values mentioned above.

Reference

 S. Franco, Design with Operation Amplifiers and Analog Integrated Circuits, McGraw-Hill, 1998.