ee101_voltage_doubler_1.sqproj

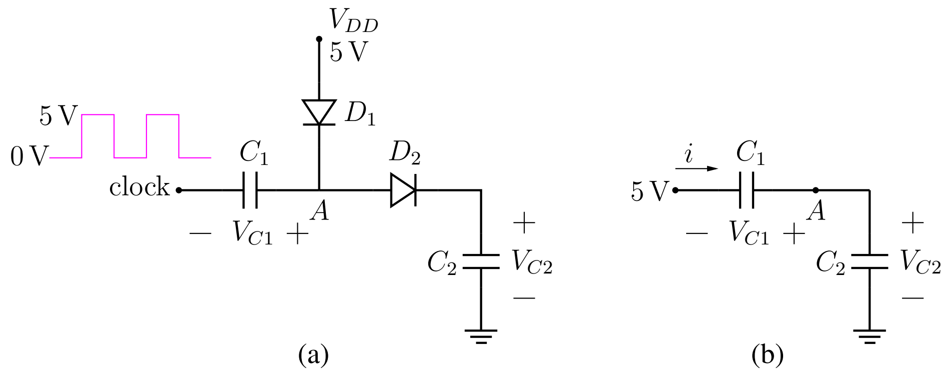

Figure 1: (a) Voltage pump circuit, (b) Equivalent circuit during $T/2 < t < T$.

The circuit shown in Fig. 1 (a) acts as a "voltage pump," giving an output $V_o \equiv V_{C2} = 2V_{DD}$ in the steady state if the diodes are ideal with $V_{\text{on}} = 0\,\text{V}$. Let us consider the case $C_1 = C_2$. We will assume the on resistance of the diodes to be negligibly small (which means that the capacitors charge or discharge instantaneously as the clock changes) and the off resistance to be large (which means that the capacitor voltage does not change unless there is a current path involving a forward-biased diode).

Let us begin with $V_{C1} = V_{C2} = 0\,\text{V}$. At $t = 0$, $V_{\text{clock}} = 0\,\text{V}$. As a result, both C_1 and C_2 get charged to $V_{DD} = 5\,\text{V}$ (see Fig. 2). At $t = T/2$, V_{clock} changes from 0 V to 5 V. The voltage at the other end of C_1 (node A) would then also tend to increase by 5 V, i.e., it would tend to change from its previous value of 5 V to the new value of 10 V. However, this would turn on D_2 (whose n end is at 5 V), and V_A would not quite reach 10 V but settle at some intermediate value. Note that all of these changes happen instantaneously thanks to our assumption of ideal diodes.

What intermediate value will V_A reach? To answer this question, let us note the following points regarding the circuit operation in the interval $T/2 < t < T$.

(a) V_{C2} can only increase since the diode D_2 will not allow C_2 to discharge.

(b) D_1 does not conduct in this interval since $V_A > 5\,\text{V}$.

(c) D_2 does conduct for the reason mentioned above, viz., the node voltage at A would tend to increase to 10 V.

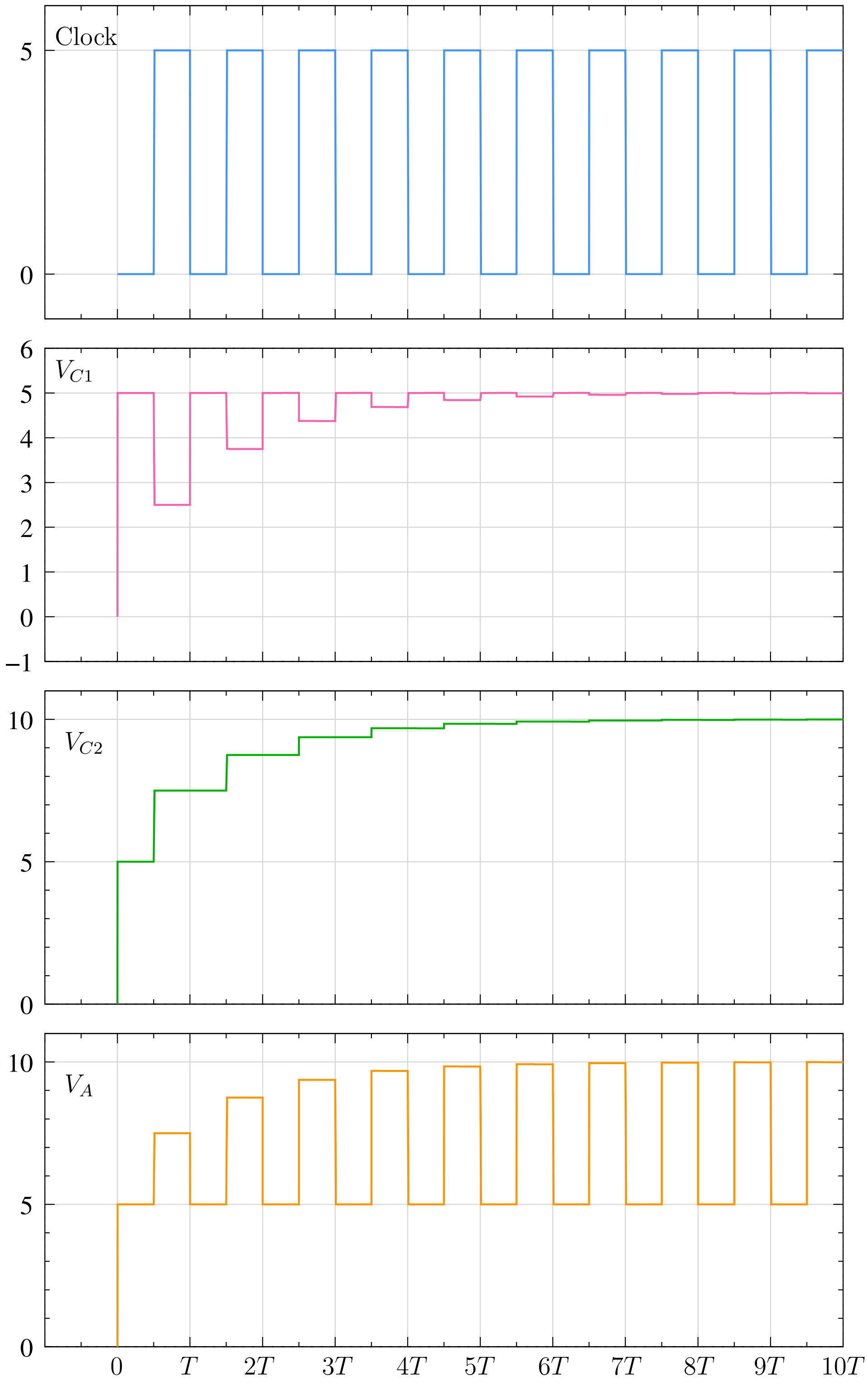

Figure 2: Waveforms for voltage pump circuit of Fig. 1.

The circuit then simplifies to that shown in Fig. 1 (b) in which D_1 has been replaced with an open circuit and D_2 with a short circuit. Since $C_1 = C_2$, the two capacitors will experience the same voltage change (see `ee101_rc8.sqproj`). Since V_{C1} and V_{C2} have opposite polarity (see Fig. 1 (a)), when V_{C2} increases by ΔV, V_{C1} decreases by the same amount. In other words, V_{C1} changes from 5 to $5 - \Delta V$, and V_{C2} changes from 5 to $5 + \Delta V$. This continues until the current stops flowing due to the following condition.

$$V_{\text{clock}} + V_{C1} = V_{C2}, \text{ i.e., } 5 + (5 - \Delta V) = (5 + \Delta V) \rightarrow \Delta V = 2.5\,\text{V}\,. \tag{1}$$

The new V_{C2} is therefore $5 + 2.5 = 7.5\,\text{V}$, and the new V_{C1} is $5 - 2.5 = 2.5\,\text{V}$, as seen in Fig. 2. At $t = T$, V_{clock} goes to 0 V again which makes C_1 charge from 2.5 V to 5 V once again. D_2 does not conduct since its n end is already at a voltage greater than V_{DD}.

At $t = 3T/2$, V_{clock} changes from 0 V to 5 V. Following the above analysis for the transition at $t = T/2$, we can say that V_{C1} will now change from 5 to $5 - \Delta V$, and V_{C2} from 7.5 to $7.5 + \Delta V$ until $V_{\text{clock}} + V_{C1}$ becomes equal to V_{C2}, i.e.,

$$5 + (5 - \Delta V) = (7.5 + \Delta V) \rightarrow \Delta V = 1.25\,\text{V}\,, \tag{2}$$

as seen in Fig. 2. Eventually, $V_{C2} \rightarrow 2V_{DD}$ as desired.

Exercise Set

1. Work out the next few values of V_{C2}. Verify with simulation.

2. How will the waveforms change if

   (a) $C_1 = 1\,\text{pF}$, $C_2 = 0.25\,\text{pF}$.

   (b) $C_1 = 0.25\,\text{pF}$, $C_2 = 1\,\text{pF}$.

   Verify with simulation.

3. For $C_1 = C_2 = 1\,\text{pF}$, how will the waveforms change if V_{on} for the diodes is 0.7 V instead of 0 V. Verify with simulation.

4. If V_{on} is 0.5 V and 1 V for D_1 and D_2, respectively, what would be the steady-state values of V_{C1} and V_{C2}? Verify with simulation.